BB301C

Build in Biasing Circuit MOS FET IC
VHF RF Amplifier

HITACHI

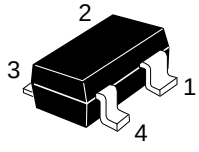
ADE-208-507
1st. Edition

Features

- Build in Biasing Circuit; To reduce using parts cost & PC board space.
- Low noise characteristics; (NF = 1.3 dB typ. at f = 200 MHz)
- Withstanding to ESD; Build in ESD absorbing diode . Withstand up to 200 V at C = 200 pF, Rs = 0 conditions.

Outline

CMPAK–4



1. Source
2. Gate1
3. Gate2
4. Drain

Hitachi semiconductor

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DS}	6	V
Gate 1 to source voltage	V_{G1S}	+6 –0	V
Gate 2 to source voltage	V_{G2S}	±6	V
Drain current	I_D	25	mA
Channel power dissipation	Pch	100	mW
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

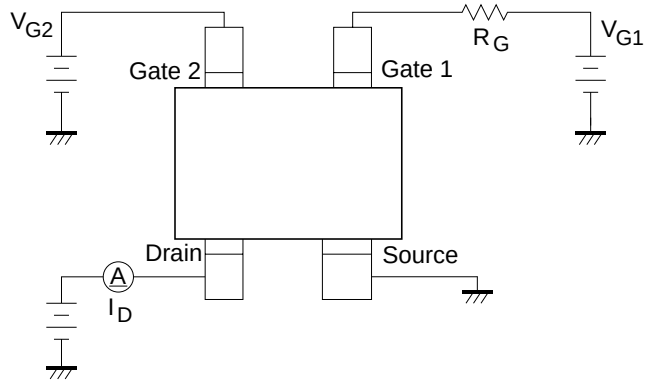
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	6	—	—	V	I_D = 200 µA $V_{G1S} = V_{G2S}$ = 0
Gate 1 to source breakdown voltage	$V_{(BR)G1SS}$	+6	—	—	V	I_{G1} = +10 µA $V_{G2S} = V_{DS}$ = 0
Gate 2 to source breakdown voltage	$V_{(BR)G2SS}$	±6	—	—	V	I_{G2} = ±10 µA $V_{G1S} = V_{DS}$ = 0
Gate 1 to source cutoff current	I_{G1SS}	—	—	+100	nA	V_{G1S} = +5 V $V_{G2S} = V_{DS}$ = 0
Gate 2 to source cutoff current	I_{G2SS}	—	—	±100	nA	V_{G2S} = ±5 V $V_{G1S} = V_{DS}$ = 0
Gate 1 to source cutoff voltage	$V_{G1S(off)}$	0.4	—	1.0	V	V_{DS} = 5 V, V_{G2S} = 4 V I_D = 100 µA
Gate 2 to source cutoff voltage	$V_{G2S(off)}$	0.4	—	1.0	V	V_{DS} = 5 V, V_{G1S} = 5 V I_D = 100 µA
Drain current	$I_{D(op)}$	10	15	20	mA	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V, R_G = 100 kΩ
Forward transfer admittance	$\|y_{fs}\|$	15	20	—	mS	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V R_G = 100 kΩ, f = 1 kHz
Input capacitance	Ciss	2.2	3.0	4.0	pF	V_{DS} = 5 V, V_{G1} = 5 V
Output capacitance	Coss	0.9	1.2	1.6	pF	V_{G2S} = 4 V, R_G = 100 kΩ
Reverse transfer capacitance	Crss	—	0.018	0.04	pF	f = 1 MHz
Power gain	PG	22	26	—	dB	V_{DS} = 5 V, V_{G1} = 5 V V_{G2S} = 4 V
Noise figure	NF	—	1.3	1.9	dB	R_G = 100 kΩ, f = 200 MHz

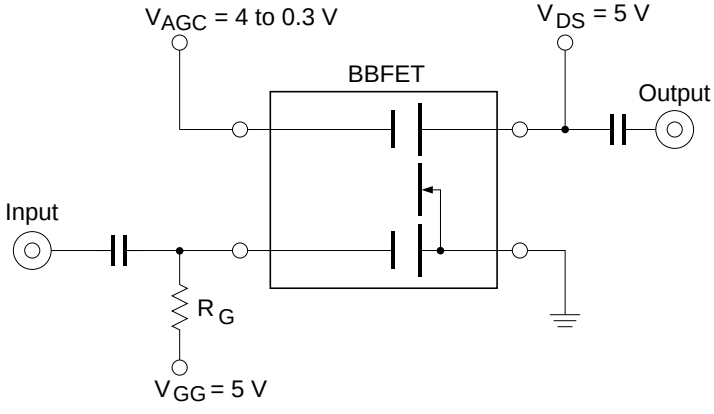
Note: Marking is “AW–”.

Main Characteristics

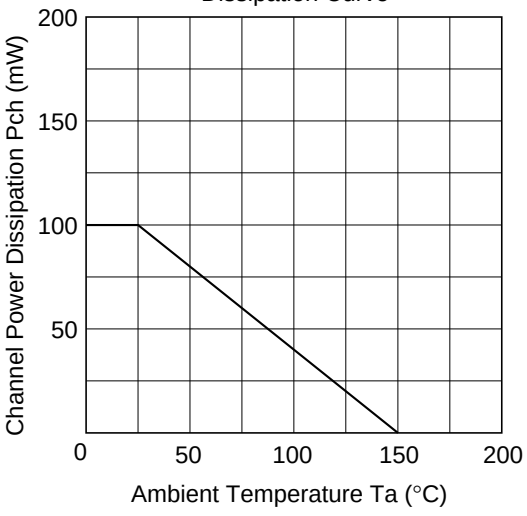
Test Circuit for Operating Items ($I_{D(op)}$, |yfs|, Ciss, Coss, Crss, NF, PG)



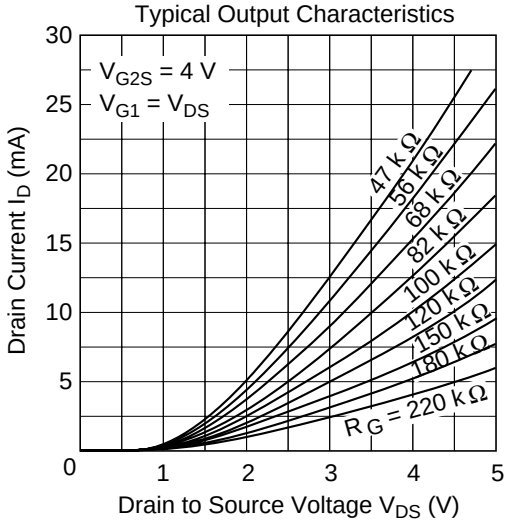
Application Circuit



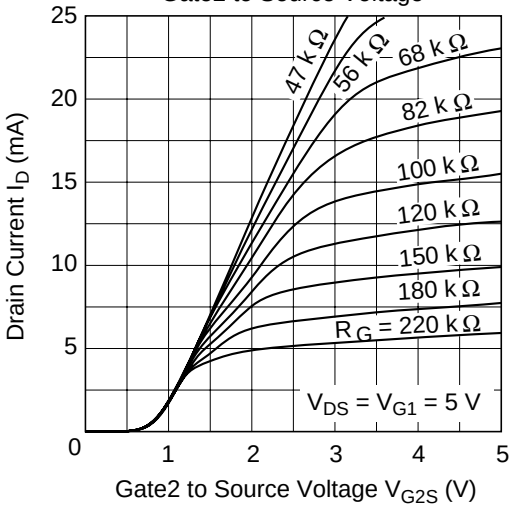
Maximum Channel Power Dissipation Curve



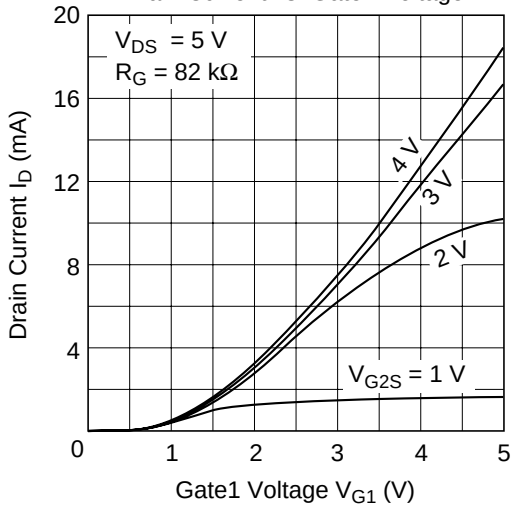
Typical Output Characteristics

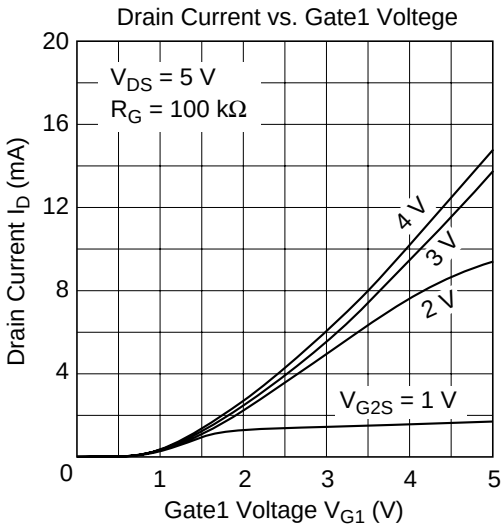


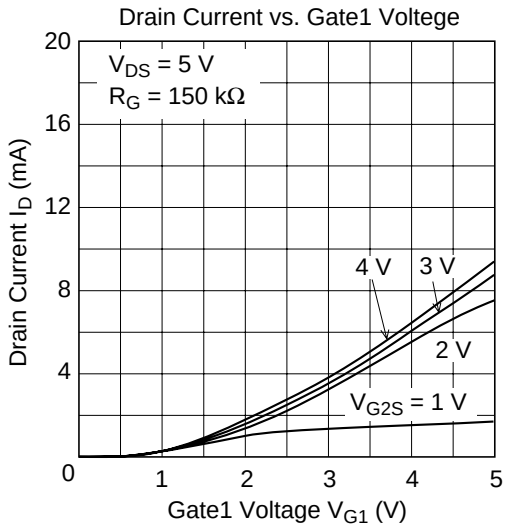
Drain Current vs. Gate2 to Source Voltage

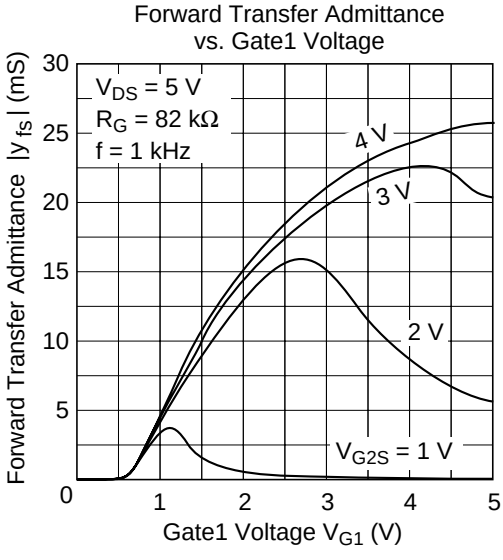


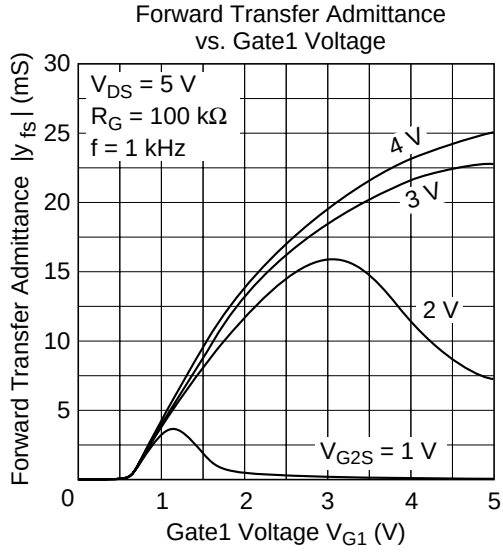
Drain Current vs. Gate1 Voltage



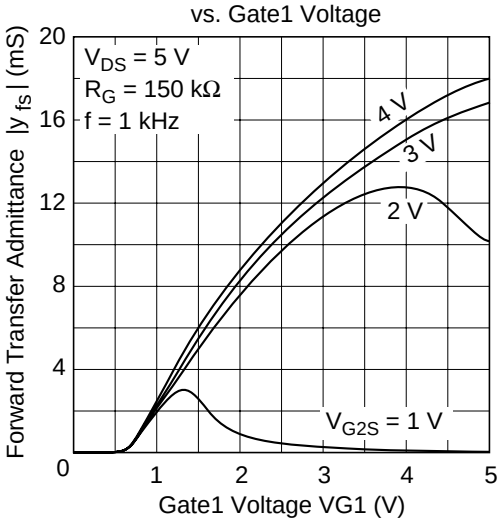

Drain Current vs. Gate1 Voltege
V_{DS} = 5 V
R_G = 100 kΩ
4 V
3 V
2 V
V_{G2S} = 1 V
Drain Current I_D (mA)
Gate1 Voltage V_{G1} (V)


Drain Current vs. Gate1 Voltege
V_{DS} = 5 V
R_G = 150 kΩ
4 V
3 V
2 V
V_{G2S} = 1 V
Drain Current I_D (mA)
Gate1 Voltage V_{G1} (V)

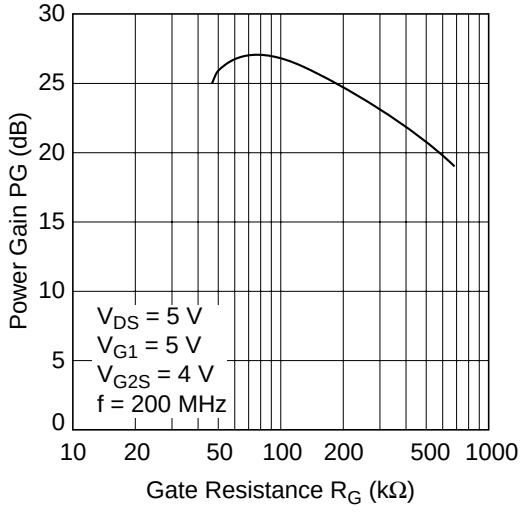

Forward Transfer Admittance
vs. Gate1 Voltage
V_{DS} = 5 V
R_G = 82 kΩ
f = 1 kHz
4 V
3 V
2 V
V_{G2S} = 1 V
Forward Transfer Admittance $|y_{fs}|$ (mS)
Gate1 Voltage V_{G1} (V)


Forward Transfer Admittance
vs. Gate1 Voltage
V_{DS} = 5 V
R_G = 100 kΩ
f = 1 kHz
4 V
3 V
2 V
V_{G2S} = 1 V
Forward Transfer Admittance $|y_{fs}|$ (mS)
Gate1 Voltage V_{G1} (V)

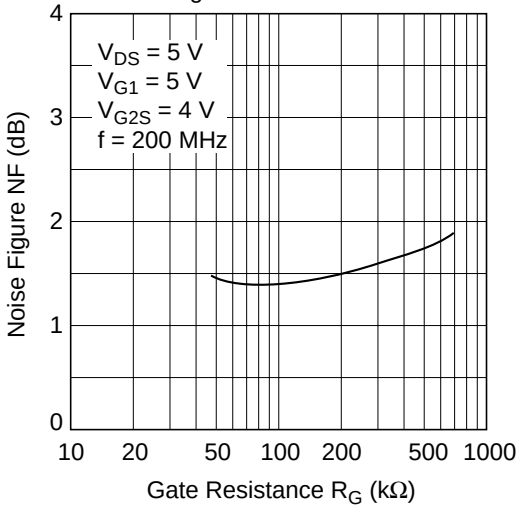
Forward Transfer Admittance vs. Gate1 Voltage



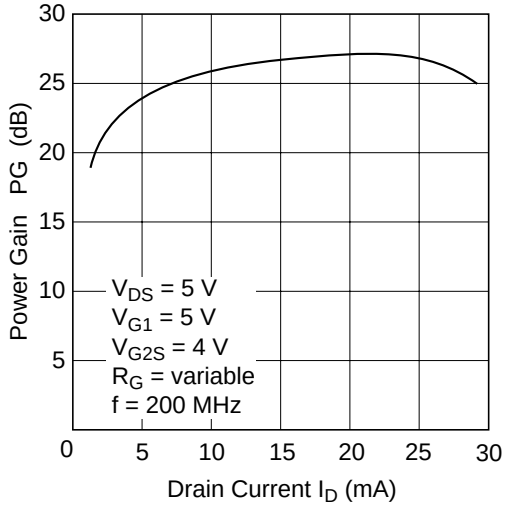
Power Gain vs. Gate Resistance



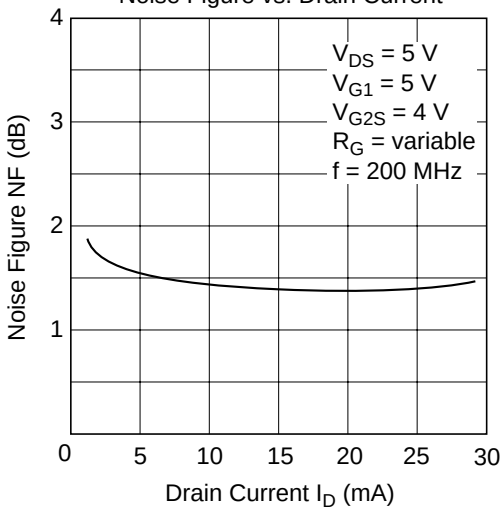
Noise Figure vs. Gate Resistance



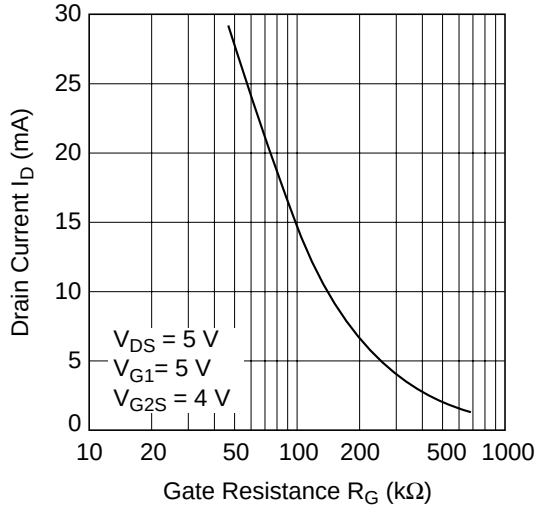
Power Gain vs. Drain Current



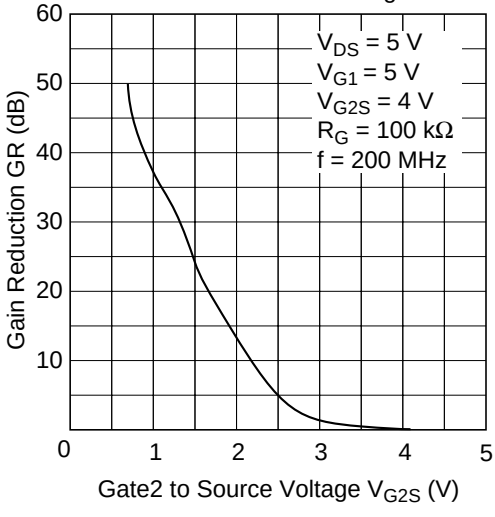
Noise Figure vs. Drain Current



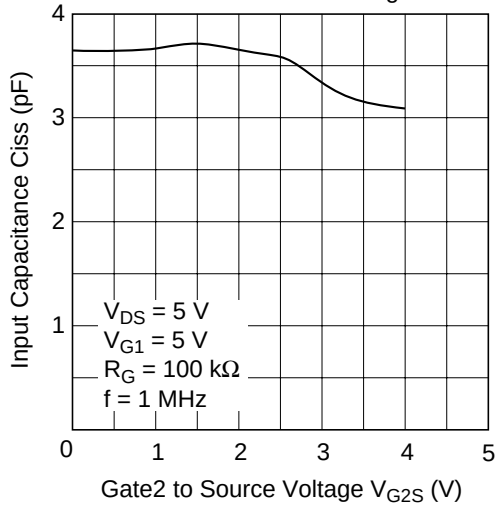
Drain Current vs. Gate Resistance



Gain Reduction vs.
Gate2 to Source Voltage

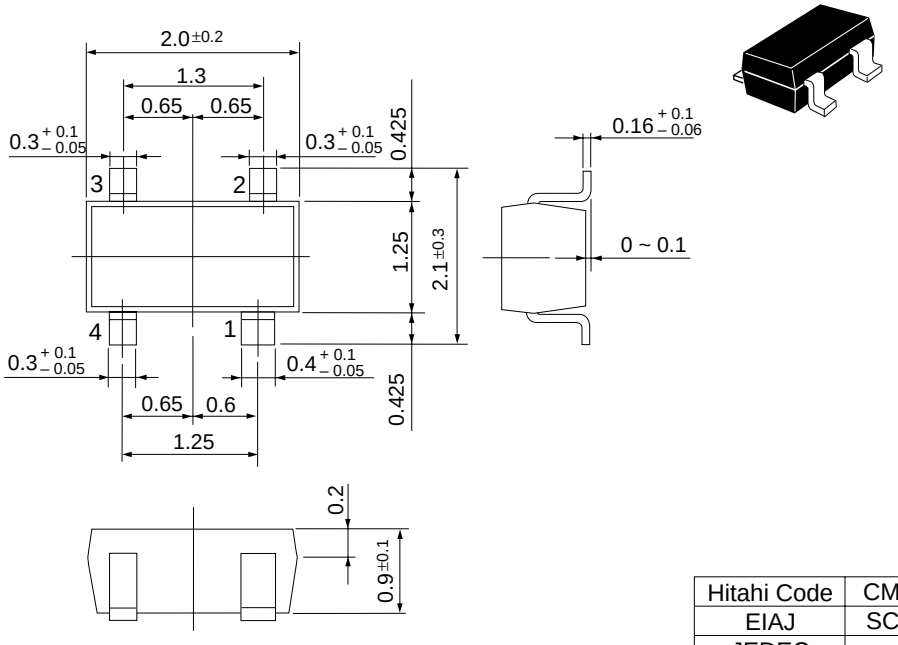


Input Capacitance vs.
Gate2 to Source Voltage



Package Dimentions

Unit: mm



Hitahi Code	CMPAK-4
EIAJ	SC-82AB
JEDEC	—

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HITACHI

Hitachi, Ltd.
Semiconductor & Integrated Circuits.
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan
Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose,CA 95134
Tel: <1> (408) 433-1990
Fax: <1>(408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building. No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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