Device
Engineering
Incorporated

385 East Alamo Drive
Chandler, AZ 85225
Phone: (480) 303-0822
Fax: (480) 303-0824
E-mail: admin@deiaz.com

DEI1160
PROGRAMMABLE GND/OPN & 28V/OPN DISCRETE INPUT INTERFACE IC

FEATURES

- Eight discrete inputs
  - Individually configurable to sense either GND/OPEN or 28V/OPEN(or 28V/GND) discrete signals
  - Hysteresis provides noise immunity
  - 1mA input current to prevent dry relay contacts.
  - Internal isolation diode
  - Inputs protected from Lightning Induced Transients per DO160E, Section 22, Cat A3 and B3.
  - Inputs protected from Power Input Abnormal Surge per DO160E, Section 16, Cat Z.
- Serial I/O interface to read data register and write configuration register
  - Direct interface to Serial Peripheral Interface (SPI) port.
  - TTL/CMOS compatible inputs and Tristate output
  - 10MHz Data Rate
  - Serial input to expand Shift Register
- Logic Supply Voltage (VCC): 3.3V or 5V
- Analog Supply Voltage (VDD): 15V +/-10%
- 16L SOIC EP package

PIN ASSIGNMENTS

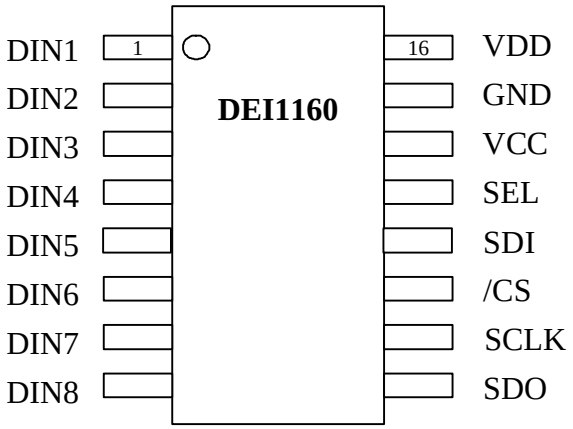


Figure 1 DEI1160 Pin Assignment (16 Lead SOIC)

FUNCTIONAL DESCRIPTION

The DEI1160 is an eight-channel discrete-to-digital interface IC implemented in an HV DMOS technology. It senses eight discrete signals of the type commonly found in avionic systems and converts them to serial logic data. Each input can be individually configured as either GND/OPEN or 28V/OPEN format input via a serial data input command. The discrete data is read from the device via an eight-bit serial shift register with 3-state output. This serial interface is compatible with the industry standard Serial Peripheral Interface (SPI) bus.

Table 1 Pin Descriptions

PINS	NAME	DESCRIPTION
1-8	DIN[1:8]	Discrete Inputs. Eight discrete signals which can be individually configured as either GND/OPEN or 28V/OPEN format inputs.
9	SDO	Logic Output. Serial Data Output. This pin is the output from MSB (Bit 8) of the selected shift register (Data/Configuration). It is clocked by the rising edge of SCLK. This is a 3-state output enabled by /CS.
10	SCLK	Logic Input. Serial Shift Clock. A low-to-high transition on this input shifts data on the serial data input into Bit 0 of the selected shift register. The selected shift register is shifted from Bit 0 to Bit 7. Bit 7 of the selected shift register is driven on DOUT.
11	/CS	Logic Input. Chip Select. A low level on this input enables the SDO 3-state output and the selected shift register. A high level on this input forces DOUT to the high impedance state and disables the shift registers so SCLK transitions have no effect. When the Data register is selected, a high-to-low transition causes the Discrete Input data to be loaded into the Data register. When the Configuration Register is selected, a low-to-high transition causes the Serial Configuration register data to be loaded into the parallel configuration outputs.
12	SDI	Logic Input. Serial Data Input. Data on this input is shifted into the LSB (Bit 1) of the selected shift register on the rising edge of the SCLK when /CS input is low.
13	SEL	Logic Input. Selects between the Serial DATA and CONFIGURATION registers. H = DATA, L = CONF.
14	VCC	Logic Supply Voltage. 3.3V or 5V
15	GND	Logic/Signal Ground
16	VDD	Analog Supply Voltage. +15V+/-10%

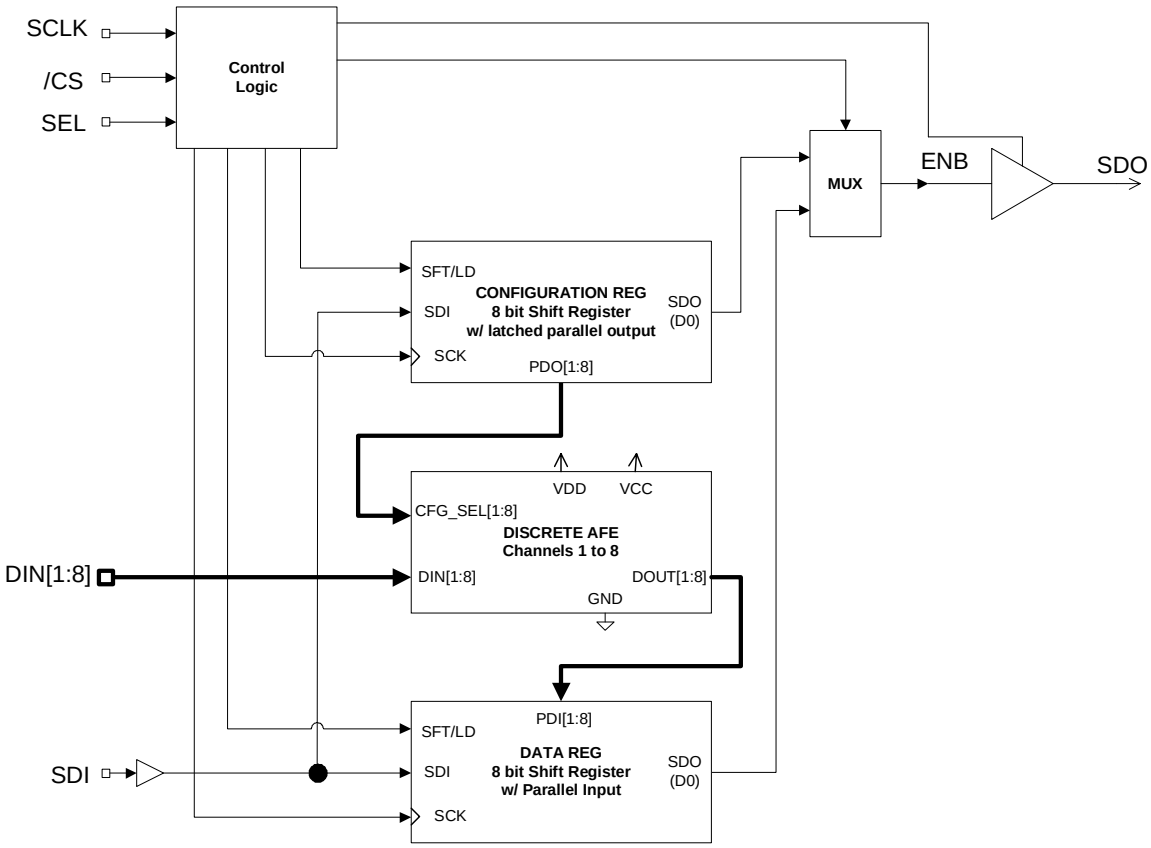


Figure 2 FUNCTION DIAGRAM

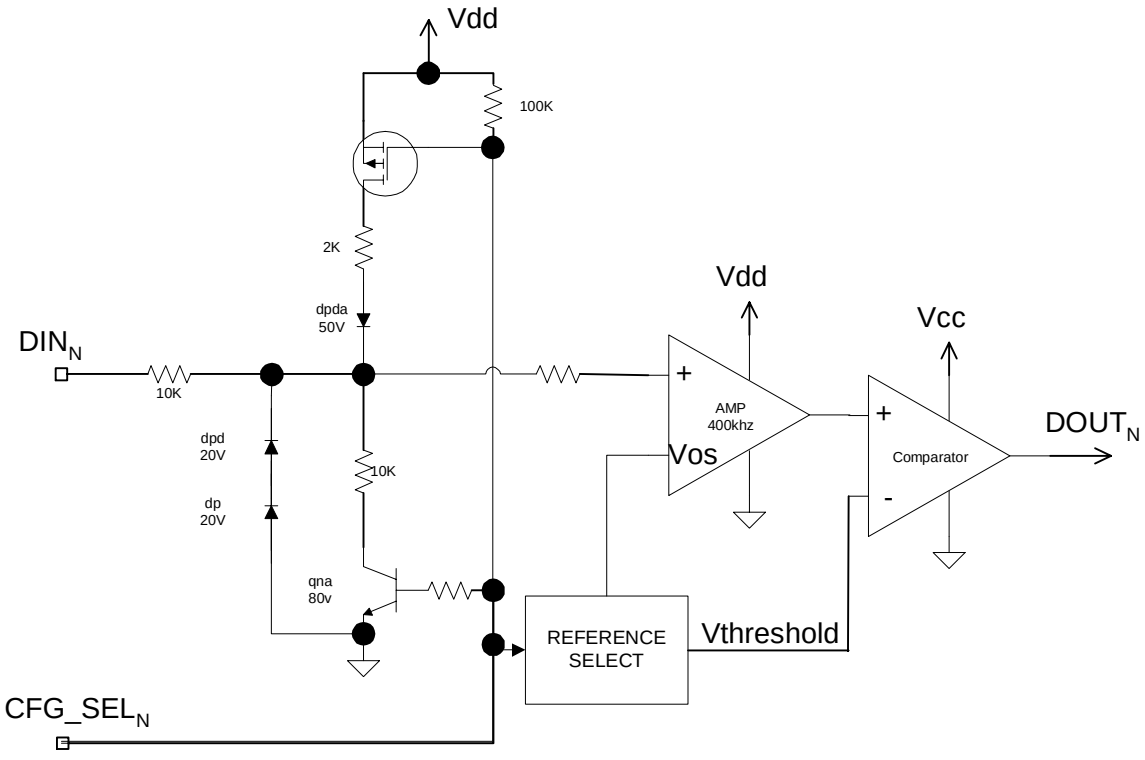


Figure 3 DISCRETE AFE FUNCTION DIAGRAM

Table 2 Truth Table

SEL	/CS	SCLK	SDI	DIN[1:8]	SDO	DESCRIPTION
X	H	X	X	X	HI Z	Not Selected
H	↓	L	X	Valid	DIN[8]	DR[1:8]← DIN[1:8]
H	L	↑	DR[1]	X	DR[8]	DR[n+1] ← DR[n], DR[1] ← SDI
L	L	↑	CR[1]	X	CR[8]	CR[n+1] ← CR[n], CR[1] ← SDI
L	↑	L	X	X	HI Z	CL[1:8]← CR[1:8]

Legend:
DR = Data Register
CR = Configuration Register
CL = Configuration Latch

DIN[1:8] Discrete AFE

The Discrete Input Analog Front End circuit function is represented in Figure 3. Each DINn signal is conditioned by the resistor / diode network and presented to an amplifier followed by a comparator with hysteresis. When the input is configured for GND/OPEN operation, the pull-up resistor & diode is enabled and the appropriate amplifier offset voltage and comparator threshold voltage are selected. When configured for 28V/OPEN, the pull-down resistor is enabled and the amp/comparator is appropriately configured.

Some notable features are:

- The input current is ~1mA. This current will prevent a "dry" relay contact.
- The input threshold voltage and hysteresis:
  - The falling Vth > 3.5V.
  - The rising Vth < 14V.
  - Hysteresis is maximum practical to meet the threshold requirements.
- Input noise immunity is maximized with a combination of voltage hysteresis and use of a slow input voltage comparator
- The inputs can withstand continuous input voltages of 40V minimum. The isolation diode breakdown voltage is greater than 45V. The 10K Ohm input resistor is designed to limit diode breakdown current to safe levels during transient events.

Data Register

The 8-bit Data Register is a "parallel-input, serial-output" register that samples the input channels and reads-out the data to the Serial Data Output. The register is read via the SDO output as described in Figure 4 and Figure 5. A low input level results in a Logic 0, and a high input level results in a Logic 1.

Configuration Register

The 8-bit Configuration Register is a "serial-input, parallel-output with data latch" register that individually configures each AFE input as either GND/OPEN or 28V/OPEN format. The register is programmed via the serial data input as described in Figure 6 and Figure 7. Logic 0 sets the respective input to 28V/OPEN mode (pull-down); Logic 1 sets the respective input to GND/OPEN mode (pull-up).

The register is Reset to 0's when the Vcc Logic Supply voltage transitions from low to hi, thus initializing the AFE inputs to a pull-down state.

Serial Interface

The DEI1160 incorporates a serial IO interface for programming the Discrete Input configuration and for reading the Discrete Input status. Refer to Figure 2. The interface is SPI compatible and consists of /CS, SEL, SCLK, SDO, and SDI signals. Waveform Figures 4 – 7 depict the Data Read sequence and Configuration Write sequence for both 8-Bit cycles and also 16 bit "daisy chain" applications.

Power Up Initialization

The DEI1160 incorporates an on-chip power-up reset circuit and power sequencing provisions to force the DIN inputs to the 28V/Open (internal pull down) state upon power. The reset circuit monitors the VCC logic supply and forces the Configuration Register to the Logic 0 (28V/Open) while VCC is stabilizing. The AFE circuit is designed to present the 28V/Open (internal pull down) condition when VDD supply is present and VCC is below operational voltage.

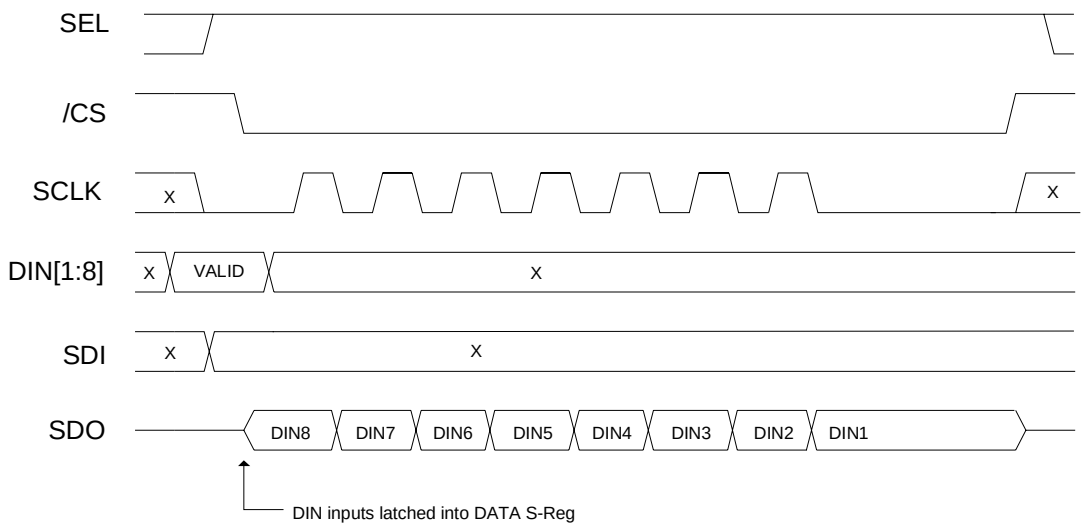


Figure 4 Read Data Register

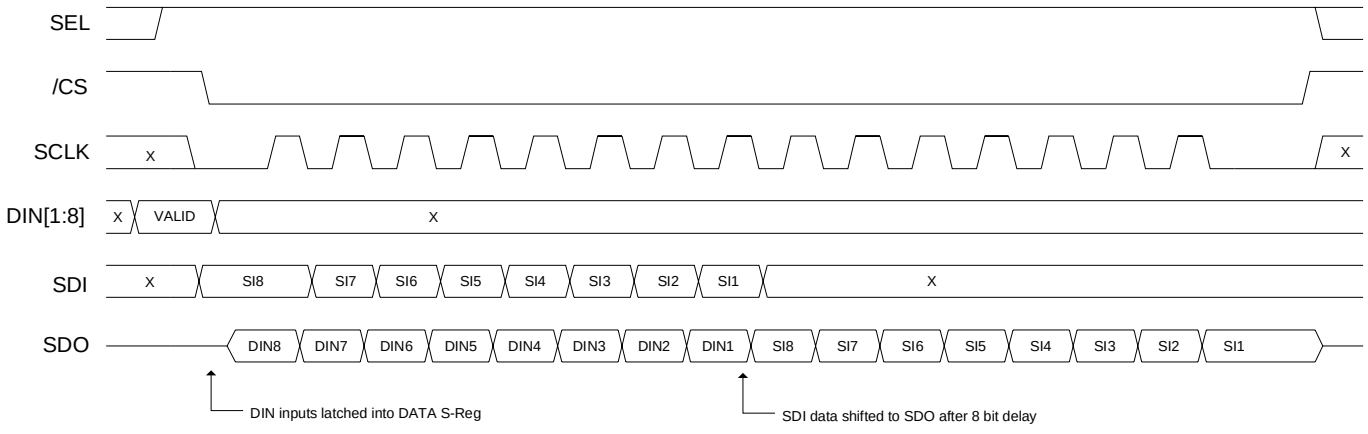


Figure 5 Read Data Register, 16 Bit Daisy Chain

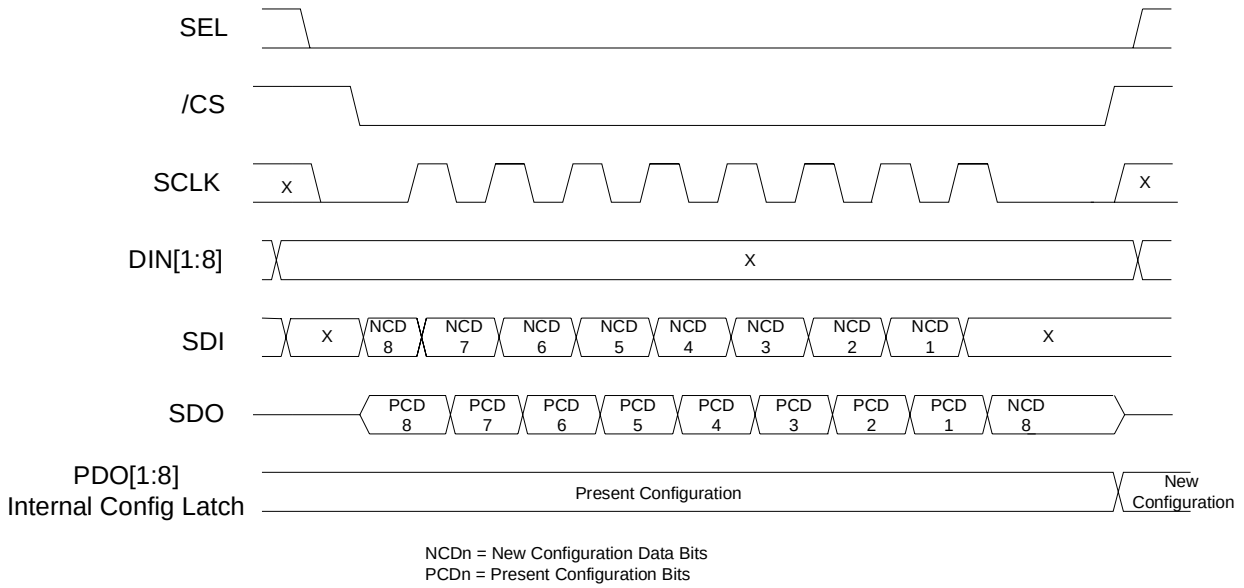


Figure 6 Write Configuration Register

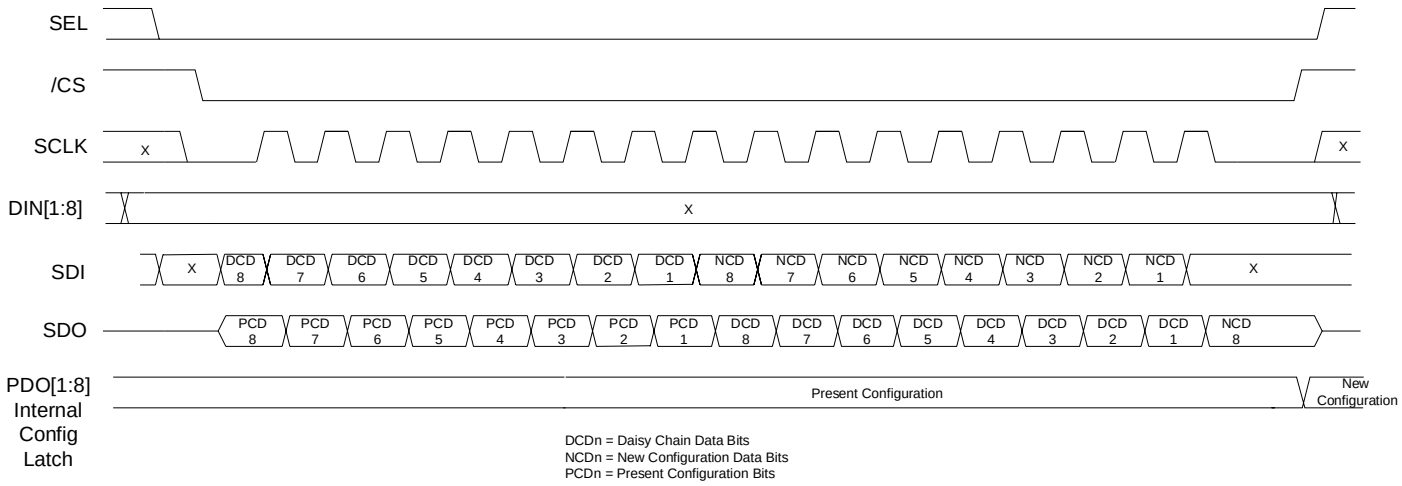


Figure 7 Write Configuration Register, 16 bit Daisy Chain

LIGHTNING PROTECTION

DINn inputs are designed to survive lightning induced transients as defined by RTCA DO160E, Section 22, Cat A3 and B3, Waveforms 3, 4, and 5A, Level 3. See waveforms below.

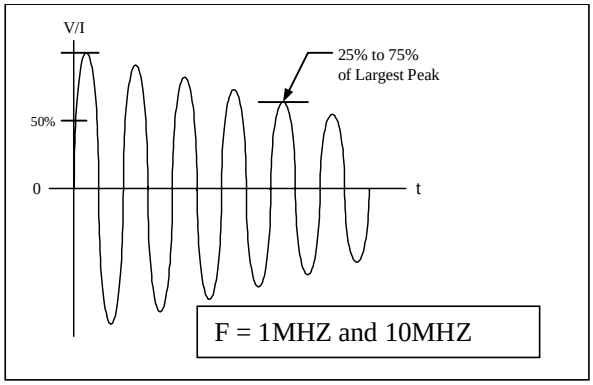


Figure 8 Voltage / Current Waveform 3

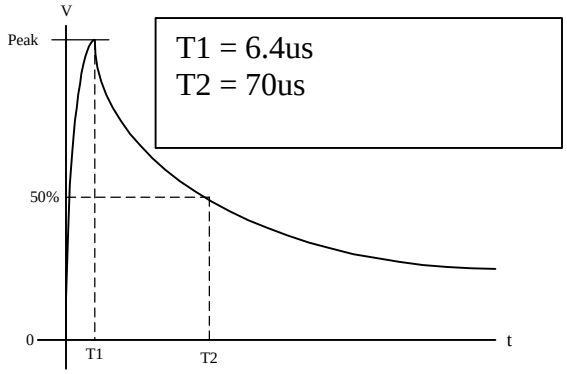


Figure 9 Voltage Waveform 4

Waveform Source Impedance characteristics:

- Waveform 3 Voc/Isc = 600V / 24A => 25 Ohms
- Waveform 4 Voc/Isc = 500 V / 100A => 5 Ohms*
- Waveform 5A Voc / Isc = 500V / 500A => 1 Ohm*

*Amplitude tolerances are +20%, -0%.

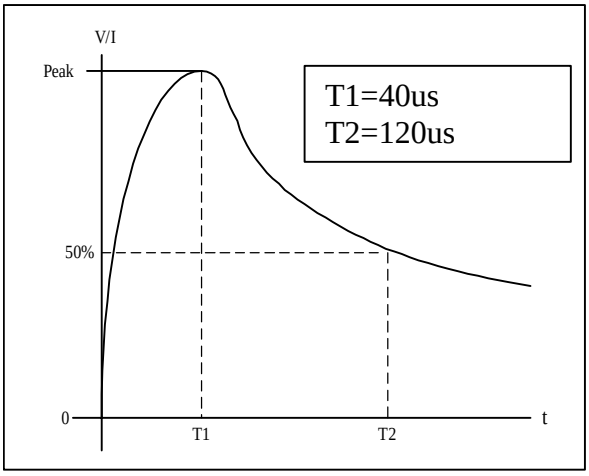


Figure 10 Current/Voltage Waveform 5A

ELECTRICAL DESCRIPTION

Table 3 Absolute Maximum Ratings

PARAMETER		MIN	MAX	UNITS
Vcc Supply Voltage		-0.3	+7.0	V
Vdd Supply Voltage		-0.3	18	V
Operating Temperature Plastic Package		-55	+125	°C
Storage Temperature Plastic Package		-55	+150	°C
Input Voltage				
DIN[1:8]	Continuous	-10	+49	V
	DO160E, Waveform 3, Level 3	-600	+600	V
	DO160E, Waveform 4 and 5, Level 3+	-600	+600	V
	DO160E, Abnormal Surge Voltage, 100ms		80	V
Logic Inputs		-1.5	VCC + 1.5	V
DOUT		-0.5	VCC + 0.5	V
Power Dissipation @ 125 °C: (> 10 Sec) 16L SOIC			0.3	W
Junction Temperature: Tjmax, Plastic Packages			145	°C
ESD per JEDEC A114-A Human Body Model Logic and Supply pins DIN pins			2000 1000	V
Peak Body Temperature (10 sec duration)			235	°C

Notes:
1. Stresses above absolute maximum ratings may cause permanent damage to the device.
2. Voltages referenced to Ground

Table 4 Recommended Operating Conditions

PARAMETER	SYMBOL	CONDITIONS
Supply Voltage	VCC VDD	5.0V±10%, 3.3V±10% 15V±10%
Logic Inputs and Outputs		0 to VCC
Discrete Inputs	DIN[1:8]	0 to 40V
Operating Temperature Plastic	Ta	-55 to +125 ºC

Table 5 DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS (1)	LIMITS			UNIT
			MIN	NOM	MAX	
Logic Inputs/Outputs						
V_{IH}	HI level input voltage	VCC = 5V VCC = 3.3V	3.1 2.0			V
V_{IL}	LO level input voltage				0.8	V
V_{Ihst}	Input hysteresis voltage, SCLK input	(3)	50			mV
V_{OH}	HI level output voltage	IOUT = -20uA	VCC – 0.1		VCC	V
		IOUT = -4mA, Vcc = 3V	2.4		3	V
V_{OL}	LO level output voltage	IOUT = 20uA			0.1	V
		IOUT = 4mA, Vcc = 3V			0.4	V
I_{IN}	Input leakage	Vin = Vcc or GND	-10		10	uA
I_{OZ}	3-state leakage current	Output in Hi Impedance state. VOUT = VIHmin, VILmax	-10		10	uA
Discrete Inputs, Configured as Ground/Open (internal pull-up)						
V_{IH}	HI level input voltage		14		49	V
R_{IH}	HI level Din-to-GND resistance	Resistor from Din to GND to guarantee HI input condition.	50K			Ohm
I_{IH}	HI level input current	Vin = 28V, VDD = 15V Vin = 49V, VDD = 15V		0 1.7	240	uA mA
V_{IL}	LO level input voltage		-3		3.5	V
R_{IL}	LO level Din-to-GND resistance	Resistor from Din to GND to guarantee LO input condition.			500	Ohm
I_{IL}	LO level input current	Vin = 0V, VDD = 15V	-0.9	-1.1	-1.25	mA
V_{Ihst}	Input hysteresis voltage		1			V
Discrete Inputs, Configured as 28V/Open (internal pull-down)						
V_{IH}	HI level input voltage		14		49	V
I_{IH}	HI level input current	Vin = 28V, VDD = 15V	1.1	1.3	1.75	mA
V_{IL}	LO level input voltage		-3		3.5	V
I_{IL}	LO level input current	Vin = 1V, VDD = 15V		48	100	uA
V_{Ihst}	Input hysteresis voltage		1			V
Power Supply						
ICC	Max quiescent logic supply current	Vin(logic) = Vcc or GND VIN[1:8]= open		1	13.5	mA
IDD	Max quiescent analog supply current	Vin(logic) = Vcc or GND VIN[1:8]= Open VIN[1:8]= GND, All configured as Ground/Open		2 6	25 34	mA

Notes:

1. Ta = -55 to +125 ºC. VDD = +15V±10%, VCC = 3.0 to 5.5V unless otherwise noted.
2. Current flowing into device is positive. Current flowing out of device is negative. Voltages are referenced to Ground.
3. Guaranteed by design. Not production tested.

Table 6 AC Electrical Characteristics (4)

SYMBOL	PARAMETER	CONDITIONS (6, 7)	LIMITS		UNIT
			Min	Max	
f_{MAX}	SCLK frequency. (50% duty cycle) (5)	VCC = 3.0V VCC = 4.5V		8.6 14	MHz
t_W	SCLK pulse width. (5)	VCC = 3.0V VCC = 4.5V	50 30		ns
t_{su1}	Setup time, SCLK low to /CS↓.	VCC = 3.0V VCC = 4.5V	25 25		ns
t_{h1}	Hold time, /CS↓ to SCLK↑.	VCC = 3.0V VCC = 4.5V	30 20		ns
t_{su2}	Setup time, DIN valid to /CS↓.		2		us
t_{h2}	Hold time, /CS↓ to DIN not valid.		15		ns
t_{su3}	Setup time, SDIN valid to SCLK↑.	VCC = 3.0V VCC = 4.5V	25 20		ns
t_{h3}	Hold time, SCLK↑ to SDIN not valid.	VCC = 3.0V VCC = 4.5V	25 20		ns
t_{su4}	Setup time, SEL valid to /CS↓.	VCC = 3.0V VCC = 4.5V	30 25		ns
t_{h4}	Hold time, SEL valid to /CS↑.	VCC = 3.0V VCC = 4.5V	25 20		ns
t_{p1}	Propagation delay, /CS↓ to DOUT valid. (1)	VCC = 3.0V VCC = 4.5V		105 60	ns
t_{p2}	Propagation delay, SCLK↑ to DOUT valid. (1)	VCC = 3.0V VCC = 4.5V		90 50	ns
t_{p3}	Propagation delay, /CS↑ to DOUT HI-Z. (1) (2) (3)	VCC = 3.0V VCC = 4.5V		80 60	ns
t_{p4}	Delay time between /CS active. (5)	VCC = 3.0V VCC = 4.5V	20 20		ns
C_{in}	Maximum logic input pin Capacitance. (5)			10	pf
C_{out}	Maximum DOUT pin capacitance, output in HI-Z state. (5)			15	pf

Notes:
1. DOUT loaded with 50pF to GND.
2. DOUT loaded with 1K Ohms to GND for Hi output, 1K Ohms to VCC for Low output.
3. Timing measured at 25%VCC for “0” to Hi-Z, 75%VCC for “1” to Hi-Z.
4. Sample tested on lot basis.
5. Not tested
6. Ta = -55 to +125ºC. VDD = +15V, VIL = 0V, VIH = VCC unless otherwise noted.
7. Measurements made at 50%VCC.

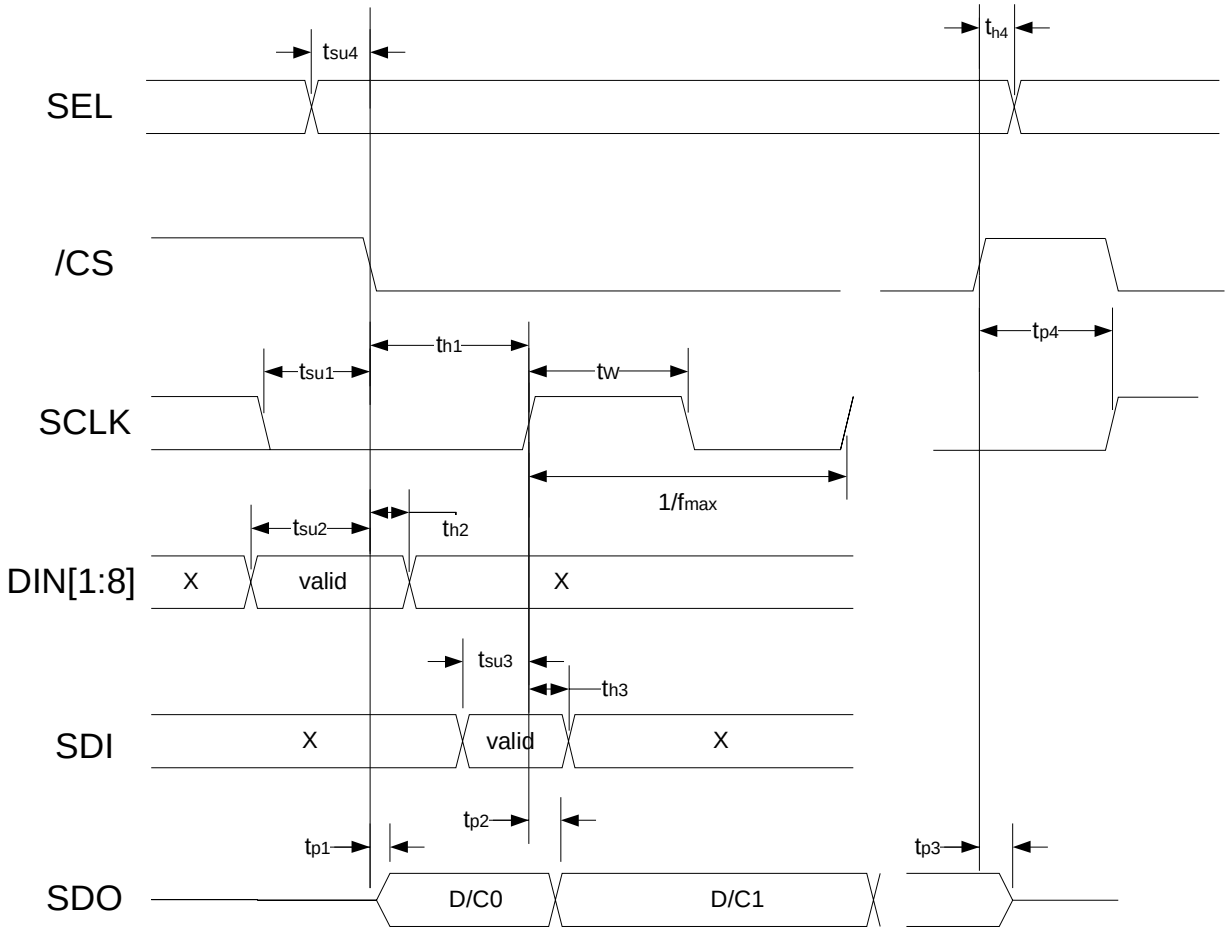


Figure 11 Switching Waveforms

ORDERING INFORMATION

Part Number	Marking	Package	Burn In	Temperature
DEI1160-SES	DEI1160 SES	16 EP SOIC	No	-55 / +85 ºC
DEI1160-SMS	DEI1160 SMS	16 EP SOIC	No	-55 / +125 ºC

DEI reserves the right to make changes to any products or specifications herein. DEI makes no warranty, representation, or guarantee regarding suitability of its products for any particular purpose.

APPLICATION INFORMATION

The 1160 power dissipation varies with channel configuration and operating conditions. Figure 12 shows the device package power dissipation for various conditions. This includes the contributions from Supply currents and Input currents. The four curves are as follows:

Table 7 Legend for Power Dissipation Curves

CURVE ID	CONFIGURATION	SUPPLY VOLTAGE / TEMPERATURE	PROCESS CONDITION	ACTIVE CHANNEL
+28V/OPN-Nom	All channels = 28V/OPN	3.3V, 15V / 27ºC	Typical	28V
+28V/OPN-Wst	All channels = 28V/OPN	5.5V, 16.5V/ 125ºC	Worst case (Low resistance and fast transistors)	28V
GND/OPN-Nom	All channels = GND/OPN	3.3V, 15V / 27ºC	Typical	GND
GND/OPN-Wst	All channels = GND/OPN	5.5V, 16.5V / 125ºC	Worst case (Low resistance and fast transistors)	GND

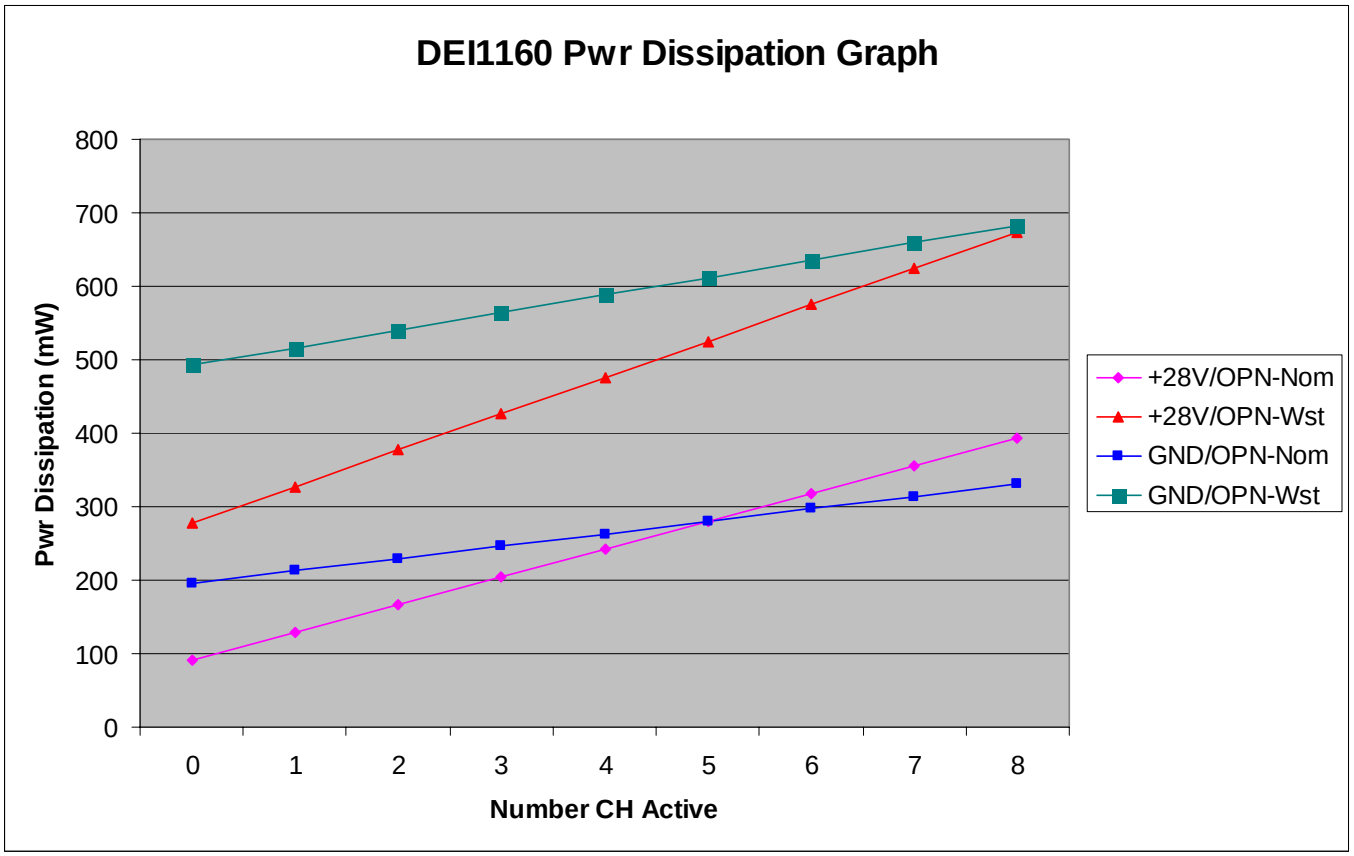
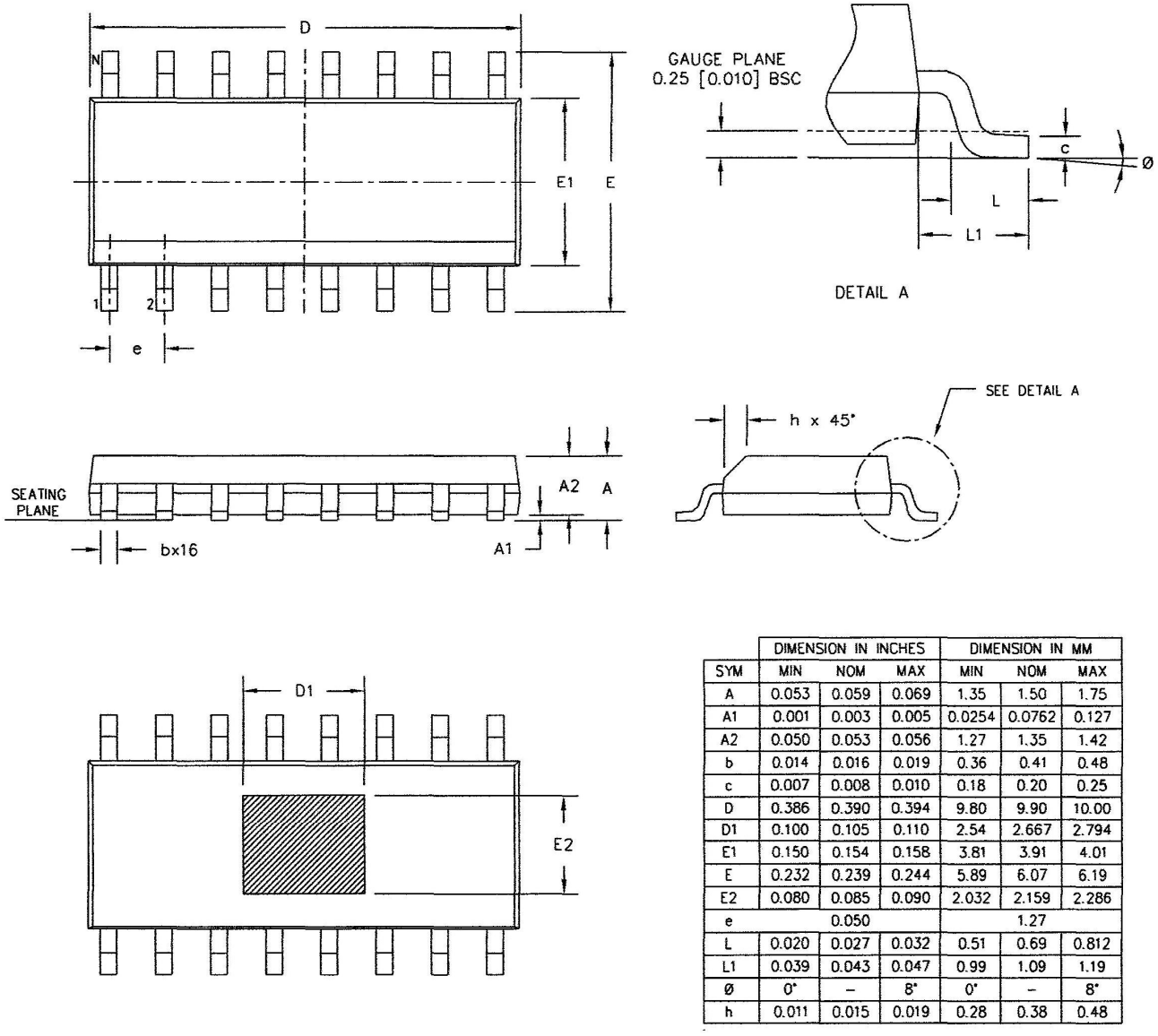


Figure 12 Power Dissipation for Various Conditions

PACKAGE DESCRIPTION - 16L Narrow Body EP SOIC

Moisture Sensitivity:	MSL 1 / 260˚C
Θja:	~40˚C/W (Mounted on 4 layer PCB with exposed pad soldered to PCB land with thermal vias to internal GND plane)
Θjc:	~10˚C/W
Lead Finish:	SnPb plated
Exposed Pad:	Electrically Isolated from IC terminals.

The PCB design and layout is a significant factor in determining thermal resistance (Θja) of the IC package**.** Use maximum trace width on all power and signal connections at the IC. These traces serve as heat spreaders which improve heat flow from the IC leads**.** The exposed heat sink pad of the SOIC package should be soldered to a heat-spreader land pattern on the PCB. The IC exposed pad is electrically isolated, so the PCB land may be at any potential, typically GND, for the best heat sink. Maximize the PCB land size by extending it beyond the IC outline if possible. A grid of thermal VIAs, which drop down and connect to the buried copper plane(s), should be placed under the heat-spreader land. A typical VIA grid is 12mil holes on a 50mil pitch. The barrel is plated to about 1.0 ounce copper. Use as many VIAs as space allows. VIAs should be plugged to prevent voids being formed between the exposed pad and PCB heat-spreader land due to solder escaping by the capillary effect. This can be avoided by tenting the VIAs with solder mask.



	DIMENSION IN INCHES			DIMENSION IN MM		
SYM	MIN	NOM	MAX	MIN	NOM	MAX
A	0.053	0.059	0.069	1.35	1.50	1.75
A1	0.001	0.003	0.005	0.0254	0.0762	0.127
A2	0.050	0.053	0.056	1.27	1.35	1.42
b	0.014	0.016	0.019	0.36	0.41	0.48
c	0.007	0.008	0.010	0.18	0.20	0.25
D	0.386	0.390	0.394	9.80	9.90	10.00
D1	0.100	0.105	0.110	2.54	2.667	2.794
E1	0.150	0.154	0.158	3.81	3.91	4.01
E	0.232	0.239	0.244	5.89	6.07	6.19
E2	0.080	0.085	0.090	2.032	2.159	2.286
e		0.050			1.27	
L	0.020	0.027	0.032	0.51	0.69	0.812
L1	0.039	0.043	0.047	0.99	1.09	1.19
Ø	0°	–	8°	0°	–	8°
h	0.011	0.015	0.019	0.28	0.38	0.48

Figure 13 16 Lead Narrow Body EP SOIC Outline