GS1582 Multi-Rate Serializer with Cable Driver, Audio Multiplexer and ClockCleaner™

Key Features

- HD-SDI, SD-SDI, DVB-ASI transmitter with audio embedding
- Integrated SMPTE 292M and 259M-C compliant cable driver
- Integrated ClockCleaner™
- User selectable video processing features, including:
  - Generic ancillary data insertion
  - Support for HVF or EIA/CEA-861 timing input
  - Automatic standard detection and indication
  - Enhanced SMPTE 352M payload identifier generation and insertion
  - TRS, CRC, ANC data checksum, and line number calculation and insertion
  - EDH packet generation and insertion
  - Illegal code remapping
  - SMPTE 292M and SMPTE 259M-C compliant scrambling and NRZ → NRZI encoding
  - Blanking of input HANC and VANC space
- User selectable audio processing features, including:
  - SMPTE 299M and SMPTE 272M-A/C compliant audio embedding
  - Support for up to 8 channels
  - Support for audio group replacement
- JTAG test interface
- 1.8V core and 3.3V charge pump power supply
- 1.8V and 3.3V digital I/O support
- Low power standby mode
- Operating temperature range: -20°C to +85°C
- Pb-free, RoHS compliant, 11mm x 11mm 100-ball BGA package

Applications

- SMPTE 292M and SMPTE 259M-C Serial Digital Interfaces
- DVB-ASI Serial Digital Interfaces

Description

The GS1582 is the next generation multi-standard serializer with an integrated cable driver. The device provides robust parallel to serial conversion, generating a SMPTE 292M/259M-C compliant serial digital output signal. The integrated cable driver features an output disable (high impedance) mode and an adjustable signal swing. Data input is accepted in 20-bit parallel format or 10-bit parallel format. An associated parallel clock input must be provided at the appropriate operating frequency; 74.25/74.1758/13.5MHz (20-bit mode) or 148.5/148.352/27MHz (10-bit mode).

The GS1582 features an internal PLL which, if desired, can be configured for a loop bandwidth below 100kHz. When used in conjunction with the GO1555 Voltage Controlled Oscillator, the GS1582 can tolerate well in excess of 300ps jitter on the input PCLK and still provide output jitter within SMPTE specifications.

In addition to serializing the input, the GS1582 performs NRZ-to-NRZI encoding and scrambling as per SMPTE 292M/259M-C when operating in SMPTE mode. When operating in DVB-ASI mode, the device will insert K28.5 sync characters and 8b/10b encode the data prior to serialization. The device also provides a range of other data processing functions. All processing features are optional and may be enabled/disabled via external control pin(s) and/or host interface programming.

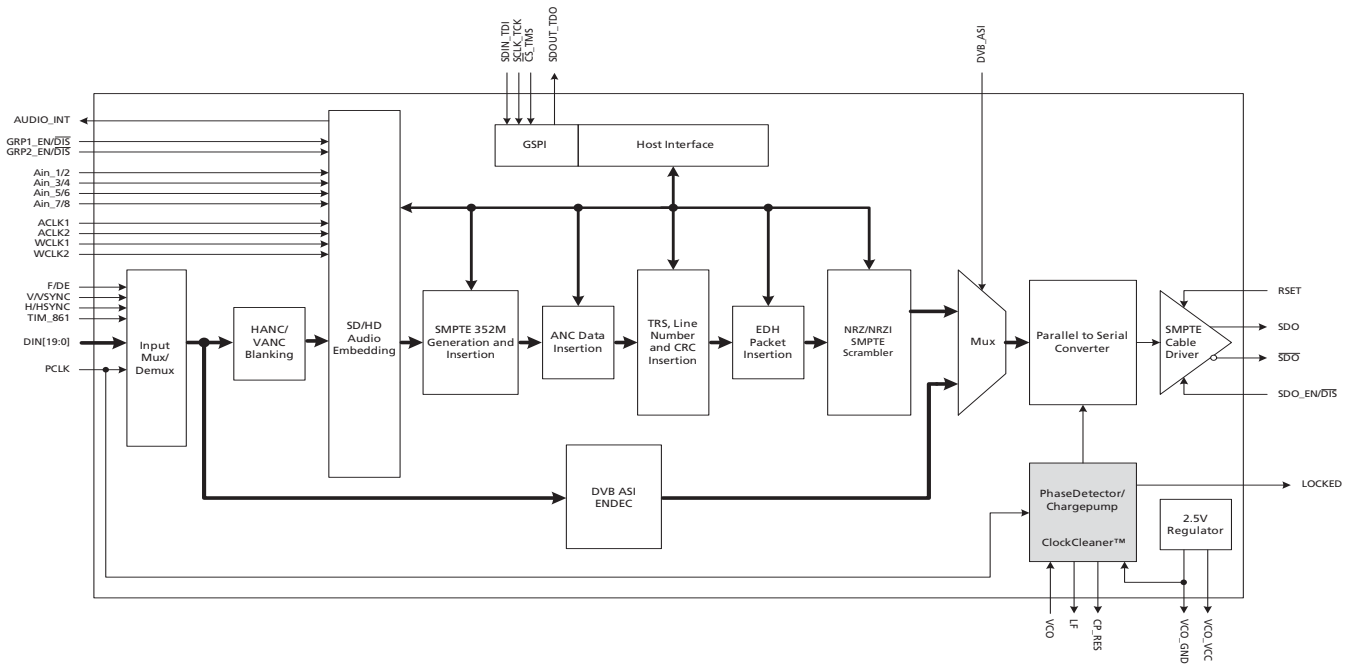
The GS1582 can embed up to 8 channels of audio into the video data stream in accordance with SMPTE 299M and SMPTE 272M. The audio input signal formats supported by the device include AES/EBU and I^2S serial digital formats with a 16, 20 or 24 bit sample size and a 48 kHz sample rate. Additional audio processing features include individual channel enable, channel swap, group swap, ECC generation and audio channel status insertion.

Typical power consumption, including the GO1555 VCO, is 500mW. The standby feature allows the power to be reduced to 125mW. Power may be reduced to less than

10mW by also removing the power to the cable driver and eliminating transitions at the parallel data and clock inputs.

The GS1582 is Pb-free and RoHS compliant.

Functional Block Diagram



GS1582 Functional Block Diagram

Revision History

Version	ECR	PCN	Date	Changes and/or Modifications
3	151526	52183	March 2009	Changed Parallel Input Data Hold Time from 2ns to 0.8ns in Table 2-3: AC Electrical Characteristics.
2	150785	51685	October 2008	Changed Figure 4-30: GSPI Write Mode Timing.
1	146167	–	November 2007	Converted to a Data Sheet. Updates to: Note 4 in Table 2-2 on page 20, Audio Modes of Operation on page 38, Arbitrary, SMPTE 352M & EDH Packet Detect on page 40, Table 4-3 on page 39, 4.8 Ancillary Data Insertion, Separate Line Mode on page 64, Concatenated Mode on page 65, Command Word Description on page 79, 4.13 GSPI Host Interface, Table 4-33, 4.9.3 Video Standard Indication, 2.3 DC Electrical Characteristics, 4.9.4.4 Ancillary Data Checksum Generation and Insertion, Table 2-3: AC Electrical Characteristics, 4.7.14 Interrupt Control,4.9.4.1 SMPTE 352M Payload Identifier Packet Insertion, 4.7.9.1 SD Formats and 4.7.9.2 HD Formats.
0	145472	–	June 2007	Converted to Preliminary Data Sheet. Changes were made in the following areas; Table 1-1: Pin Descriptions, 2.1 Absolute Maximum Ratings, 2.2 Recommended Operating Conditions, 2.3 DC Electrical Characteristics, 2.4 AC Electrical Characteristics, 4.3 SMPTE Mode, 4.3.1 HVF Timing, 4.6 Standby Mode, 4.7.20 Audio Word Clock, 4.8 Ancillary Data Insertion, 4.8.3 VANC Insertion, 4.9.4.1 SMPTE 352M Payload Identifier Packet Insertion, 4.9.4.3 EDH Generation and Insertion, 4.11.2 Loop Filter, 4.11.3 Lock Detect Output, 4.13.1 Command Word Description, Table 4-44: SD Audio Configuration and Status Registers, Table 4-45: HD Audio Configuration and Status Registers, 4.15 Device Reset, 5.1 Typical Application Circuit (Part A), 7.1 Package Dimensions, 7.2 Packaging Data, 7.2 Packaging Data, 7.5 Ordering Information,
B	144894	–	April 2007	Changed pin F4 to RSV and added drive strength values for pin H4, H7, and J9 in Pin Assignment and Pin Descriptions. Modified input voltage range parameter in Absolute Maximum Ratings. Updated serial output intrinsic jitter value in AC Electrical Characteristics. Added digital input/output circuits in Section 3. Added note to 4.7.20 Audio Word Clock.
A	141222	–	March 2007	New Document.

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1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	DIN17	DIN18	F/DE	H/HSYNC	CORE _VDD	PD_VDD	LF	VCO_ VCC	VCO	CP_VDD
B	DIN15	DIN16	DIN19	PCLK	CORE _GND	PD_VDD	CP_RES	VCO_ GND	VCO_ GND	CP_GND
C	DIN13	DIN14	DIN12	V/VSYNC	CORE _GND	PD_GND	PD_GND	PD_GND	CD_GND	SDO
D	DIN11	DIN10	STANDBY	SDO_EN/ $\overline{\text{DIS}}$	CORE _GND	NC	NC	NC	CD_GND	$\overline{\text{SDO}}$
E	CORE _VDD	CORE _GND	SD/$\overline{\text{HD}}$	NC	CORE _GND	CORE _GND	CORE _GND	NC	CD_GND	CD_VDD
F	DIN9	DIN8	DETECT _TRS	RSV	CORE _GND	CORE _GND	CORE _GND	NC	CD_GND	RSET
G	IO_VDD	IO_GND	TIM 861	20bit/ $\overline{\text{10bit}}$	DVB_ASI	$\overline{\text{SMPTE_ BYPASS}}$	IOPROC _EN/$\overline{\text{DIS}}$	$\overline{\text{RESET}}$	CORE _GND	CORE _VDD
H	DIN7	DIN6	$\overline{\text{ANC_ BLANK}}$	LOCKED	GRP2_ EN/$\overline{\text{DIS}}$	GRP1_ EN/$\overline{\text{DIS}}$	AUDIO _INT	$\overline{\text{JTAG/ HOST}}$	IO_GND	IO_VDD
J	DIN5	DIN4	DIN1	Ain_5/6	WCLK_2	Ain_1/2	WCLK_1	CORE _GND	SDOUT _TDO	SCLK _TCLK
K	DIN3	DIN2	DIN0	Ain_7/8	ACLK_2	Ain_3/4	ACLK_1	CORE _VDD	CS_ TMS	SDIN _TDI

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Timing	Type	Description	
A1, A2, B1, B2, B3, C1, C2, C3, D1, D2	DIN[19:10]	Synchronous with PCLK	Input	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DIN19 is the MSB and DIN10 is the LSB.	
				HD 20-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = HIGH	Luma data input in SMPTE mode $\overline{SMPTE_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{HD}$ = LOW 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode $\overline{SMPTE_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = LOW
				SD 20-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = HIGH	Luma data input in SMPTE mode $\overline{SMPTE_BYPASS}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data input in DVB-ASI mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{HD}$ = HIGH 20bit/$\overline{10bit}$ = LOW	Multiplexed Luma and Chroma data input in SMPTE mode $\overline{SMPTE_BYPASS}$ = HIGH DVB_ASI = LOW Data input in data through mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = LOW DVB-ASI data input in DVB-ASI mode $\overline{SMPTE_BYPASS}$ = LOW DVB_ASI = HIGH

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
A3	F/DE	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: Used to indicate the ODD / EVEN field of the video signal when DETECT_TRS is set LOW. The device will set the F bit in all outgoing TRS signals for the entire period that the F input signal is HIGH (IOPROC_EN/$\overline{DIS}$ must also be HIGH). The F signal should be set HIGH for the entire period of field 2 and should be set LOW for all lines in field 1 and for all lines in progressive scan systems. The F signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The DE signal is used to indicate the active video period. DE is HIGH for active data and LOW for blanking. See Section 4.3.1 and Section 4.3.2 for timing details. The DE signal is ignored when DETECT_TRS = HIGH.
A4	H/HSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: The H signal is used to indicate the portion of the video line containing active video data, when DETECT_TRS is set low. Active Line Blanking The H signal should be set HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words, and LOW otherwise. This is the default setting. TRS Based Blanking (H_CONFIG = 1_h) The H signal should be set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS ID words, and LOW otherwise. The H signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The HSYNC signal indicates horizontal timing. See Section 4.3.1 for timing details. The HSYNC signal is ignored when DETECT_TRS = HIGH.
A5, E1, G10, K8	CORE_VDD	Non Synchronous	Input Power	Power supply connection for the digital core logic. Connect to +1.8V DC digital.
A6, B6	PD_VDD	Analog	Input Power	Power supply connection for the phase detector. Connect to +1.8V DC analog.
A7	LF	Analog	Input	PLL loop filter connection.
A8	VCO_VCC	Analog	Output Power	Power supply for the external voltage controlled oscillator. 2.5V DC supplied by the device to the external VCO.
A9	VCO	Analog	Input	Input from external VCO.
A10	CP_VDD	Analog	Input Power	Power supply connection for the charge pump and on chip VCO regulator. Connect to +3.3V DC analog.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
B4	PCLK	–	Input	PARALLEL DATA BUS CLOCK Signal levels are LVCMOS/LVTTL compatible.
				HD 20-bit mode — PCLK = 74.25MHz or 74.25/1.001MHz
				HD 10-bit mode — PCLK = 148.5MHz or 148.5/1.001MHz
				SD 20-bit mode — PCLK = 13.5MHz
				SD 10-bit mode — PCLK = 27MHz
B5, C5, D5, E2, E5, E6, E7, F5, F6, F7, G9, J8	CORE_GND	Non Synchronous	Input Power	Ground connection for the digital core logic. Connect to digital GND.
C6, C7, C8	PD_GND	Analog	Input Power	Ground connection for the phase detector. Connect to analog GND.
B7	CP_RES	–	Input	Charge pump current setting resistor.
B8, B9	VCO_GND	Analog	Output Power	Ground pins for the VCO.
B10	CP_GND	Analog	Input Power	Ground pin for the charge pump and PLL.
C4	V/VSYNC	Synchronous with PCLK	Input	PARALLEL DATA TIMING Signal levels are LVCMOS/LVTTL compatible. TIM_861 = LOW: The V signal is used to indicate the portion of the video field/frame that is used for vertical blanking, when DETECT_TRS is set LOW. The V signal should be set HIGH for the entire vertical blanking period and should be set LOW for all lines outside of the vertical blanking interval. The V signal is ignored when DETECT_TRS = HIGH. TIM_861 = HIGH: The VSYNC signal indicates vertical timing. See Section 4.3.1 for timing details. The VSYNC signal is ignored when DETECT_TRS = HIGH.
C9, D9, E9, F9	CD_GND	Analog	Input Power	Ground connection for the serial digital cable driver. Connect to analog GND.
C10, D10	SDO, $\overline{\text{SDO}}$	Analog	Output	Serial digital output signal operating at 1.485Gb/s, 1.485/1.001Gb/s, or 270Mb/s. The slew rate of these outputs is automatically controlled to meet SMPTE 292M and 259M requirements according to the setting of the SD/$\overline{\text{HD}}$ pin. Serial digital output signal from the internal cable driver. NOTE: The SDO/$\overline{\text{SDO}}$ output signals will be set to high impedance when $\overline{\text{RESET}}$ = LOW.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
D3	STANDBY	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Power down input. When set HIGH, the device will be in standby mode.
D4	SDO_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable the serial digital output stage. When set LOW, the serial digital output signals SDO and $\overline{\text{SDO}}$ are disabled and become high impedance. When set HIGH, the serial digital output signals SDO and $\overline{\text{SDO}}$ are enabled. The SDO and $\overline{\text{SDO}}$ outputs will also be high impedance when the $\overline{\text{RESET}}$ pin is LOW.
D6, D7, D8, E4, E8, F8	NC	–	–	No connect. Not connected internally.
E3	SD/$\overline{\text{HD}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set LOW, the device will be configured to transmit signals of 1.485Gb/s - 1.485/1.001Gb/s rates only. When set HIGH, the device will be configured to transmit signals of a 270Mb/s rate only.
E10	CD_VDD	Analog	Input Power	Power supply connection for the serial digital cable driver. Connect to +3.3V DC analog.
F1, F2, H1, H2, J1, J2, J3, K1, K2, K3	DIN[9:0]	Synchronous with PCLK	Input	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible. DIN9 is the MSB and DIN0 is the LSB.
				HD 20-bit mode SD/$\overline{\text{HD}}$ = LOW 20bit/$\overline{\text{10bit}}$ = HIGH — Chroma data input in SMPTE mode $\overline{\text{SMPTE_BYPASS}}$ =HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{\text{SMPTE_BYPASS}}$ = LOW DVB_ASI = LOW
				HD 10-bit mode SD/$\overline{\text{HD}}$ = LOW 20bit/$\overline{\text{10bit}}$ = LOW — High impedance in all modes.
				SD 20-bit mode SD/$\overline{\text{HD}}$ = HIGH 20bit/$\overline{\text{10bit}}$ = HIGH — Chroma data input in SMPTE mode $\overline{\text{SMPTE_BYPASS}}$ = HIGH DVB_ASI = LOW Data input in Data-Through mode $\overline{\text{SMPTE_BYPASS}}$ = LOW DVB_ASI = LOW Forced low in DVB-ASI mode $\overline{\text{SMPTE_BYPASS}}$ = LOW DVB_ASI = HIGH
				SD 10-bit mode SD/$\overline{\text{HD}}$ = HIGH 20bit/$\overline{\text{10bit}}$ = LOW — High impedance in all modes.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
F3	DETECT_TRS	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select external HVF timing mode or TRS Extraction timing mode. When DETECT_TRS = LOW, the device will use timing from the externally supplied H:V:F or CEA-861 timing signals, dependent on the state of the TIM_861 pin. When DETECT_TRS = HIGH, the device will extract timing from TRS signals embedded in the supplied video stream.
F4	RSV	–	–	Reserved. Do not connect.
F10	RSET	Analog	Input	An external 1% resistor connected to this input is used to set the SDO/$\overline{\text{SDO}}$ output amplitude.
G1, H10	IO_VDD	Non Synchronous	Input Power	Power supply connection for digital I/O buffers. Connect to +3.3V or +1.8V DC digital.
G2, H9	IO_GND	Non Synchronous	Input Power	Ground connection for digital I/O buffers. Connect to digital GND.
G3	TIM_861	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select external CEA-861 timing mode. When DETECT_TRS = LOW and TIM_861 = LOW, the device will use externally supplied H:V:F timing signals. When DETECT_TRS = LOW and TIM_861 = HIGH, the device will use externally supplied HSYNC, VSYNC, DE timing signals. When DETECT_TRS = HIGH, the device will extract timing from TRS signals embedded in the supplied video stream.
G4	20bit/$\overline{\text{10bit}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select the input data bus width.
G5	DVB_ASI	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When set HIGH, the device is configured for the transmission of DVB-ASI data in SD mode (SD/$\overline{\text{HD}}$ = HIGH). When set LOW, the device will not support the encoding of DVB-ASI data. NOTE: When operating in DVB-ASI mode the SD/$\overline{\text{HD}}$ pin must be set HIGH and $\overline{\text{SMPTE_BYPASS}}$ must be set LOW.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
G6	$\overline{\text{SMPTE_BYPASS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable all forms of encoding/decoding, scrambling and EDH insertion. When set LOW, the device will operate in data through mode (DVB_ASI = LOW), or in DVB-ASI mode (DVB_ASI = HIGH). No SMPTE scrambling will take place and none of the I/O processing features of the device will be available when $\overline{\text{SMPTE_BYPASS}}$ is set LOW. When set HIGH, the device will perform SMPTE scrambling and I/O processing.
G7	IOPROC_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable I/O processing features. When set HIGH, the following I/O processing features of the device are enabled: • Audio Embedding • EDH Packet Generation and Insertion (SD-only) • SMPTE 352M Packet Generation and Insertion • ANC Data Checksum Calculation • ANC Data Insertion • Line-based CRC Generation and Insertion (HD-only) • Line Number Generation and Insertion (HD-only) • TRS Generation and Insertion • Illegal Code Remapping To enable a subset of these features, set IOPROC_EN/$\overline{\text{DIS}}$ = HIGH and disable the individual feature(s) in the IOPROC_DISABLE register accessible via the host interface. When set LOW, the I/O processing features of the device are disabled, and can not be enabled by changing the settings in the IOPROC_DISABLE register.
G8	$\overline{\text{RESET}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG test sequence. Normal Mode (JTAG/$\overline{\text{HOST}}$ = LOW) When set LOW, all functional blocks will be set to default conditions and all input and output signals become high impedance including the serial digital outputs SDO and $\overline{\text{SDO}}$. When set HIGH, normal operation of the device resumes 10usec after the low to high transition of the $\overline{\text{RESET}}$ signal. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) When set LOW, all functional blocks will be set to default and the JTAG test sequence will be held in reset. When set HIGH, normal operation of the JTAG test sequence resumes.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
H3	$\overline{\text{ANC_BLANK}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable or disable ANC data blanking. When set LOW, the HANC and VANC data is mapped to the appropriate blanking levels.
H4	LOCKED	Synchronous with PCLK	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS / LVTTL compatible. This signal is set HIGH by the device when the internal PLL has achieved lock to the supplied PCLK signal. This pin is set LOW by the device under all other conditions. IO_VDD = 3.3V Drive Strength = 8mA IO_VDD = 1.8V Drive Strength = 4mA
H5	GRP2_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	Enable Input for Audio Group 2.
H6	GRP1_EN/$\overline{\text{DIS}}$	Non Synchronous	Input	Enable Input for Audio Group 1.
H7	AUDIO_INT	Non Synchronous	Output	STATUS SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Summary Interrupt from Audio Processing. This signal is set HIGH by the device to indicate a problem with the audio processing which requires the Host processor to interrogate the interrupt status registers. IO_VDD = 3.3V Drive Strength = 8mA IO_VDD = 1.8V Drive Strength = 4mA
H8	JTAG/$\overline{\text{HOST}}$	Non Synchronous	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG Test Mode or Host Interface Mode. When set HIGH, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured for JTAG boundary scan testing. When set LOW, $\overline{\text{CS}}$_TMS, SDOUT_TDO, SDI_TDI and SCLK_TCK are configured as Gennum Serial Peripheral Interface (GSPI) pins for normal host interface operation.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
J4	AIN_5/6	Synchronous with ACLK_2	Input	Serial Audio Input; Channels 5 and 6.
J5	WCLK_2	Clock	Input	48kHz word clock for Audio Group 2.
J6	AIN_1/2	Synchronous with ACLK_1	Input	Serial Audio Input; Channels 1 and 2.
J7	WCLK_1	Clock	Input	48kHz word clock for Audio Group 1.
J9	SDOUT_TDO	Synchronous with SCLK_TCK	Output	COMMUNICATION SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Output / Test Data Output Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial output, used to read status and configuration information from the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift test results and operates as the JTAG test data output, TDO. NOTE: If the host interface is not being used leave this pin unconnected. IO_VDD = 3.3V Drive Strength = 12mA IO_VDD = 1.8V Drive Strength = 4mA
J10	SCLK_TCK	Non Synchronous	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data Clock / Test Clock. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) SCLK_TCK operates as the host interface burst clock, SCLK. Command and data read/write words are clocked into the device synchronously with this clock. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is the TEST MODE START pin, used to control the operation of the JTAG test clock, TCK. NOTE: If the host interface is not being used, tie this pin HIGH.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Timing	Type	Description
K4	AIN_7/8	Synchronous with ACLK_2	Input	Serial Audio Input; Channels 7 and 8.
K5	ACLK_2	Clock	Input	3.072MHz audio clock for Audio Group 2 (channels 5-8).
K6	AIN_3/4	Synchronous with ACLK_1	Input	Serial Audio Input; Channels 3 and 4.
K7	ACLK_1	Clock	Input	3.072MHz audio clock for Audio Group 1(channels 1-4).
K9	CS_TMS	Synchronous with SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip Select / Test Mode Start. Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) $\overline{\text{CS}}$_TMS operates as the host interface chip select, $\overline{\text{CS}}$, and is active LOW. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) $\overline{\text{CS}}$_TMS operates as the JTAG test mode start, TMS, used to control the operation of the JTAG test, and is active HIGH. NOTE: If the host interface is not being used, tie this pin HIGH.
K10	SDIN_TDI	Synchronous with SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial Data In / Test Data Input Host Mode (JTAG/$\overline{\text{HOST}}$ = LOW) This pin operates as the host interface serial input, SDIN, used to write address and configuration information to the internal registers of the device. JTAG Test Mode (JTAG/$\overline{\text{HOST}}$ = HIGH) This pin is used to shift and operates as the JTAG test data input, TDI. NOTE: If the host interface is not being used, tie this pin HIGH.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Core (CORE_VDD)	-0.3V to +2.1V
Supply Voltage, Analog 1.8V (PD_VDD)	-0.3V to +2.1V
Supply Voltage, I/O (IO_VDD)	-0.3V to +3.6V
Supply Voltage, Analog 3.3V (CP_VDD, CD_VDD)	-0.3V to +3.6V
Input Voltage Range (ACLK, WCLK, AIN, PCLK, DIN)	-0.5V to IO_VDD+0.25V
Input Voltage Range (VCO, CP_RES, LF, RSET)	-0.5V to +3.6V
Input Voltage Range (All other pins)	-0.5V to +5.25V
Ambient Operating Temperature	$-40°C \leq T_A \leq 95°C$
Storage Temperature	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	4000V
ESD Sensitivity, MM (JESD22-A115)	200V

NOTES:

1. Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-1: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	25	85	°C	
Supply Voltage, Digital Core	CORE_VDD	–	1.71	1.8	1.89	V	
Supply Voltage, Phase Detector	PD_VDD	–	1.71	1.8	1.89	V	
Supply Voltage, Charge Pump	CP_VDD	–	3.13	3.3	3.47	V	
Supply Voltage, Cable Driver	CD_VDD	–	3.13	3.3	3.47	V	
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	
Supply Voltage, Digital I/O	IO_VDD	3.3V mode	3.13	3.3	3.47	V	

2.3 DC Electrical Characteristics

Table 2-2: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
External VCO Power Supply Voltage (VCO_VDD)			2.375	2.5	2.625	V	1
+1.8V Supply Current	I_{1V8}	10/20bit HD, Audio Enabled	–	138	165	mA	2,4
		10/20bit HD, Audio Disabled	–	109	130	mA	2,4
		10/20bit SD, Audio Enabled	–	112	130	mA	2,4
		10/20bit SD, Audio Disabled	–	104	120	mA	2,4
		DVB_ASI	–	100	120	mA	2,4
+3.3V Supply Current	I_{3V3}	10/20bit HD, Audio Enabled	–	74	86	mA	3,4
		10/20bit HD, Audio Disabled	–	74	86	mA	3,4
		10/20bit SD, Audio Enabled	–	74	86	mA	3,4
		10/20bit SD, Audio Disabled	–	74	86	mA	3,4
		DVB_ASI	–	74	86	mA	3,4
Total Device Power	P_D	10/20bit HD, Audio Enabled	–	491	600	mW	4
		10/20bit HD, Audio Disabled	–	440	540	mW	4
		10/20bit SD, Audio Enabled	–	445	545	mW	4
		10/20bit SD, Audio Disabled	–	430	530	mW	4
		DVB_ASI	–	424	510	mW	4
		Reset	–	310	–	mW	–
		Standby	10	125	–	mW	5
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	–	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	–	V	–
Output Logic LOW	V_{OL}	1.8V mode	–	–	0.3	V	–
		3.3V mode	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	1.8V mode	1.4	–	–	V	–
		3.3V mode	2.4	–	–	V	–

Table 2-2: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Output							
Output Common Mode Voltage	V_{CMOUT}	75Ω load, RSET=750Ω SD and HD mode	–	CD_VDD - ΔV_{SDD}	–	V	–

NOTES

1. VCO_VDD guaranteed only when GO1555 is connected.
2. Sum of all 1.8V supplies.
3. Sum of all 3.3V supplies.
4. IO_VDD = 3.3V. When IO_VDD = 1.8V, the current/power consumption is lower by up to 5mA/10mW.
5. See Standby Section for details.

2.4 AC Electrical Characteristics

Table 2-3: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Device Latency	–	10-bit SD	–	–	550	PCLK	–
	–	20-bit HD	–	–	1065	PCLK	–
	–	DVB-ASI	–	–	15	PCLK	–
	–	10-bit SD or 20-bit HD; All Audio Disabled	–	–	27	PCLK	–
Reset Pulse Width	t_{reset}	–	10	–	–	ms	1
Parallel Input							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–
Input Data Setup Time	t_{su}	50% levels; 3.3V or 1.8V operation	2	–	–	ns	4
Input Data Hold Time	t_{ih}		0.8	–	–	ns	4
Serial Audio Data Input							
Input Data Set-up Time	t_{su}	50% levels; 3.3V or 1.8V operation	74	–	–	ns	–
Input Data Hold Time	t_{ih}		74	–	–	ns	–
Serial Digital Output							
Serial Output Data Rate	DR_{SDO}	–	–	1.485	–	Gb/s	–
		–	–	1.485/1.001	–	Gb/s	–
		–	–	270	–	Mb/s	–
Serial Output Swing	V_{SDD}	RSET = 750Ω 75Ω load	750	800	850	mVp-p	–
Serial Output Rise/Fall Time 20% ~ 80%	trf_{SDO}	HD mode	–	120	270	ps	–
	trf_{SDO}	SD mode	400	660	800	ps	–

Table 2-3: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Mismatch in rise/fall time	$\Delta t_r, \Delta t_f$	–	–	–	35	ps	–
Duty Cycle Distortion	–	–	–	1	5	%	5
Overshoot	–	SD/$\overline{HD}$=0	–	5	10	%	5
	–	SD/$\overline{HD}$=1	–	3	8	%	5
Output Return Loss	ORL	5 MHz - 1.485 GHz	–	18	–	dB	6
Serial Output Intrinsic Jitter	t_{OJ}	Pseudorandom and SMPTE Colour Bars HD signal	–	35	80	ps	2
	t_{OJ}	Pseudorandom and SMPTE Colour Bars SD signal	–	100	200	ps	3
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	10	MHz	–
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	–
GSPI Input Data Setup Time	–		1.5	–	–	ns	–
GSPI Input Data Hold Time	–		1.5	–	–	ns	–
GSPI Output Data Hold Time	–	15pF load	1.5	–	–	ns	–
CS low before SCLK rising edge	–	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	–
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	–	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	–
CS high after SCLK falling edge	–	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	–

NOTES:

1. See 'Device Reset' on page 108, Figure 4-33.
2. Alignment Jitter = measured from 100kHz to 148.5MHz
3. Alignment Jitter = measured from 1kHz to 27MHz
4. Input setup and hold time is dependent on the rise and fall time on the parallel input. Parallel clock and data with rise time or fall time greater than 500ps require larger setup and hold times.
5. Single Ended into 75Ω external load.
6. ORL depends on board design. The GS1582 achieves this specification on Gennum's evaluation boards.

3. Input/Output Circuits

All resistors in ohms, all capacitors in farads, unless otherwise shown.

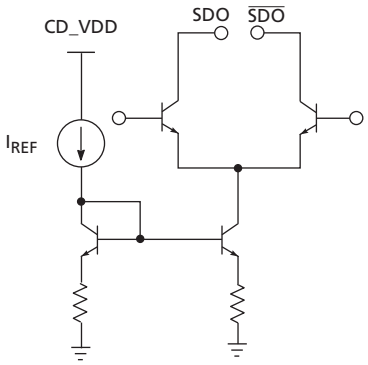


Figure 3-1: Differential Output Stage (SDO/$\overline{\text{SDO}}$)

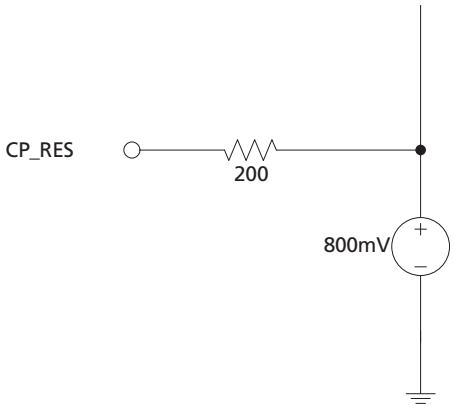


Figure 3-2: Charge Pump Current Setting Resistor (CP_RES)

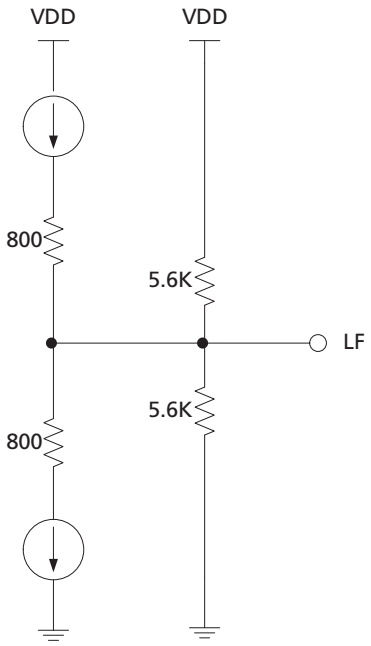


Figure 3-3: PLL Loop Filter

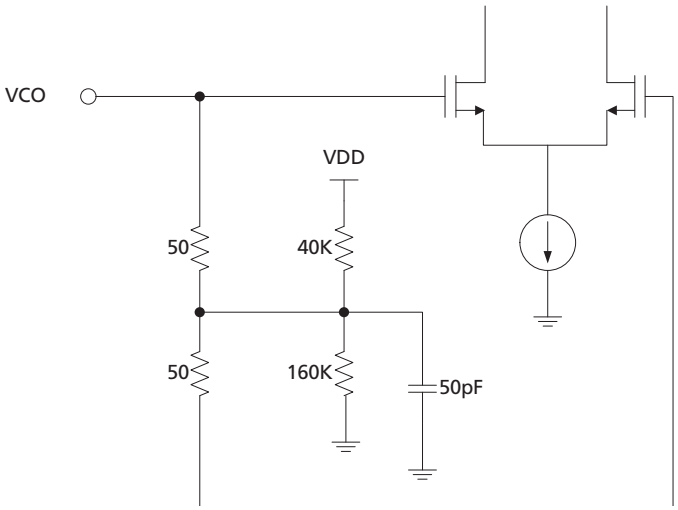


Figure 3-4: VCO Input

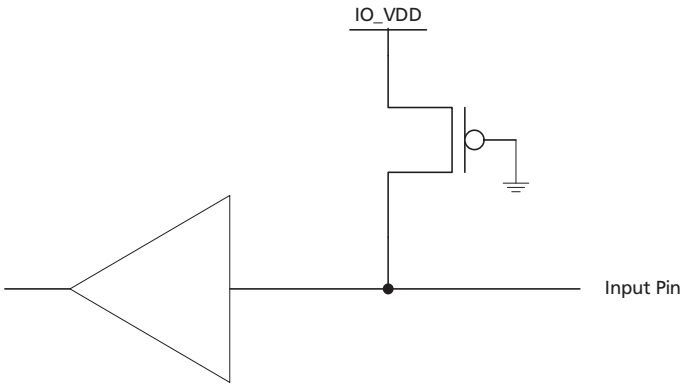


Figure 3-5: Digital Input Pin with Weak Pull Up(>33kΩ)
(ACLK[2:1], WCLK[2:1], AIN[4:1], PCLK, DIN[19:0])

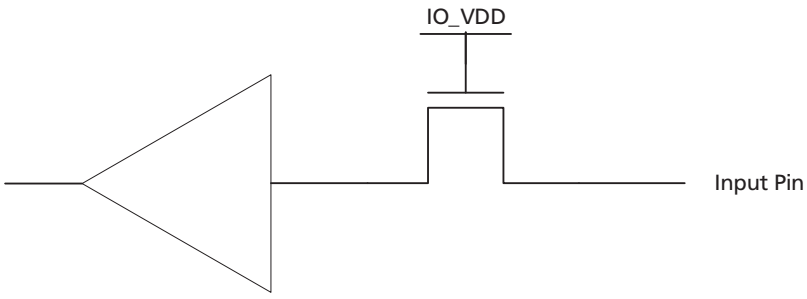


Figure 3-6: 5V Tolerant Input Pin (All Other Input Pins)

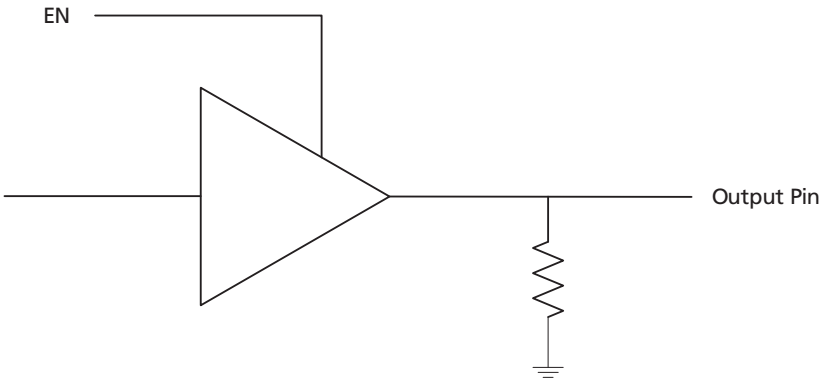


Figure 3-7: Digital Output Pin with High Impedance Mode
(LOCKED, AUDIO_INT, SDOUT_TDO)

4. Detailed Description

4.1 Functional Overview

The GS1582 is a multi-rate serializer with an integrated cable driver and embedded audio multiplexer. When used in conjunction with the external GO1555 Voltage Controlled Oscillator, a transmit solution at 1.485Gb/s, 1.485/1.001Gb/s or 270Mb/s is realized.

The device has three basic modes of operation that must be set through external device pins; SMPTE mode, DVB-ASI mode, and Data-Through mode.

In SMPTE mode, the device will accept 10-bit multiplexed or 20-bit demultiplexed SMPTE compliant data at both HD and SD signal rates. By default, the device's additional processing features, including audio embedding, will be enabled in this mode.

In DVB-ASI mode, the GS1582 will accept an 8-bit parallel DVB-ASI compliant transport stream on DIN[17:10]. The serial output data stream will be 8b/10b encoded with stuffing characters added as per the standard.

Data-Through mode allows for the serializing of data not conforming to SMPTE or DVB-ASI streams. No additional processing will be done in this mode.

In Standby mode, the device power consumption will be reduced.

The serial digital output features a high impedance mode and adjustable signal swing. The output slew rate is automatically set by the SD/$\overline{\text{HD}}$ pin setting.

GS1582 provides several data processing functions including generic ANC insertion, SMPTE 352M and EDH data packet generation and insertion, automatic video standards detection, and TRS, CRC, ANC data checksum, and line number calculation and insertion. These features are all enabled/disabled collectively using the external IO processing pin, but may be individually disabled via internal registers accessible through the GSPI host interface.

Finally, the GS1582 contains a JTAG interface for boundary scan test implementations.

4.2 Parallel Data Inputs

Data is clocked into the device on the rising edge of PCLK as shown in Figure 4-1.

The input data format is defined by the setting of the external SD/$\overline{\text{HD}}$, $\overline{\text{SMPTE_BYPASS}}$, and DVB_ASI pins and may be presented in 10-bit or 20-bit format. The input data bus width is controlled by the 20bit/$\overline{\text{10bit}}$ input pin.

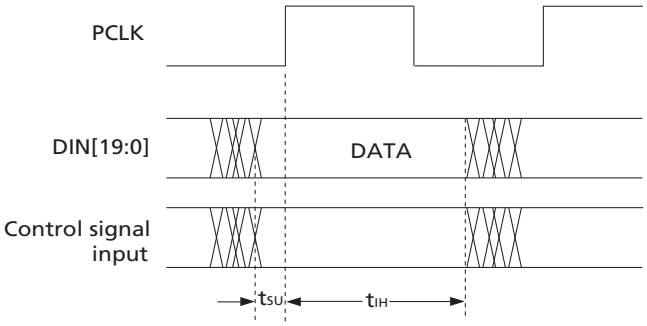


Figure 4-1: PCLK to Data Timing

4.2.1 Parallel Input in SMPTE Mode

When the device is operating in SMPTE mode, see SMPTE Mode on page 29, both SD and HD data may be presented to the input bus in either multiplexed or demultiplexed form depending on the setting of the 20bit/$\overline{10bit}$ input pin.

In 20-bit mode, (20bit/$\overline{10bit}$ = HIGH), the input data format should be word aligned, demultiplexed luma and chroma data. Luma words should be presented on DIN[19:10] while chroma words should be presented on DIN[9:0].

In 10-bit mode, (20bit/$\overline{10bit}$ = LOW), the input data format should be word aligned, multiplexed luma and chroma data. The data should be presented on DIN[19:10]. DIN[9:0] will be high impedance in this mode.

4.2.2 Parallel Input in DVB-ASI Mode

When operating in DVB-ASI mode, see DVB-ASI mode on page 35, the GS1582 must be set to 10-bit operation mode by setting the 20bit/$\overline{10bit}$ pin LOW.

The device will accept 8-bit data words on DIN[17:10]. DIN17 = HIN is the most significant bit of the encoded transport stream data and DIN10 = AIN is the least significant bit.

In addition, DIN19 and DIN18 will be configured as the DVB-ASI control signals INSSYNCIN and KIN respectively. See DVB-ASI mode on page 35 for a description of these DVB-ASI specific input signals.

DIN[9:0] will have a Logic Level HIGH in DVB-ASI mode.

4.2.3 Parallel Input in Data-Through Mode

When operating in Data-Through mode, see Data-Through Mode on page 36, the GS1582 passes data from the parallel input bus to the serial output without performing any encoding or scrambling. The input data bus width is controlled by the setting of the 20bit/$\overline{10bit}$ pin.

4.2.4 Parallel Input Clock (PCLK)

The frequency of the PCLK input signal required by the GS1582 is determined by the input data format. Table 4-1 below lists the possible input signal formats and their corresponding parallel clock rates. Note that the DVB-ASI input will only be in 10-bit format, when setting the 20bit/$\overline{10bit}$ pin LOW.

Table 4-1: Parallel Data Input Format

Input Data Format	DIN [19:10]	DIN [9:0]	PCLK	Control Signals			
				20bit/ $\overline{10bit}$	SD/ $\overline{HD}$	$\overline{SMPTE_BYPASS}$	DVB_ASI
SMPTE MODE							
20-bit DEMULTIPLEXED SD	LUMA	CHROMA	13.5MHz	HIGH	HIGH	HIGH	LOW
10-bit MULTIPLEXED SD	LUMA / CHROMA	HIGH IMPEDANCE	27MHz	LOW	HIGH	HIGH	LOW
20-bit DEMULTIPLEXED HD	LUMA	CHROMA	74.25 or 74.25/ 1.001MHz	HIGH	LOW	HIGH	LOW
10-bit MULTIPLEXED HD	LUMA / CHROMA	HIGH IMPEDANCE	148.5 or 148.5/ 1.001MHz	LOW	LOW	HIGH	LOW
DVB-ASI MODE							
10-bit DVB-ASI	DVB-ASI DATA	HIGH IMPEDANCE	27MHz	LOW	HIGH	LOW	HIGH
				LOW	HIGH	LOW	HIGH
DATA-THROUGH MODE							
20-bit SD	DATA	DATA	13.5MHz	HIGH	HIGH	LOW	LOW
10-bit SD	DATA	HIGH IMPEDANCE	27MHz	LOW	HIGH	LOW	LOW
20-bit HD	DATA	DATA	74.25 or 74.25/ 1.001MHz	HIGH	LOW	LOW	LOW
10-bit HD	DATA	HIGH IMPEDANCE	148.5 or 148.5/ 1.001MHz	LOW	LOW	LOW	LOW

4.3 SMPTE Mode

The GS1582 operates in SMPTE mode when the $\overline{\text{SMPTE_BYPASS}}$ pin is set HIGH and the DVB_ASI pin is set LOW.

In this mode, the parallel data will be scrambled according to SMPTE 259M or 292M, and NRZ-to-NRZI encoded prior to serialization.

4.3.1 HVF Timing

In SMPTE mode, the GS1582 can automatically detect the video standard and generate all internal timing signals. The total line length, active line length, total number of lines per field/frame and total active lines per field/frame are calculated for the received parallel video.

When DETECT_TRS is LOW, the video standard and timing signals are based on the externally supplied H_Blanking, V_Blanking, and F_Digital signals. These signals go to the H/HSYNC, V/VSYNC and F/DE pins respectively. When DETECT_TRS is HIGH, the video standard timing signals will be extracted from the embedded TRS ID words in the parallel input data. Both 8-bit and 10-bit TRS code words will be identified by the device.

NOTE: IO processing must be enabled for the device to remap 8-bit TRS words to the corresponding 10-bit value for transmission. See Section 4.9.4.2 for more information.

The GS1582 determines the video standard by timing the horizontal and vertical reference information supplied at the H/HSYNC, V/VSYNC, and F/DE input pins, or contained in the TRS ID words of the received video data. Therefore, full synchronization to the received video standard requires one complete video frame. Once synchronization has been achieved, the GS1582 will continue to monitor the received TRS timing or the supplied H, V, and F timing information to maintain synchronization. GS1582 will lose all timing information immediately following loss of H, V and F.

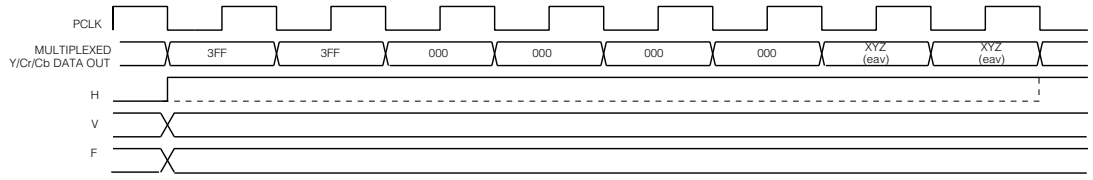
The H signal timing should also be configured via the H_CONFIG bit of the internal IOPROC_DISABLE register as either active line based blanking or TRS based blanking. See Packet Generation and Insertion on page 69.

Active line based blanking is enabled when the H_CONFIG bit is set LOW. In this mode, the H input should be HIGH for the entire horizontal blanking period, including the EAV and SAV TRS words. This is the default H timing used by the device.

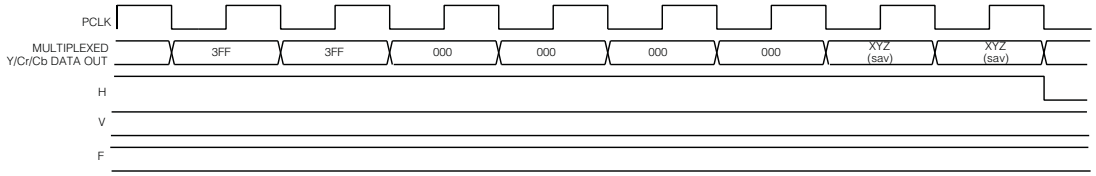
The timing of these signals is shown in Figure 4-2.



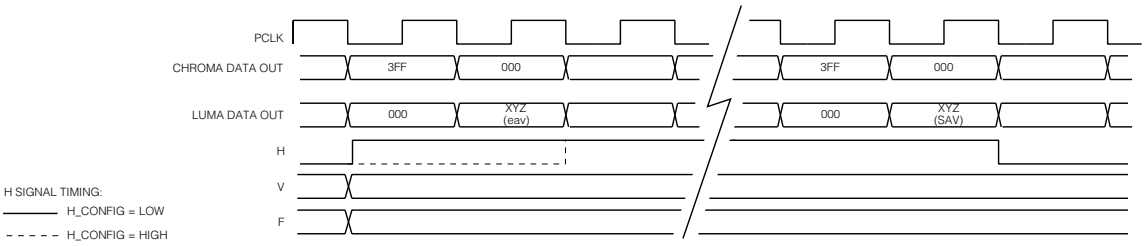
H_Blanking: V_Blanking: F_Digital TIMING - HD 20-BIT INPUT MODE



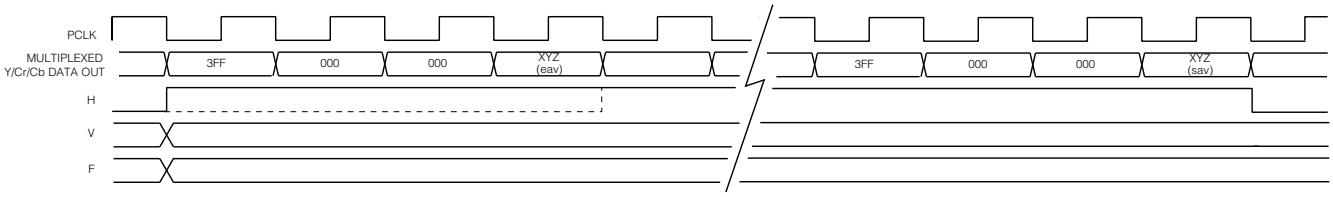
H_Blanking: V_Blanking: F_Digital TIMING AT EAV - HD 10-BIT INPUT MODE



H_Blanking: V_Blanking: F_Digital TIMING AT SAV - HD 10-BIT INPUT MODE



H_Blanking: V_Blanking: F_Digital TIMING - SD 20-BIT INPUT MODE



H_Blanking: V_Blanking: F_Digital TIMING - SD 10-BIT INPUT MODE

Figure 4-2: H_Blanking, V_Blanking, F_Digital Timing

4.3.2 CEA 861 Timing

The GS1582 extracts timing information from externally provided HSYNC, VSYNC, and DE signals when CEA 861 timing mode is selected by setting DETECT_TRS = LOW and the TIM_861 = HIGH.

Horizontal sync (H), Vertical sync (V), and Data Enable (DE) timing must be provided via the H/HSYNC, V/VSYNC and F/DE input pins. The host interface register bit H_CONFIG will be ignored in the CEA 861 input timing mode.

The GS1582 will determine the EIA/CEA-861 standard and embed EAV and SAV TRS words in the output serial video stream.

Video standard detection is not dependent on the HSYNC pulse width or the VSYNC pulse width and therefore the GS1582 will tolerate non-standard pulse widths. In addition, the device can compensate for up to ±1 PCLK cycle of jitter on VSYNC with respect to HSYNC and sample VSYNC correctly.

NOTE 1: The period between the leading edge of the HSYNC pulse and the leading edge of Data Enable (DE) must follow the timing requirements described in the EIA/CEA-861 specification. The GS1582 embeds TRS words according to this timing relationship to maintain compatibility with the corresponding SMPTE standard.

NOTE 2: When CEA 861 standards 6 & 7 [720(1440)x480i] are presented to the GS1582, the device will embed TRS words corresponding to the timing defined in SMPTE 125M to maintain SMPTE compatibility.

CEA 861 standards 6 & 7 [720(1440)x480i] define the active area on lines 22 to 261 and 285 to 524 inclusive (240 active lines per field). SMPTE 125M defines the active area on lines 20 to 263 and 283 to 525 inclusive (244 lines on field 1; 243 lines on field 2).

Therefore, in the first field, the GS1582 adds two active lines above and two active lines below the original active image. In the second field it adds two lines above and one line below the original active image.

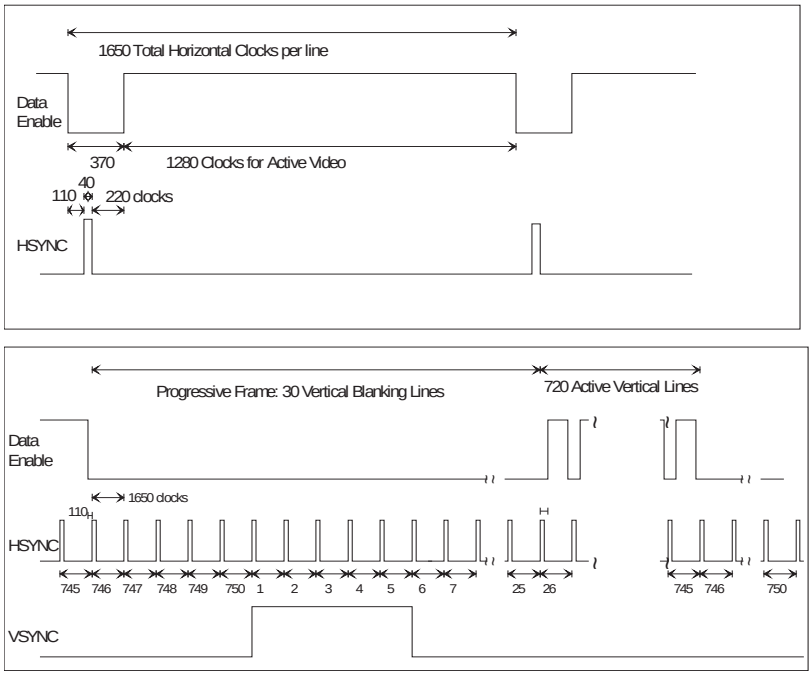


Figure 4-3: HSYNC:VSYNC:DE Input Timing 1280 x 720p @ 59.94/60

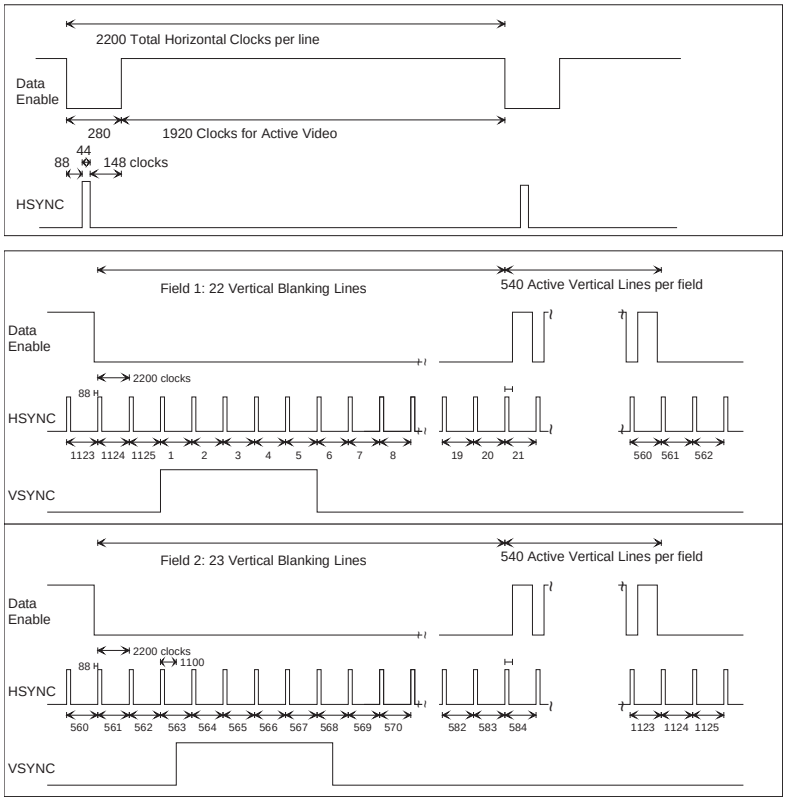


Figure 4-4: HSYNC:VSYNC:DE Input Timing 1920 x 1080i @ 59.94/60

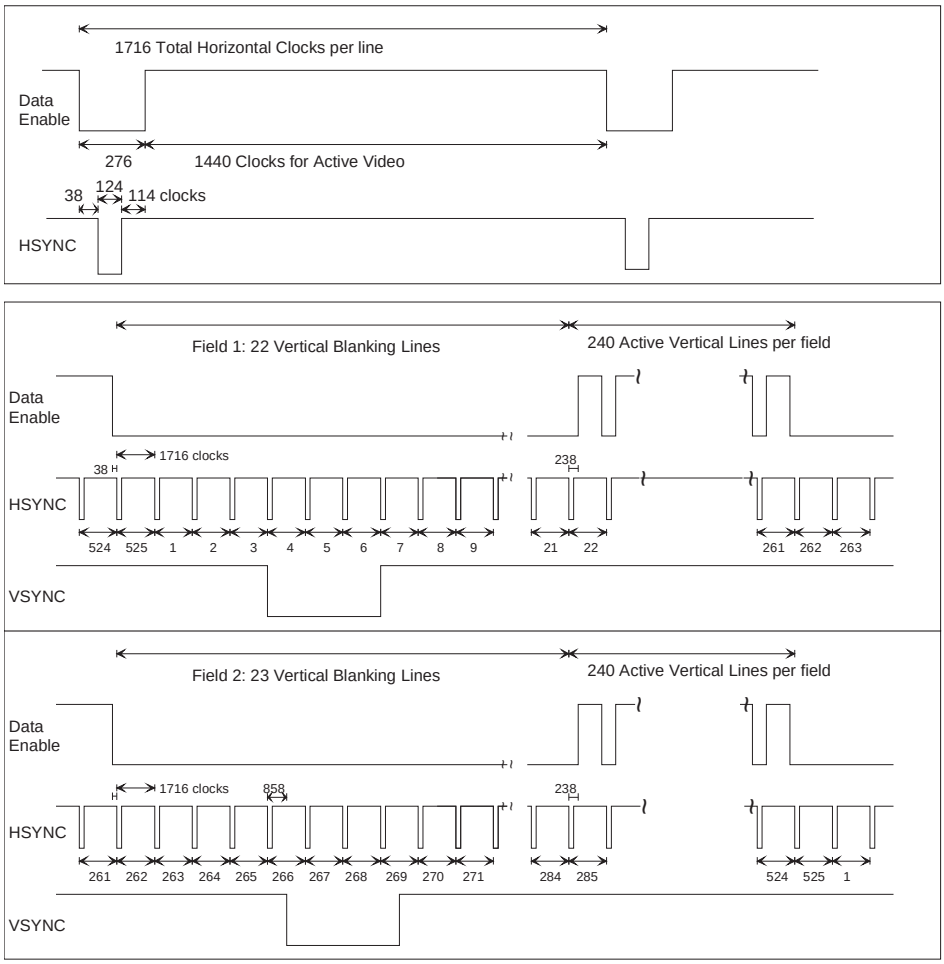


Figure 4-5: HSYNC:VSYNC:DE Input Timing 720 (1440) x 480i @ 59.94/60

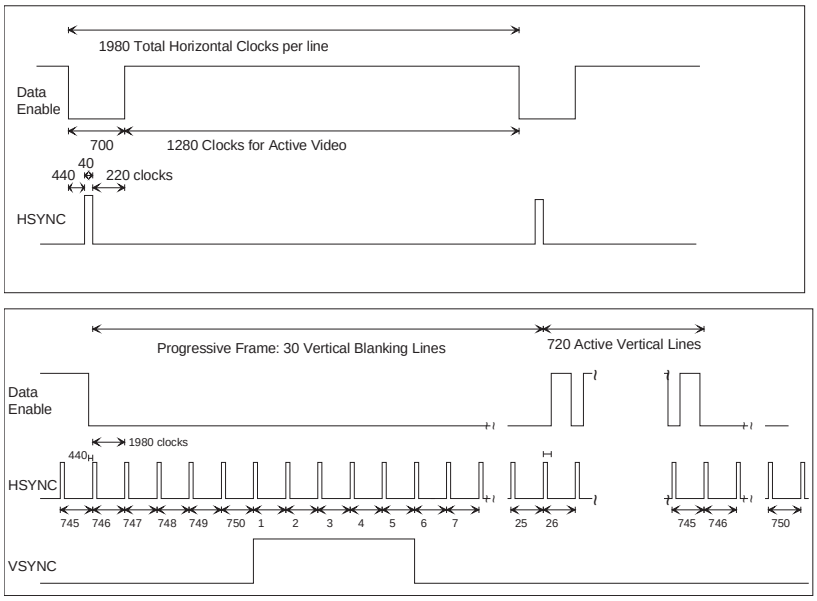


Figure 4-6: HSYNC:VSYNC:DE Input Timing 1280 x 720p @ 50

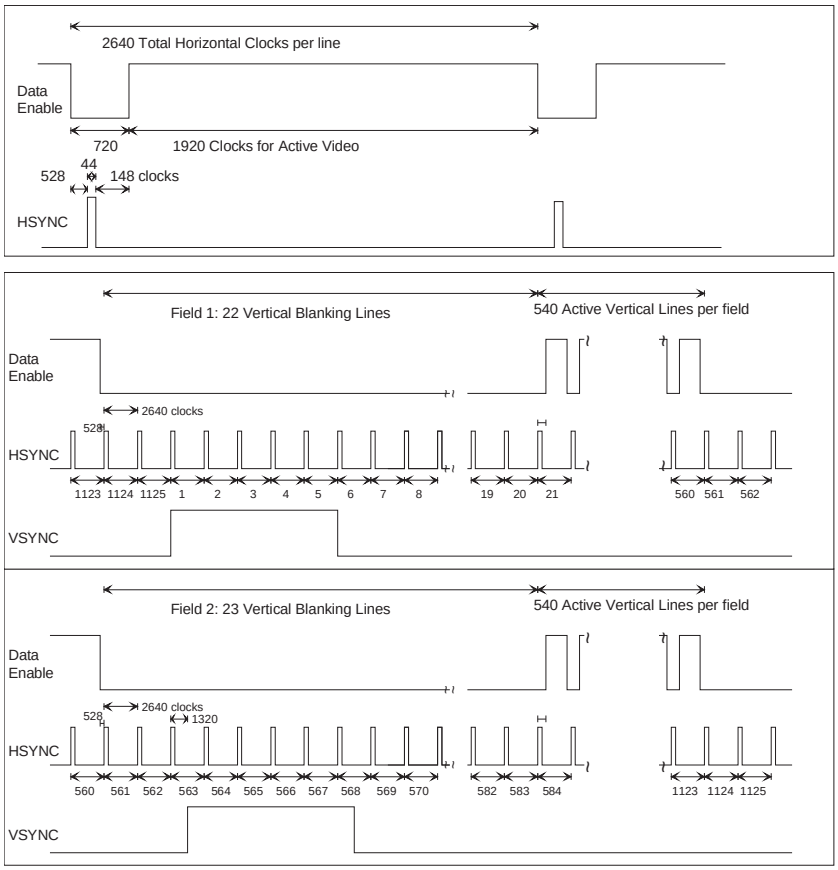


Figure 4-7: HSYNC:VSYNC:DE Input Timing 1920 x 1080i @ 50

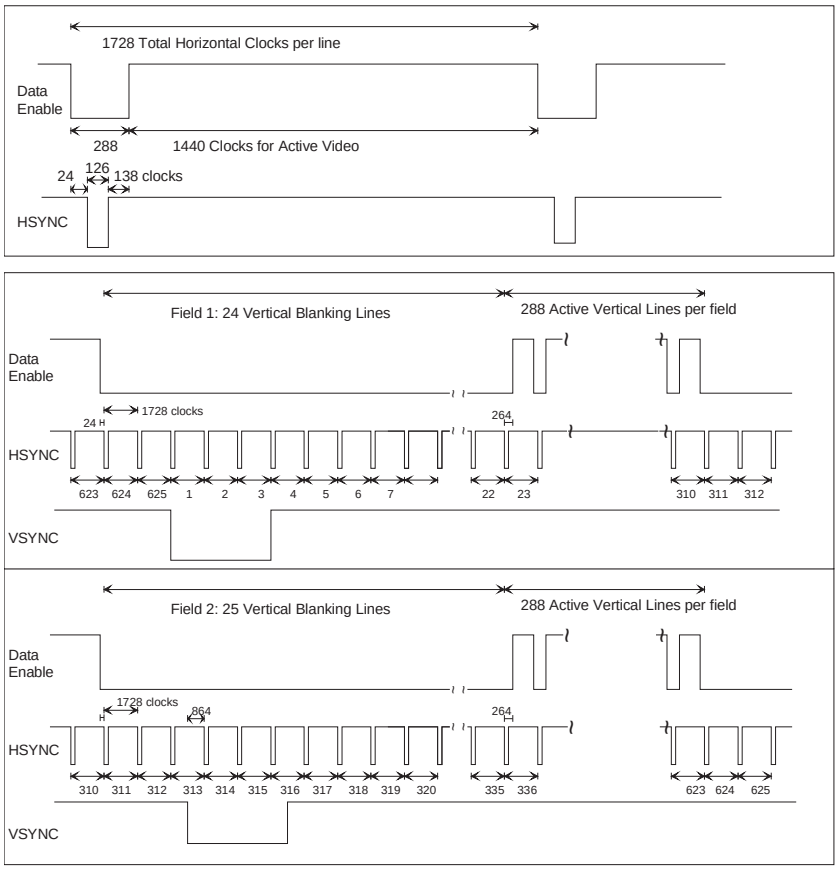


Figure 4-8: HSYNC:VSYNC:DE Input Timing 720 (1440) x 576 @ 50

4.4 DVB-ASI mode

The GS1582 operates in DVB-ASI mode when the $\overline{\text{SMPTE_BYPASS}}$ pin is set LOW and the DVB_ASI and SD/$\overline{\text{HD}}$ pins are set HIGH.

In this mode, all SMPTE processing functions are disabled, and the 8-bit transport stream data will be 8b/10b encoded prior to serialization.

4.4.1 Control Signal Inputs

In DVB-ASI mode, the DIN19 and DIN18 pins are configured as DVB-ASI control signals INSSYNCIN and KIN respectively.

When INSSYNCIN is set HIGH, the device will insert K28.5 sync characters into the data stream. This function is used in system implementations where the GS1582 is preceded by an external data FIFO. Parallel DVB-ASI data may be clocked into the FIFO at some rate less than 27MHz. The INSSYNCIN input may then be connected to the FIFO empty signal, providing a means of padding the data transmission rate to 27MHz. See Figure 4-9.

NOTE: 8b/10b encoding will take place after K28.5 sync character insertion.

KIN should be set HIGH whenever the parallel data input is to be interpreted as any special character defined by the DVB-ASI standard (including the K28.5 sync character). This pin should be set LOW when the input is to be interpreted as data.

NOTE: When operating in DVB-ASI mode, DIN[9:0] are set to high impedance.

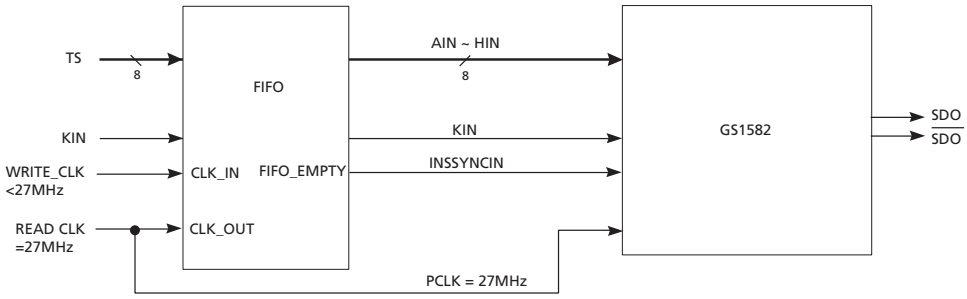


Figure 4-9: DVB-ASI FIFO Implementation using the GS1582

4.5 Data-Through Mode

The GS1582 may be configured to operate as a simple parallel-to-serial converter. In this mode, the device passes data to the serial output without performing any scrambling or encoding.

Data-through mode is enabled only when both the $\overline{\text{SMPTE_BYPASS}}$ and DVB_ASI pins are set LOW.

4.6 Standby Mode

In standby mode, the power consumption of the GS1582 is reduced to 125mW. Standby mode is enabled when the STANDBY pin is set HIGH. Once the STANDBY pin is set HIGH, it may take up to 50ms for power reduction to take place.

In this mode, the serial output pins are set to high impedance, and the GS1582 loses lock to the reference input PCLK. While in standby mode, the programmed register values are retained. However, no registers can be accessed for reading or writing via the GSPI port. No write bits will be captured and all read functions will return a value of 0.

The power in standby mode can be further reduced through two means:

1. Eliminate activity on all parallel data and clock inputs. This can be achieved by setting the parallel data and clock HIGH, or not driving them. Setting the parallel inputs to LOW is not recommended as it will result in a smaller power saving.
2. Remove the 3.3V supply to the CD_VDD pin of the device.

The standby power consumption under various conditions is shown in Table 4-2: Standby Power Consumption.

In order to return to normal operation from standby mode, the STANDBY pin must be set to LOW. Once normal operation is resumed, the GS1582 will re-lock to the reference

PCLK. The recovery time from standby mode is the same as initial power-up but no reset is required. Once the GS1582 re-locks to the reference PCLK, operation is resumed according to the configuration held before entering standby mode.

Table 4-2: Standby Power Consumption

Standby Condition	Typical Power Consumption (mW)
STANDBY asserted	125
STANDBY asserted Parallel data and clock inactive	100
STANDBY asserted 3.3V supply removed from CD_VDD	35
STANDBY asserted Parallel data and clock inactive 3.3V supply removed from CD_VDD	<10

4.7 Audio Multiplexer

Up to eight channels of audio may be embedded into the GS1582 video data stream in accordance with SMPTE 299M and SMPTE 272M. The audio data is input in two groups of four channels, with corresponding clock signals.

The audio input signal formats supported include AES/EBU and three other industry standard serial digital formats. 16, 20 and 24-bit audio sample sizes are supported at 48kHz synchronous for SD formats and 48kHz synchronous or asynchronous for HD formats.

Additional audio processing features include audio mute, individual channel enable, channel re-mapping, audio group replacement, cascade, group selection, and audio channel status insertion.

The audio system clock can be provided by Gennum's GEN-Clocks™ series of clock generation ICs. In serial formats, the audio clocks required by the core are two word clocks and two signals that are a multiple of 64fs.

The SD audio multiplexer core is compliant with SMPTE 272M A and C. The HD audio multiplexer core is fully compliant with SMTPE 299M.

4.7.1 Audio Core Configurations

Figure 4-10 shows the top level block diagrams of both the SD and HD multiplexer cores.

Each group of audio has one word clock signal and one audio clock signal. Data present at Ain_1/2 and Ain_3/4 share clocks present at WCLK1 and ACLK1, while data present at Ain_5/6 and Ain_7/8 share clocks present at WCLK2 and ACLK2.

Audio embedding may be disabled for each group independently using the pins GRP1_EN/$\overline{\text{DIS}}$ and GRP2_EN/$\overline{\text{DIS}}$.

NOTE: Disabling a single group does not reduce the power consumption of the GS1582, however disabling both groups results in a power reduction.

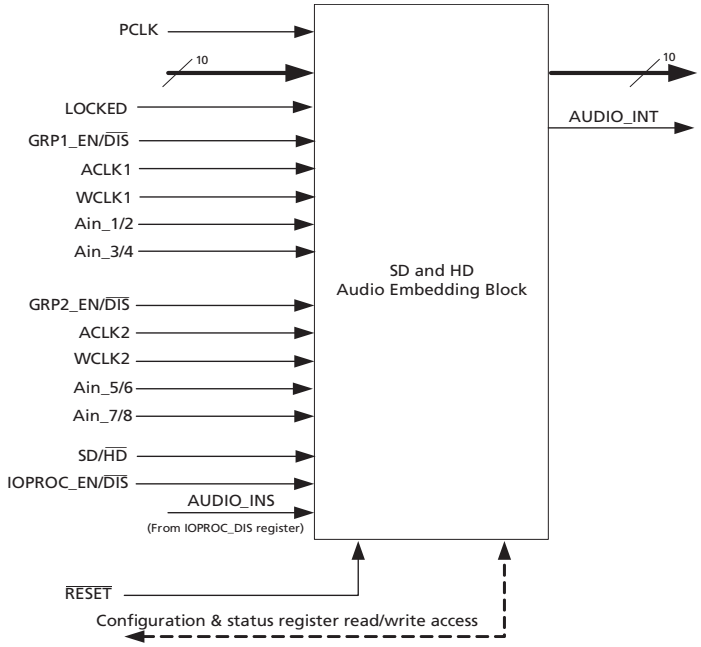


Figure 4-10: Audio Multiplexer Top Level

4.7.2 Audio Detection

The audio multiplexer detects the presence of audio data and control packets in any of four embedded audio groups. The presence of audio data is indicated by the ADPGx_DET bits in the host interface, while the presence of control packets is indicated by the ACPGx_DET bits in the host interface. In SD mode, the presence of extended audio data packets is indicated by the AXPGx_DET bits in the host interface.

These detection flags are asserted for the duration that audio data packets are detected.

For SD formats, the first Ancillary Data Flag (ADF) must always be contiguous after the EAV words. For HD formats, the first Ancillary Data Flag must always be contiguous after the two EAV CRC words. By default, the device will delete all incoming ancillary data with audio data or control packet DID's.

Refer to Section 4.13.3 for HD and SD audio multiplexer status and configuration registers.

4.7.3 Audio Modes of Operation

The audio multiplexer operates in three distinct modes: normal mode, cascade mode, and audio group replacement mode.

In normal operating mode, up to two audio groups can be added to the output video. (See Table 4-3: Audio Multiplexer Modes of Operation). All existing audio packets are

deleted from the video input, however arbitrary packets, SDTI packets and SMPTE 352M packets are not deleted.

When the EN_CASCADE host interface bit is set HIGH, the audio multiplexer operates in cascade mode. Up to two audio groups can be added to the video output. The added groups will not replace existing embedded audio groups. No existing packets are deleted from the video input, and the added audio packets are appended to the last packet in the video input.

In cascade mode, if the audio multiplexer is configured to add group 1 audio data packets with the same group number as an existing group, MUX_ERRA will be asserted in the host interface. Similarly, MUX_ERRB will be asserted if the configuration leads to replacing existing groups with group 2.

When the AGR bit in the host interface is set HIGH, the audio multiplexer operates in group replacement mode. In this mode, added audio groups can replace existing embedded audio groups. The embedded audio groups will be sorted by audio group number. No packets will be deleted from the video input (except for the audio packets being replaced). SDTI packets and SMPTE 352M packets are placed before the audio packets, and arbitrary packets are placed after the audio packets in SD mode.

NOTE 1: When audio group replacement mode is selected, the cascade function is disabled.

NOTE 2: In normal SD mode, if the incoming stream has a completely full HANC space, the outgoing HANC space will only get filled with up to 235 words and the remainder of the space is left blank. This will not occur if there are one or more words free in the incoming HANC space.

NOTE 3: SD audio in cascade mode may only be inserted if the HANC space of the incoming stream is not completely full. If the incoming stream has a full HANC space, audio packets will be inserted beyond the HANC boundary. The space following the inserted audio packets will then be blanked until the next EAV is detected in the video stream. This will not occur if there are two or more words free at the end of the incoming HANC space after the existing packets.

NOTE 4: HD audio in normal mode may only be inserted if the HANC space of the incoming stream is not completely full. If the incoming stream has a full HANC space, packets will be inserted beyond the HANC boundary. The space following the inserted packets will then be blanked until the next EAV is detected in the video stream. This will not occur if there are two or more words free at the end of the incoming HANC space after the existing packets.

Table 4-3: Audio Multiplexer Modes of Operation

Host Interface Registers	Operating Mode
EN_CASCADE = 0, AGR = 0	Normal Mode
EN_CASCADE = 1, AGR = 0	Cascade Mode
EN_CASCADE = 0, AGR = 1	Audio Group Replacement Mode
EN_CASCADE = 1, AGR = 1	Audio Group Replacement Mode

4.7.4 Audio Packet Delete

Ancillary data packets with non-audio data ID words, such as arbitrary, EDH, SDTI header and SMPTE 352M, will not be deleted from the data stream. On lines where SMPTE 352M or SDTI header packets exist, the audio data packets must be contiguous to the 352M and SDTI packets in SD mode. For HD formats, the audio data packets must always be contiguous after the two EAV CRC words. If this is not the case, all existing audio data and control packets will be deleted.

When the EN_CASCADE host interface bit is set HIGH, all existing audio data and control packets will remain in the video stream.

When the AGR bit in the host interface is set HIGH, audio group replacement mode is selected. In this mode, existing audio data and control packets will not be deleted from the data stream with the exception of any packets of groups being replaced.

In cases where the ADF is not placed immediately after the CRC or EAV words, or there are gaps between the packets, the audio core will delete all existing audio data and control packets, regardless of the EN_CASCADE or AGR setting. Figure 4-11 shows an example of correct and incorrect placement of ancillary data packets for a SD format.

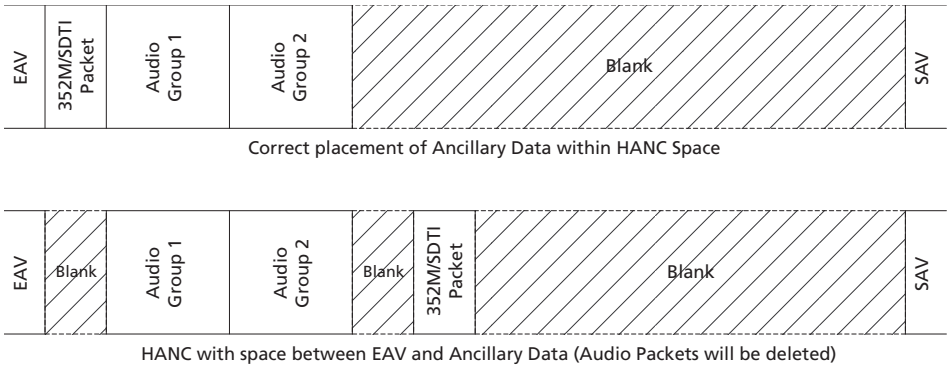


Figure 4-11: Ancillary Data Packet Placement Example

4.7.5 Arbitrary, SMPTE 352M & EDH Packet Detect

The audio multiplexer detects the presence of any arbitrary data packets. If present, these packets will be removed and stored for re-insertion after audio packets have been embedded. If there is insufficient HANC space available, the arbitrary data packet will be discarded.

To detect the arbitrary data packet, the audio core looks for any ancillary data packets which have a DID other than audio, extended audio, control, SDTI header, SMPTE 352M or EDH packets. Arbitrary data packets and formatting are defined in SMPTE 291M. Arbitrary data packets are only present on the luma channel of the HD video input.

All EDH processing is carried out following the audio core, as the CRC's will require updating. The audio core detects the presence of EDH packets in the HANC region. These packets are preserved and re-embedded after multiplexing of audio packets, according to RP 165. The audio core does not perform EDH CRC calculation and flag updates.

Since the audio core multiplexes audio packets on to lines where the ancillary data packet containing EDH checkwords and status flags is to be placed (lines 9 and 272 in 525, and lines 5 and 318 in 625), if there is insufficient horizontal ancillary data space available after audio multiplexing, the EDH block will overwrite audio packets. This problem may occur in both 525 and 625 when 16 channels (4 audio groups) of 24-bit audio are embedded.

NOTE 1: The audio sample distribution used by the SD audio core for both 525 and 625 will increase the available space in the horizontal ancillary data space.

NOTE 2: Due to the large size of the horizontal ancillary data space in 720p/24, 720p/25 and 720p/30 video standards, the maximum number of ancillary data words the audio core can process is limited to 1024 when configured to these standards.

Table 4-4 lists the data ID's and packet lengths for arbitrary, EDH, SDTI header and SMPTE 352M packets.

When the presence of a SMPTE 352M packet is detected, the audio core extracts and stores the packet for re-insertion. Audio data packets will always be placed after the SMPTE 352M packet.

Table 4-4: Non-audio Ancillary Data Packet DIDs

Ancillary Data Packet	DID	SDID	Packet Length (Words)
Arbitrary (SMPTE 291M)	User	User	262 max
EDH (RP 165)	1F4h	–	23
Payload Identifier (SMPTE 352M)	241h	101h	11
SDTI Header (SMPTE 305M)	140h	101h	53

NOTE: When serializing SDTI signals, it is recommended that the user ensure there are no SMPTE 352M packets present in the input video data.

4.7.6 Audio Packet Multiplexing

The SD core places audio data packets contiguously after the EAV. Any Extended Audio Data Packets are placed immediately following the Audio Data Packet of the same audio group.

The HD core places audio data packets contiguously after the two line CRC words.

In cases where the SMPTE 352M packet or SDTI header are present after the EAV or CRC, the audio data will be placed contiguously from the 352M or SDTI header packets. On lines where the 352M or SDTI header packets are present, there may be insufficient HANC space for embedding 4 audio groups. If there is insufficient HANC space available, the 352M or SDTI header packets are always re-inserted and the remaining audio group packet to be inserted is discarded.

On lines where the EDH packet is present, the audio data will be embedded up to the point reserved for the EDH packet. If there is insufficient HANC space available, the EDH packet is always re-inserted and the audio data packet discarded.

In the case where there is insufficient room in the HANC space to embed the selected audio data packets, the multiplexer core will delete any arbitrary data packets. If there is still insufficient room in the HANC space, the multiplexer core will not embed audio data packets.

4.7.7 Audio Insertion After Video Switching Point

4.7.7.1 SD Formats

The switching lines for SD formats are defined in SMPTE RP 168 as lines 10 and 273 for 525-line based formats, and lines 6 and 319 for 625-line based formats. The audio core does not place any audio data or control packets in the line immediately after the video switching line. For example, with the standard switch point of line 10 for field 1 in 525, there will be no audio data or control packets on line 11. The next packets will appear on line 12.

4.7.7.2 HD Formats

The video switching lines for HD formats are defined in SMPTE 299M as lines 7 and 569. The audio core does not place any audio data or control packets in the line immediately after the video switching point. For example, with the standard switch point of line 7 for field 1, there will be no audio data packets in line 8. The next packets will appear on line 9. The audio control packets will be multiplexed once per field, two lines after the video switch point, on lines 9 and 571.

4.7.8 Audio Data Packets

4.7.8.1 SD Formats

Figure 4-12 shows the structure of the SD audio data packet as defined in SMPTE 272M. Table 4-5 lists the descriptions of the audio data packet words. The audio core automatically generates certain audio data packet words, as shown in Table 4-5.

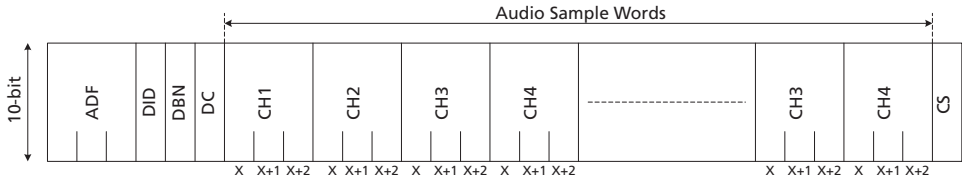


Figure 4-12: SD Audio Data Packet Structure

Table 4-5: Audio Data Packet Word Descriptions

Name	No. of Words	Description	Data	Auto-Generation
ADF	3	Ancillary Data Flag	000h 3FFh 3FFh	Yes
DID	1	Audio Group Data ID	2FFh 1FDh 1FBh 2F9h	See Table 4-10
DBN	1	Data Block Number	Repeat 1-255	Yes
DC	1	Data Count	–	Yes
CH1	4	Channel 1 ancillary data words	–	
CH2	4	Channel 2 ancillary data words	–	
CH3	4	Channel 3 ancillary data words	–	
CH4	4	Channel 4 ancillary data words	–	
CS	1	Checksum	–	Yes

Figure 4-13 shows the structure of the extended audio data packets as defined in SMPTE 272M. Table 4-6 lists the descriptions of the extended audio data packet words. The audio core automatically generates certain audio data packet words. The extended audio data packet is embedded immediately after the audio data packet with same group DID.

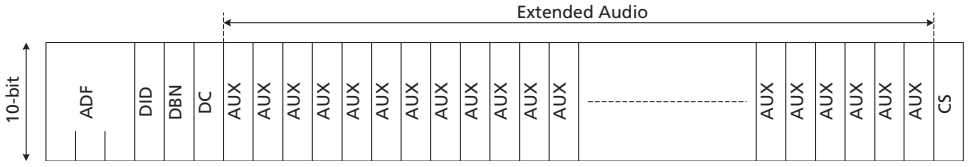


Figure 4-13: SD Extended Audio Data Packet Structure

Table 4-6: Extended Audio Data Packet Word Descriptions

Name	No. of Words	Description	Data	Auto-Generation
ADF	3	Ancillary Data Flag	000h 3FFh 3FFh	Yes
DID	1	Audio Group Data ID	1FEh 2FCh 2FAh 1F8h	See Table 4-10
DBN	1	Data Block Number	Repeat 1-255	Yes
DC	1	Data Count	–	Yes
AUX	4	Auxiliary data from one channel pair words	–	
CS	1	Checksum	–	Yes

For both audio data and extended audio packets, the Data Block Number is embedded with a running sequence of 1 to 255.

4.7.8.2 HD Formats

Figure 4-14 shows the structure of the audio data packets as defined in SMPTE 299M. The audio data packets are multiplexed into the chroma channel of the video data stream. Table 4-7 lists the descriptions of the audio data packet words. The audio core automatically generates certain audio data packet words, as shown in Table 4-7.

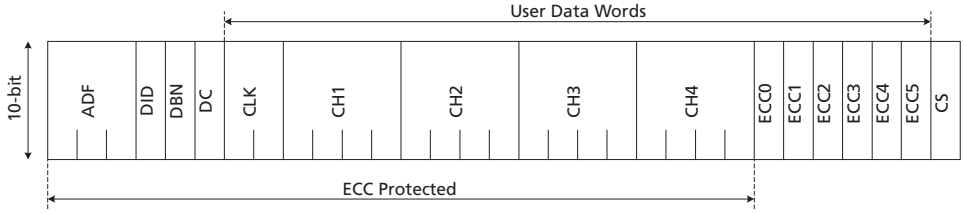


Figure 4-14: HD Audio Data Packet Structure

Table 4-7: Audio Data Packet Word Descriptions

Name	No. of Words	Description	Data	Auto-Generation
ADF	3	Ancillary Data Flag	000h 3FFh 3FFh	Yes
DID	1	Audio Group Data ID	2E7h 1E6h 1E5h 2E4h	See Table 4-10
DBN	1	Data Block Number	Repeat 1-255	Yes
DC	1	Data Count	218h	Yes
CLK	2	Audio Clock Phase Data	–	Yes
CH1	4	Channel 1 ancillary data words	–	
CH2	4	Channel 2 ancillary data words	–	
CH3	4	Channel 3 ancillary data words	–	
CH4	4	Channel 4 ancillary data words	–	
ECC0-5	6	Error correction code for lower 8 bits of first 24 words	–	Yes
CS	1	Checksum. Calculates the sum of lower 9 bits of 22 words from DID	–	Yes

4.7.9 Audio Control Packets

4.7.9.1 SD Formats

In SD mode, the control packets are inserted in the first line after the blanking line, and following the audio data packets.

Figure 4-15 shows the structure of the SD audio control packet as defined in SMPTE 272M. An audio control packet is multiplexed once per field in the video data stream. Table 4-8 lists descriptions of the audio control packet words. The audio core automatically generates certain audio control packet words.

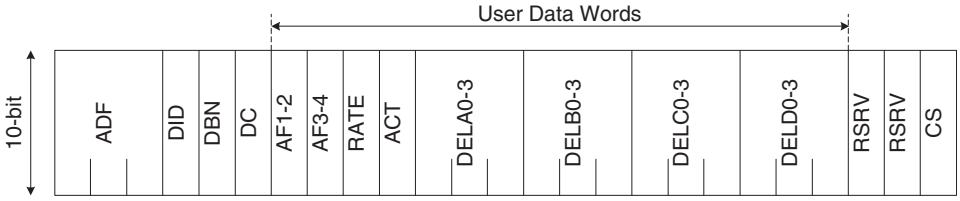


Figure 4-15: SD Audio Control Packet Structure

Table 4-8: Audio Control Packet Word Descriptions

Name	No. of Words	Description	Data	Auto-Generation
ADF	3	Ancillary Data Flag	000h 3FFh 3FFh	Yes
DID	1	Audio Group Data ID	1EFh 2EEh 2EDh 1ECh	See Table 4-10
DBN	1	Data Block Number	Repeat 1-255	Yes
DC	1	Data Count	–	Yes
AF1-2	1	Ch1/2 Audio Frame Number	–	Yes
AF3-4	1	Ch3/4 Audio Frame Number	–	Same as AF1-2
RATE	1	Sampling Frequency	–	Yes
ACT	1	Active Channel	–	ACT[8:1] setting
DELA0-3	3	Ch1/Ch1&2 Delay Data	–	27-bit Host Interface setting
DELB0-3	3	Ch3/Ch3&4 Delay Data	–	27-bit Host Interface setting
DELC0-3	3	Ch2 Delay Data	–	27-bit Host Interface setting

Table 4-8: Audio Control Packet Word Descriptions (Continued)

Name	No. of Words	Description	Data	Auto-Generation
DELD0-3	3	Ch4 Delay Data	–	27-bit Host Interface setting
RSRV	2	Reserved Words	200h	Yes
CS	1	Checksum. Calculates the sum of lower 9 bits of 22 words from DID	–	Yes

4.7.9.2 HD Formats

In HD mode, the control packets are inserted in the first line after the blanking line in the Luma channel in the first available space.

Figure 4-16 shows the structure of the HD audio control packet as defined in SMPTE 299M. An audio control packet is multiplexed once per field in the luma channel of the video data stream. Table 4-9 lists descriptions of the individual audio control packet words. The audio core automatically generates certain audio control packet words.

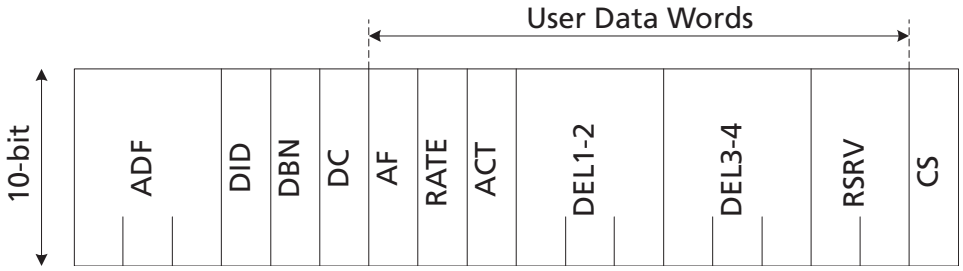


Figure 4-16: HD Audio Control Packet Structure

Table 4-9: Audio Control Packet Word Descriptions

Name	No. of Words	Description	Data	Auto-Generation
ADF	3	Ancillary Data Flag	000h 3FFh 3FFh	Yes
DID	1	Audio Group Data ID	1E3h 2E2h 2E1h 1E0h	See Table 4-10
DBN	1	Data Block Number	200h	Yes
DC	1	Data Count	10Bh	Yes
AF	1	Audio Frame Number	–	Yes

Table 4-9: Audio Control Packet Word Descriptions (Continued)

Name	No. of Words	Description	Data	Auto-Generation
RATE	1	Sampling Frequency	–	Yes
ACT	1	Active Channel	–	ACT[8:1] setting
DELA0-3	3	Ch1/2 Delay Data	–	27-bit Host Interface setting
DELB0-3	3	Ch3/4 Delay Data	–	27-bit Host Interface setting
RSRV	2	Reserved Words	200h	Yes
CS	1	Checksum. Calculates the sum of lower 9 bits of 15 words from DID	–	Yes

4.7.9.3 Audio Control Packet Insertion

To multiplex audio control packets for audio group 1 channels 1 to 4 (inputs Ain_1/2 and Ain_3/4), the CTRA_ON bit of the host interface must be set HIGH. To multiplex audio control packets for audio group 2 channels 5 to 8 (inputs Ain_5/6 and Ain_7/8), the CTRB_ON bit must be set HIGH. In addition, the multiplexer will only embed or replace group 1 control packets if one or more of ACT1, ACT2, ACT3 and ACT4 are set. Similarly, group 2 control packets will only be embedded or replaced if ACT5, ACT6, ACT7 or ACT8 are set.

By default, the audio control packets are embedded. The audio frame sequence is also embedded for 29.97fps video standards. Setting the AFNA_AUTO and AFNB_AUTO bits in the host interface LOW disable the audio frame sequence insertion. When set LOW, the audio frame number will be set to zero (200h). The RATE word is always set to zero to denote 48kHz audio only.

Control packet data can be programmed via the corresponding registers in the host interface.

Refer to Section 4.13.3 for HD and SD audio multiplexer status and configuration registers.

4.7.10 Setting Packet DID

The audio group DID for audio group 1 input channels 1 to 4 (Ain_1/2 and Ain_3/4) is set in the IDA[1:0] bits of the host interface. The audio group DID for audio group 2 input channels 5 to 8 (Ain_5/6 and Ain_7/8) is set in IDB[1:0] of the host interface. Table 4-10 shows the 2-bit host interface setting for the corresponding audio group DID.

For 24-bit audio support using the SD core, the extended audio group DID for audio group 1 input channels 1 to 4 is set to the same group in IDA[1:0] of the host interface. The extended audio group DID for audio group 2 input channels 5 to 8 is set to the same

group in IDB[1:0] of the host interface. 24-bit support is selected by setting the 24BIT bit of host interface HIGH.

When the host interface CASCADE bit is set LOW, the audio core defaults to audio groups 1 and 2, where Ain_1/2 and Ain_3/4 are multiplexed with audio group 1 DID, and Ain_5/6 and Ain_7/8 with audio group 2 DID.

Table 4-10: Audio Group DID Host Interface Settings

Audio Group	SD Data DID	SD Extended DID	HD Data DID	SD Control DID	HD Control DID	Host Interface Register Setting (2-bit)
1	2FFh	1FEh	2E7h	1EFh	1E3h	00b
2	1FDh	2FCh	1E6h	2EEh	2E2h	01b
3	1FBh	2FAh	1E5h	2EDh	2E1h	10b
4	2F9h	1F8h	2E4h	1ECh	1E0h	11b

Table 4-11: Audio Data and Control Packet DID Setting Register

Name	Description	Default CASCADE set LOW	Default CASCADE set HIGH
IDA[1:0]	Group 1 audio data and control packet DID setting	00b	10b
IDB[1:0]	Group 2 audio data and control packet DID setting	01b	11b

When the CASCADE bit is set HIGH, the GS1582 defaults to audio groups 3 and 4, where Ain_1/2 and Ain_3/4 are multiplexed with audio group 3 DID, and Ain_5/6 and Ain_7/8 with audio group 4 DID.

NOTE: If IDA and IDB are set to the same value, these bits will automatically revert to their default values.

Any other configurations can be programmed for the audio groups as required.

4.7.11 Audio Group Replacement

Audio group replacement mode allows the multiplexing of new audio groups, whilst replacing existing embedded audio with the same group DID. All other embedded audio groups will remain in the video stream. Up to two groups of audio (and extended audio for SD formats) can be replaced at once.

The first function performed by the GS1582 is deleting the audio group or groups to be replaced. The next step is removing and storing any other audio packets that are to be preserved. The final step is to embed the new and stored audio data packets so they are contiguous from the EAV (for HD formats, they will be contiguous after the line CRC words). See Figure 4-17.

On lines where the SMPTE 352M packet is already present, the audio core places new and existing audio data packets contiguously after the 352M packets. For HD formats, the 352M packets are embedded in the luma channel of the video data stream; therefore, no audio data packets will be placed after the 352M packets.

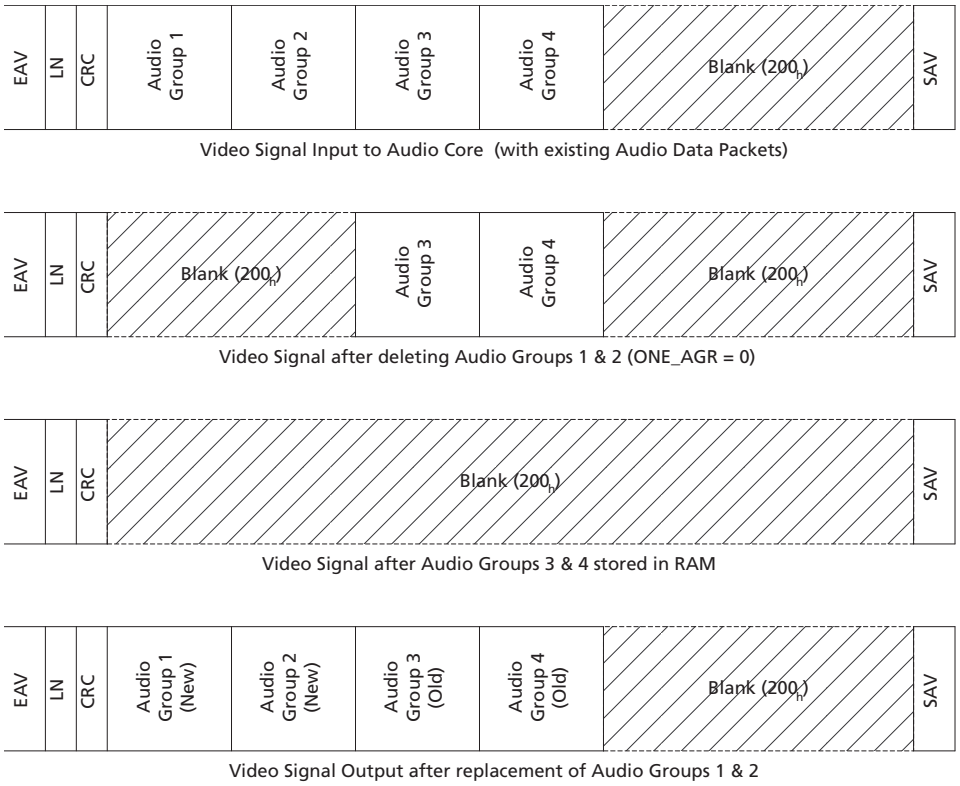


Figure 4-17: Audio Group Replacement Example (HD Formats)

Audio group replacement mode is selected by setting the AGR bit of the host interface HIGH. By default, the GS1582 replaces two audio groups with their DID set in IDA[1:0] and IDB[1:0]. To replace only one audio group, with group DID set in IDA[1:0], set the ONE_AGR bit in the host interface HIGH. The audio control packets, if present, will not be replaced unless the CTR_AGR host interface bit is set HIGH. The audio control packet information will be replaced with data programmed in the associated registers in the host interface. See Audio Control Packets on page 46.

Refer to Section 4.13.3 for HD and SD multiplexer core status and configuration registers.

4.7.12 Channel and Group Activation

Multiplexing of individual audio channels is enabled by setting the $\overline{ACT}$ bits in host interface register 0Ch. When set HIGH, the corresponding audio channel is multiplexed into the video data stream. Channels designated as not active ($\overline{ACT}$ set LOW) will be embedded with null samples (all bits set to zero). When all $\overline{ACT}$ bits are set LOW, no audio data packets will be multiplexed.

When ACT[1-4] are set LOW, the audio group set in IDA[1:0] will not be multiplexed. Similarly, when ACT[5-8] are set LOW, the audio group set in IDB[1:0] will not be multiplexed. This allows four channel, single group operation.

By default, all audio channels are enabled.

Refer to Section 4.13.3 for HD and SD audio multiplexer status and configuration registers.

4.7.13 ECC Error Detection & Correction (HD Mode Only)

The GS1582 will generate the error detection and correction fields in the audio data packets.

All generated error detection and correction complies with SMPTE 299M.

4.7.14 Interrupt Control

The GS1582 can be programmed to assert the interrupt signal (AUDIO_INT, pin H7) whenever an internal interrupt condition exists.

To enable a particular type of interrupt, the corresponding bit in the host interface must be set. If the audio interrupt bit is un-masked, and the interrupt condition is met, the AUDIO_INT pin will go HIGH. For example, if the EN_ADPG_1 is enabled, and the incoming video has embedded audio in group one, then the AUDIO_INT pin will go HIGH.

Please refer to Section 4.13.3 for HD and SD audio multiplexer status and configuration registers for a complete listing of the audio interrupts.

4.7.15 Audio Clocks

The audio multiplexer has 4 clock inputs: ACLK_1, ACLK_2, WCLK_1 and WCLK_2. For serial audio input modes ACLK_1/2 must be provided at 64fs, where fs is the fundamental sampling frequency of 48kHz. An audio word clock at 48kHz must also be supplied at the WCLK_1/2 inputs. For AES/EBU audio input mode, the ACLK_1/2 and WLCK_1/2 inputs are not required. All required clocks will automatically be derived from the AES/EBU preambles. ACLK_1/2 and WCLK_1/2 will be HIGH impedance in AES/EBU audio input mode.

Table 4-12: GS1582 Serial Audio Data Inputs

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Data Set-up Time	t_{SU}	50% levels; 3.3V or 1.8V operation	74	–	–	ns
Input Data Hold Time	t_{IH}		74	–	–	ns

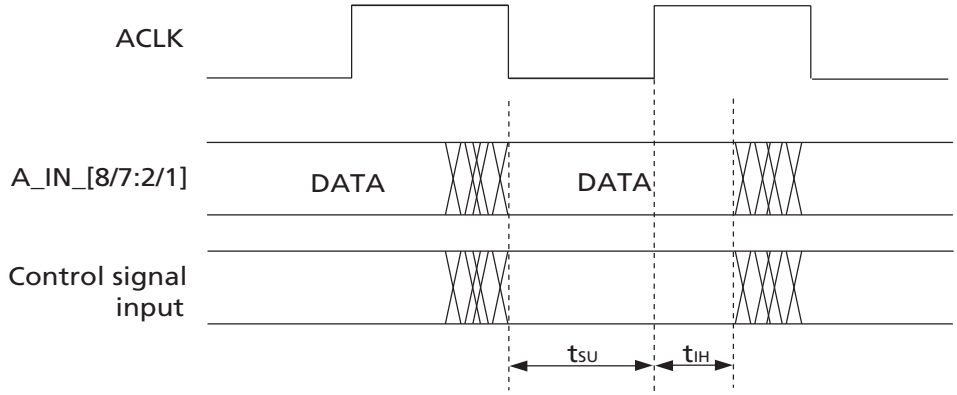


Figure 4-18: ACLK to Data & Control Signal Input Timing

4.7.16 5-frame Sequence Detection

5-frame sequence detection is required for 525-line based standard definition formats and to embed the Audio Frame Number word in the audio control packets for synchronous audio in both HD and SD formats.

4.7.16.1 SD Audio Multiplexing

The GS1582 detects the frame sequence that describes the sample distribution for synchronous audio. This information is used in the generation of the Audio Frame Number (AFN) field, describing the position of the current frame within the sequence. AFN values will only be generated for group A if the AFNA_AUTO bit in the host interface, and for group B if the AFNB_AUTO bit is set.

If the GS1582 is not configured to generate AFN values, the AFN field will be set to 0 at all times. However, if the core is configured to generate AFN values, the AFN value will be between 1 and 5, depending on where the given frame lies in the frame sequence. With a frame rate of 25 Hz, each frame will contain 1920 samples, and each frame will have an AFN of one (see Table 4-13). For a frame rate of 29.97 Hz, 8008 samples are distributed over 5 frames, as shown in Table 4-14.

The GS1582 will add the offset specified in the AFN_OFS[2:0] host interface field to the generated AFN. The result will wrap around, leaving the resulting AFN in the range of 1 through 5.

4.7.16.2 HD Audio Multiplexing

If the ASXA bit of the host interface is set to asynchronous audio, the GS1582 will set the AFN of the group 1 control packets to zero. The GS1582 will also set the AFN of the group 1 control packets to zero if the AFNA_AUTO bit in the host interface is not set. The same relationship holds for the ASXB and AFNB_AUTO bits for group 2.

The GS1582 will detect video standards with 29.97 and 59.94 frame rates by using the 5-frame sequence detect block. If a 5-frame sequence is detected, the Audio Frame Number word in the audio control packets will be embedded with the running sequence 1 through 5.

The GS1582 will add the offset specified in the AFN_OFS[2:0] host interface field to the generated AFN. The result will wrap around, leaving the resulting AFN in the range of 1 through 5.

In cases where each frame has the same number of samples, the Multiplexer will set the AFN to zero for every frame. These cases are shown in Table 4-13. In cases where each frame has a different number of samples, the sequences shown in Table 4-14 are used.

Table 4-13: Frame Rates with AFN = 0

Frame Rate (fps)	Samples per Video Frame
30	1600
25	1920
60	800
24	2000
23.98	2002

Table 4-14: Frame Rates with varying samples per frame

Frame Rate (fps)	Samples, AFN = 1[1]	Samples, AFN = 2[1]	Samples, AFN = 3[1]	Samples, AFN = 4[1]	Samples, AFN = 5[1]
29.97	1602	1601	1602	1601	1602
59.94	801	800	801	801	801

NOTES:

1. AFNs are assuming AFN_OFS = 0.

4.7.17 Audio Input Format

The GS1582 accepts two audio input formats, AES/EBU digital audio input and serial digital audio input, as listed in Table 4-15. The serial audio input can be formatted in the following five modes:

- I^2S
- Left Justified; MSB first

- Left Justified; LSB first
- Right Justified; MSB first
- Right Justified; LSB first

The audio input format for each audio group is configured using the AMA[1:0] (group 1 channels 1 and 2/Stereo Pair A), AMB[1:0] (group 1 channels 3 and 4/Stereo Pair B), AMC[1:0] (group 2 channels 5 and 6/Stereo Pair C), and AMD[1:0] (group 2 channels 7 and 8/Stereo Pair D) host interface registers. The default audio mode is I^2S input. For serial input formats, MSB first is default, and LSB first is available via the LSB_FIRSTx bit in the host interface.

NOTE: Since the audio clocks are common to all channels within one group, all channels in each group of four must be the same format. However there is no restriction on the format of different channels in one group when audio is in AES/EBU format. Also, the audio format of each group may be different.

Table 4-15: Audio Input Formats

AMx[1:0]	LSB_FIRSTx	Audio Output Format
00	0	AES/EBU audio input
01	0	Serial audio input: Left justified; MSB first
01	1	Serial audio input: Left justified; LSB first
10	0	Serial audio input: Right justified; MSB first
10	1	Serial audio input: Right justified; LSB first
11	0	I^2S serial audio input (Default)

4.7.17.1 AES/EBU Mode

In AES/EBU input mode, the audio sample bit rate of 64fs (3.072MHz) is effectively doubled by the bi-phase mark encoding, resulting in an effective input data rate at 128fs (6.144MHz). The AES/EBU sub-frame formatting is shown in Figure 4-19 below.

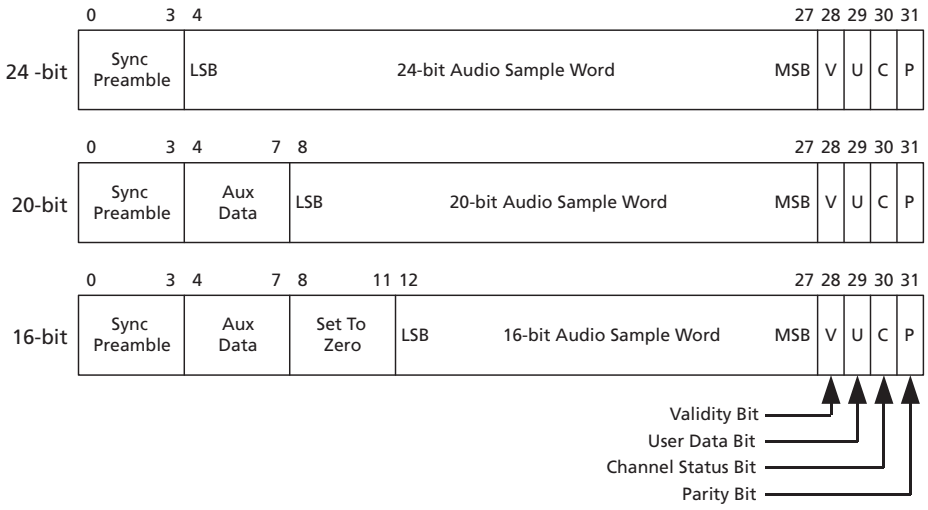


Figure 4-19: AES/EBU Sub-frame Formatting

The audio clock to data timing and input format is shown in Figure 4-20.

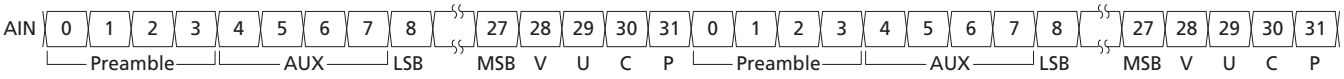


Figure 4-20: AES/EBU Audio Input Format

NOTE: Due to the bi-phase mark encoding used in AES/EBU mode, for each logic 1 bit period, there will be an additional transition. In Figure 4-20, this additional transition is not shown.

In the event of a parity error in Stereo Pair A in AES/EBU mode, the GS1582 will set the AES_ERRA bit in the host interface. The same is true of AES_ERRB for Stereo Pair B, AES_ERRC for Stereo Pair C, and AES_ERRD for Stereo Pair D.

NOTE: In order to read back the parity error bits of register 1, register 2 must be read first to trigger an update of these bits. The parity error bits will be cleared when read from register 1.

4.7.17.2 Serial Audio Input Mode

In serial audio input modes, the GS1582 clocks the audio data input on the rising edge of the ACLK_1/2 input clock at 64fs (3.072MHz), as shown in Figure 4-21, Figure 4-24 and Figure 4-25 below.

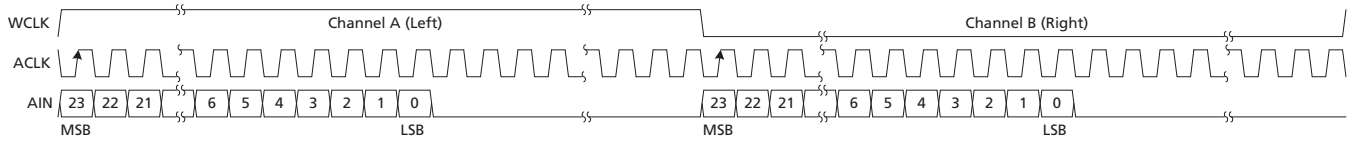


Figure 4-21: Serial Audio Input: Left Justified; MSB First

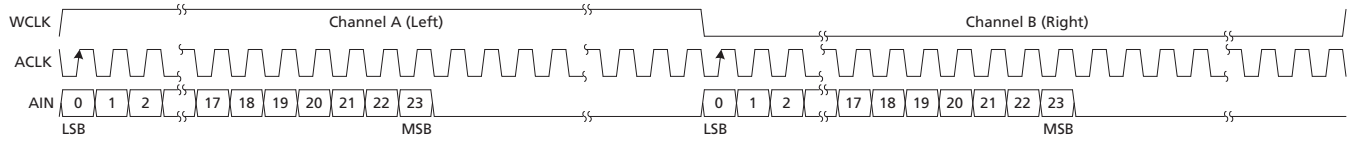


Figure 4-22: Serial Audio Input: Left Justified; LSB First

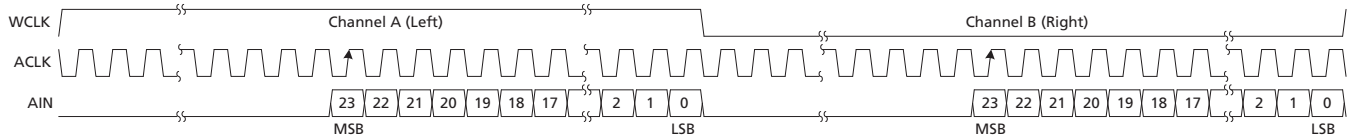


Figure 4-23: Serial Audio Input: Right Justified; MSB First

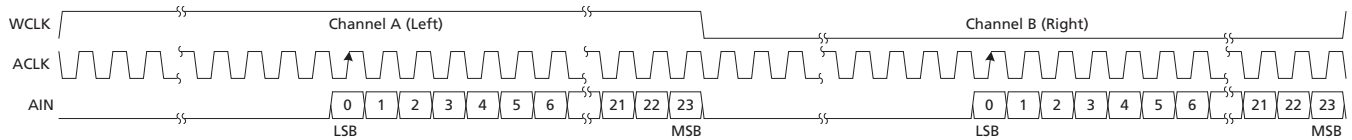


Figure 4-24: Serial Audio Input: Right Justified; LSB First

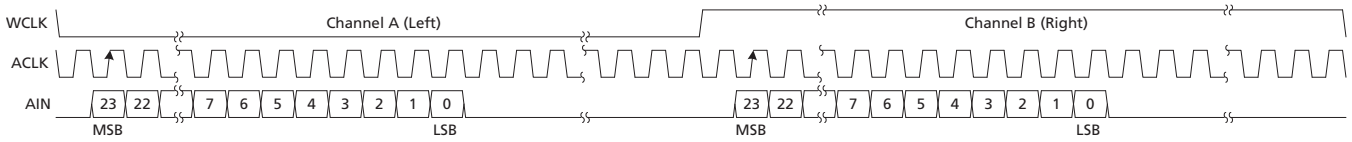


Figure 4-25: I^2S Audio Input

4.7.18 Audio Channel Status Input

The Audio Channel Status block information can be programmed via the host interface using the ACSR[183:0] register (see Table 4-17: Audio Channel Status Information Register Settings). The Audio Channel Status input consists of 24 bytes transmitted 1 bit per audio sample over a 192-frame sequence. The same audio channel status information is embedded for each sample in an audio frame, over all 8 input channels. The GS1582 generates the Z bit to denote the start of the Audio Channel Status block.

When the ACS_REGEN bit in the host interface is set HIGH, the GS1582 will use the Audio Channel Status information programmed in the ACSR[183:0] register to replace the Audio Channel Status block in all eight channels. The CRC for the Audio Channel Status block will be calculated automatically. The GS1582 will use this new Audio Channel Status information only when ACS_APPLY is HIGH and a new status boundary at this point. When the ACS_APPLY is set, the APPLY_WAITA host interface bit will be asserted until a status boundary for audio group 1 occurs. Similarly, APPLY_WAITB will be asserted starting when ACS_APPLY is set, and ending when a status boundary for audio group 2 occurs.

Table 4-16 shows the default settings for the Audio Channel Status block. The GS1582 automatically generates the CRC byte.

Table 4-16: Audio Channel Status Block Default Settings

Name	Byte	Bit	Default	Mode
PRO	0	0	1b	Professional use of channel status block
Emphasis	0	2-4	100b	None. Receiver manual override disabled
Sample Frequency	0	6-7	01b	48kHz. Manual override or auto disabled
Channel Mode	1	0-3	0001b	Two channels. Manual override disabled
AUX	2	0-2	000b	SD Mode: Maximum audio word length is 20 bits
			001b	HD Mode: Maximum audio word length is 24 bits
Source Word Length	2	3-5	101b	Maximum word length (based on AUX setting). 24-bit for HD formats; 20-bit for SD formats

Table 4-17: Audio Channel Status Information Register Settings

Name	Description	Default
ACSR[7-0]	Audio channel status block byte 0 set	85h
ACSR[15-8]	Audio channel status block byte 1 set	08h
ACSR[23-16]	Audio channel status block byte 2 set	28h (SD)
		2Ch (HD)
ACSR[31-24] ACSR[183-176]	Audio channel status block set for bytes 3 to 22	00h

4.7.19 Audio Crosspoint

The audio crosspoint allows any single input channel to be embedded as one or more of the 8 embedded audio channels. The default setting is for one-to-one mapping, where Ain_1/2 is embedded as Ch1 and Ch2, Ain_3/4 is embedded as Ch3 and Ch4, and so on.

The same audio channel cannot be used in both group 1 and 2 at the same time. The GS1582 will assert the XPOINT_ERROR host interface bit if any audio channel is programmed to be included in both groups.

The source channel is set via the host interface. Table 4-18 lists the 3-bit address for audio channel mapping.

Table 4-18: Audio Channel Mapping Codes

Audio Input Channel	3-bit Host Interface Source Address
Group 1 channel 1	000b
Group 1 channel 2	001b
Group 1 channel 3	010b
Group 1 channel 4	011b
Group 2 channel 1	100b
Group 2 channel 2	101b
Group 2 channel 3	110b
Group 2 channel 4	111b

Table 4-19: Source Input Address Registers

Name	Description	Default
GP1_CH1_SRC[2:0]	Group 1 channel 1 source selector	000b
GP1_CH2_SRC[2:0]	Group 1 channel 2 source selector	001b
GP1_CH3_SRC[2:0]	Group 1 channel 3 source selector	010b
GP1_CH4_SRC[2:0]	Group 1 channel 4 source selector	011b
GP2_CH1_SRC[2:0]	Group 2 channel 1 source selector	100b
GP2_CH2_SRC[2:0]	Group 2 channel 2 source selector	101b
GP2_CH3_SRC[2:0]	Group 2 channel 3 source selector	110b
GP2_CH4_SRC[2:0]	Group 2 channel 4 source selector	111b

NOTE: Audio channels can be paired only when both channels are derived from the same word clock and are synchronous.

4.7.20 Audio Word Clock

The GS1582 uses two word clocks, WCLK_1 and WCLK_2. By default, Audio group 1 will use the clock at the WCLK_1 input, and Audio group 2 will use the word clock at WCLK_2. The word clock assignment for each audio group can be changed by programming the GP1_WCLK_SRC[1:0] and GP2_WCLK_SRC[1:0] registers.

In AES mode, the audio clocks are extracted from the input audio data. By default, audio clock for group 1 is extracted from channel pair 1/2, and audio clock group 2 is extracted from channel pair 5/6. The default can be changed by programming the GP1_WCLK_SRC[1:0] and GP2_WCLK_SRC[1:0] register. Table 4-20: Audio Clock Selection Host Interface Settings shows the audio clock source for each setting of the registers.

Each audio group consists of 4 channels, which share the same word clock. Therefore, the audio data applied to each channel within the group must be the same format and have identical word clock requirements.

NOTE: In AES mode, by default, word clock is extracted from channels 1/2 for Audio group 1 and channels 5/6 for Audio group 2. If audio is applied only to 3/4 or 7/8 only, then no audio is embedded until the word clock source is changed from channels 1/2 or 5/6, to channels 3/4 or 7/8.

Table 4-20: Audio Clock Selection Host Interface Settings

GP_WCLK_SRC[1:0]	Word Clock Extraction Source (AES Mode)	WCLK Source (Serial Audio Mode)
00b	Channels 1/2	WCLK_1
01b	Channels 3/4	WCLK_1
10b	Channels 5/6	WCLK_2
11b	Channels 7/8	WCLK_2

4.7.21 GS1582 SD Audio FIFO Block

The GS1582 SD audio FIFO block contains the audio sample buffers. There is a buffer per audio channel, which are 52 audio samples deep. At power up or reset, the read pointer is held at the zero position until 26 samples have been written into the FIFO. Once audio is being multiplexed, the offset between the audio sample buffer read and write pointers is maintained at an average of 26 samples.

The position of the write pointer with respect to the read pointer is checked constantly. If the write pointer is less than 6 samples ahead of the read pointer, a sample is repeated from the read-side of the buffer. If the write pointer is less than 6 samples behind the read pointer, a sample is dropped. This scheme avoids buffer underflow/overflow conditions.

The repeat or drop sample operation is performed up to a maximum of 28 consecutive times. After 28 repeat/drops, the GS1582 will mute (null audio packets are embedded).

The audio buffer pointer offset can be reduced from 26 samples to 12 or 6 samples using the OS_SEL[1:0] host interface register. The default setting is 26 samples (see Table 4-21). When the OS_SEL[1:0] bits are set for 6-sample pointer offset, no boundary checking is performed.

Table 4-21: Audio Buffer Pointer Offset Settings

OS_SEL[1:0]	Buffer Pointer Offset
00	26 samples (default)
01	12 samples
10	6 samples

The CLEAR_AUDIO bit in the host interface can be used to clear the FIFOs. When asserted, this bit resets the FIFOs to the start-up state.

4.7.22 Audio Sample Distributions

4.7.22.1 525-line Audio Sample Distribution

This following sample distribution allows the embedding of 16 channels (4 audio groups) of 24-bit sampled audio into the HANC of 525-line based video formats.

The sample distribution is established for group 1 and then offset by 1 line for each subsequent group. The sample distribution is as follows (start line is 12):

$\{[3]^{(10+G)},([4],[3]^{15})^{15},[4],[3]^{(11-G)},[0],[3]^{(3+G)},([4],[3]^{15})^{15},[4/3],[3]^{12},[4],[3]^{(4-G)},[0]\}^{5}$

[#] = Number of samples / line
[4/3] = One line with either 3 or 4 samples depending on five-frame sequence
$^{(\#)}$ = Number of times to repeat the sequence. When this # is 0, no samples are inserted
G = Audio group number from 1 to 4
$\{\ldots\}^{5}$ = 5-frame sequence as shown in Table 4-22:

Table 4-22: 5-frame Sequence Sample Distribution

Frame	Number of samples
1	1602
2	1601
3	1602
4	1601
5	1602

Table 4-23, Table 4-24, Table 4-25, and Table 4-26 show the audio sample distributions for each of the four audio groups. Each distribution has 525 lines with either 1602 or 1601 samples based on the frame number of the five-frame sequence.

NOTE: When 1602 samples are required, the [4/3] term represents a line with 4 samples. When 1601 samples are required, the [4/3] term represents a line with 3 samples.

Table 4-23: Group 1 Audio Sample Distribution

	$[3]^{(10+1)}$	$([4],[3]^{15})^{15}$	$[4],[3]^{(11-1)}$	$[0],[3]^{(3+1)}$	$([4],[3]^{15})^{15}$	$[4/3],[3]^{12}$	$[4],[3]^{(4-1)},[0]$
Samples	33	735	34	12	735	40 / 39	13
Lines	11	240	11	5	240	13	5

Table 4-24: Group 2 Audio Sample Distribution

	$[3]^{(10+2)}$	$([4],[3]^{15})^{15}$	$[4],[3]^{(11-2)}$	$[0],[3]^{(3+2)}$	$([4],[3]^{15})^{15}$	$[4/3],[3]^{12}$	$[4],[3]^{(4-2)},[0]$
Samples	36	735	31	15	735	40 / 39	10
Lines	12	240	10	6	240	13	4

Table 4-25: Group 3 Audio Sample Distribution

	$[3]^{(10+3)}$	$([4],[3]^{15})^{15}$	$[4],[3]^{(11-3)}$	$[0],[3]^{(3+3)}$	$([4],[3]^{15})^{15}$	$[4/3],[3]^{12}$	$[4],[3]^{(4-3)},[0]$
Samples	39	735	28	18	735	40 / 39	7
Lines	13	240	9	7	240	13	3

Table 4-26: Group 4 Audio Sample Distribution

	$[3]^{(10+4)}$	$([4],[3]^{15})^{15}$	$[4],[3]^{(11-4)}$	$[0],[3]^{(3+4)}$	$([4],[3]^{15})^{15}$	$[4/3],[3]^{12}$	$[4],[3]^{(4-4)},[0]$
Samples	42	735	25	21	735	40 / 39	4
Lines	14	240	8	8	240	13	2

4.7.22.2 625-line Audio Sample Distribution

The following sample distribution is for 625-line video standards which leaves more free HANC space when inserting 16 channels (4 audio groups) of 24-bit sampled audio.

The sample distribution is established for group 1 and then offset by 1 line for each subsequent group. The sample distribution is as follows (start line is 8):

$[3]^{(G-1)},([4],[3]^{11})^{25},[4],[3]^{(12-G)},[0],\ [3]^{(G-1)},([4],[3]^{11})^{24},[4],[3]^{(23-G)},[0]$

[#] = Number of samples / line
$^{(\#)}$ = Number of times to repeat the sequence
$[3]^{(0)}$ = No lines with no samples
G = Audio group number from 1 to 4

NOTE: For audio group 1, the $[3]^{(G-1)}$ terms are 0 (zero) and lines 8 and 321 start with the 4 samples of the $([4],[3]^{11})^{25}$ and $([4],[3]^{11})^{24}$ sequences, respectively.

Table 4-27, Table 4-28, Table 4-29, and Table 4-30 show the audio sample distributions for each of the four audio groups. Each distribution has 625 lines with 1920 samples.

Table 4-27: Group 1 Audio Sample Distribution

	$[3]^{(1-1)}$	$([4],[3]^{11})^{25}$	$[4],[3]^{(12-1)}$	$[0],[3]^{(1-1)}$	$([4],[3]^{11})^{24}$	$[4],[3]^{(23-1)},[0]$
Samples	0	925	37	0	888	70
Lines	0	300	12	1	288	24

Table 4-28: Group 2 Audio Sample Distribution

	$[3]^{(2-1)}$	$([4],[3]^{11})^{25}$	$[4],[3]^{(12-2)}$	$[0],[3]^{(2-1)}$	$([4],[3]^{11})^{24}$	$[4],[3]^{(23-2)},[0]$
Samples	3	925	34	3	888	67
Lines	1	300	11	2	288	23

Table 4-29: Group 3 Audio Sample Distribution

	$[3]^{(3-1)}$	$([4],[3]^{11})^{25}$	$[4],[3]^{(12-3)}$	$[0],[3]^{(3-1)}$	$([4],[3]^{11})^{24}$	$[4],[3]^{(23-3)},[0]$
Samples	6	925	31	6	888	64
Lines	2	300	10	3	288	22

Table 4-30: Group 4 Audio Sample Distribution

	$[3]^{(4-1)}$	$([4],[3]^{11})^{25}$	$[4],[3]^{(12-4)}$	$[0],[3]^{(4-1)}$	$([4],[3]^{11})^{24}$	$[4],[3]^{(23-4)},[0]$
Samples	9	925	28	9	888	61
Lines	3	300	9	4	288	21

4.7.22.3 Synchronous Audio Sample Distributions

Table 4-31 lists the audio sample distributions for synchronous audio at all the video frame rates supported by the GS1582.

Table 4-31: Synchronous Audio Sample Distributions

Frame Rate (fps)	Samples per Video Frame
30	1600/1
29.97	8008/5
25	1920/1
60	800/1
59.94	4004/5
24	2000/1
23.98	2002/1

4.7.23 Audio Mute

When the AUDIO_MUTEn bits of the host interface are set HIGH, the embedded audio sample data will be set to all zeros (null audio packets). To set all the embedded audio channels to mute, set the host interface AUDIO_ALL bit HIGH.

Refer to Section 4.13.3 for GS1582 status and configuration registers.

4.8 Ancillary Data Insertion

Horizontal or vertical ancillary data words may be inserted on up to four different lines per video frame. In order to insert HANC data, the ANC_TYPE bit in the host interface, must be set LOW. VANC data can be inserted by setting the ANC_TYPE bit in the host interface HIGH. By default, at power up, HANC data insertion is selected.

The user must write the ancillary data words to be inserted, the line number for the insertion, and the total number of words to be inserted to the designated registers in the host interface. At power up, or after system reset, all ANC data insertion line numbers and total number of words default to zero.

All data words including the ancillary packet ADF, DBN, DC, DID, SDID, and CHECKSUM (placeholder) must be provided. The user provided CHECKSUM word is a placeholder. The correct value will be calculated and inserted automatically.

Two modes of operation are provided – separate line mode and concatenated mode. By default, at power up or after system reset, separate line operating mode is selected.

The GS1582 ancillary data insertion provides no error checking or correction. The provided ancillary data must be fully SMPTE compliant.

The PACKET_MISSED bit in the host interface is set if:

- An ancillary data packet is only partially inserted because there is no more free space in the HANC or VANC region of the selected line
- An ancillary data packet is not inserted at all because there is no free space in the HANC or VANC region of the selected line
- The number of words to insert programmed through the host interface is greater than the maximum allowed for the operating mode (128 in separate line mode or 512 in concatenated line mode). Under this condition, the bit will be set once the maximum number has been reached

This bit is cleared once per frame on the rising edge of V or when it is read through the host interface.

In SD mode, two modes of operation are provided – separate line mode and concatenated mode. By default, at power up or after system reset, separate line operating mode is selected.

Ancillary data packets are inserted into the multiplexed YCbCr video stream. In HD mode, by default ancillary data packets will be inserted into the luma channel. Insertion in the chroma channel may be selected via the host interface. Ancillary data insertion in the luma and chroma channels can be selected on a per line basis.

Ancillary data insertion only takes place if the IOPROC_EN/$\overline{\text{DIS}}$ pin is set HIGH, $\overline{\text{SMPTE_BYPASS}}$ is set HIGH, and the ANC_INS bit in the IOPROC_DISABLE register is set LOW.

NOTE 1: It is good practice to program the ancillary data words prior to programming the line number and number of words. Ancillary data insertion only begins once the line number and number of words are set to a non-zero value. Therefore, this practice ensures that no data is written to the ANC space before the programming is complete. As such, no unintended data is written to the ANC space, even if the programmed line number is reached before the programming is complete. Also, read/write conflicts are avoided.

NOTE 2: In both separate line mode and concatenated mode, more than one ANC packet may be inserted per line. The user provided ANC packets must contain a checksum place holder word. The correct checksum for each packet will then be re-calculated and inserted by GS1582. The total number of words for all the provided ancillary data packets with checksum should not exceed 128 in separate line mode and 512 in concatenated mode.

4.8.1 Ancillary Data Insertion Operating Mode

4.8.1.1 Separate Line Mode

In separate line mode, it is possible to insert horizontal or vertical ancillary data on up to four lines per video frame. For each of the four video lines, up to 128 8-bit HANC or VANC data words can be inserted. Separate line mode is selected by setting the ANC_INS_MODE bit in the host interface LOW. By default, at power up, separate line mode is selected.

The non-zero video line numbers on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert per line must be provided via the host interface. At power up, or after system reset, all ancillary data insertion line numbers and total number of words default to zero.

If the total number of data words specified per line exceeds 128 only the first 128 data words will be inserted.

The device automatically converts the provided 8-bit data words into the 10-bit data, formatted according to SMPTE 291M prior to insertion.

4.8.1.2 Concatenated Mode

In concatenated mode, it is possible to insert up to 512 8-bit horizontal or vertical ancillary data words on one line per video frame. Concatenated line mode can be selected by setting the ANC_INS_MODE bit in the host interface HIGH. By default, at power up, separate line mode is selected.

The non-zero video line number on which to insert the ancillary data, the ancillary data type (HANC or VANC), and the total number of words to insert must be provided via the host interface. At power up, or after system reset, the ancillary data insertion line number and total number of words default to zero.

If the total number of data words specified exceeds 512 only the first 512 data words will be inserted.

The device automatically converts the provided 8-bit data words into the 10-bit data formatted according to SMPTE 291M prior to insertion.

4.8.2 HANC Insertion

By default, at power up or after system reset, all ancillary data is inserted in the HANC space. Data is inserted contiguously starting at the TRS EAV or the first available location following any audio and pre-existing ancillary data packets. Data insertion terminates when all provided data words have been inserted or at the start of the TRS SAV code, whichever occurs first. If termination occurs before all words have been inserted, the PACKET_MISSED bit will be set in the host interface.

NOTE 1: EDH packet insertion in SD mode occurs following ancillary data insertion. Thus, any HANC data inserted on the same line as the EDH packet may be overwritten during EDH insertion. When HANC data is inserted on an EDH line, the PACKET_MISSED bit may be erroneously set, even though the ancillary data packet has been inserted correctly.

NOTE 2: HANC space ancillary data headers undergo 8-bit to 10-bit remapping. This means that when the 8 MSBs are all zero, the value gets mapped to 000 and when the 8 MSBs are all 1, the value gets mapped to 3FF. (i.e. 000, 001, 002, 003 –—> 000 and 3FE, 3FD, 3FC –—> 3FF)

4.8.3 VANC Insertion

Ancillary data insertion into the VANC space can be selected via the host interface. Data is inserted contiguously starting at the TRS SAV or the first available location following any pre-existing ancillary data packets. Data insertion terminates when all provided data words have been inserted or at the start of the TRS EAV code, whichever occurs first. If termination occurs before all words have been inserted, the PACKET_MISSED bit will be set in the host interface.

NOTE: When ancillary data is inserted into the active region of the video raster using the VANC feature, if the ILLEGAL_REMAP in the IOPROC_DISABLE register bit is set to 0, then the ADFs are remapped to '004 | 3FB | 3FB' and the downstream devices will not detect the ancillary data packets.

4.9 Additional Processing Functions

The GS1582 incorporates additional data processing which is available in SMPTE mode only, see SMPTE Mode on page 29.

4.9.1 ANC Data Blanking

The horizontal and vertical ancillary spaces of the input video may be 'blanked' by the GS1582. In this mode, the TRS words and active video will be preserved. Any additional processing functions including audio embedding, including ancillary data insertion, occur after blanking and will be present in the output video stream.

This function is enabled by setting the $\overline{\text{ANC_BLANK}}$ pin LOW.

4.9.2 Automatic Video Standard Detection

The GS1582 can detect the input video standard by using the timing parameters extracted from the received TRS ID words, the supplied H_Blanking, V_Blanking, and F_Digital timing signals, or the CEA 861 timing signals, see HVF Timing on page 29 and CEA 861 Timing on page 31. This information is presented in the VIDEO_STANDARD register (Table 4-32).

Total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are also calculated and available via the RASTER_STRUCTURE registers (Table 4-33). These line and sample count registers are updated once per frame at the end of line 12.

After device reset, the four RASTER_STRUCTURE registers default to zero.

Table 4-32: Host Interface Description for Video Standard Register

Register Name	Bit	Name	Description	R/W	Default
VIDEO_STANDARD Address: 004h	15	–	Not Used.	–	–
	14-10	VD_STD[4:0]	Video Data Standard (see Table 4-34).	R	0
	9	INT_$\overline{\text{PROG}}$	Interlace/Progressive: Set LOW if detected video standard is PROGRESSIVE and is set HIGH if it is INTERLACED.	R	0
	8	STD_LOCK	Standard Lock: Set HIGH when the device has achieved full synchronization.	R	0
	7-0	–	Not Used.	–	–

Table 4-33: Host Interface Description for Raster Structure Registers

Register Name	Bit	Name	Description	R/W	Default
RASTER_STRUCTURE1 Address: 00Eh	15-12	–	Not Used.	–	–
	11-0	RASTER_STRUCTURE_1[11:0]	Words Per Active Line	R	0
RASTER_STRUCTURE2 Address: 00Fh	15-13	–	Not Used.	–	–
	12-0	RASTER_STRUCTURE_2[12:0]	Words Per Total Line.	R	0
RASTER_STRUCTURE3 Address: 010h	15-11	–	Not Used.	–	–
	10-0	RASTER_STRUCTURE_3[10:0]	Total Lines Per Frame	R	0
RASTER_STRUCTURE4 Address: 011h	15-11	–	Not Used.	–	–
	10-0	RASTER_STRUCTURE_4[10:0]	Active Lines Per Field	R	0

4.9.3 Video Standard Indication

The value reported in the VD_STD[4:0] bits of the VIDEO_STANDARD register corresponds to the SMPTE standards as shown in Table 4-34.

In addition to the 5-bit video standard code word, the VIDEO_STANDARD register also contains two status bits. The STD_LOCK bit will be set HIGH whenever the device has achieved full synchronization. The INT_$\overline{\text{PROG}}$ bit will be set LOW if the detected video standard is progressive and HIGH if the detected video standard is interlaced.

The VD_STD[4:0], STD_LOCK and INT_$\overline{\text{PROG}}$ bits of the VIDEO_STANDARD register will default to zero after device reset. The VD_STD[4:0] and INT_$\overline{\text{PROG}}$ bits will also default to zero if the $\overline{\text{SMPTE_BYPASS}}$ pin is asserted LOW. The STD_LOCK bit will retain its previous value if the PCLK is removed.

Table 4-34: Supported Video Standards

VD_STD[4:0]	SMPTE Standard	Video Format	Length of HANC	Length of Active Video	Total Samples	SMPTE352M Lines
00h	296M (HD)	1280x720/60 (1:1)	358	1280	1650	13
01h	296M (HD)	1280x720/60 (1:1) - EM	198	1440	1650	13
02h	296M (HD)	1280x720/30 (1:1)	2008	1280	3300	13
03h	296M (HD)	1280x720/30 (1:1) - EM	408	2880	3300	13
04h	296M (HD)	1280x720/50 (1:1)	688	1280	1980	13
05h	296M (HD)	1280x720/50 (1:1) - EM	240	1728	1980	13
06h	296M (HD)	1280x720/25 (1:1)	2668	1280	3960	13
07h	296M (HD)	1280x720/25 (1:1) - EM	492	3456	3960	13
08h	296M (HD)	1280x720/24 (1:1)	2833	1280	4125	13
09h	296M (HD)	1280x720/24 (1:1) - EM	513	3600	4125	13
0Ah	274M (HD)	1920x1080/60 (2:1) or 1920x1080/30 (PsF)	268	1920	2200	10, 572
0Bh	274M (HD)	1920x1080/30 (1:1)	268	1920	2200	18
0Ch	274M (HD)	1920x1080/50 (2:1) or 1920x1080/25 (PsF)	708	1920	2640	10, 572
0Dh	274M (HD)	1920x1080/25 (1:1)	708	1920	2640	18
0Eh	274M (HD)	1920x1080/25 (1:1) - EM	324	2304	2640	18
0Fh	274M (HD)	1920x1080/25 (PsF) - EM	324	2304	2640	10, 572
10h	274M (HD)	1920x1080/24 (1:1)	818	1920	2750	18
11h	274M (HD)	1920x1080/24 (PsF)	818	1920	2750	10, 572
12h	274M (HD)	1920x1080/24 (1:1) - EM	338	2400	2750	18
13h	274M (HD)	1920x1080/24 (PsF) - EM	338	2400	2750	10, 572
14h	295M (HD)	1920x1080/50 (2:1)	444	1920	2376	10, 572
15h	260M (HD)	1920x1035/60 (2:1)	268	1920	2200	10, 572
16h	125M (SD)	1440x487/60 (2:1) (Or dual link progressive)	268	1440	1716	13, 276
17h	125M (SD)	1440x507/60 (2:1)	268	1440	1716	13, 276
19h	125M (SD)	525-line 487 generic	–	–	1716	13, 276
1Bh	125M (SD)	525-line 507 generic	–	–	1716	13, 276
18h	ITU-R BT.656 (SD)	1440x576/50 (2:1) (Or dual link progressive)	280	1440	1728	9, 322

Table 4-34: Supported Video Standards (Continued)

VD_STD[4:0]	SMPTE Standard	Video Format	Length of HANC	Length of Active Video	Total Samples	SMPTE352M Lines
1Ah	ITU-R BT.656 (SD)	625-line generic (EM)	–	–	1728	9, 322
1Dh	Unknown HD	–	–	–	–	–
1Eh	Unknown SD	–	–	–	–	–
1Ch, 1Fh	Reserved	–	–	–	–	–

NOTE: Though the GS1582 will work correctly on and serialize both 59.94Hz and 60Hz formats, it will not distinguish between them.

4.9.4 Packet Generation and Insertion

The GS1582 can also calculate, assemble and insert TRS ID words, and various types of ancillary data packets.

These features are only available when the IOPROC_EN/$\overline{\text{DIS}}$ pin is set HIGH. Individual insertion features may be enabled or disabled via the IOPROC_DISABLE register (Table 4-35).

All of the IOPROC_DISABLE register bits default to '0' after device reset, enabling all of the processing features. To disable any individual error correction feature, set the corresponding bit HIGH in this register.

Table 4-35: Host Interface Description for Internal Processing Disable Register

Register Name	Bit	Name	Description	R/W	Default
IOPROC_DISABLE Address: 000h	15-13	–	Not Used. Set to zero.	–	0
	12	TIM_861_PIN_EN	Setting this bit LOW allows the timing mode to be selectable through the CEA_861bit. Setting this bit HIGH allows the timing mode to be selectable through the CEA_861 bit, regardless of the pin setting.	R/W	0
	11	ANC_INS	Enable or disable ancillary data insertion. Set LOW for enable. Set HIGH for disable.	R/W	0
	10	AUDIO_EMBED	Disable audio embedding.	R/W	0
	9	CEA_861	CEA_861 pin override bit. Active when TIM_861_PIN_EN bit is set HIGH. Set CEA_861 bit LOW to enable CEA 861 timing. Set this bit HIGH to disable CEA 861 timing.	R/W	0
	8	H_CONFIG	Horizontal blanking timing configuration. Set LOW when the H/HSYNC input timing is based on active line blanking (default). Set HIGH when the H input timing is based on the H bit of the TRS words. See Figure 4-2.	R/W	0
	7	–	Not Used. Set to zero.	–	0
	6	352M_INS	SMPTE352M packet insertion. In HD mode, 352M packets are inserted in the luma channel only when one of the bytes in the VIDEO_FORMAT_A or VIDEO_FORMAT_B registers are programmed with non-zero values. Set HIGH to disable.	R/W	0
	5	ILLEGAL_REMAP	Illegal Code Remapping. Detection and correction of illegal code words within the active picture area (AP). Set HIGH to disable.	R/W	0
	4	EDH_CRC_INS	Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error correction. In SD mode the GS1582 will generate and insert EDH packets. Set HIGH to disable.	R/W	0
	3	ANC_CSUM_INS	Ancillary Data Checksum insertion. Set HIGH to disable.	R/W	0
	2	CRC_INS	Luma and chroma line-based CRC insertion. In HD mode, line-based CRC words are inserted in both the luma and chroma channels. Set HIGH to disable	R/W	0
	1	LNUM_INS	Luma and chroma line number insertion - HD mode only. Set HIGH to disable.	R/W	0
	0	TRS_INS	Timing Reference Signal Insertion. Set HIGH to disable.	R/W	0

4.9.4.1 SMPTE 352M Payload Identifier Packet Insertion

The GS1582 can generate and insert SMPTE 352M payload identifier ancillary data packets.

When this feature is enabled, the device will automatically generate the ancillary data preambles, (DID, SDID, DBN, DC), and calculate the checksum. The SMPTE 352M packet will be inserted into the data stream according to the line numbers programmed in the LINE_352M_f1 and LINE_352M_f2 registers (Table 4-36).

Packet insertion will only take place if at least one of the bytes in the VIDEO_FORMAT_A or VIDEO_FORMAT_B registers are programmed with a non-zero value (Table 4-37). In addition, the 352M_INS bit must be set LOW (Table 4-35).

NOTE: If there are existing 352M packets in the input stream, and $\overline{\text{ANC_BLANK}}$ is set HIGH (disabled), then the existing data is preserved and new 352M is inserted. The GS1582 does not overwrite existing 352M data.

The GS1582 will differentiate between PsF and interlaced formats based on bits 14 and 15 of the VIDEO_FORMAT_A register.

The packets will be inserted immediately after the EAV word in SD video streams and immediately after the line-based CRC word in the luma channel of HD video streams. If other ancillary packets exist in the horizontal ancillary space 352M packets will be inserted immediately following these packets. SMPTE 352M packets will not be inserted if there is insufficient room in the HANC space.

Table 4-36: Host Interface Description for SMPTE 352M Packet Line Number Insertion Registers

Register Name	Bit	Name	Description	R/W	Default
LINE_0_352M Address: 01Bh	15-11	–	Not Used.	–	–
	10-0	LINE_0_352M[10:0]	Line number where SMPTE352M packet is inserted in field 1.	R/W	0
LINE_1_352M Address: 01Ch	15-11	–	Not Used.	–	–
	10-0	LINE_1_352M[10:0]	Line number where SMPTE352M packet is inserted in field 2.	R/W	0

Table 4-37: Host Interface Description for SMPTE 352M Payload Identifier Registers

Register Name	Bit	Name	Description	R/W	Default
VIDEO_FORMAT_B Address: 00Bh	15-8	Video_Format[2] [7:0]	SMPTE352M Byte 4 information must be programmed in this register when 352M_INS = LOW.	R/W	0
	7-0	Video_Format[1] [7:0]	SMPTE352M Byte 3information must be programmed in this register when 352M_INS = LOW.	R/W	0
VIDEO_FORMAT_A Address: 00Ah	15-8	Video_Format[4] [7:0]	SMPTE352M Byte 2information must be programmed in this register when 352M_INS = LOW.	R/W	0
	7-0	Video_Format[3] [7:0]	SMPTE352M Byte 1information must be programmed in this register when 352M_INS = LOW.	R/W	0

4.9.4.2 Illegal Code Remapping

If the ILLEGAL_REMAP bit of the IOPROC_DISABLE register is set LOW, the GS1582 will remap all codes within the active picture between the values of 3FCh and 3FFh to 3FBh. All codes within the active picture area between the values of 000h and 003h will be remapped to 004h.

In addition, 8-bit TRS and ancillary data preambles will be remapped to 10-bit values.

4.9.4.3 EDH Generation and Insertion

When operating in SD mode, (SD/$\overline{HD}$ = HIGH), the GS1582 will generate and insert complete EDH packets. Packet generation and insertion will only take place if the EDH_CRC_INS bit of the IOPROC_DISABLE register is set LOW.

The GS1582 will generate all of the required EDH packet data including all ancillary data preambles DID, DBN, DC, reserved code words, and the checksum. Calculation of both full field (FF) and active picture (AP) CRC's will be carried out by the device.

SMPTE RP165 specifies the calculation ranges and scope of EDH data for standard 525 and 625 component digital interfaces. The GS1582 uses these standard ranges by default.

If the received video format does not correspond to 525 or 625 digital component video standards, then the ranges will be determined from the received TRS ID words or supplied H_Blanking, V_Blanking, and F_Digital timing signals; or HSYNC, VSYNC and DE CEA 861 timing signals. See HVF Timing on page 29, and CEA 861 Timing on page 31.

The first active and full field pixel will always be the first pixel after the SAV TRS code word. The last active and full field pixel will always be the last pixel before the start of the EAV TRS code words.

EDH error flags (EDH, EDA, IDH, IDA and UES) for ancillary data, full field and active picture will also be inserted when the corresponding bit of the EDH_FLAG register is set HIGH. (Table 4-38).

NOTE 1: The EDH flag registers must be updated once per field. The prepared EDH packet will be inserted at the appropriate line according to SMPTE RP165. The start pixel position of the inserted packet will be based on the SAV position of that line such that the last byte of the EDH packet (the checksum) will be placed in the sample immediately preceding the start of the SAV TRS word.

NOTE 2: EDH packets will not be inserted if there is insufficient room in the HANC space.

Table 4-38: Host Interface Description for EDH Flag Register (SD Mode Only)

Register Name	Bit	Name	Description	R/W	Default
EDH_FLAG Address: 002h	15	–	Not Used.	–	–
	14	ANC-UES	Ancillary Unknown Error Status flag will be generated and inserted.	R/W	0
	13	ANC-IDA	Ancillary Internal device error Detected Already flag will be generated and inserted.	R/W	0
	12	ANC-IDH	Ancillary Internal device error Detected Here flag will be generated and inserted.	R/W	0
	11	ANC-EDA	Ancillary Error Detected Already flag will be generated and inserted.	R/W	0
	10	ANC-EDH	Ancillary Error Detected Here flag will be generated and inserted.	R/W	0
	9	FF-UES	Full Field Unknown Error flag will be generated and inserted.	R/W	0
	8	FF-IDA	Full Field Internal device error Detected Already flag will be generated and inserted.	R/W	0
	7	FF-IDH	Full Field Internal device error Detected flag will be generated and inserted.	R/W	0
	6	FF-EDA	Full Field Error Detected Already flag will be generated and inserted.	R/W	0
	5	FF-EDH	Full Field Error Detected Here flag will be generated and inserted.	R/W	0
	4	AP-UES	Active Picture Unknown Error Status flag will be generated and inserted.	R/W	0
	3	AP-IDA	Active Picture Internal device error Detected Already flag will be generated and inserted.	R/W	0
	2	AP-IDH	Active Picture Internal device error Detected Here flag will be generated and inserted.	R/W	0
	1	AP-EDA	Active Picture Error Detected Already flag will be generated and inserted.	R/W	0
	0	AP-EDH	Active Picture Error Detected Here flag will be generated and inserted.	R/W	0

4.9.4.4 Ancillary Data Checksum Generation and Insertion

The GS1582 will calculate checksums for all detected ancillary data packets presented to the device. These calculated checksum values are inserted into the data stream prior to serialization.

Ancillary data checksum generation and insertion will only take place if the ANC_CSUM_INS bit of the IOPROC_DISABLE register is set LOW.

NOTE: The GS1582 will recalculate the checksum and, if incorrect, will re-insert the correct value. However, the GS1582 does not check the correctness of the parity bit. That is, if all the bits from 0 to 8 in the checksum word are correct and only bit 9 (the parity bit, which is the inverse of bit 8) is incorrect, then the checksum word is not re-calculated. If even one of bit 0 to bit 8 has an incorrect value, then the checksum word is re-calculated and re-inserted.

4.9.4.5 Line Based CRC Generation and Insertion

The GS1582 will generate and insert line based CRC words into both the luma and chroma channels of the data stream. This feature is only available in HD mode and is enabled by setting the CRC_INS bit of the IOPROC_DISABLE register LOW.

4.9.4.6 HD Line Number Generation and Insertion

In HD mode, the GS1582 will calculate and insert line numbers into the luma and chroma channels of the output data stream.

Line number generation is in accordance with the relevant HD video standard as determined by the device, see Automatic Video Standard Detection on page 66.

This feature is enabled when SD/$\overline{\text{HD}}$ = LOW, and the LNUM_INS bit of the IOPROC_DISABLE register is set LOW.

4.9.4.7 TRS Generation and Insertion

The GS1582 can generate and insert 10-bit TRS code words into the data stream as required. This feature is enabled by setting the TRS_INS bit of the IOPROC_DISABLE register LOW.

TRS word generation will be performed in accordance with the timing parameters generated by the device which will be locked either to the received TRS ID words, the supplied H_Blanking, V_Blanking, and F_Digital timing signals, or the CEA 861 timing signals, see HVF Timing on page 29 and CEA 861 Timing on page 31.

4.10 Parallel to Serial Conversion

The GS1582 can accept either 10-bit or 20-bit parallel data in both SD and HD modes. The supplied PCLK rate must correspond to the settings of the SD/$\overline{\text{HD}}$ and 20bit/$\overline{\text{10bit}}$ pins as shown in Table 4-39.

Table 4-39: Serial Digital Output Rates

Supplied PCLK Rate	Serial Digital Output Rate	Pin Settings	
		SD/$\overline{HD}$	20bit/$\overline{10bit}$
74.25 or 74.25/1.001 MHz	1.485 or 1.485/1.001Gb/s	LOW	HIGH
148.5 or 148.5/1.001MHz	1.485 or 1.485/1.001Gb/s	LOW	LOW
13.5MHz	270Mb/s	HIGH	HIGH
27MHz	270Mb/s	HIGH	LOW

4.11 Internal ClockCleaner™ PLL

To obtain a clean clock signal for serialization and transmission, an external VCO signal is locked to the input PCLK via the GS1582's integrated phase-locked loop. This high quality analog PLL has a bang-bang implementation, which automatically narrows the loop bandwidth in the presence of jitter, allowing the GS1582 to significantly attenuate jitter on the incoming PCLK.

4.11.1 External VCO

The GS1582 requires the GO1555 external voltage controlled oscillator as part of its internal PLL.

Power for the external VCO is generated by the GS1582 from an integrated voltage regulator. The internal regulator uses +3.3V supplied on the CP_VDD / CP_GND pins to provide +2.5V on the VCO_VCC / VCO_GND pins.

The external VCO produces a 1.485GHz signal for the PLL, input on the VCO pin of the device. See Typical Application Circuit (Part A) on page 109.

NOTE: The VCO_VCC output voltage is guaranteed to be 2.5V only when supplying power to the GO1555. The VCO_VCC pin should not be shorted to GND under any circumstances.

4.11.2 Loop Filter

The GS1582 PLL loop filter is an external first order filter formed by a series RC connection as shown in the Typical Application Circuit (Part A) on page 109. The loop filter resistor value sets the bandwidth of the PLL and the capacitor value controls its stability and lock time. A loop filter resistor value between 1Ω to 20Ω and a loop filter capacitor value between 1µF to 33µF are recommended.

The GS1582 uses a non-linear, bang-bang, PLL, therefore its bandwidth scales with the input jitter amplitude - greater input jitter results in a smaller loop bandwidth causing more of the input jitter to be rejected. For a given input jitter amplitude, a smaller loop filter resistor produces a narrower loop bandwidth. With an input jitter amplitude of 300ps, for example, the PLL bandwidth can be adjusted from 2KHz to 40KHz by varying

the loop filter resistor, as shown in Table 4-40: Loop Filter Component Values. For use with the GEN-Clocks™ timing generators, a narrow loop bandwidth is recommended.

Increasing the loop filter capacitor value increases the stability of the PLL, but results in a longer lock time. For loop filter resistors smaller than 7Ω, a capacitor value of 33µF is recommended, while larger resistor values can accommodate smaller capacitors. Sample combinations of the loop filter resistor and capacitor values are shown in Table 4-40: Loop Filter Component Values, along with the resulting loop bandwidth. Additional loop bandwidths can be achieved by using different loop filter resistor values.

Table 4-40: Loop Filter Component Values

Loop Filter Resistor Value	Typical Loop Bandwidth*	Recommended Loop Filter Capacitor Value	Comments
1Ω	2kHz	33µF	Narrow bandwidth - provides maximum jitter reduction. Long lock-time.
7Ω	8kHz	10µF	
20Ω	40kHz	1µF	Wide bandwidth. Fast lock-time.

* Measured with 300ps pk-pk input jitter on PCLK

4.11.3 Lock Detect Output

The LOCKED output will be asserted HIGH when the internal PLL has locked to the input PCLK signal. In the absence of the PCLK, when frequency lock has not been achieved, and during device reset, the LOCKED output will be LOW.

Lock time, the time it takes for the internal PLL to frequency-lock to the reference PCLK following power-up or standby, is determined by the loop filter capacitor value chosen. A 1µF loop filter capacitor, for example, will result in lock times of less than 500µs. A 33µF loop filter capacitor, on the other hand, will result in a lock time of greater than 5s.

NOTE 1: When the PLL is in the process of locking to the reference PCLK, the LOCKED pin may generate LOW and HIGH pulses. The durations of these pulses are dependent on the loop filter capacitor value, but do not exceed 30ms. Once the PLL has achieved frequency lock, the LOCKED pin will remain HIGH and not change state.

NOTE 2: When the GS1582 is placed in standby mode, the value of LOCKED is maintained although the PLL does lose lock to the reference PCLK. When STANDBY is released, the PLL will re-lock. During this time, if the LOCKED pin was previously HIGH, it will de-assert approximately 6µs later, and re-assert once the PLL has re-locked to the input PCLK.

4.12 Serial Digital Output

The GS1582 includes a SMPTE compliant current mode differential serial digital cable driver with automatic slew rate control. The serial output has improved eye quality, exceptional ORL performance, and reduced duty cycle distortion.

The cable driver uses a separate +3.3V DC power supply provided via the CD_VDD and CD_GND pins.

To enable the output, SDO_EN/$\overline{\text{DIS}}$ must be set HIGH. Setting the SDO_EN/$\overline{\text{DIS}}$ signal LOW will set the SDO and $\overline{\text{SDO}}$ output pins to high impedance, resulting in reduced device power consumption.

4.12.1 Output Swing

Nominally, the voltage swing of the serial digital output is 800mVp-p single-ended into a 75Ω load. This is set externally by connecting the RSET pin to CD_VDD through 750Ω ±1% resistor.

4.13 GSPI Host Interface

The GS1582 host interface, also called the Gennum Serial Peripheral Interface (GSPI), provides access to configuration/status registers for the video processing and SD and HD audio processing functions of the chip.

By default, the device will be “live at power up” with all major functional blocks active in the defined default operating conditions described below.

Dedicated configuration pins are provided for basic configuration of the device.

The host interface is provided to allow optional configuration of some of the more advanced functions and operating modes of the device.

To simplify host interface access to the configuration and status registers, a single contiguous register map is provided for the video and audio functions.

Registers are grouped by like function and wherever possible functional configuration will not be spread across multiple registers.

The GSPI is comprised of a serial data input signal (SDIN), serial data output signal (SDOUT), an active low chip select ($\overline{\text{CS}}$), and a burst clock (SCLK). The burst clock must have a duty cycle between 40% and 60% while active.

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG/$\overline{\text{HOST}}$ is provided. When JTAG/$\overline{\text{HOST}}$ is LOW, the GSPI interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{\text{CS}}$ are inputs to the device. The SDOUT loops the SDIN back out when GSPI is in write mode, or when $\overline{\text{CS}}$ is HIGH, allowing multiple devices to be connected in series. During reset, SDOUT is held in high-impedance mode. The interface is illustrated in the Figure 4-26.

Each GSPI access begins with a 16-bit command word on SDIN indicating the address of the register of interest. This is followed by a 16-bit data word on SDIN in write mode, or a 16-bit data word on SDOUT in read mode.

NOTE 1: When operating in SD mode, SD/$\overline{HD}$ is set HIGH, only the SD video and audio registers are accessible for read or write. Similarly, when operating in HD mode, SD/$\overline{HD}$ is set LOW, only the HD video and audio registers are accessible for read or write.

NOTE 2: When the device is in standby mode (STANDBY = HIGH) no host interface register can be read back or written to. Attempting a read or write will not damage the device. However, all reads will return a value of 0, and no writes will take effect.

NOTE 3: In the Configuration and Status Registers, there are several registers that have been designated as Reserved. If possible, writing to these registers should be avoided. If writing a value to these registers is not avoidable, then only a value of 0 should be written to these registers. Writing a value of 1 may alter the functional behaviour of GS1582 but will not permanently damage the device.

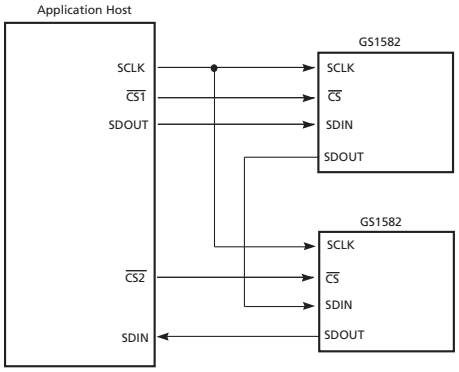


Figure 4-26: Gennum Serial Peripheral Interface (GSPI)

4.13.1 Command Word Description

The command word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address. Figure 4-27 shows the command word format and bit configurations.

Command words are clocked into the GS1582 on the rising edge of the serial clock SCLK, which operates in a burst fashion.

When the Auto-Increment bit is set LOW, each command word must be followed by only one data word to ensure proper operation. If the Auto-Increment bit is set HIGH, the following data word will be written into the address specified in the command word, and subsequent data words will be written into incremental addresses from the previous data word. This facilitates multiple address writes without sending a command word for each data word.

NOTE: All registers can be written to through single address access or through the auto-increment feature. However, the LSB of the video registers cannot be read through single address read-back. Single address read-back will return a 0 value for the LSB. If auto-increment is used to read back the values from at least two registers, the LSB value read will always be correct. Therefore, for register read-back, it is recommended that auto-increment be used and that at least two registers be read back at a time.

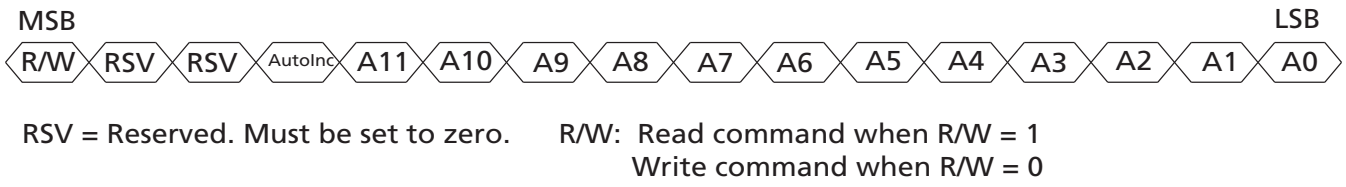


Figure 4-27: Command Word

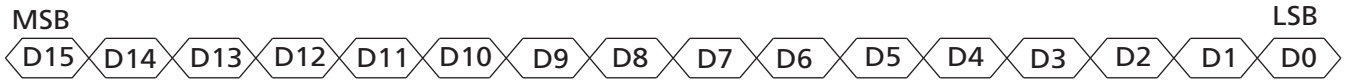


Figure 4-28: Data Word

4.13.2 Data Read and Write Timing

Read and write mode timing for the GSPI interface is shown in Figure 4-29 and Figure 4-30 respectively. The timing parameters are defined in Table 4-41.

When several devices are connected to the GSPI chain, only one $\overline{CS}$ must be set LOW during a read sequence.

During the write sequence, all command and subsequent data words are looped through from SDIN to SDOUT. When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices that have $\overline{CS}$ set LOW.

Table 4-41: GSPI Timing Parameters

Parameter	Definition	Specification
t_0	The minimum duration of time chip select, $\overline{CS}$, must be LOW before the first SCLK rising edge.	1.5 ns
t_1	The minimum SCLK period.	100 ns
t_2	Duty cycle tolerated by SCLK.	40% to 60%
t_3	Minimum input setup time.	1.5 ns
t_4	Write Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	37.1 ns
t_5	Read Cycle: the minimum duration of time between the last SCLK command (or data word if the Auto-Increment bit is HIGH) and the first SCLK of the data word.	148.4 ns
t_6	Minimum output hold time.	1.5 ns
t_7	The minimum duration of time between the last SCLK of the GSPI transaction and when $\overline{CS}$ can be set HIGH.	37.1 ns
t_8	Minimum input hold time.	1.5 ns

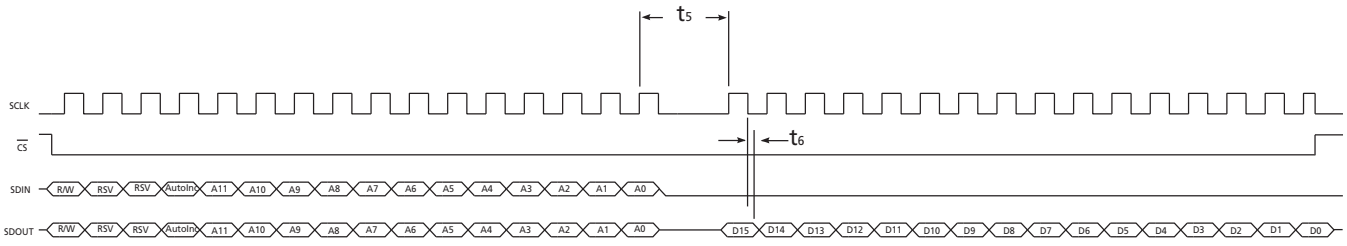


Figure 4-29: GSPI Read Mode Timing

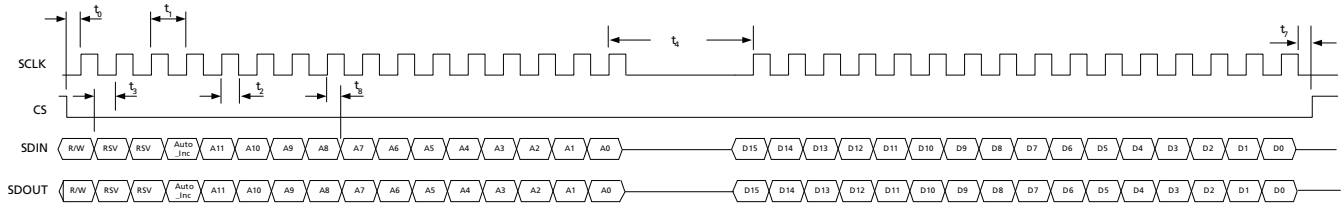


Figure 4-30: GSPI Write Mode Timing

4.13.3 Configuration and Status Registers

Table 4-42 summarizes the GS1582's internal status and configuration registers.

Table 4-43 summarizes the video status and configuration registers. Table 4-44 and Table 4-45 summarizes the SD and HD audio status and configuration registers.

All bits are available to the host via the GSPI.

Table 4-42: GS1582 Internal Registers

Address	Register Name	See Section
000h	IOPROC_DISABLE	Section 4.9.4
002h	EDH_FLAG	Section 4.9.4.3
004h	VIDEO_STANDARD	Section 4.9.2
005h - 009h	ANC_DATA_TYPE	
00Ah - 00Bh	VIDEO_FORMAT	Section 4.9.4.1
00Eh - 011h	RASTER_STRUCTURE	Section 4.9.2
01Ah	GLOBAL_ERROR_MASK_VECTOR	
01Bh - 01Ch	LINE_352M	Section 4.9.4.1

4.13.3.1 Video Registers

Table 4-43: Video Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
000h	Reserved	15-13	Reserved.	R	000b
	TIM_861_PIN_EN	12	Selects pin for control for 861 timing converter. Reference: Section 4.3.2 on page 31.	R/W	0
	ANC_INS	11	Disable for ancillary data insertion feature. Reference: Section 4.8 on page 63.	R/W	0
	AUDIO_EMBED	10	Disable audio embedding. Reference: Section 4.7 on page 37.	R/W	0
	CEA_861	9	Disable 861 timing converter. Reference: Section 4.3.2 on page 31.	R/W	0
	H_CONFIG	8	Horizontal sync timing input configuration. Set LOW when the H input timing is based on active line blanking (default). Set HIGH when the H input timing is based on the H bit of the TRS words. Reference: Section 4.3.1 on page 29.	R/W	0
	Reserved	7	Reserved.	R	0
	352M_INS	6	SMPTE352M packet insertion. In HD mode, 352M packets are inserted in the luma channel only when one of the bytes in the VIDEO_FORMAT_A or VIDEO_FORMAT_B registers are programmed with non-zero values. Set HIGH to disable. Reference: Section 4.9.4.1 on page 70.	R/W	0
	ILLEGAL_REMAP	5	Illegal Code Remapping. Detection and correction of illegal code words within the active picture area (AP). Set HIGH to disable. Reference: Section 4.9.4.2 on page 72.	R/W	0
	EDH_CRC_INS	4	Error Detection & Handling (EDH) Cyclical Redundancy Check (CRC) error correction. In SD mode the GS1582 will generate and insert EDH packets. Set HIGH to disable. Reference: Section 4.9.4.3 on page 72.	R/W	0
	ANC_CSUM_INS	3	Ancillary Data Checksum insertion. Set HIGH to disable. Reference: Section 4.9.4.4 on page 74.	R/W	0
	CRC_INS	2	Luma and chroma line-based CRC insertion. In HD mode, line-based CRC words are inserted in both the luma and chroma channels. Set HIGH to disable Reference: Section 4.9.4.5 on page 74.	R/W	0
	LNUM_INS	1	Luma and chroma line number insertion - HD mode only. Set HIGH to disable. Reference: Section 4.9.4.6 on page 74.	R/W	0

Table 4-43: Video Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
000h	TRS_INS	0	Timing Reference Signal Insertion. Set HIGH to disable. Reference: Section 4.9.4.7 on page 74.	R/W	0
001h	Reserved	15-0	Reserved.	R	N/A
002h	Reserved	15	Reserved.	R/W	0
	ANC-UES	14	Ancillary Unknown Error Status flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	ANC-IDA	13	Ancillary Internal device error Detected Already flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	
	ANC-IDH	12	Ancillary Internal device error Detected Here flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	ANC-EDA	11	Ancillary Error Detected Already flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	ANC-EDH	10	Ancillary Error Detected Here flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	FF-UES	9	Full Field Unknown Error flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	FF-IDA	8	Full Field Internal device error Detected Already flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	FF-IDH	7	Full Field Internal device error Detected flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	FF-EDA	6	Full Field Error Detected Already flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	FF-EDH	5	Full Field Error Detected Here flag will be generated and inserted. SD mode only. Reference: Section 4.9.4.3 on page 72.	R/W	0
	AP-UES	4	Active Picture Unknown Error Status flag will be generated and inserted. SD mode only.	R/W	0
	AP-IDA	3	Active Picture Internal device error Detected Already flag will be generated and inserted. SD mode only.	R/W	0
	AP-IDH	2	Active Picture Internal device error Detected Here flag will be generated and inserted. SD mode only.	R/W	0

Table 4-43: Video Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
002h	AP-EDA	1	Active Picture Error Detected Already flag will be generated and inserted. SD mode only.	R/W	0
	AP-EDH	0	Active Picture Error Detected Here flag will be generated and inserted. SD mode only.	R/W	0
003h	Reserved	15-0	Reserved.	R	N/A
004h	Reserved	15	Reserved	R	0
	VID_STD[4:0]	14-10	Reports the detected video standard. Reference: Section 4.9.3 on page 67.	R	00000b
	INT_$\overline{\text{PROG}}$	9	Interlace/Progressive: Set LOW if detected video standard is PROGRESSIVE and is set HIGH if it is INTERLACED. Reference: Section 4.9.3 on page 67.	R	0
	STD_LOCK	8	Standard Lock: Set HIGH when the device has achieved full synchronization. Reference: Section 4.9.3 on page 67.	R	0
	Reserved	7-0	Reserved.	R	N/A
005h-009h	Reserved	15-0	Reserved.	R	N/A
00Ah	Video_Format_A[15:8]	15-8	SMPTE 352M Byte 2 information must be programmed in this register when 352M_INS = LOW. Reference: Section 4.9.4.1 on page 70.	R/W	0
	Video_Format_A[7:0]	7-0	SMPTE 352M Byte 1 information must be programmed in this register when 352M_INS = LOW. Reference: Section 4.9.4.1 on page 70.	R/W	0
00Bh	Video_Format_B[15:8]	15-8	SMPTE 352M Byte 4 information must be programmed in this register when 352M_INS = LOW. Reference: Section 4.9.4.1 on page 70.	R/W	0
	Video_Format_B[7:0]	7-0	SMPTE 352M Byte 3 information must be programmed in this register when 352M_INS = LOW. Reference: Section 4.9.4.1 on page 70.	R/W	0
00Ch-00Dh	Reserved	15-0	Reserved.	R	N/A
00Eh	Reserved	15-12	Reserved.	–	–
	RASTER_STRUCTURE_1	11-0	Words Per Active Line Reference: Section 4.9.2 on page 66.	R	0
00Fh	Reserved	15-13	Reserved.	–	–
	RASTER_STRUCTURE_2	12-0	Words Per Total Line. Reference: Section 4.9.2 on page 66.	R	0
010h	Reserved	15-11	Reserved.	–	–
	RASTER_STRUCTURE_3	10-0	Total Lines Per Frame Reference: Section 4.9.2 on page 66.	R	0

Table 4-43: Video Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
011h	Reserved	15-11	Reserved.	–	–
	RASTER_STRUCTURE_4	10-0	Active Lines Per Field Reference: Section 4.9.2 on page 66.	R	0
012h	Reserved	15-10	Not Used. Set to zero.	–	0
	AP_LINE_START_F0[9:0]	9-0	Field 0 Active Picture start line data used to set EDH calculation range outside of RP 165 values.	R/W	0
013h	Reserved	15-10	Reserved.	–	–
	AP_LINE_END_F0[9:0]	9-0	Field 0 Active Picture end line data used to set EDH calculation range outside of RP 165 values.	R/W	0
014h	Reserved	15-10	Reserved.	–	–
	AP_LINE_START_F1[9:0]	9-0	Field 1 Active Picture start line data used to set EDH calculation range outside of RP 165 values.	R/W	0
015h	Reserved	15-10	Reserved.	–	–
	AP_LINE_END_F1[9:0]	9-0	Field 1 Active Picture end line data used to set EDH calculation range outside of RP 165 values.	R/W	0
016h	Reserved	15-10	Reserved.	–	–
	FF_LINE_START_F0[9:0]	9-0	Field 0 Full Field start line data used to set EDH calculation range outside of RP 165 values.	R/W	0
017h	Reserved	15-10	Reserved.	–	–
	FF_LINE_END_F0[9:0]	9-0	Field 0 Full Field end line data used to set EDH calculation range outside of RP 165 values.	R/W	0
018h	Reserved	15-10	Reserved.	–	–
	FF_LINE_START_F1[9:0]	9-0	Field 1 Full Field start line data used to set EDH calculation range outside of RP-165 values.	R/W	0
019h	Reserved	15-10	Reserved.	–	–
	FF_LINE_END_F1[9:0]	9-0	Field 1 Full Field end line data used to set EDH calculation range outside of RP-165 values.	R/W	0
01Ah	Reserved	15-0	Reserved.	R	N/A
01Bh	Reserved	15-11	Reserved.	–	–
	LINE_0_352M[10:0]	10-0	Line number where SMPTE352M packet is inserted in field 1. Reference: Section 4.9.4.1 on page 70.	R/W	0
01Ch	Reserved	15-11	Reserved.	–	–
	LINE_1_352M[10:0]	10-0	Line number where SMPTE352M packet is inserted in field 2. Reference: Section 4.9.4.1 on page 70.	R/W	0
01Dh-01Eh	Reserved	15-0	Reserved.	R	N/A

Table 4-43: Video Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
01Fh	FORMAT_ERR	15	861 timing format error flag.	R	0
	Reserved	14-9	Reserved.	R	0
	LINE_OFFSET	8-6	Shifts the timing of the output 861 timing signal by up to +/-3 lines.	R/W	0
	PIXEL_OFFSET	5-3	Shifts the timing of the output 861 timing signal by up to +/-3 pixels.	R/W	0
	Reserved	2-1	Reserved.	R	0
	FSYNC_INVERT	0	Inverts the polarity of the detected field.	R/W	0
020h	ANC_INS_MODE	15	Selects the ANC data insertion operating mode. 0 Separate line mode 1 Concatenated mode Reference: Section 4.8.1 on page 64.	R/W	0
	PACKET_MISSED	14	Flag to indicate ancillary data packet could not be inserted in its entirety. Reference: Section 4.8 on page 63.	R	0
	RW_CONFLICT	13	Flag to indicate the same RAM address was read and written at the same time.	R	0
	Reserved	12-11	Reserved	R/W	0000b
	FIRST_LINE_NUMBER	10-0	Defines the line number for the first line in separate line mode or the single line for concatenated mode.	R/W	0
021h	ANC_TYPE	15	Selects the ANC data type as HANC or VANC. 0 HANC 1 VANC Reference: Section 4.8.2 & Section 4.8.3	R/W	0
	STREAM_TYPE	14	Selects the luma or chroma stream for ANC insertion. 0 Luma stream 1 Chroma stream This field is ignored in SD mode. Reference: Section 4.8.2 & Section 4.8.3	R/W	0
	Reserved	13-10	Reserved	R/W	0000b
	FIRST_LINE_NUMBER_OF_WORDS	9-0	Defines the total number of data words to insert on the first line in separate line mode or single line in the concatenated mode.	R/W	0
022h	Reserved	15-11	Reserved	R/W	00000b
	SECOND_LINE_NUMBER	10-0	Defines the line number for ANC data insertion for the 2nd line in separate line mode.	R/W	0

Table 4-43: Video Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
023h	ANC_TYPE	15	Selects the ANC data type as HANC or VANC. 0 HANC 1 VANC Reference: Section 4.8.2 & Section 4.8.3	R/W	0
	STREAM_TYPE	14	Selects the luma or chroma stream for ANC insertion. 0 Luma stream 1 Chroma stream This field is ignored in SD mode. Reference: Section 4.8.2 & Section 4.8.3	R/W	0
	Reserved	13-10	Reserved	R/W	0000b
	SECOND_LINE_NUMBER_OF_WORDS	9-0	Defines the total number of data words to insert on the 2nd line in separate line mode.	R/W	0
024h	Reserved	15-11	Reserved	R/W	00000b
	THIRD_LINE_NUMBER	10-0	Defines the line number for ANC data insertion for the 3rd line in separate line mode.	R/W	0
025h	ANC_TYPE	15	Selects the ANC data type as HANC or VANC. 0 HANC 1 VANC Reference: Section 4.8.2 & Section 4.8.3	R/W	0
	STREAM_TYPE	14	Selects the luma or chroma stream for ANC insertion. 0 Luma stream 1 Chroma stream This field is ignored in SD mode. Reference: Section 4.8.2 & Section 4.8.3	R/W	0
	Reserved	13-10	Reserved.	R/W	0000b
	THIRD_LINE_NUMBER_OF_WORDS	9-0	Defines the total number of data words to insert on the 3rd line in separate line mode.	R/W	0
026	Reserved	15-11	Reserved	R/W	00000b
	FOURTH_LINE_NUMBER	10-0	Defines the line number for ANC data insertion for the 4th line in separate line mode.	R/W	0
027h	ANC_TYPE	15	Selects the ANC data type as HANC or VANC. 0 HANC 1 VANC Reference: Section 4.8.2 & Section 4.8.3	R/W	0
	STREAM_TYPE	14	Selects the luma or chroma stream for ANC insertion. 0 Luma stream 1 Chroma stream This field is ignored in SD mode. Reference: Section 4.8.2 & Section 4.8.3	R/W	0
	Reserved	13-10	Reserved	R/W	0000b
	FOURTH_LINE_NUMBER_OF_WORDS	9-0	Defines the total number of data words to insert on the 4th line in separate line mode.	R/W	0

Table 4-43: Video Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
040h-07Fh	ANC_DATA_BANK1	15-0	First bank of user defined 8 bit words. 15-8: High order byte 7-0: Low order byte	W	0
080h-0BFh	ANC_DATA_BANK2	15-0	Second bank of user defined 8 bit words. 15-8: High order byte 7-0: Low order byte	W	0
0C0h-0FFh	ANC_DATA_BANK3	15-0	Third bank of user defined 8 bit words. 15-8: High order byte 7-0: Low order byte	W	0
100h-13Fh	ANC_DATA_BANK4	15-0	Fourth bank of user defined 8 bit words. 15-8: High order byte 7-0: Low order byte	W	0

4.13.3.2 SD Audio Registers

Table 4-44: SD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
400h	CTR_AGR	15	Selects replacement of audio control packets. 0: Do not replace audio control packets. 1: Replace all audio control packets. Reference: Section 4.7.11 on page 49.	R/W	0
	AGR	14	Selects Audio Group Replacement operating mode. Reference: Section 4.7.11 on page 49.	R/W	0
	ONE_AGR	13	Specifies the replacement of just the group 1 audio. 0: Do not replace only Group 1. 1: Replace only Group 1. Reference: Section 4.7.11 on page 49.	R/W	0
	CTRB_ON	12	Specifies the embedding of group 2 audio control packets. Reference: Section 4.7.9 on page 46.	R/W	1
	CLEAR_AUDIO	11	Clears all audio FIFO buffers and puts them in start-up state Reference: Section 4.7.21 on page 59.	R/W	0
	AFNB_AUTO	10	Group 2 audio frame number generation. Reference: Section 4.7.9 on page 46.	R/W	1
	CTRA_ON	9	Specifies the embedding of group 1 audio control packets. Reference: Section 4.7.9 on page 46.	R/W	1
	24BIT	8	Specifies the sample size for embedded audio. Reference: Section 4.7.10 on page 48.	R/W	0
	AFNA_AUTO	7	Enables group 1 audio frame number generation. Reference: Section 4.7.9 on page 46.	R/W	1
	AFN_OFS[2:0]	6-4	Offset to add to generated Audio Frame Number. Must be in the range of 0 to 4. The resulting audio frame number will wrap around so as to always be in the 1-5 range. Reference: Section 4.7.16 on page 52.	R/W	000b
	IDB[1:0]	3-2	Specifies the group 2 audio to embed. NOTE: Should IDA and IDB be set to the same value, they automatically revert to their default values. Reference: Section 4.7.10 on page 48.	R/W	01b (normal mode) 11b (cascade mode)
	IDA[1:0]	1-0	Specifies the group 1 audio to embed. NOTE: Should IDA and IDB be set to the same value, they automatically revert to their default values. Reference: Section 4.7.10 on page 48.	R/W	00b (normal mode) 10b (cascade mode)

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
401h	Reserved	15-11	Reserved	R	00000b
	AES_ERRD	10	Stereo Pair D audio input parity error when using AES format. Automatically cleared when read. Reference: Section 4.7.17.1 on page 54.	R	0
	AES_ERRC	9	Stereo Pair C audio input parity error when using AES format. Automatically cleared when read. Reference: Section 4.7.17.1 on page 54.	R	0
	AES_ERRB	8	Stereo Pair B audio input parity error when using AES format. Automatically cleared when read. Reference: Section 4.7.17.1 on page 54.	R	0
	AES_ERRA	7	Stereo Pair A audio input parity error when using AES format. Automatically cleared when read. Reference: Section 4.7.17.1 on page 54.	R	0
	Reserved	6-3	Reserved	R	0
	OFFSET_DISABLE	2	Set to disable staggering of group 2 audio sample distribution by one line. Reference: Section 4.7.20 on page 59.	R/W	0
	OS_SEL[1:0]	1-0	Specifies the audio FIFO buffer size. 00: 52 samples deep, 26 sample start-up count 01: 24 samples deep, 12 sample start-up count 10: 12 samples deep, 6 sample start-up count 11: Reserved. Reference: Section 4.7.21 on page 59.	R/W	00b

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
402h	Reserved	15	Reserved.	R	0
	AXPG4_DET	14	Set while Group 4 audio extended packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	AXPG3_DET	13	Set while Group 3 audio extended packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	AXPG2_DET	12	Set while Group 2 audio extended packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	AXPG1_DET	11	Set while Group 1 audio extended packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ACPG4_DET	10	Set while Group 4 audio control packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ACPG3_DET	9	Set while Group 3 audio control packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ACPG2_DET	8	Set while Group 2 audio control packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ACPG1_DET	7	Set while Group 1 audio control packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ADPG4_DET	6	Set while Group 4 audio data packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ADPG3_DET	5	Set while Group 3 audio data packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ADPG2_DET	4	Set while Group 2 audio data packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ADPG1_DET	3	Set while Group 1 audio data packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ACS_APPLY_WAITB	2	Set while the multiplexer is waiting for a status boundary in the Group B group before applying the ACSR[183:0] data to that group. Reference: Section 4.7.18 on page 56.	R	0
	ACS_APPLY / ACS_APPLY_WAITA	1	ACS_APPLY: Cause channel status data in ACSR[183:0] to be transferred to the channel status replacement mechanism. The transfer shall not occur until the next status boundary. ACS_APPLY_WAITA: Set while the multiplexer is waiting for a status boundary in Group 1 before applying the ACSR[183:0] data. Reference: Section 4.7.18 on page 56.	R/W	0

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
402h	ACS_REGEN	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. 0: Do not replace Channel Status 1: Replace Channel Status of all channels Reference: Section 4.7.18 on page 56.	R/W	0
403h	Reserved	15-10	Reserved.	R	N/A
	EN_CASCADE	9	Cascade.	R/W	
	Reserved	8-0	Reserved.	R	N/A
404h-407h	Reserved	15-0	Reserved.	R	N/A
408h	AMD[1:0]	15-14	Audio input format selector for Stereo Pair D input channels 7 and 8. Reference: Section 4.7.17 on page 53.	R/W	11b
	AMC[1:0]	13-12	Audio input format selector for Stereo Pair C input channels 5 and 6. Reference: Section 4.7.17 on page 53.	R/W	11b
	AMB[1:0]	11-10	Audio input format selector for Stereo Pair B input channels 3 and 4. Reference: Section 4.7.17 on page 53.	R/W	11b
	AMA[1:0]	9-8	Audio input format selector for Stereo Pair A input channels 1 and 2. Reference: Section 4.7.4 on page 40.	R/W	11b
	MUTE8	7	Audio input channel 8 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE7	6	Audio input channel 7 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE6	5	Audio input channel 6 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE5	4	Audio input channel 5 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE4	3	Audio input channel 4 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE3	2	Audio input channel 3 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE2	1	Audio input channel 2 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE1	0	Audio input channel 1 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
409h	Reserved	15, 12	Reserved	R/W	0
	GP1_WCLK_SRC[2:0]	14-13	Audio group 1 word clock source selector. Reference: Section 4.7.20 on page 59.	R/W	0
	GP1_CH4_SRC[2:0]	11-9	Audio group 1 channel 4 source selector. Reference: Section 4.7.19 on page 58.	R/W	011b
	GP1_CH3_SRC[2:0]	8-6	Audio group 1 channel 3 source selector. Reference: Section 4.7.19 on page 58.	R/W	010b
	GP1_CH2_SRC[2:0]	5-3	Audio group 1 channel 2 source selector. Reference: Section 4.7.19 on page 58.	R/W	001b
	GP1_CH1_SRC[2:0]	2-0	Audio group 1 channel 1 source selector. Reference: Section 4.7.19 on page 58.	R/W	000b
40Ah	Reserved	15, 12	Reserved	R/W	0
	GP2_WCLK_SRC[1:0]	14-13	Audio group 2 word clock source selector. Reference: Section 4.7.20 on page 59.	R/W	10
	GP2_CH4_SRC[1:0]	11-9	Audio group 2 channel 4 source selector. Reference: Section 4.7.19 on page 58.	R/W	111b
	GP2_CH3_SRC[2:0]	8-6	Audio group 2 channel 3 source selector. Reference: Section 4.7.19 on page 58.	R/W	110b
	GP2_CH2_SRC[2:0]	5-3	Audio group 2 channel 2 source selector. Reference: Section 4.7.19 on page 58.	R/W	101b
	GP2_CH1_SRC[2:0]	2-0	Audio group 2 channel 1 source selector. Reference: Section 4.7.19 on page 58.	R/W	100b

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
40Bh	EN_NOT_LOCKED	15	Asserts AUDIO_INT when LOCKED is not asserted. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_NO_VIDEO	14	Asserts AUDIO_INT when the video format is unknown. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_MUX_ERRB	13	Asserts AUDIO_INT when the MUX_ERRB flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_MUX_ERRA	12	Asserts AUDIO_INT when the MUX_ERRA flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_AES_ERRD	11	Asserts AUDIO_INT when the AES_ERRD flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_AES_ERRC	10	Asserts AUDIO_INT when the AES_ERRC flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_AES_ERRB	9	Asserts AUDIO_INT when the AES_ERRB flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_AES_ERRA	8	Asserts AUDIO_INT when the AES_ERRA flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ACPG4_DET	7	Asserts AUDIO_INT when the ACPG4_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ACPG3_DET	6	Asserts AUDIO_INT when the ACPG3_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ACPG2_DET	5	Asserts AUDIO_INT when the ACPG2_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ACPG1_DET	4	Asserts AUDIO_INT when the ACPG1_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ADPG4_DET	3	Asserts AUDIO_INT when the ADPG4_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ADPG3_DET	2	Asserts AUDIO_INT when the ADPG3_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ADPG2_DET	1	Asserts AUDIO_INT when the ADPG2_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ADPG1_DET	0	Asserts AUDIO_INT when the ADPG1_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
40Ch	MUX_ERRB	15	Set in Cascade mode when the incoming video contains packets with the same group number as Group 2. Reference: Section 4.7.3 on page 38.	R	0

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
40Ch	MUX_ERRA	14	Set in Cascade mode when the incoming video contains packets with the same group number as Group 1. Reference: Section 4.7.3 on page 38.	R	0
	XPOINT_ERROR	13	Set when the crosspoint switch is configured to put the same audio channel in both Group 1 and Group 2. Reference: Section 4.7.19 on page 58.	R	0
	MUTE_ALL	12	Mutes all input audio channels. Reference: Section 4.7.23 on page 63.	R/W	0
	LSB_FIRSTD	11	Causes the fourth stereo pair serial input formats to use LSB first. Reference: Section 4.7.17 on page 53.	R/W	0
	LSB_FIRSTC	10	Causes the third stereo pair serial input formats to use LSB first. Reference: Section 4.7.17 on page 53.	R/W	0
	LSB_FIRSTB	9	Causes the second stereo pair serial input formats to use LSB first. Reference: Section 4.7.17 on page 53.	R/W	0
	LSB_FIRSTA	8	Causes the first stereo pair serial input formats to use LSB first. Reference: Section 4.7.17 on page 53.	R/W	0
	ACT8	7	Specifies embedding of audio group 2 channel 4. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT7	6	Specifies embedding of audio group 2 channel 3. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT6	5	Specifies embedding of audio group 2 channel 2. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT5	4	Specifies embedding of audio group 2 channel 1. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT4	3	Specifies embedding of audio group 1 channel 4. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT3	2	Specifies embedding of audio group 1 channel 3. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT2	1	Specifies embedding of audio group 1 channel 2. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT1	0	Specifies embedding of audio group 1 channel 1. Reference: Section 4.7.12 on page 51.	R/W	1
40Dh-41Fh	Reserved	15-0	Reserved.	W	N/A
420h-436h	Reserved	15-8	Reserved	W	N/A

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
420h	ACSR[7:0]	7-0	Audio status block byte 0. Reference: Section 4.7.18 on page 56.	W	85h
421h	ACSR[15:8]	7-0	Audio status block byte 1. Reference: Section 4.7.18 on page 56.	W	08h
422h	ACSR[23:16]	7-0	Audio status block byte 2. Reference: Section 4.7.18 on page 56.	W	2Ch
423h-436h	ACSR[183:24]	7-0	Remaining audio status. Reference: Section 4.7.18 on page 56.	W	0
440h	Reserved	15-9	Reserved	W	0000000b
	DEL1A[7:0]	8-1	Audio group 1 delay data for channel 1. Reference: Section 4.7.9 on page 46.	W	0
	EBIT1A	0	Audio group 1 delay data valid flag for channel 1. Reference: Section 4.7.9 on page 46.	W	0
441h	Reserved	15-9	Reserved	W	0000000b
	DEL1A[16:8]	8-0	Audio group 1 delay data for channel 1. Reference: Section 4.7.9 on page 46.	W	0
442h	Reserved	15-9	Reserved	W	0000000b
	DEL1A[25:17]	8-0	Audio group 1 delay data for channel 1. Reference: Section 4.7.9 on page 46.	W	0
443h	Reserved	15-9	Reserved	W	0000000b
	DEL2A[7:0]	8-1	Audio group 1 delay data for channel 2. Reference: Section 4.7.9 on page 46.	W	0
	EBIT2A	0	Audio group 1 delay data valid flag for channel 2. Reference: Section 4.7.9 on page 46.	W	0
444h	Reserved	15-9	Reserved	W	0000000b
	DEL2A[16:8]	8-0	Audio group 1 delay data for channel 2. Reference: Section 4.7.9 on page 46.	W	0
445h	Reserved	15-9	Reserved	W	0000000b
	DEL2A[25:17]	8-0	Audio group 1 delay data for channel 2. Reference: Section 4.7.9 on page 46.	W	0
446h	Reserved	15-9	Reserved	W	0000000b
	DEL3A[7:0]	8-1	Audio group 1 delay data for channel 3. Reference: Section 4.7.9 on page 46.	W	0
	EBIT1A	0	Audio group 1 delay data valid flag for channel3. Reference: Section 4.7.9 on page 46.	W	0

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
447h	Reserved	15-9	Reserved	W	0000000b
	DEL3A[16:8]	8-0	Audio group 1 delay data for channel 3. Reference: Section 4.7.9 on page 46.	W	0
448h	Reserved	15-9	Reserved	W	0000000b
	DEL3A[25:17]	8-0	Audio group 1 delay data for channel 3. Reference: Section 4.7.9 on page 46.	W	0
449h	Reserved	15-9	Reserved	W	0000000b
	DEL4A[7:0]	8-1	Audio group 1 delay data for channel 4. Reference: Section 4.7.9 on page 46.	W	0
	EBIT4A	0	Audio group 1 delay data valid flag for channel 4. Reference: Section 4.7.9 on page 46.	W	0
44Ah	Reserved	15-9	Reserved	W	0000000b
	DEL4A[16:8]	8-0	Audio group 1 delay data for channel 4. Reference: Section 4.7.9 on page 46.	W	0
44Bh	Reserved	15-9	Reserved	W	0000000b
	DEL4A[25:17]	8-0	Audio group 1 delay data for channel 4. Reference: Section 4.7.9 on page 46.	W	0
450h	Reserved	15-9	Reserved	W	0000000b
	DEL1B[7:0]	8-1	Audio group 2 delay data for channel 1. Reference: Section 4.7.9 on page 46.	W	0
	EBIT1B	0	Audio group 2 delay data valid flag for channel 1. Reference: Section 4.7.9 on page 46.	W	0
451h	Reserved	15-9	Reserved	W	0000000b
	DEL1B[16:8]	8-0	Audio group 2 delay data for channel 1. Reference: Section 4.7.9 on page 46.	W	0
452h	Reserved	15-9	Reserved	W	0000000b
	DEL1B[25:17]	8-0	Audio group 2 delay data for channel 1. Reference: Section 4.7.9 on page 46.	W	0
453h	Reserved	15-9	Reserved	W	0000000b
	DEL2B[7:0]	8-1	Audio group 2 delay data for channel 2. Reference: Section 4.7.9 on page 46.	W	0
	EBIT2B	0	Audio group 2 delay data valid flag for channel 2. Reference: Section 4.7.9 on page 46.	W	0
454h	Reserved	15-9	Reserved	W	0000000b
	DEL2B[16:8]	8-0	Audio group 2 delay data for channel 2. Reference: Section 4.7.9 on page 46.	W	0

Table 4-44: SD Audio Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
455h	Reserved	15-9	Reserved	W	0000000b
	DEL2B[25:17]	8-0	Audio group 2 delay data for channel 2. Reference: Section 4.7.9 on page 46.	W	0
456h	Reserved	15-9	Reserved	W	0000000b
	DEL3B[7:0]	8-1	Audio group 2 delay data for channel 3. Reference: Section 4.7.9 on page 46.	W	0
	EBIT1B	0	Audio group 2 delay data valid flag for channel3. Reference: Section 4.7.9 on page 46.	W	0
457h	Reserved	15-9	Reserved	W	0000000b
	DEL3B[16:8]	8-0	Audio group 2 delay data for channel 3. Reference: Section 4.7.9 on page 46.	W	0
458h	Reserved	15-9	Reserved	W	0000000b
	DEL3B[25:17]	8-0	Audio group 2 delay data for channel 3. Reference: Section 4.7.9 on page 46.	W	0
459h	Reserved	15-9	Reserved	W	0000000b
	DEL4B[7:0]	8-1	Audio group 2 delay data for channel 4. Reference: Section 4.7.9 on page 46.	W	0
	EBIT4B	0	Audio group 2 delay data valid flag for channel 4. Reference: Section 4.7.9 on page 46.	W	0
45Ah	Reserved	15-9	Reserved	W	0000000b
	DEL4B[16:8]	8-0	Audio group 2 delay data for channel 4. Reference: Section 4.7.9 on page 46.	W	0
45Bh	Reserved	15-9	Reserved	W	0000000b
	DEL4B[25:17]	8-0	Audio group 2 delay data for channel 4. Reference: Section 4.7.9 on page 46.	W	0

4.13.3.3 HD Audio Registers

Table 4-45: HD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
800h	CTR_AGR	15	Selects replacement of audio control packets. 0: Do not replace audio control packets. 1: Replace all audio control packets. Reference: Section 4.7.11 on page 49.	R/W	0
	AGR	14	Selects Audio Group Replacement operating mode. Reference: Section 4.7.11 on page 49.	R/W	0
	ONE_AGR	13	Specifies the replacement of just the group 1 audio. 0: Do not replace only Group 1. 1: Replace only Group 1. Reference: Section 4.7.11 on page 49.	R/W	0
	CTRB_ON	12	Specifies the embedding of group B audio control packets. Reference: Section 4.7.9 on page 46.	R/W	1
	ASXB	11	Group 2 asynchronous mode. Reference: Section 4.7.9 on page 46.	R/W	0
	AFNB_AUTO	10	Group 2 audio frame number generation. Reference: Section 4.7.9 on page 46.	R/W	1
	CTRA_ON	9	Specifies the embedding of group 1 audio control packets. Reference: Section 4.7.9 on page 46.	R/W	1
	ASXA	8	Group 1 asynchronous mode. Reference: Section 4.7.9 on page 46.	R/W	0
	AFNA_AUTO	7	Enables group 1 audio frame number generation. Reference: Section 4.7.9 on page 46.	R/W	1
	AFN_OFS[2:0]	6-4	Offset to add to generated Audio Frame Number. Must be in the range of 0 to 4. The resulting audio frame number will wrap around so as to always be in the 1-5 range. Reference: Section 4.7.16 on page 52.	R/W	000b
	IDB[1:0]	3-2	Specifies the group 2 audio to embed. NOTE: Should IDA and IDB be set to the same value, they automatically revert to their default values. Reference: Section 4.7.10 on page 48.	R/W	01b (normal mode) 11b (cascade mode)

Table 4-45: HD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
800h	IDA[1:0]	1-0	Specifies the group 1 audio to embed. NOTE: Should IDA and IDB be set to the same value, they automatically revert to their default values. Reference: Section 4.7.10 on page 48.	R/W	00b (normal mode) 10b (cascade mode)
801h	Reserved	15-0	Reserved.	W	N/A
802h	Reserved	15	Reserved	R	0
	AES_ERRD	14	Stereo Pair D audio input parity error when using AES format. Automatically cleared when read. Reference: Section 4.7.17.1 on page 54.	R	0
	AES_ERRC	13	Stereo Pair C audio input parity error when using AES format. Automatically cleared when read. Reference: Section 4.7.17.1 on page 54.	R	0
	AES_ERRB	12	Stereo Pair B audio input parity error when using AES format. Automatically cleared when read. Reference: Section 4.7.17.1 on page 54.	R	0
	AES_ERRA	11	Stereo Pair A audio input parity error when using AES format. Automatically cleared when read. Reference: Section 4.7.17.1 on page 54.	R	0
	ACPG4_DET	10	Set while Group 4 audio control packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ACPG3_DET	9	Set while Group 3 audio control packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ACPG2_DET	8	Set while Group 2 audio control packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ACPG1_DET	7	Set while Group 1 audio control packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ADPG4_DET	6	Set while Group 4 audio data packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ADPG3_DET	5	Set while Group 3 audio data packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ADPG2_DET	4	Set while Group 2 audio data packets are detected. Reference: Section 4.7.2 on page 38.	R	0
	ADPG1_DET	3	Set while Group 1 audio data packets are detected. Reference: Section 4.7.2 on page 38.	R	0

Table 4-45: HD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
802h	ACS_APPLY_WAITB	2	Set while the GS1582 is waiting for a status boundary in the Group B group before applying the ACSR[183:0] data to that group. Reference: Section 4.7.18 on page 56.	R	0
	ACS_APPLY / ACS_APPLY_WAITA	1	Set while the GS1582 is waiting for a status boundary in Group A before applying the ACSR[183:0] data. Reference: Section 4.7.18 on page 56.	R/W	0
	ACS_REGEN	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. 0: Do not replace Channel Status 1: Replace Channel Status of all channels Reference: Section 4.7.18 on page 56.	R/W	0
803h	Reserved	15-10	Reserved.	R	N/A
	EN_CASCADE	9	Cascade.	R/W	
	Reserved	8-0	Reserved.	R	N/A
804h-807h	Reserved	15-0	Reserved.	R	N/A
808h	AMD[1:0]	15-14	Audio input format selector for Stereo Pair D channels 7 and 8. Reference: Section 4.7.17 on page 53.	R/W	11b
	AMC[1:0]	13-12	Audio input format selector for Stereo Pair C channels 5 and 6. Reference: Section 4.7.17 on page 53.	R/W	11b
	AMB[1:0]	11-10	Audio input format selector for Stereo Pair B channels 3 and 4. Reference: Section 4.7.17 on page 53.	R/W	11b
	AMA[1:0]	9-8	Audio input format selector for Stereo Pair A channels 1 and 2. Reference: Section 4.7.17 on page 53.	R/W	11b
	MUTE8	7	Audio input channel 8 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE7	6	Audio input channel 7 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE6	5	Audio input channel 6 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE5	4	Audio input channel 5 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0

Table 4-45: HD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
808h	MUTE4	3	Audio input channel 4 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE3	2	Audio input channel 3 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE2	1	Audio input channel 2 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
	MUTE1	0	Audio input channel 1 mute enable. Reference: Section 4.7.23 on page 63.	R/W	0
809h	Reserved	15, 12	Reserved	R/W	0
	GP1_WCLK_SRC[1:0]	14-13	Audio group 1 word clock source selector. Reference: Section 4.7.20 on page 59.	R/W	0
	GP1_CH4_SRC[2:0]	11-9	Audio group 1 channel 4 source selector. Reference: Section 4.7.19 on page 58.	R/W	011b
	GP1_CH3_SRC[2:0]	8-6	Audio group 1 channel 3 source selector. Reference: Section 4.7.19 on page 58.	R/W	010b
	GP1_CH2_SRC[2:0]	5-3	Audio group 1 channel 2 source selector. Reference: Section 4.7.19 on page 58.	R/W	001b
	GP1_CH1_SRC[2:0]	2-0	Audio group 1 channel 1 source selector. Reference: Section 4.7.19 on page 58.	R/W	000b
80Ah	Reserved	15, 12	Reserved	R/W	0
	GP2_WCLK_SRC[1:0]	14-13	Audio group 2 word clock source selector. Reference: Section 4.7.20 on page 59.	R/W	10
	GP2_CH4_SRC[2:0]	11-9	Audio group 2 channel 4 source selector. Reference: Section 4.7.19 on page 58.	R/W	111b
	GP2_CH3_SRC[2:0]	8-6	Audio group 2 channel 3 source selector. Reference: Section 4.7.19 on page 58.	R/W	110b
	GP2_CH2_SRC[2:0]	5-3	Audio group 2 channel 2 source selector. Reference: Section 4.7.19 on page 58.	R/W	101b
	GP2_CH1_SRC[2:0]	2-0	Audio group 2 channel 1 source selector. Reference: Section 4.7.19 on page 58.	R/W	100b

Table 4-45: HD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
80Bh	EN_NOT_LOCKED	15	Asserts AUDIO_INT when LOCKED is not asserted. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_NO_VIDEO	14	Asserts AUDIO_INT when the video format is unknown. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_MUX_ERRB	13	Asserts AUDIO_INT when the MUX_ERRB flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_MUX_ERRA	12	Asserts AUDIO_INT when the MUX_ERRA flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_AES_ERRD	11	Asserts AUDIO_INT when the AES_ERRD flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_AES_ERRC	10	Asserts AUDIO_INT when the AES_ERRC flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_AES_ERRB	9	Asserts AUDIO_INT when the AES_ERRB flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_AES_ERRA	8	Asserts AUDIO_INT when the AES_ERRA flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ACPG4_DET	7	Asserts AUDIO_INT when the ACPG4_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ACPG3_DET	6	Asserts AUDIO_INT when the ACPG3_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ACPG2_DET	5	Asserts AUDIO_INT when the ACPG2_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ACPG1_DET	4	Asserts AUDIO_INT when the ACPG1_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ADPG4_DET	3	Asserts AUDIO_INT when the ADPG4_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ADPG3_DET	2	Asserts AUDIO_INT when the ADPG3_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ADPG2_DET	1	Asserts AUDIO_INT when the ADPG2_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0
	EN_ADPG1_DET	0	Asserts AUDIO_INT when the ADPG1_DET flag is set. Reference: Section 4.7.14 on page 51.	R/W	0

Table 4-45: HD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
80Ch	MUX_ERRB	15	Set in Cascade mode when the incoming video contains packets with the same group number as Group 2. Reference: Section 4.7.3 on page 38.	R	0
	MUX_ERRA	14	Set in Cascade mode when the incoming video contains packets with the same group number as Group 1. Reference: Section 4.7.3 on page 38.	R	0
	XPOINT_ERROR	13	Set when the crosspoint switch is configured to put the same audio channel in both Group 1 and Group 2. Reference: Section 4.7.19 on page 58.	R	0
	MUTE_ALL	12	Mutes all input audio channels. Reference: Section 4.7.23 on page 63.	R/W	0
	LSB_FIRSTD	11	Causes the fourth stereo pair serial input formats to use LSB first. Reference: Section 4.7.17 on page 53.	R/W	0
	LSB_FIRSTC	10	Causes the third stereo pair serial input formats to use LSB first. Reference: Section 4.7.17 on page 53.	R/W	0
	LSB_FIRSTB	9	Causes the second stereo pair serial input formats to use LSB first. Reference: Section 4.7.17 on page 53.	R/W	0
	LSB_FIRSTA	8	Causes the first stereo pair serial input formats to use LSB first. Reference: Section 4.7.17 on page 53.	R/W	0
	ACT8	7	Specifies embedding of audio group 2 channel 4. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT7	6	Specifies embedding of audio group 2 channel 3. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT6	5	Specifies embedding of audio group 2 channel 2. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT5	4	Specifies embedding of audio group 2 channel 1. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT4	3	Specifies embedding of audio group 1 channel 4. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT3	2	Specifies embedding of audio group 1 channel 3. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT2	1	Specifies embedding of audio group 1 channel 2. Reference: Section 4.7.12 on page 51.	R/W	1
	ACT1	0	Specifies embedding of audio group 1 channel 1. Reference: Section 4.7.12 on page 51.	R/W	1

Table 4-45: HD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
80Dh	Reserved	15-0	Reserved.	W	N/A
820h-836h	Reserved	15-8	Reserved.	W	N/A
820h	ACSR[7:0]	7-0	Audio status block byte 0. Reference: Section 4.7.18 on page 56.	W	85h
821h	ACSR[15:8]	7-0	Audio status block byte 1. Reference: Section 4.7.18 on page 56.	W	08h
822h	ACSR[23:16]	7-0	Audio status block byte 2. Reference: Section 4.7.18 on page 56.	W	2Ch
823h-836h	ACSR[183:24]	7-0	Remaining audio status. Reference: Section 4.7.18 on page 56.	W	0
840h	Reserved	15-9	Reserved	W	0000000b
	DEL1_2A[7:0]	8-1	Audio group 1 delay data for channels 1 and 2. Reference: Section 4.7.9 on page 46.	W	0
	EBIT1_2A	0	Audio group 1 delay data valid flag for channels 1 and 2. Reference: Section 4.7.9 on page 46.	W	0
841h	Reserved	15-9	Reserved	W	0000000b
	DEL1_2A[16:8]	8-0	Audio group 1 delay data for channels 1 and 2. Reference: Section 4.7.9 on page 46.	W	0
842h	Reserved	15-9	Reserved	W	0000000b
	DEL1_2A[25:17]	8-0	Audio group 1 delay data for channels 1 and 2. Reference: Section 4.7.9 on page 46.	W	0
843h	Reserved	15-9	Reserved	W	0000000b
	DEL3_4A[7:0]	8-1	Audio group 1 delay data for channels 3 and 4. Reference: Section 4.7.9 on page 46.	W	0
	EBIT3_4A	0	Audio group 1 delay data valid flag for channels 3 and 4. Reference: Section 4.7.9 on page 46.	W	0
844h	Reserved	15-9	Reserved	W	0000000b
	DEL3_4A[16:8]	8-0	Audio group A delay data for channels 3 and 4. Reference: Section 4.7.9 on page 46.	W	0
845h	Reserved	15-9	Reserved	W	0000000b
	DEL3_4A[25:17]	8-0	Audio group 1 delay data for channels 3 and 4. Reference: Section 4.7.9 on page 46.	W	0

Table 4-45: HD Audio Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
846h	Reserved	15-9	Reserved	W	0000000b
	DEL1_2B[7:0]	8-1	Audio group 2 delay data for channels 1 and 2. Reference: Section 4.7.9 on page 46.	W	0
	EBIT1_2B	0	Audio group 2 delay data valid flag for channels 1 and 2. Reference: Section 4.7.9 on page 46.	W	0
847h	Reserved	15-9	Reserved	W	0000000b
	DEL1_2B[16:8]	8-0	Audio group 2 delay data for channels 1 and 2. Reference: Section 4.7.9 on page 46.	W	0
848h	Reserved	15-9	Reserved	W	0000000b
	DEL1_2B[25:17]	8-0	Audio group 2 delay data for channels 1 and 2. Reference: Section 4.7.9 on page 46.	W	0
849h	Reserved	15-9	Reserved	W	0000000b
	DEL3_4B[7:0]	8-1	Audio group 2 delay data for channels 3 and 4. Reference: Section 4.7.9 on page 46.	W	0
	EBIT3_4B	0	Audio group 2 delay data valid flag for channels 3 and 4. Reference: Section 4.7.9 on page 46.	W	0
84Ah	Reserved	15-9	Reserved	W	0000000b
	DEL3_4B[16:8]	8-0	Audio group 2 delay data for channels 3 and 4. Reference: Section 4.7.9 on page 46.	W	0
84Bh	Reserved	15-9	Reserved	W	0000000b
	DEL3_4B[25:17]	8-0	Audio group 2 delay data for channels 3 and 4. Reference: Section 4.7.9 on page 46.	W	0

4.14 JTAG Test Operation

When the JTAG/$\overline{\text{HOST}}$ input pin of the GS1582 is set HIGH, the host interface port will be configured for JTAG test operation. In this mode, pins J9, J10, K9, and K10 become TDO, TCK, TMS, and TDI. In addition, the $\overline{\text{RESET_TRST}}$ pin will operate as the test reset pin.

Boundary scan testing using the JTAG interface will be enabled in this mode.

There are two ways in which JTAG can be used on the GS1582:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly; *or*
2. Under control of a host processor for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG/$\overline{\text{HOST}}$ input signal. This is shown in Figure 4-31.

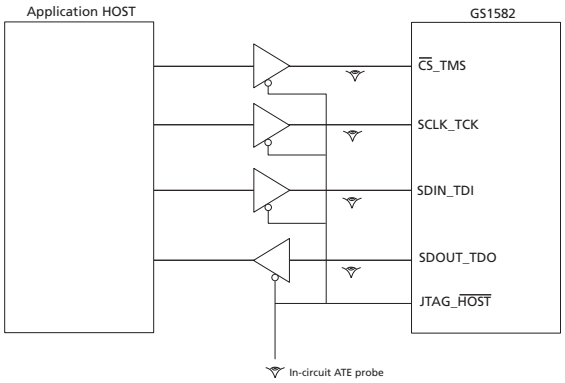


Figure 4-31: In-Circuit JTAG

Alternatively, if the test capabilities are to be used in the system, the host processor may still control the JTAG/$\overline{\text{HOST}}$ input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 4-32.

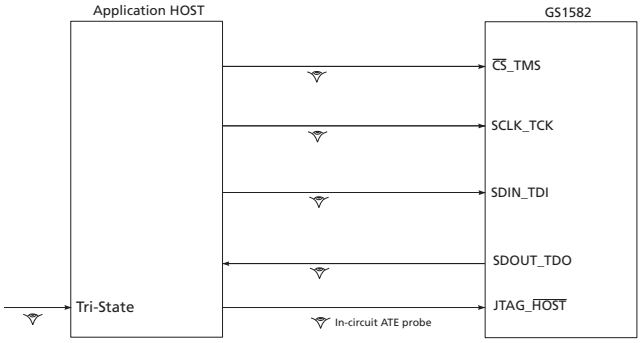


Figure 4-32: System JTAG

NOTE: Scan coverage is limited to digital pins only. There is no scan coverage for analog pins VCO, SDO/$\overline{\text{SDO}}$, RSET, LF, and CP_RES.

NOTE: The SD/$\overline{\text{HD}}$ pin must be held LOW during scan and therefore has no scan coverage.

Please contact your Gennum representative to obtain the BSDL model for the GS1582.

4.15 Device Reset

In order to initialize all internal operating conditions to their default states, hold the $\overline{\text{RESET_TRST}}$ signal LOW for a minimum of t_{reset} = 10ms after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs will be driven to a high-impedance state.

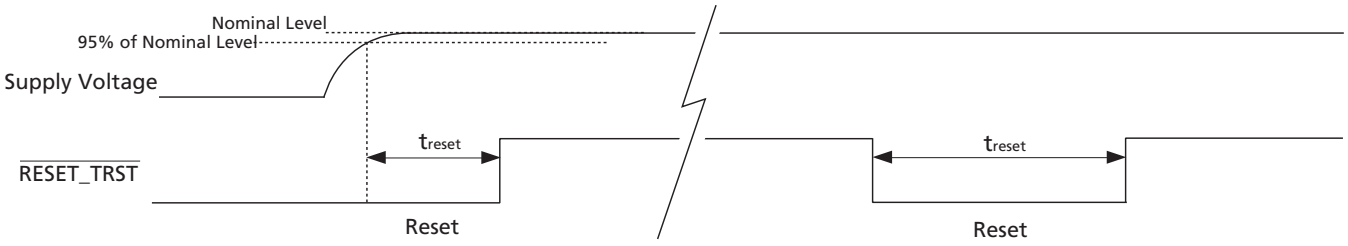
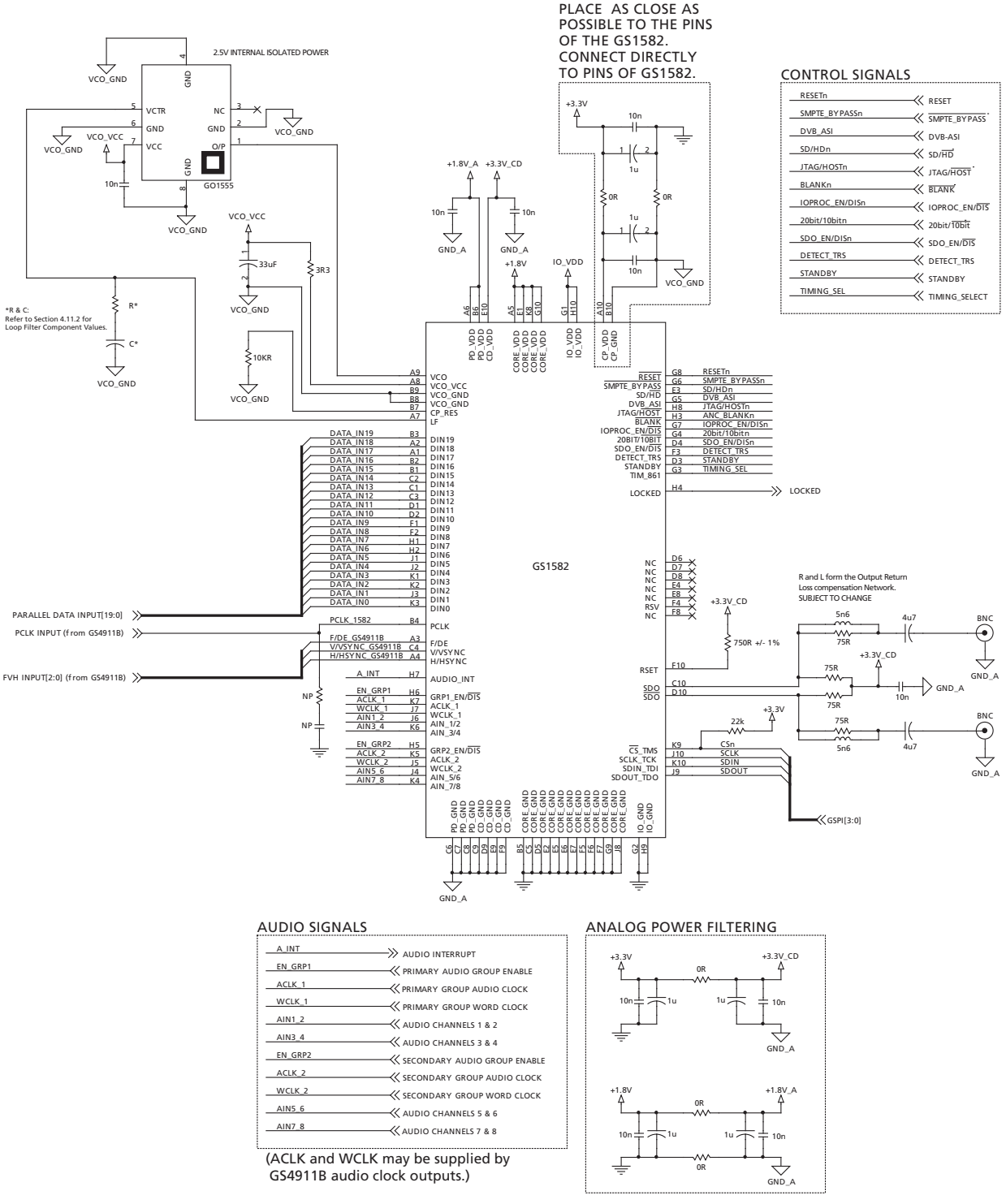


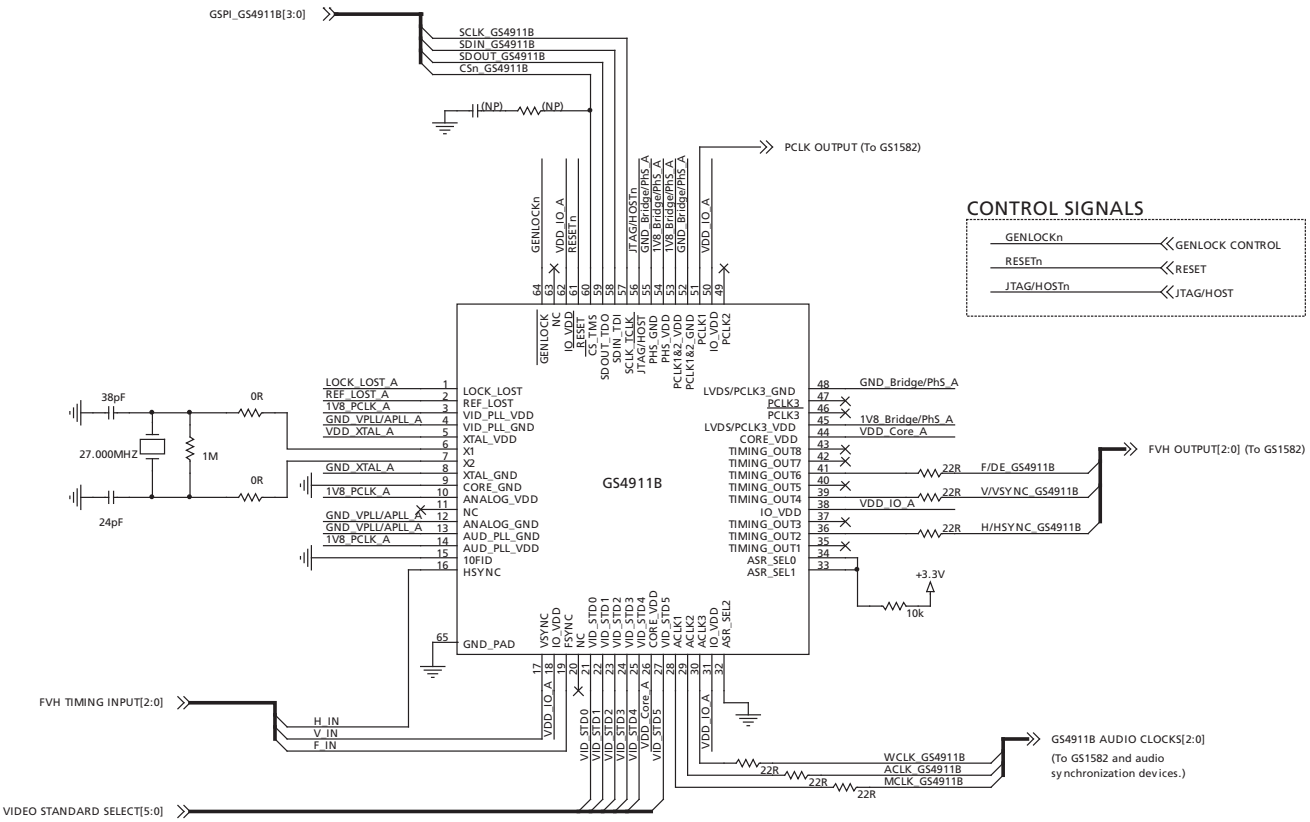
Figure 4-33: Reset Pulse

5. Application Reference Design

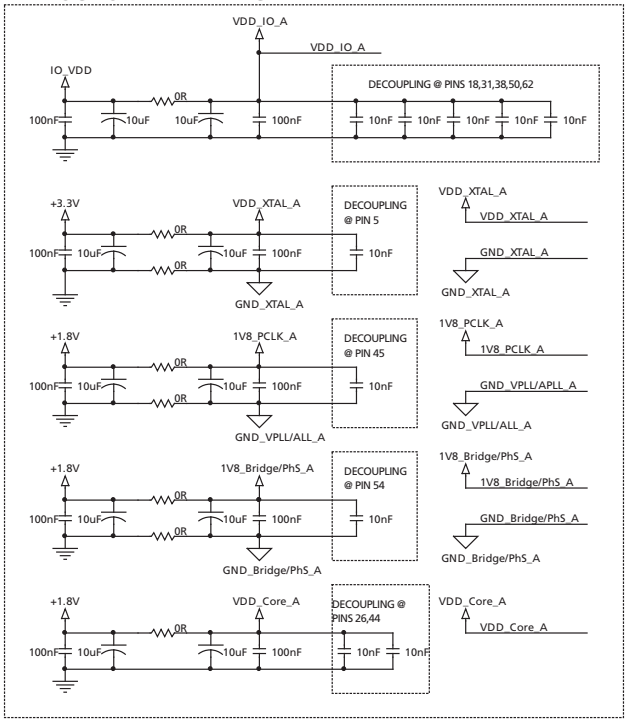
5.1 Typical Application Circuit (Part A)



5.2 Typical Application Circuit (Part B)



ANALOG POWER FILTERING

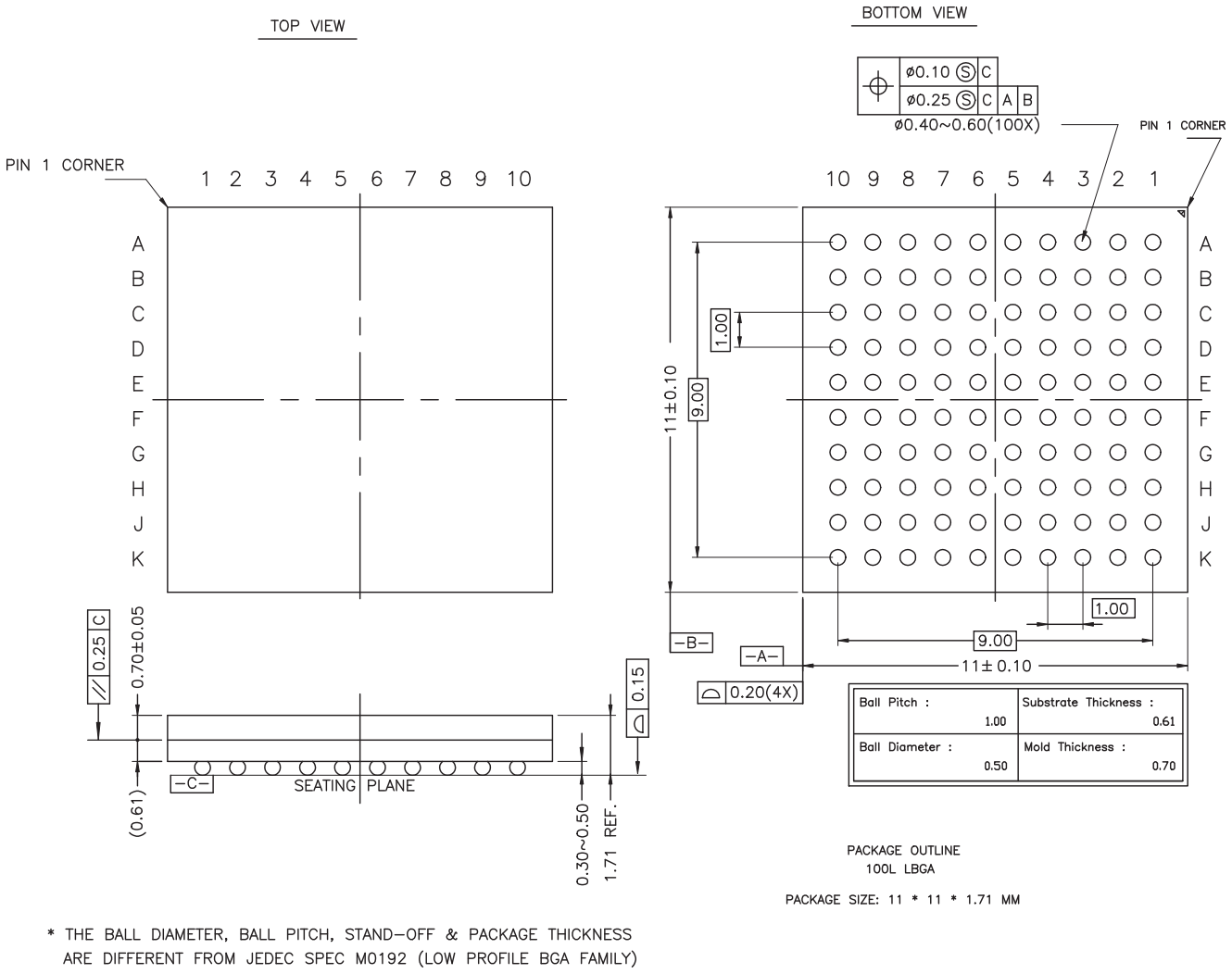


6. References & Relevant Standards

SMPTE 125M	Component video signal 4:2:2 – bit parallel interface
SMPTE 259M	10-bit 4:2:2 Component and 4fsc Composite Digital Signals - Serial Digital Interface
SMPTE 260M	1125 / 60 high definition production system – digital representation and bit parallel interface
SMPTE 267M	Bit parallel digital interface – component video signal 4:2:2 16 x 9 aspect ratio
SMPTE 272M	Formatting AES/EBU Audio and Auxiliary Data into Digital Video Ancillary Space
SMPTE 274M	1920 x 1080 scanning analog and parallel digital interfaces for multiple picture rates
SMPTE 291M	Ancillary Data Packet and Space Formatting
SMPTE 292M	Bit-Serial Digital Interface for High-Definition Television Systems
SMPTE 293M	720 x 483 active line at 59.94 Hz progressive scan production – digital representation
SMPTE 296M	1280 x 720 scanning, analog and digital representation and analog interface
SMPTE 299M	24-Bit Digital Audio Format for HDTV Bit-Serial Interface
SMPTE 352M	Video Payload Identification for Digital Television Interfaces
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television
SMPTE RP168	Definition of Vertical Interval Switching Point for Synchronous Video Switching

7. Package & Ordering Information

7.1 Package Dimensions



* THE BALL DIAMETER, BALL PITCH, STAND–OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC M0192 (LOW PROFILE BGA FAMILY)

7.2 Packaging Data

Table 7-1: Packaging Data

Parameter	Value
Package Type	11mm x 11mm 100-ball LBGA
Package Drawing Reference	JEDEC M0192 (with exceptions noted in Package Dimensions on page 112).
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	15.4°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	37.1°C/W
Junction to Board Thermal Resistance, θ_{j-b}	26.4°C/W
Psi, ψ	0.4°C/W
Pb-free and RoHS Compliant	Yes

7.3 Marking Diagram



7.4 Solder Reflow Profile

The GS1582 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 7-1.

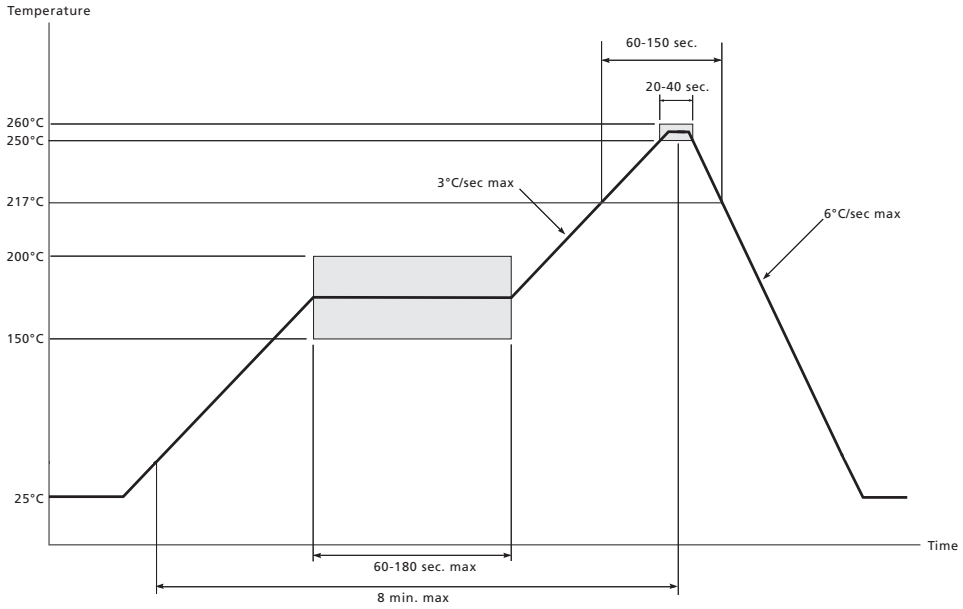


Figure 7-1: Pb-free Solder Reflow Profile

7.5 Ordering Information

Part Number	Package	Pb-free	Temperature Range
GS1582-IBE3	100-ball BGA	Yes	-20°C to 85°C

DOCUMENT IDENTIFICATION
DATA SHEET
The product is in production. Gennum reserves the right to make changes to the product at any time without notice to improve reliability, function or design, in order to provide the best product possible.

CAUTION
ELECTROSTATIC SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE EXCEPT AT A STATIC-FREE WORKSTATION



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