Integrated Device Technology, Inc.

CMOS SyncBiFIFO™ 256 x 18 x 2 and 512 x 18 x 2

IDT72605
IDT72615

FEATURES:

- Two independent FIFO memories for fully bidirectional data transfers
- 256 x 18 x 2 organization (IDT 72605)
- 512 x 18 x 2 organization (IDT 72615)
- Synchronous interface for fast (20ns) read and write cycle times
- Each data port has an independent clock and read/write control
- Output enable is provided on each port as a three-state control of the data bus
- Built-in bypass path for direct data transfer between two ports
- Two fixed flags, Empty and Full, for both the A-to-B and the B-to-A FIFO
- Programmable flag offset can be set to any depth in the FIFO
- The synchronous BiFIFO is packaged in a 64-pin TQFP (Thin Quad Flatpack), 68-pin PGA and 68-pin PLCC
- Industrial temperature range (-40oC to +85oC) is available, tested to military electrical specifications

DESCRIPTION:

The IDT72605 and IDT72615 are very high-speed, low-power bidirectional First-In, First-Out (FIFO) memories, with synchronous interface for fast read and write cycle times. The SyncBiFIFO™ is a data buffer that can store or retrieve information from two sources simultaneously. Two Dual-Port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction.

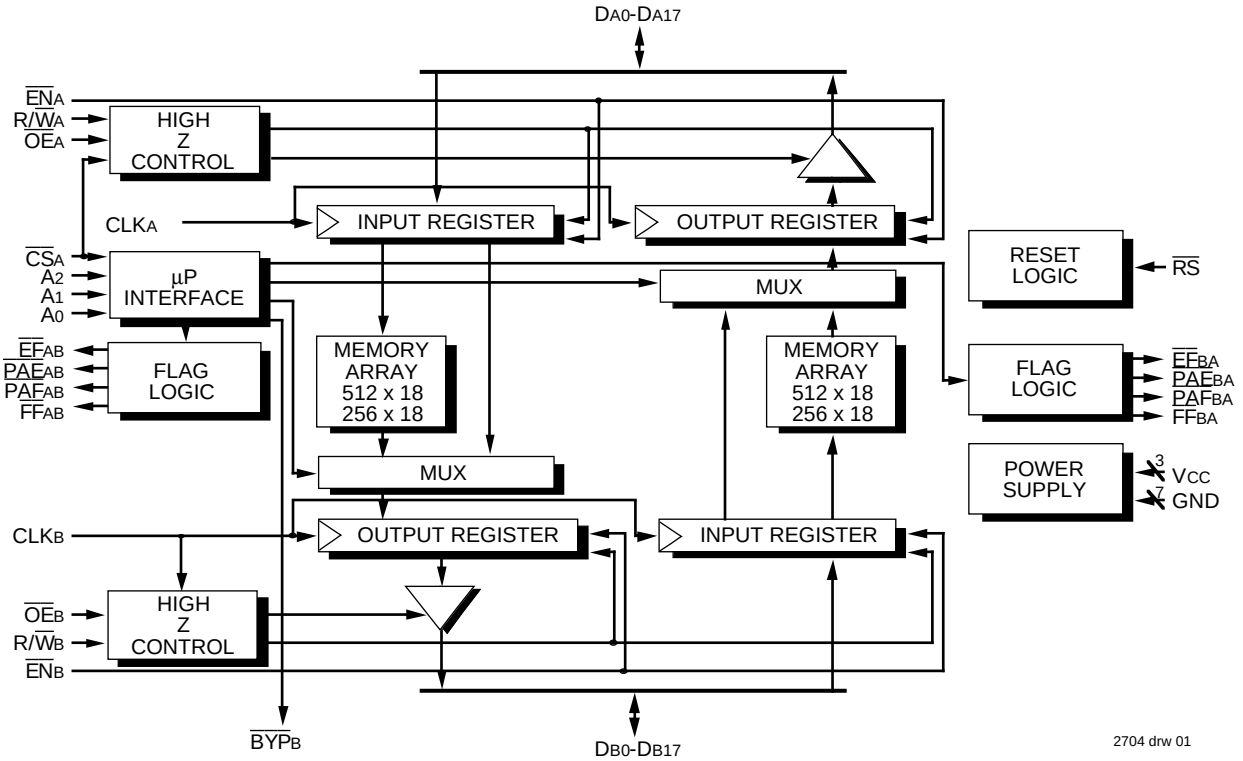
The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Each Port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high-impedance state.

Bypass control allows data to be directly transferred from input to output register in either direction.

The SyncBiFIFO has eight flags. The flag pins are full, empty, almost-full, and almost-empty for both FIFO memories. The offset depths of the almost-full and almost-empty flags can be programmed to any location.

The SyncBiFIFO is fabricated using IDT's high-speed, submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM

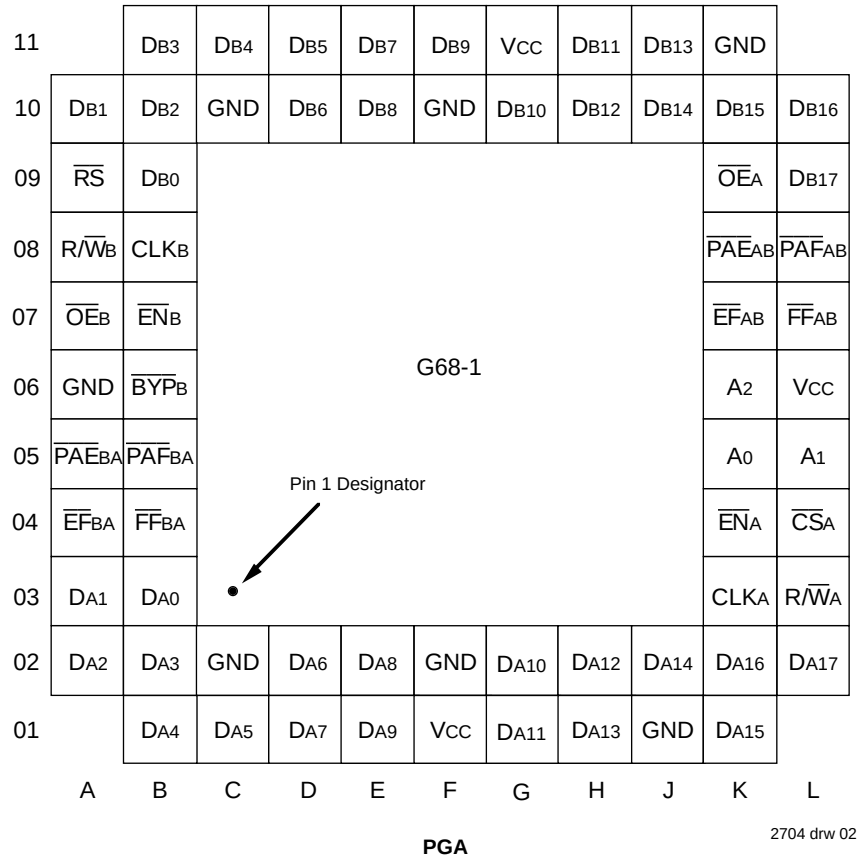


SyncBiFIFO is a trademark and the IDT logo is a registered trademark of Integrated Device Technology, Inc.

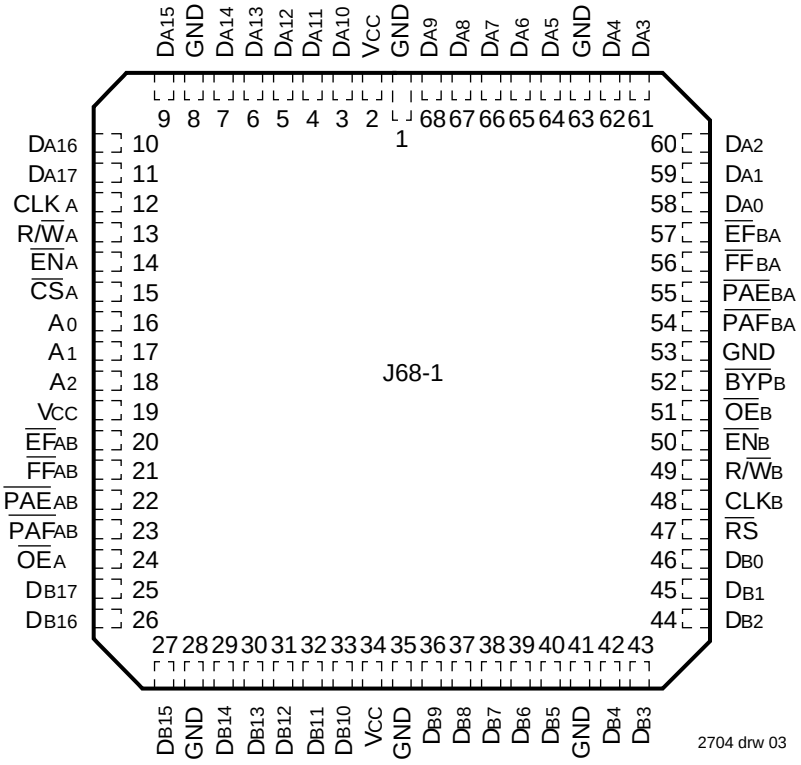
COMMERCIAL TEMPERATURE RANGES **DECEMBER 1996**

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PIN CONFIGURATIONS

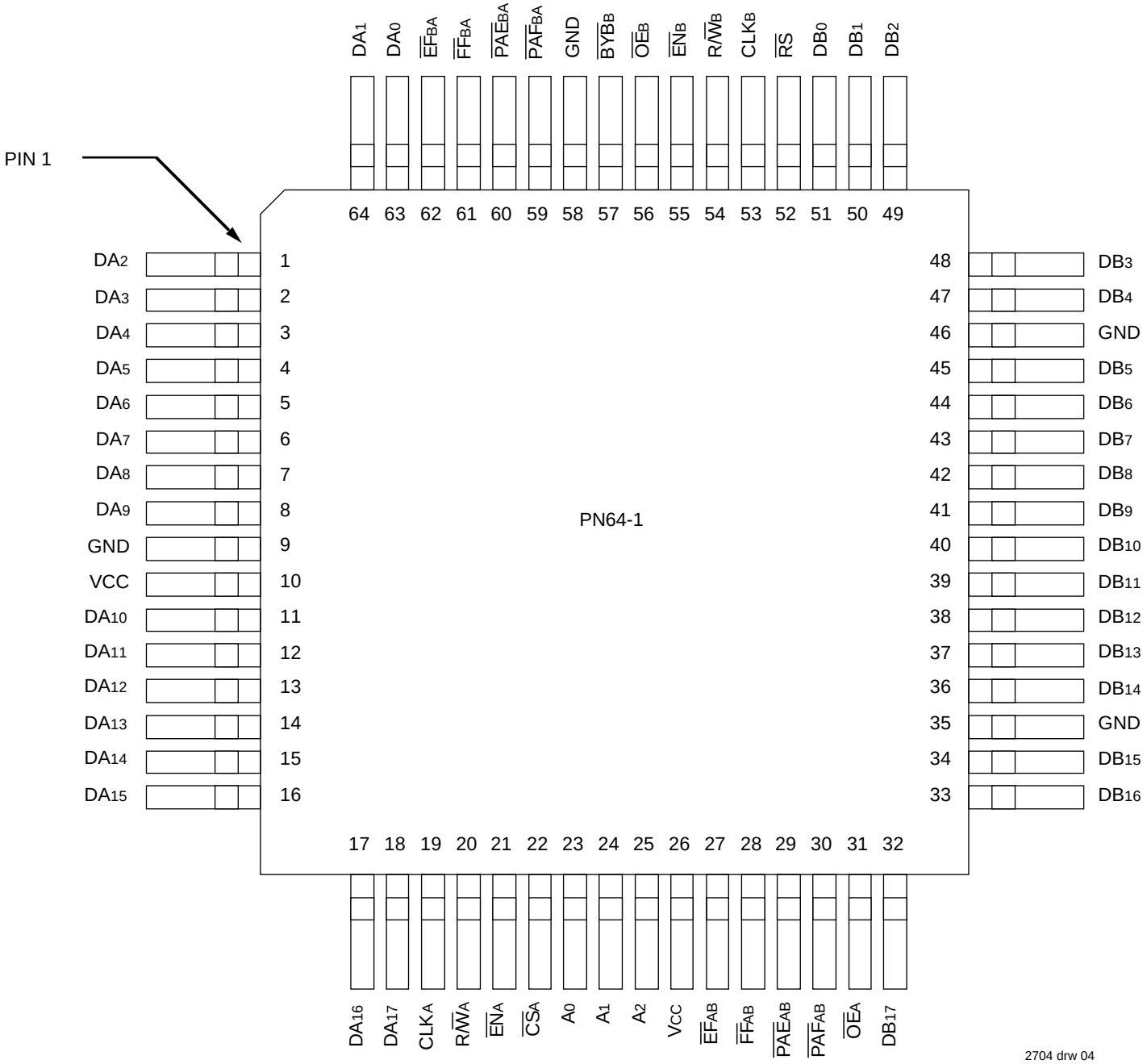


PGA
Top View



PLCC
Top View

PIN CONFIGURATIONS



TQFP
Top View

PIN DESCRIPTION

Symbol	Name	I/O	Description
D_{A0}-D_{A17}	Data A	I/O	Data inputs & outputs for the 18-bit Port A bus.
$\overline{CS}_A$	Chip Select A	I	Port A is accessed when $\overline{CS}_A$ is LOW. Port A is inactive if $\overline{CS}_A$ is HIGH.
R/$\overline{W}_A$	Read/Write A	I	This pin controls the read or write direction of Port A. If R/$\overline{W}_A$ is LOW, Data A input data is written into Port A. If R/$\overline{W}_A$ is HIGH, Data A output data is read from Port A. In bypass mode, when R/$\overline{W}_A$ is LOW, message is written into A→B output register. If R/$\overline{W}_A$ is HIGH, message is read from B→A output register.
CLK_A	Clock A	I	CLK_A is typically a free running clock. Data is read or written into Port A on the rising edge of CLK_A.
$\overline{EN}_A$	Enable A	I	When $\overline{EN}_A$ is LOW, data can be read or written to Port A. When $\overline{EN}_A$ is HIGH, no data transfers occur.
$\overline{OE}_A$	Output Enable A	I	When R/$\overline{W}_A$ is HIGH , Port A is an output bus and $\overline{OE}_A$ controls the high-impedance state of D_{A0}-D_{A17}. If $\overline{OE}_A$ is HIGH, Port A is in a high-impedance state. If $\overline{OE}_A$ is LOW while $\overline{CS}_A$ is LOW and R/$\overline{W}_A$ is HIGH, Port A is in an active (low-impedance) state.
A_0, A_1, A_2	Addresses	I	When $\overline{CS}_A$ is asserted, A_0, A_1, A_2 and R/$\overline{W}_A$ are used to select one of six internal resources.
D_{B0}-D_{B17}	Data B	I/O	Data inputs & outputs for the 18-bit Port B bus.
R/$\overline{W}_B$	Read/Write B	I	This pin controls the read or write direction of Port B. If R/$\overline{W}_B$ is LOW, Data B input data is written into Port B. If R/$\overline{W}_B$ is HIGH, Data B output data is read from Port B. In bypass mode, when R/$\overline{W}_B$ is LOW, message is written into B→A output register. If R/$\overline{W}_B$ is HIGH, message is read from A→B output register.
CLK_B	Clock B	I	Clock B is typically a free running clock. Data is read or written into Port B on the rising edge of CLK_B.
$\overline{EN}_B$	Enable B	I	When $\overline{EN}_B$ is LOW, data can be read or written to Port B. When $\overline{EN}_B$ is HIGH, no data transfers occur.
$\overline{OE}_B$	Output Enable B	I	When R/$\overline{W}_B$ is HIGH , Port B is an output bus and $\overline{OE}_B$ controls the high-impedance state of D_{B0}-D_{B17}. If OE_B is HIGH, Port B is in a high-impedance state. If $\overline{OE}_B$ is LOW while R/$\overline{W}_B$ is HIGH, Port B is in an active (low-impedance) state.
$\overline{EF}_{AB}$	A→B Empty Flag	O	When $\overline{EF}_{AB}$ is LOW, the A→B FIFO is empty and further data reads from Port B are inhibited. When $\overline{EF}_{AB}$ is HIGH, the FIFO is not empty. $\overline{EF}_{AB}$ is synchronized to CLK_B. In the bypass mode, $\overline{EF}_{AB}$ HIGH indicates that data D_{A0}-D_{A17} is available for passing through. After the data D_{B0}-D_{B17} has been read, $\overline{EF}_{AB}$ goes LOW.
$\overline{PAE}_{AB}$	A→B Programmable Almost-Empty Flag	O	When $\overline{PAE}_{AB}$ is LOW, the A→B FIFO is almost empty. An almost empty FIFO contains less than or equal to the offset programmed into $\overline{PAE}_{AB}$ Register. When $\overline{PAE}_{AB}$ is HIGH, the A→B FIFO contains more than offset in $\overline{PAE}_{AB}$ Register. The default offset value for $\overline{PAE}_{AB}$ Register is 8. $\overline{PAE}_{AB}$ is synchronized to CLK_B.
$\overline{PAF}_{AB}$	A→B Programmable Almost-Full Flag	O	When $\overline{PAF}_{AB}$ is LOW, the A→B FIFO is almost full. An almost full FIFO contains greater than the FIFO depth minus the offset programmed into $\overline{PAF}_{AB}$ Register. When PAF_{AB} is HIGH, the A→B FIFO contains less than or equal to the depth minus the offset in PAF_{AB} Register. The default offset value for PAF_{AB} Register is 8. $\overline{PAF}_{AB}$ is synchronized to CLK_A.
$\overline{FF}_{AB}$	A→B Full Flag	O	When $\overline{FF}_{AB}$ is LOW, the A→B FIFO is full and further data writes into Port A are inhibited. When $\overline{FF}_{AB}$ is HIGH, the FIFO is not full. $\overline{FF}_{AB}$ is synchronized to CLK_A. In bypass mode, $\overline{FF}_{AB}$ tells Port A that a message is waiting in Port B's output register. If $\overline{FF}_{AB}$ is LOW, a bypass message is in the register. If $\overline{FF}_{AB}$ is HIGH, Port B has read the message and another message can be written into Port A.
$\overline{EF}_{BA}$	B→A Empty Flag	O	When $\overline{EF}_{BA}$ is LOW, the B→A FIFO is empty and further data reads from Port A are inhibited. When $\overline{EF}_{BA}$ is HIGH, the FIFO is not empty. $\overline{EF}_{BA}$ is synchronized to CLK_A. In the bypass mode, $\overline{EF}_{BA}$ HIGH indicates that data D_{B0}-D_{B17} is available for passing through. After the data D_{A0}-D_{A17} has been read, $\overline{EF}_{BA}$ goes LOW on the following cycle.
$\overline{PAE}_{BA}$	B→A Programmable Almost-Empty Flag	O	When $\overline{PAE}_{BA}$ is LOW, the B→A FIFO is almost empty. An almost empty FIFO contains less than or equal to the offset programmed into $\overline{PAE}_{BA}$ Register. When $\overline{PAE}_{BA}$ is HIGH, the B→A FIFO contains more than offset in $\overline{PAE}_{BA}$ Register. The default offset value for $\overline{PAE}_{BA}$ Register is 8. $\overline{PAE}_{BA}$ is synchronized to CLK_A.
$\overline{PAF}_{BA}$	B→A Programmable Almost-Full Flag	O	When $\overline{PAF}_{BA}$ is LOW, the B→A FIFO is almost full. An almost full FIFO contains greater than the FIFO depth minus the offset programmed into $\overline{PAF}_{BA}$ Register. When $\overline{PAF}_{BA}$ is HIGH, the B→A FIFO contains less than or equal to the depth minus the offset in $\overline{PAF}_{BA}$ Register. The default offset value for $\overline{PAF}_{BA}$ Register is 8. $\overline{PAF}_{BA}$ is synchronized to CLK_B.

2704 tbl 01

PIN DESCRIPTION (Continued)

Symbol	Name	I/O	Description
$\overline{FF}_{BA}$	B→A Full Flag	O	When $\overline{FF}_{BA}$ is LOW, the B→A FIFO is full and further data writes into Port B are inhibited. When $\overline{FF}_{BA}$ is HIGH, the FIFO is not full. $\overline{FF}_{BA}$ is synchronized to CLK_B. In bypass mode, $\overline{FF}_{BA}$ tells Port B that a message is waiting in Port A's output register. If $\overline{FF}_{BA}$ is LOW, a bypass message is in the register. If $\overline{FF}_{BA}$ is HIGH, Port A has read the message and another message can be written into Port B.
$\overline{BYP}_B$	Port B Bypass Flag	O	This flag informs Port B that the Synchronous BiFIFO is in bypass mode. When BYP_B is LOW, Port A has placed the FIFO into bypass mode. If $\overline{BYP}_B$ is HIGH, the Synchronous BiFIFO passes data into memory. $\overline{BYP}_B$ is synchronized to CLK_B.
$\overline{RS}$	Reset	I	A LOW on this pin will perform a reset of all Synchronous BiFIFO functions.
V_{CC}	Power		There are three +5V power pins for the PLCC and PGA packages and two for the TQFP.
GND	Ground		There are seven ground pins for the PLCC and PGA packages and four for the TQFP.

2704 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to Ground	–0.5 to +7.0	–0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	–55 to +125	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	–65 to +135	°C
T_{STG}	Storage Temperature	–55 to +125	–65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE: 2704 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V

NOTE: 2704 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}(2)	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}(1,2)	Output Capacitance	V_{OUT} = 0V	10	pF

NOTES: 2704 tbl 05

1. With output deselected.
2. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72615L IDT72605L Commercial t_{CLK} = 20, 25, 35, 50ns			Unit
		Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage I_{OUT} = –2mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 8mA	—	—	0.4	V
I_{CC}(3)	Average V_{CC} Power Supply Current	—	—	230	mA

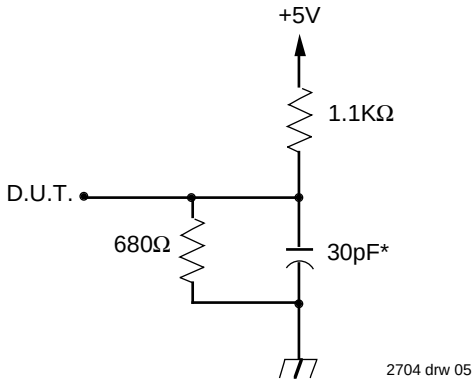
NOTES: 2704 tbl 06

1. Measurements with 0.4V ≤ V_{IN} ≤ V_{CC}.
2. $\overline{OEA}$, $\overline{OEB}$ ≥ V_{IH}; 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs open. Testing frequency f=20MHz

AC TEST CONDITIONS

In Pulse Levels	GND to 3.0V
Input Rise/Fall Times	3ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure 2

2704 tbl 07



or equivalent circuit
Figure 2. Output Load
* Includes jig and scope capacitances.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5V±10%, T_A = 0°C to +70°C)

		Commercial									
		72615L20 72605L20		72615L25 72605L25		72615L35 72605L35		72615L50 72605L50			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Timing Figures
f_{CLK}	Clock frequency	—	50	—	40	—	28	—	20	MHz	—
t_{CLK}	Clock cycle time	20	—	25	—	35	—	50	—	ns	4,5,6,7
t_{CLKH}	Clock HIGH time	8	—	10	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t_{CLKL}	Clock LOW time	8	—	10	—	14	—	20	—	ns	4,5,6,7,12,13,14,15
t_{RS}	Reset pulse width	20	—	25	—	35	—	50	—	ns	3
t_{RSS}	Reset set-up time	12	—	15	—	21	—	30	—	ns	3
t_{RSR}	Reset recovery time	12	—	15	—	21	—	30	—	ns	3
t_{RSF}	Reset to flags in intial state	—	27	—	28	—	35	—	50	ns	3
t_A	Data access time	3	10	3	15	3	21	3	25	ns	5,7,8,9,10,11
t_{CS}	Control signal set-up time(1)	6	—	6	—	8	—	10	—	ns	4,5,6,7,8,9,10,11, 12, 13,14,15
t_{CH}	Control signal hold time(1)	1	—	1	—	1	—	1	—	ns	4,5,6,7,10,11,12, 13, 14,15
t_{DS}	Data set-up time	6	—	6	—	8	—	10	—	ns	4,6,8,9,10,11
t_{DH}	Data hold time	1	—	1	—	1	—	1	—	ns	4,6
t_{OE}	Output Enable LOW to output data valid(2)	3	10	3	13	3	20	3	28	ns	5,7,8,9,10,11
t_{OLZ}	Output Enable LOW to data bus at Low-Z(2)	0	—	0	—	0	—	0	—	ns	5,7,8,9,10,11
t_{OHZ}	Output Enable HIGH to data bus at High-Z(2)	3	10	3	13	3	20	3	28	ns	5,7,10,11
t_{FF}	Clock to Full Flag time	—	10	—	15	—	21	—	30	ns	4,6,10,11
t_{EF}	Clock to Empty Flag time	—	10	—	15	—	21	—	30	ns	5,7,8,9,10,11
t_{PAE}	Clock to Programmable Almost Empty Flag time	—	12	—	15	—	21	—	30	ns	12,14
t_{PAF}	Clock to Programmable Almost Full Flag time	—	12	—	15	—	21	—	30	ns	13,15
t_{SKEW1}	Skew between CLK_A & CLK_B for Empty/Full Flags(2)	10	—	12	—	17	—	20	—	ns	4,5,6,7,8,9,10,11
t_{SKEW2}	Skew between CLK_A & CLK_B for Programmable Flags(2)	17	—	19	—	25	—	34	—	ns	4, 7,12,13,14,15

NOTES:
1. Control signals refer to $\overline{CS}_A$, R/$\overline{W}_A$, $\overline{EN}_A$, A_2, A_1, A_0, R/$\overline{W}_B$, $\overline{EN}_B$.
2. Minimum values are guaranteed by design.

2704 tbl 08

FUNCTIONAL DESCRIPTION

IDTs SyncBiFIFO is versatile for both multiprocessor and peripheral applications. Data can be stored or retrieved from two sources simultaneously.

The SyncBiFIFO has registers on all inputs and outputs. Data is only transferred into the I/O registers on clock edges, hence the interfaces are synchronous. Two Dual-Port FIFO memory arrays are contained in the SyncBiFIFO; one data buffer for each direction. Each port has its own independent clock. Data transfers to the I/O registers are gated by the enable signals. The transfer direction for each port is controlled independently by a read/write signal. Individual output enable signals control whether the SyncBiFIFO is driving the data lines of a port or whether those data lines are in a high-impedance state. The processor connected to Port A of the BiFIFO can send or receive messages directly to the Port B device using the 18-bit bypass path.

The SyncBiFIFO can be used in multiples of 18-bits. In a 36- to 36-bit configuration, two SyncBiFIFOs operate in parallel. Both devices are programmed simultaneously, 18 data bits to each device. This configuration can be extended to wider bus widths (54- to 54-bits, 72- to 72-bits, etc.) by adding more SyncBiFIFOs to the configuration. Figure 1 shows multiple SyncBiFIFOs configured for multiprocessor communication.

The microprocessor or microcontroller connected to Port A controls all operations of the SyncBiFIFO. Thus, all Port A interface pins are inputs driven by the controlling processor. Port B interfaces with a second processor. The Port B control pins are inputs driven by the second processor.

RESET

Reset is accomplished whenever the Reset ($\overline{RS}$) input is taken to a LOW state with $\overline{CS}_A$, $\overline{EN}_A$ and $\overline{EN}_B$ HIGH. During reset, both internal read and write pointers are set to the first location. A reset is required after power up before a write operation can take place. The A→B and B→A FIFO Empty Flags ($\overline{EF}_{AB}$, $\overline{EF}_{BA}$) and Programmable Almost Empty Flags ($\overline{PAE}_{AB}$, $\overline{PAE}_{BA}$) will be set to LOW after t_{RSF}. The A→B and B→A FIFO Full Flags ($\overline{FF}_{AB}$, $\overline{FF}_{BA}$) and Programmable Almost Full Flags ($\overline{PAF}_{AB}$, $\overline{PAF}_{BA}$) will be set to HIGH after t_{RSF}. After the reset, the offsets of the Almost-Empty Flags and Almost-Full Flags for the A→B and B→A FIFO offset default to 8.

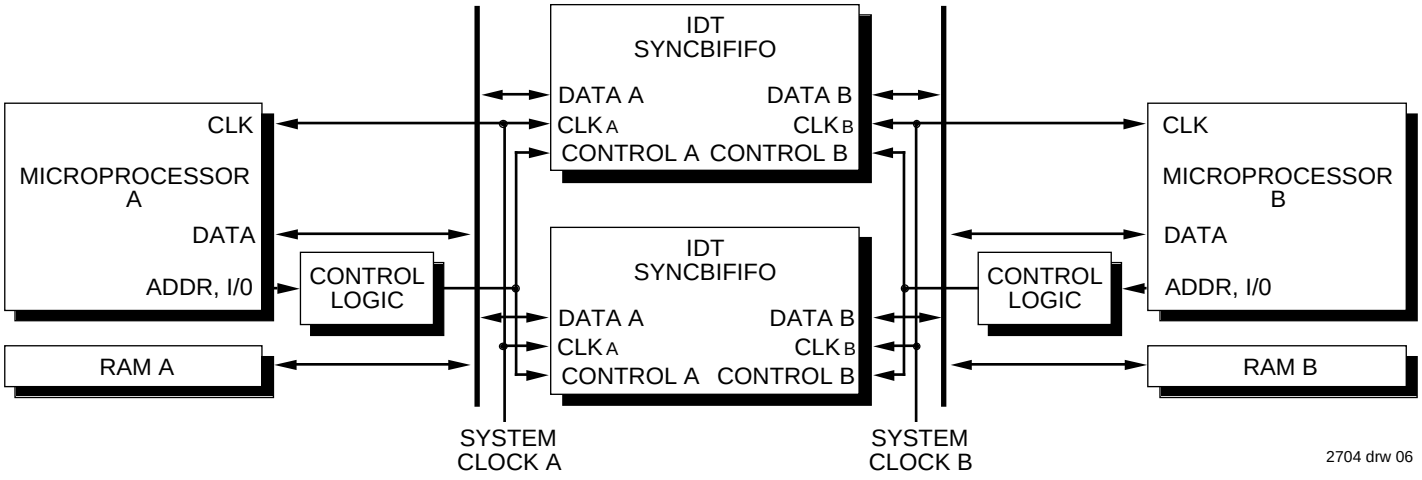
PORT A INTERFACE

The SyncBiFIFO is straightforward to use in micro-processor-based systems because each port has a standard microprocessor control set. Port A interfaces with microprocessor through the three address pins (A_2-A_0) and a Chip Select $\overline{CS}_A$ pins. When $\overline{CS}_A$ is asserted, A_2,A_1,A_0 and R/$\overline{W}_A$ are used to select one of six internal resources (Table 1).

With A_2=0 and A_1=0, A_0 determines whether data can be read out of output register or be written into the FIFO (A_0=0), or the data can pass through the FIFO through the bypass path (A_0=1).

With A_2=1, four programmable flags (two A→B FIFO programmable flags and two B→A FIFO programmable flags) can be selected: the A→B FIFO Almost-Empty Flag Offset (A_1=0, A_0=0), A→B FIFO Almost-Full Flag Offset (A_1=0, A_0=1), B→A FIFO Almost-Empty Flag Offset (A_1=1, A_0=0), B→A FIFO Almost-Full Flag Offset (A_1=1, A_0=1).

Port A is disabled when CSA is deasserted and data A is in high-impedance state.



NOTES:
1. Upper SyncBiFIFO only is used in 18- to 18-bit configuration.
2. Control A Consists of R/$\overline{W}_A$, $\overline{EN}_A$, $\overline{OE}_A$, $\overline{CS}_A$, A_2, A_1, A_0. Control B consists of R/$\overline{W}_B$, $\overline{EN}_B$, $\overline{OE}_B$.

Figure 1. 36- to 36-bit Processor Interface Configuration.

$\overline{CS}_A$	R/$\overline{W}_A$	$\overline{EN}_A$	$\overline{OE}_A$	Data A I/O	Port A Operation
0	0	0	0	I	Data A is written on CLKA ≠. This write cycle immediately following low-impedance cycle is prohibited. Note that even though OE_A = 0, a LOW logic level on R/W_A, once qualified by a rising edge on CLK_A, will put Data A into a high-impedance state.
0	0	0	1	I	Data A is written on CLKA ≠
0	0	1	X	I	Data A is ignored
0	1	0	0	O	Data is read(1) from RAM array to output register on CLKA ≠, Data A is low-impedance
0	1	0	1	O	Data is read(1) from RAM array to output register on CLKA ≠, Data A is high-impedance
0	1	1	0	O	Output register does not change(2), Data A is low-impedance
0	1	1	1	O	Output register does not change(2), Data A is high-impedance
1	0	X	X	I	Data A is ignored(3)
1	1	X	X	O	Data A is high-impedance(3)

NOTES:

2704 tbl 09

1. When $A_2A_1A_0$ = 000, the next B→A FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0$ = 001, the bypass path is selected and bypass data from the Port B input register is read from the Port A output register. If $A_2A_1A_0$0 = 1XX, a flag offset register is selected and its offset is read out through Port A output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port A output register does not change and the B→A read pointer does not advance.
3. If $CS_{A\#}$ is HIGH, then BYP_B is HIGH. No bypass occur under this condition.

Table 1. Port A Operation Control Signals

BYPASS PATH

The bypass paths provide direct communication between Port A and Port B. There are two full 18-bit bypass paths, one in each direction. During a bypass operation, data is passed directly between the input and output registers, and the FIFO memory is undisturbed.

Port A initiates and terminates all bypass operations. The bypass flag, $\overline{BYP}_B$, is asserted to inform Port B that a bypass operation is beginning. The bypass flag state is controlled by the Port A controls, although the $\overline{BYP}_B$ signal is synchronized to $\overline{CLK}_B$. So, $\overline{BYP}_B$ is asserted on the next rising edge of $\overline{CLK}_B$ when $A_2A_1A_0$=001and CS_A is LOW. When Port A returns to normal FIFO mode ($A_2A_1A_0$=000 or CS_A is HIGH), $\overline{BYP}_B$ is deasserted on the next $\overline{CLK}_B$ rising edge.

Once the SyncBiFIFO is in bypass mode, all data transfers are controlled by the standard Port A (R/$\overline{W}_A$, $\overline{CLK}_A$, $\overline{EN}_A$, $\overline{OE}_A$) and Port B (R/$\overline{W}_B$, $\overline{CLK}_B$, $\overline{EN}_B$, $\overline{OE}_B$) interface pins. Each bypass path can be considered as a one word deep FIFO. Data is held in each input register until it is read. Since the controls of each port operate independently, Port A can be reading bypass data at the same time Port B is reading bypass data.

When R/$\overline{W}_A$ and $\overline{EN}_A$ is LOW, data on pins D_{A0}-D_{A17} is written into Port A input register. Following the rising edge of $\overline{CLK}_A$ for this write, the A→B Full Flag ($\overline{FF}_{AB}$) goes LOW. Subsequent writes into Port A are blocked by internal logic until $\overline{FF}_{AB}$ goes HIGH again. On the next CLKB rising edge, the A→B Empty Flag ($\overline{EF}_{AB}$) goes HIGH indicating to Port B that data is available. Once R/$\overline{W}_B$ is HIGH and $\overline{EN}_B$ is LOW, data is read into the Port B output register. $\overline{OE}_B$ still controls whether Port B is in a high-impedance state. When $\overline{OE}_B$ is LOW, the output register data appears at D_{B0}-D_{B17}. $\overline{EF}_{AB}$ goes LOW following the $\overline{CLK}_B$ rising edge for this read. FFAB goes HIGH on the next $\overline{CLK}_A$ rising edge, letting Port A know that another word can be written through the bypass path.

Bypass data transfers from Port B to Port A work in a similar manner with $\overline{EFB}_A$ and $\overline{FFB}_A$ indicating the Port A output register state.

When the Port A address changes from bypass mode ($A_2A_1A_0$=001) to FIFO mode ($A_2A_1A_0$=000) on the rising edge of $\overline{CLK}_A$, the data held in the Port B output register may be overwritten. Unless Port A monitors the $\overline{BYP}_B$ pin and waits for Port B to clock out the last bypass word, data from the A→B FIFO will overwrite data in the Port B output register. $\overline{BYP}_B$ will go HIGH on the rising edge of $\overline{CLK}_B$ signifying that Port B has finished its last bypass operation. Port B must read any bypass data in the output register on this last $\overline{CLK}_B$ clock or it is lost and the SyncBiFIFO returns to FIFO operations. It is especially important to monitor $\overline{BYP}_B$ when $\overline{CLK}_B$ is much slower than $\overline{CLK}_A$ to avoid this condition. $\overline{BYP}_B$ will also go HIGH after $\overline{CS}_A$ is brought HIGH; in this manner the Port B bypass data may also be lost.

Since the Port A processor controls $\overline{CS}_A$ and the bypass mode, this scenario can be handled for B→A bypass data. The Port A processor must be set up to read the last bypass word before leaving bypass mode.

$\overline{CS}_A$	A_2	A_1	A_0	Read	Write
0	0	0	0	B→A FIFO	A→B FIFO
0	0	0	1	18-bit Bypass Path	
0	1	0	0	A→B FIFO Almost-Empty Flag Offset	
0	1	0	1	A→B FIFO Almost-Full Flag Offset	
0	1	1	0	B→A FIFO Almost-Empty Flag Offset	
0	1	1	1	B→A FIFO Almost-Full Flag Offset	
1	X	X	X	Port A Disabled	

2704 tbl 10

Table 2. Accessing Port A Resources Using $\overline{CS}_A$, A_2, A_1, and A_0.

PORT A CONTROL SIGNALS

The Port A control signals pins dictate the various operations shown in Table 2. Port A is accessed when $\overline{CS}_A$ is LOW, and is inactive if $\overline{CS}_A$ is HIGH. R/$\overline{W}_A$ and $\overline{EN}_A$ lines determine when Data A can be written or read. If R/$\overline{W}_A$ and $\overline{EN}_A$ are LOW, data is written into input register on the LOW-to-HIGH transition of $\overline{CLK}_A$. If R/$\overline{W}_A$ is HIGH and $\overline{OE}_A$ is LOW, data comes out of bus and is read from output register into three-state buffer. Refer to pin descriptions for more information.

PROGRAMMABLE FLAGS

The IDT SyncBiFIFO has eight flags: four flags for A→B FIFO ($\overline{EF}_{AB}$, $\overline{PAE}_{AB}$, $\overline{PAF}_{AB}$, $\overline{FF}_{AB}$), and four flags for B→A FIFO ($\overline{EF}_{BA}$, $\overline{PAE}_{BA}$, $\overline{PAF}_{BA}$, $\overline{FF}_{BA}$). The Empty and Full flags are fixed, while the Almost Empty and Almost Full offsets can be set to any depth through the Flag Offset Registers (see Table 3). The flags are asserted at the depths shown in the Flag Truth Table (Table 4). After reset, the programmable flag offsets are set to 8. This means the Almost Empty flags are asserted at Empty +8 words deep, and the Almost Full flags are asserted at Full -8 words deep.

The $\overline{PAE}_{AB}$ is synchronized to $\overline{CLK}_B$, while $\overline{PAE}_{AB}$ is synchronized to $\overline{CLK}_A$; and $\overline{PAE}_{BA}$ is synchronized to $\overline{CLK}_A$, while $\overline{PAE}_{BA}$ is synchronized to $\overline{CLK}_B$. If the minimum time (t_{SKEW2}) between a rising $\overline{CLK}_B$ and a rising $\overline{CLK}_A$ is met, the flag will change state on the current clock; otherwise, the flag may not change state until the next clock rising edge. For the specific flag timings, refer to Figures 12-15.

PORT B CONTROL SIGNALS

The Port B control signal pins dictate the various operations shown in Table 5. Port B is independent of $\overline{CS}_A$. R/$\overline{W}_B$ and $\overline{EN}_B$ lines determine when Data can be written or read in Port B. If R/$\overline{W}_B$ and $\overline{EN}_B$ are LOW, data is written into input register, and on LOW-to-HIGH transition of $\overline{CLK}_B$ data is written into

	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
$\overline{PAE}_{AB}$ Register	X	X	X	X	X	X	X	X	X	A→B FIFO Almost-Empty Flag Offset								
$\overline{PAF}_{AB}$ Register	X	X	X	X	X	X	X	X	X	A→B FIFO Almost-Full Flag Offset								
$\overline{PAE}_{BA}$ Register	X	X	X	X	X	X	X	X	X	B→A FIFO Almost-Empty Flag Offset								
$\overline{PAF}_{BA}$ Register	X	X	X	X	X	X	X	X	X	B→A FIFO Almost-Full Flag Offset								

2704 tbl 11

NOTE:
1. Bit 8 must be set to 0 for the IDT72605 (256 x 18) Synchronous BiFIFO.

Table 3. Flag Offset Register Format.

Number of Words in FIFO					
From	To	$\overline{EF}$	$\overline{PAE}$	$\overline{PAF}$	$\overline{FF}$
0	0	LOW	LOW	HIGH	HIGH
1	n	HIGH	LOW	HIGH	HIGH
n+1	D-(m+1)	HIGH	HIGH	HIGH	HIGH
D-m	D-1	HIGH	HIGH	LOW	HIGH
D	D	HIGH	HIGH	LOW	LOW

2704 tbl 12

NOTES:
n = Programmable Empty Offset ($\overline{PAE}_{AB}$ Register or $\overline{PAE}_{BA}$ Register)
m = Programmable Full Offset ($\overline{PAF}_{AB}$ Register or $\overline{PAF}_{BA}$ Register)
D = FIFO Depth (IDT72605 = 256 words, IDT72615= 512 words)

Table 4. Internal Flag Truth Table.

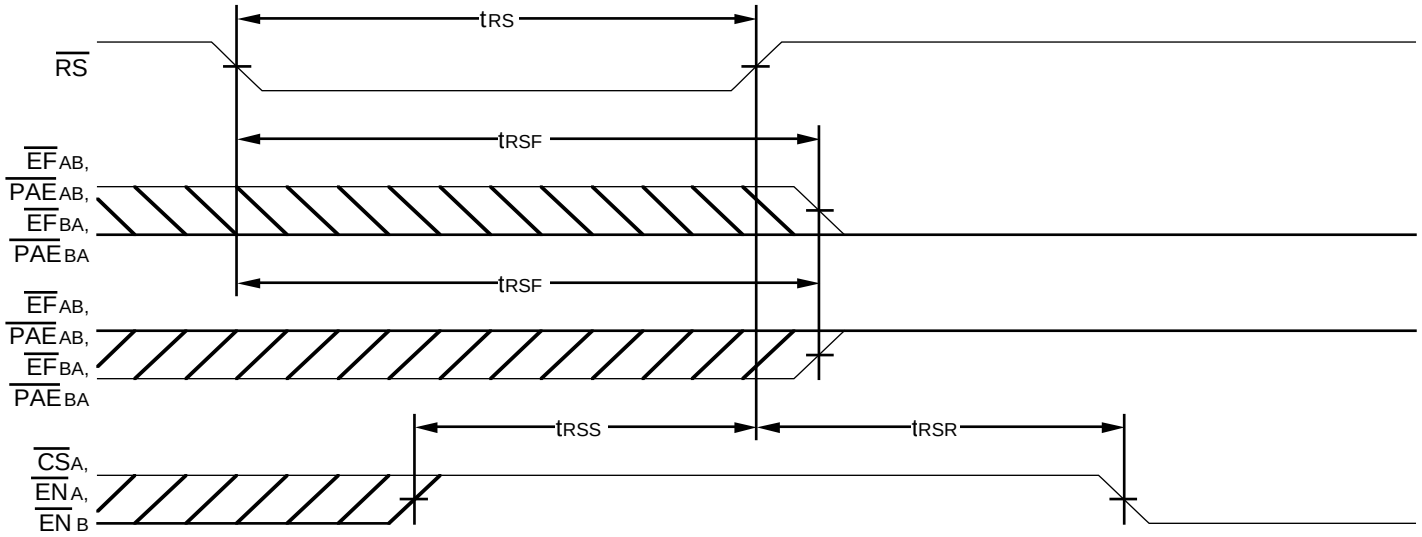
input register and the FIFO memory. If R/$\overline{W}_B$ is HIGH and $\overline{OE}_B$ is LOW, data comes out of bus and is read from output register into three-state buffer. In bypass mode, if R/$\overline{W}_B$ is LOW, bypass messages are transferred into B→A output register. If R/$\overline{W}_A$ is HIGH, bypass messages are transferred into A→B output register. Refer to pin descriptions for more information.

R/$\overline{W}_B$	$\overline{EN}_B$	$\overline{OE}_B$	Data B I/O	Port B Operation
0	0	0	I	Data B is written on CLKB ↑. This write cycle immediately following output low-impedance cycle is prohibited. Note that even though $\overline{OE}_B$ = 0, a LOW logic level on R/$\overline{W}_B$, once qualified by a rising edge on CLK_B, will put Data B into a high-impedance state.
0	0	1	I	Data B is written on CLKB ↑.
0	1	X	I	Data B is ignored
1	0	0	O	Data is read(1) from RAM array to output register on CLKB ≠, Data B is LOW impedance
1	0	1	O	Data is read(1) from RAM array to output register on CLKB ≠, Data B is HIGH impedance
1	1	0	O	Output register does not change(2), Data B is low-impedance
1	1	1	O	Output register does not change(2), Data B is high-impedance

NOTES: 2704 tbl 13

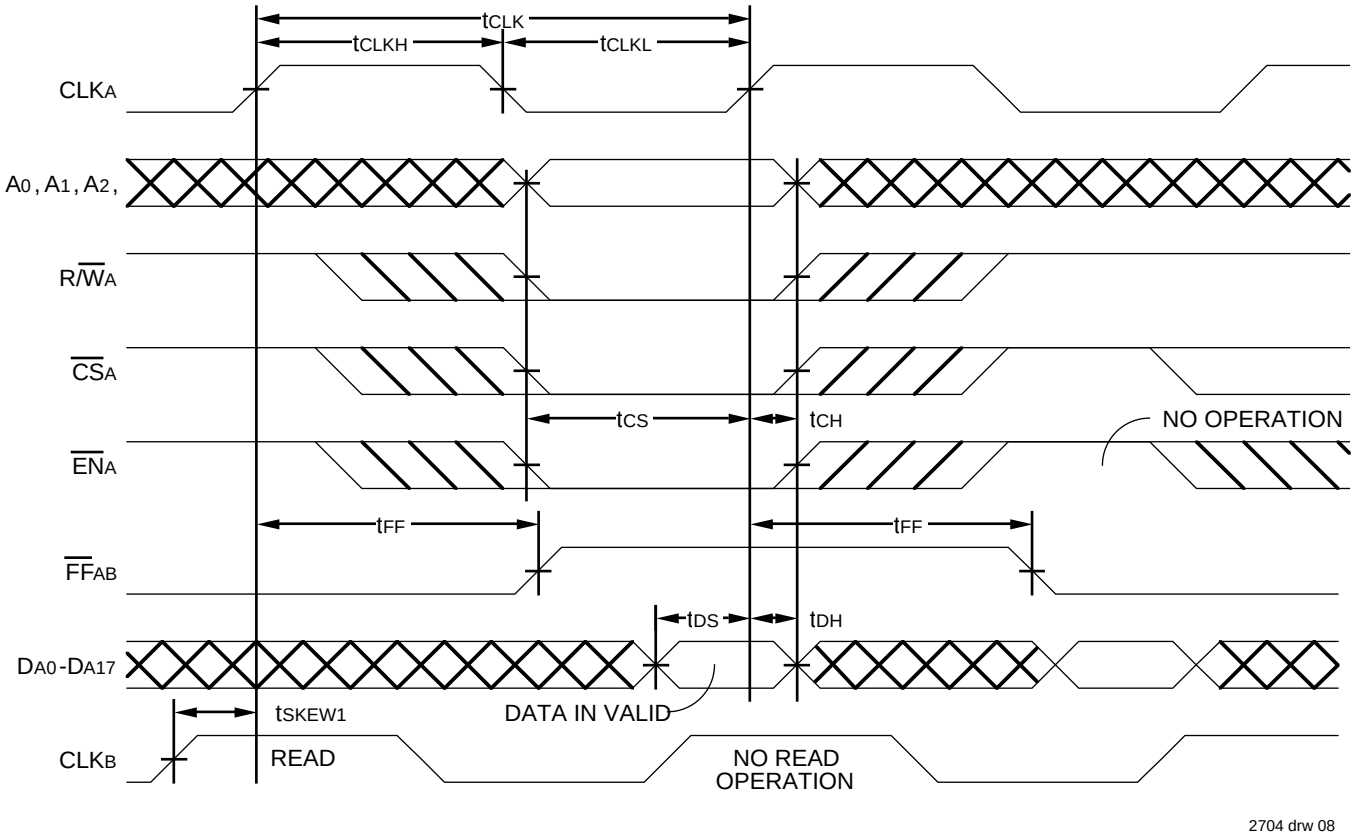
1. When $A_2A_1A_0$ = 000 or 1XX, the next A→B FIFO value is read out of the output register and the read pointer advances. If $A_2A_1A_0$ = 001, the bypass path is selected and bypass data is read from the Port B output register.
2. Regardless of the condition of $A_2A_1A_0$, the data in the Port B output register does not change and the A→B read pointer does not advance.

Table 5. Port B Operation Control Signals.



2704 drw 07

Figure 3. Reset Timing



2704 drw 08

Figure 4. Port A (A→B) Write Timing

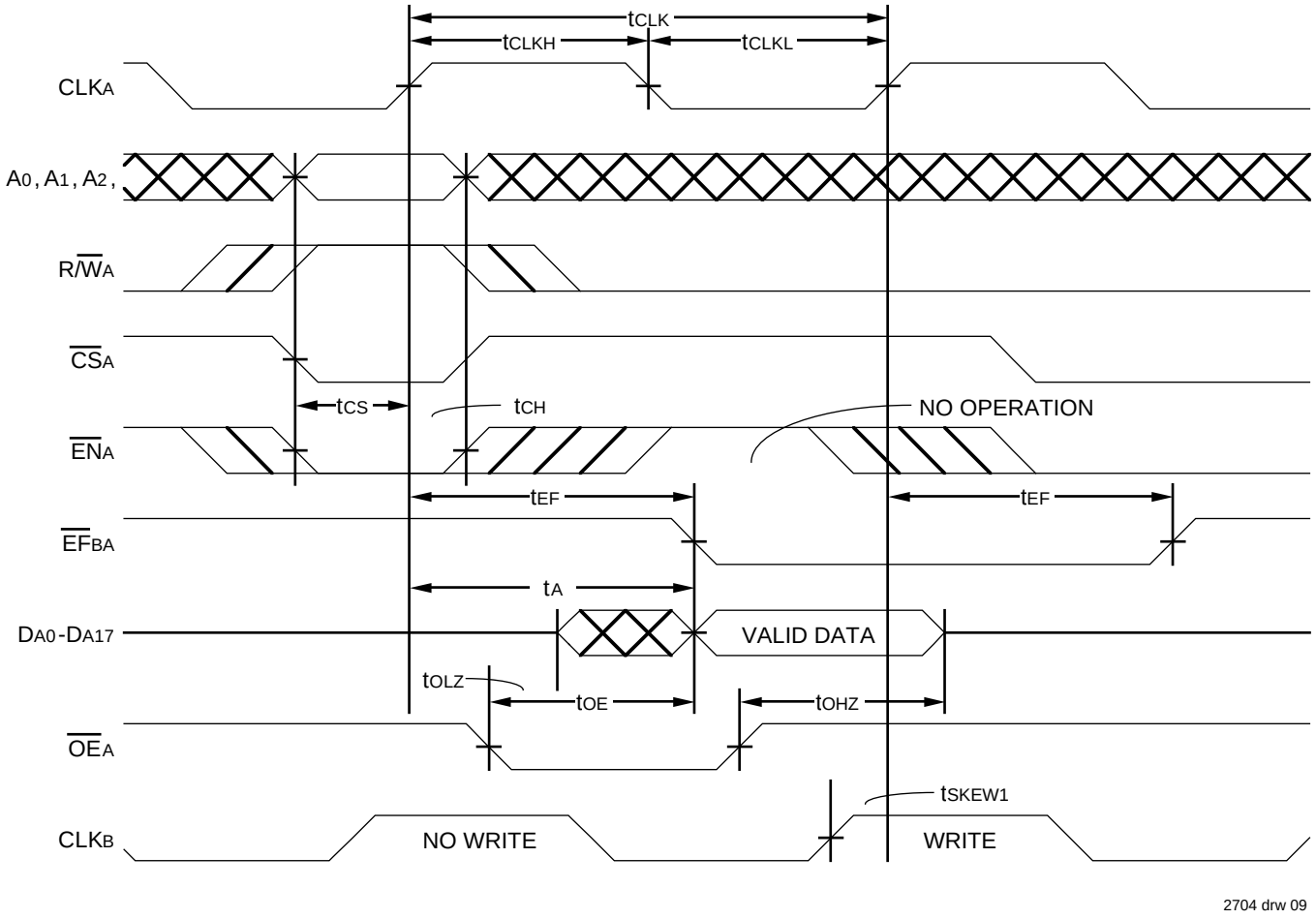


Figure 5. Port A (B→A) Read Timing

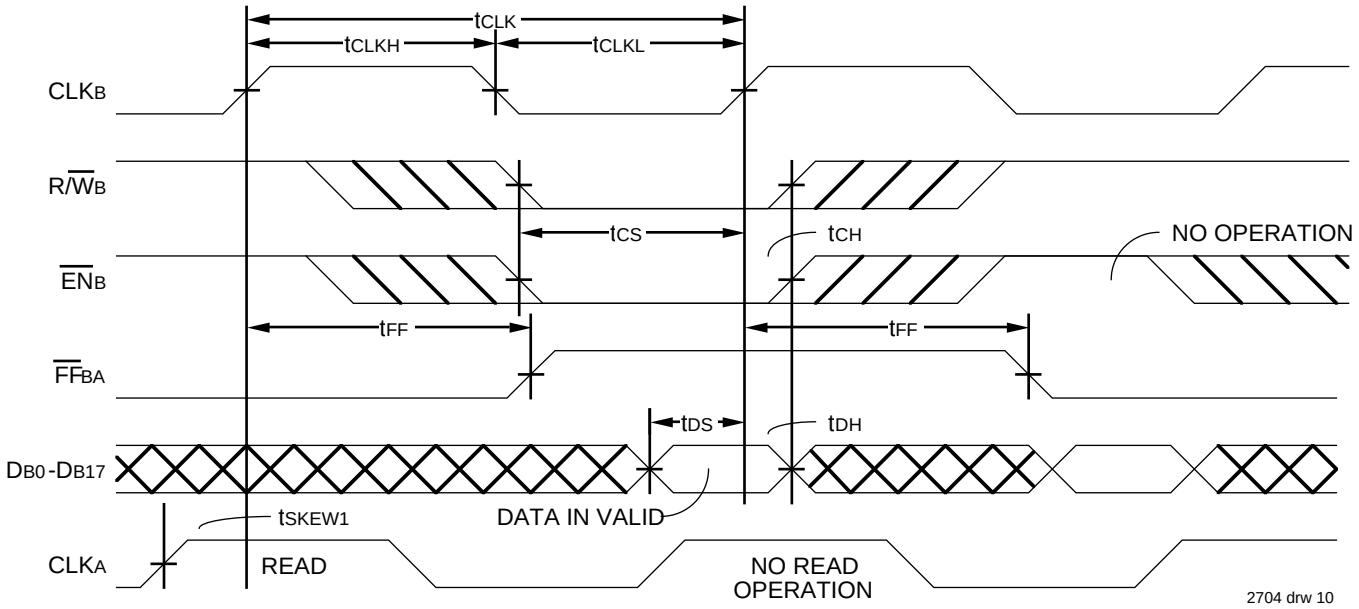


Figure 6. Port B (B→A) Write Timing

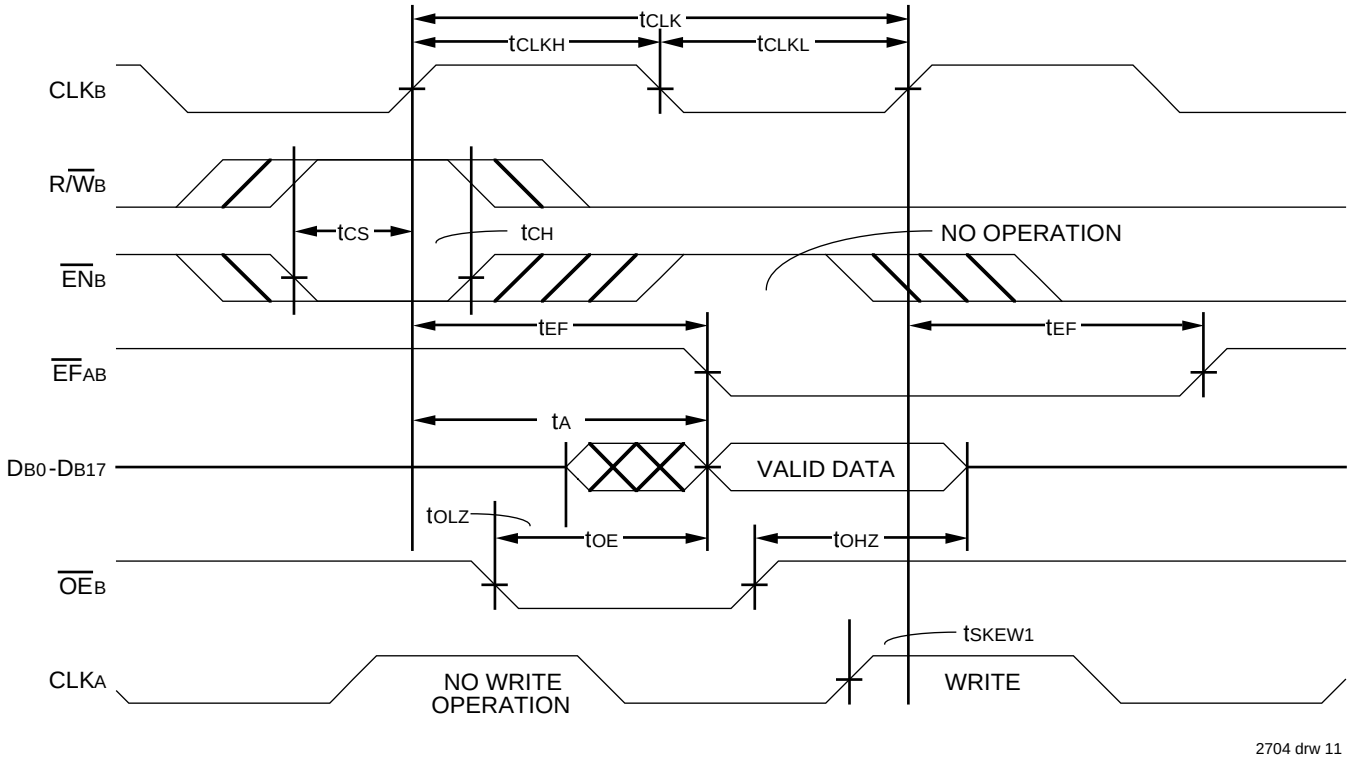
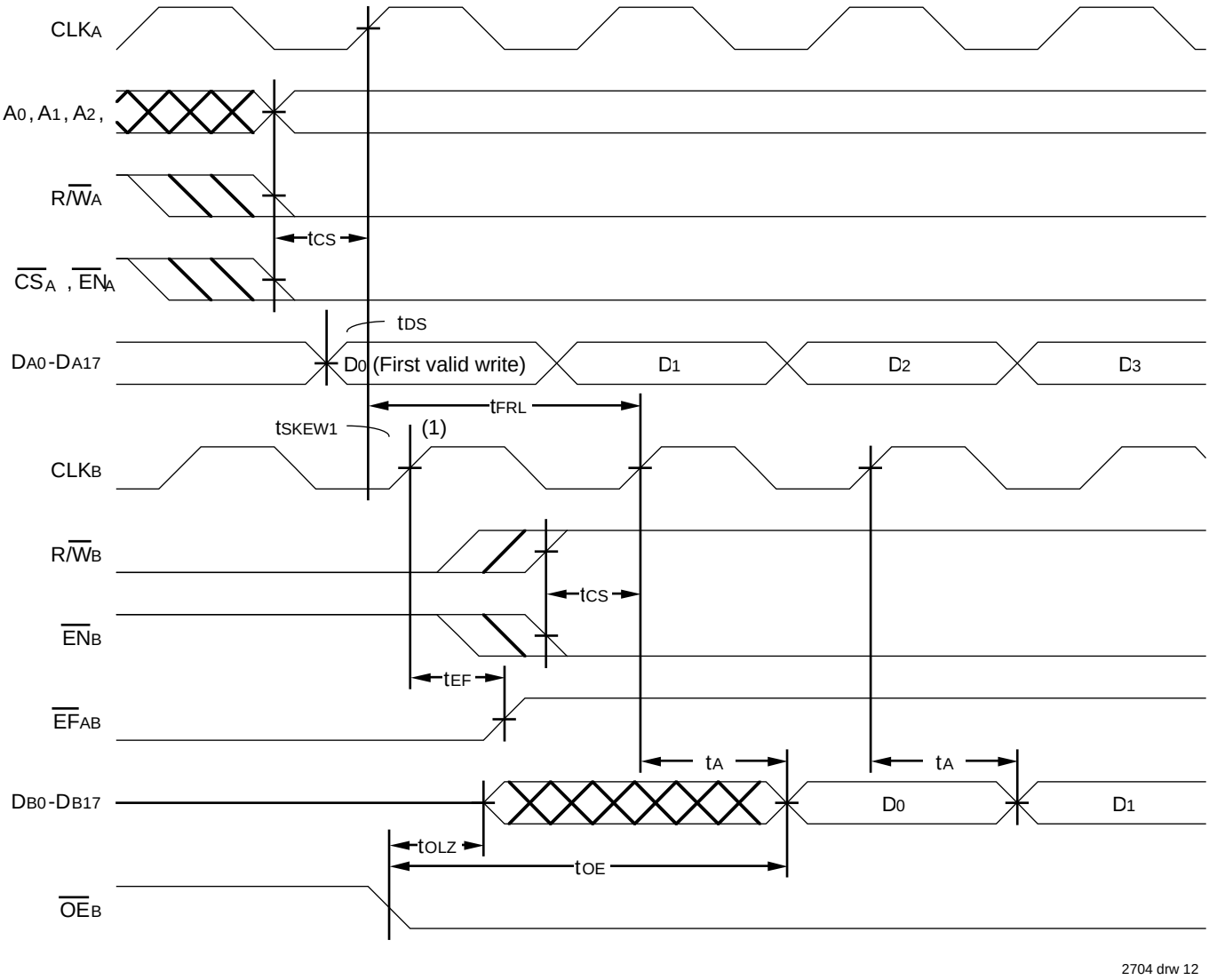
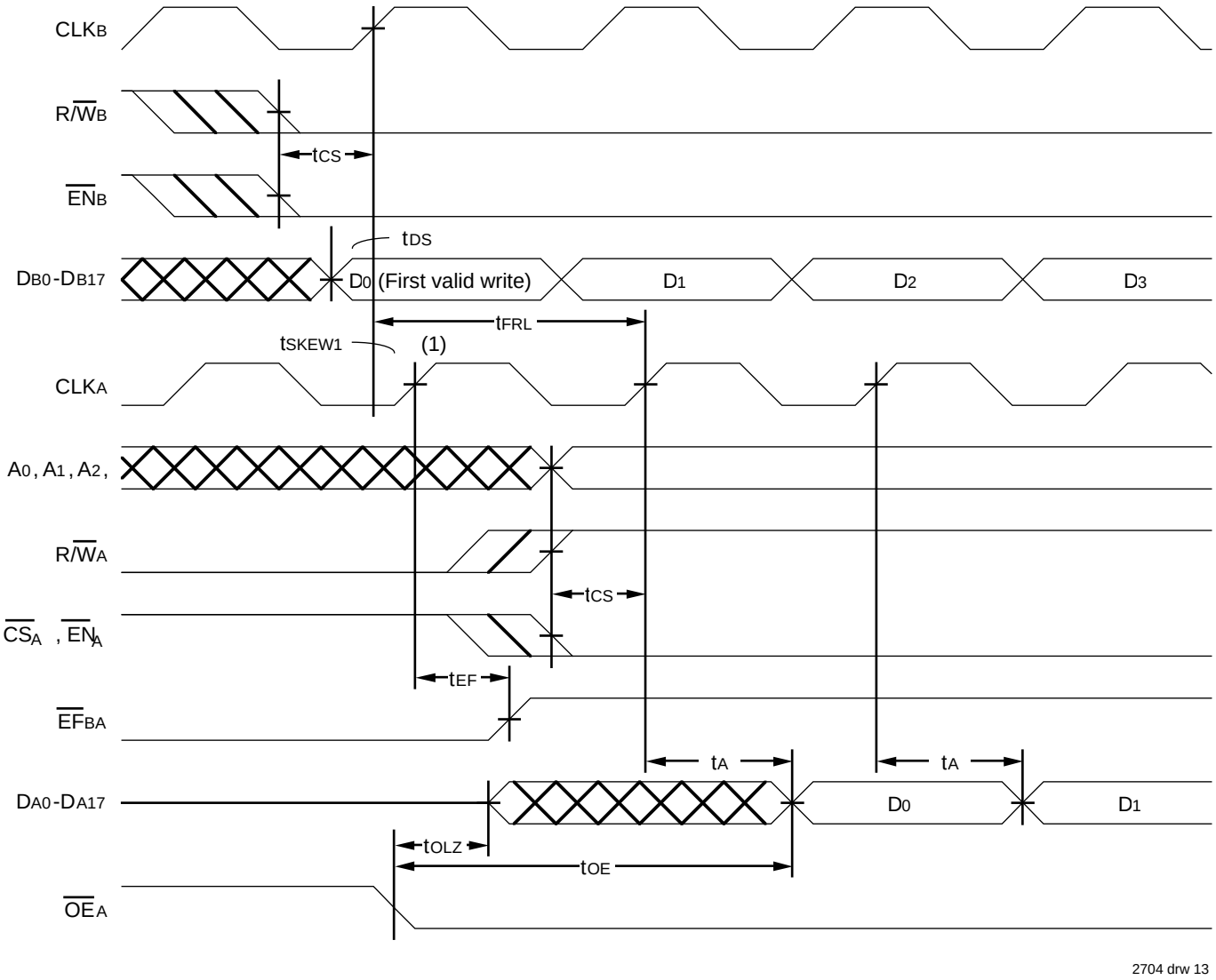


Figure 7. Port B (A→B) Read Timing



NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(Max.)} = t_{CLK} + t_{SKEW1}$
   t_{SKEW1} < minimum specification, $t_{FRL(Max.)} = 2t_{CLK} + t_{SKEW1}$ or $t_{CLK} + t_{SKEW1}$
   The Latency Timing applies only at the Empty Boundary ($\overline{EF}$ = LOW).

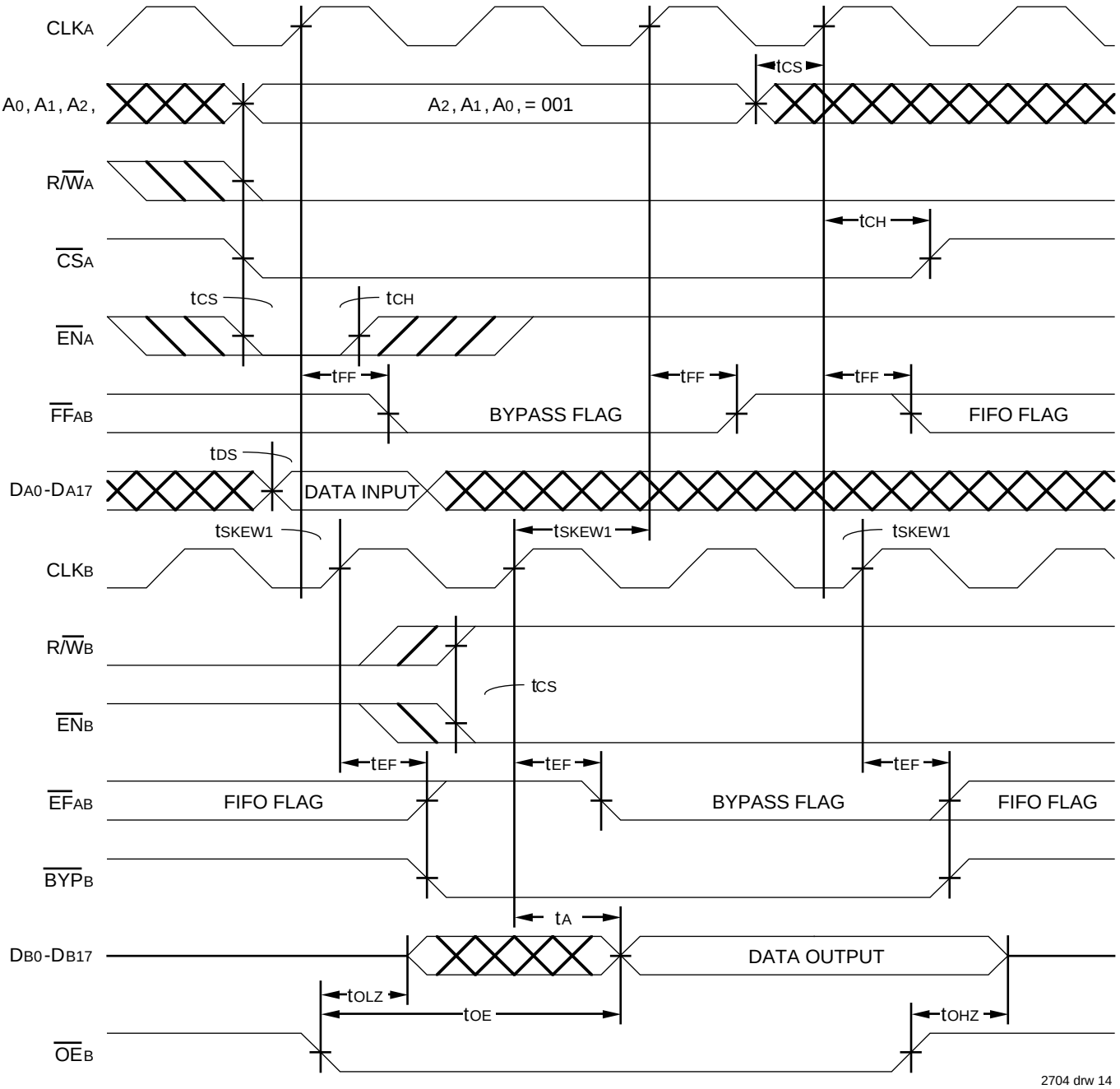
Figure 8. A→B First Data Word Latency after Reset for Simultaneous Read and Write



2704 drw 13

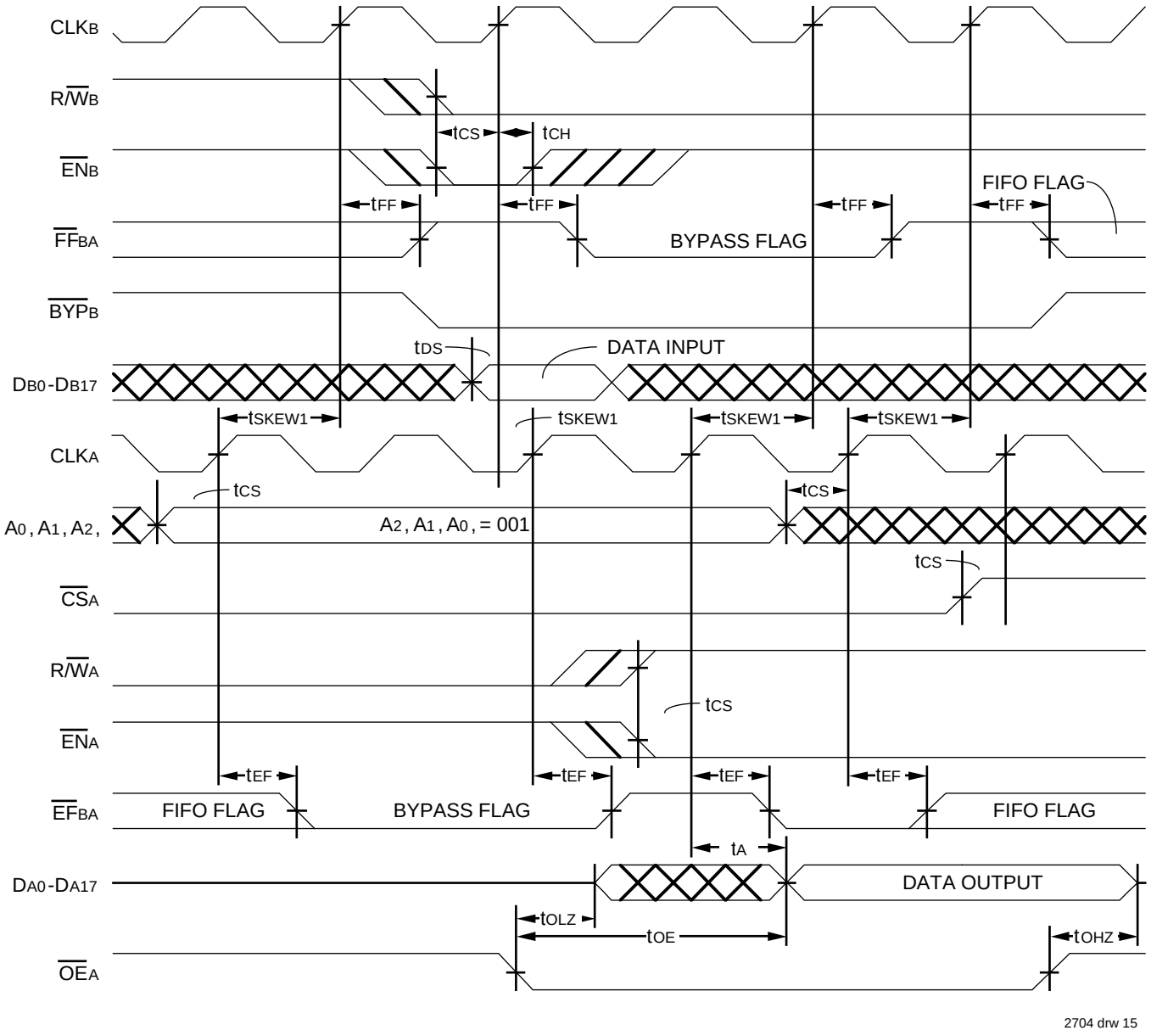
NOTE:
1. When $t_{SKEW1} \geq$ minimum specification, $t_{FRL(Max.)} = t_{CLK} + t_{SKEW1}$
   $t_{SKEW1} <$ minimum specification, $t_{FRL(Max.)} = 2t_{CLK} + t_{SKEW1}$
   The Latency Timing apply only at the Empty Boundary ($\overline{EF}$ = LOW).

Figure 9. B→A First Data Word Latency after Reset for Simultaneous Read and Write



NOTES:
1. When $\overline{CS}_A$ is brought HIGH, A→B Bypass mode will switch to FIFO mode on the following CLK_A LOW-to-HIGH transition.
2. After the bypass operation is completed, the $\overline{BYP}_B$ goes from LOW-to-HIGH; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

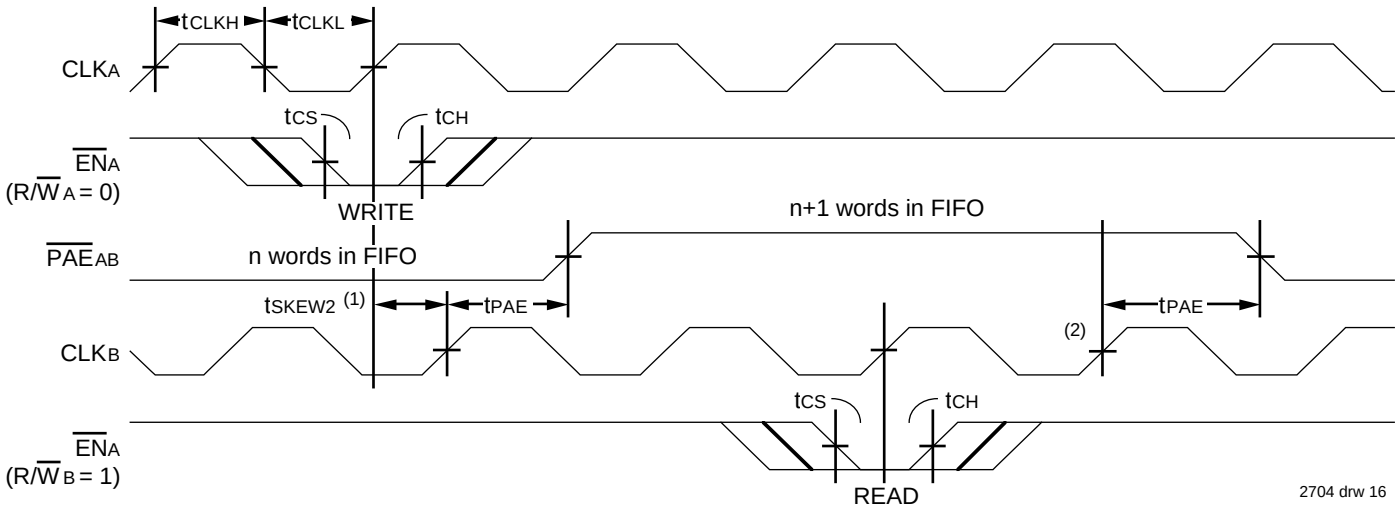
Figure 10. A→B Bypass Timing



2704 drw 15

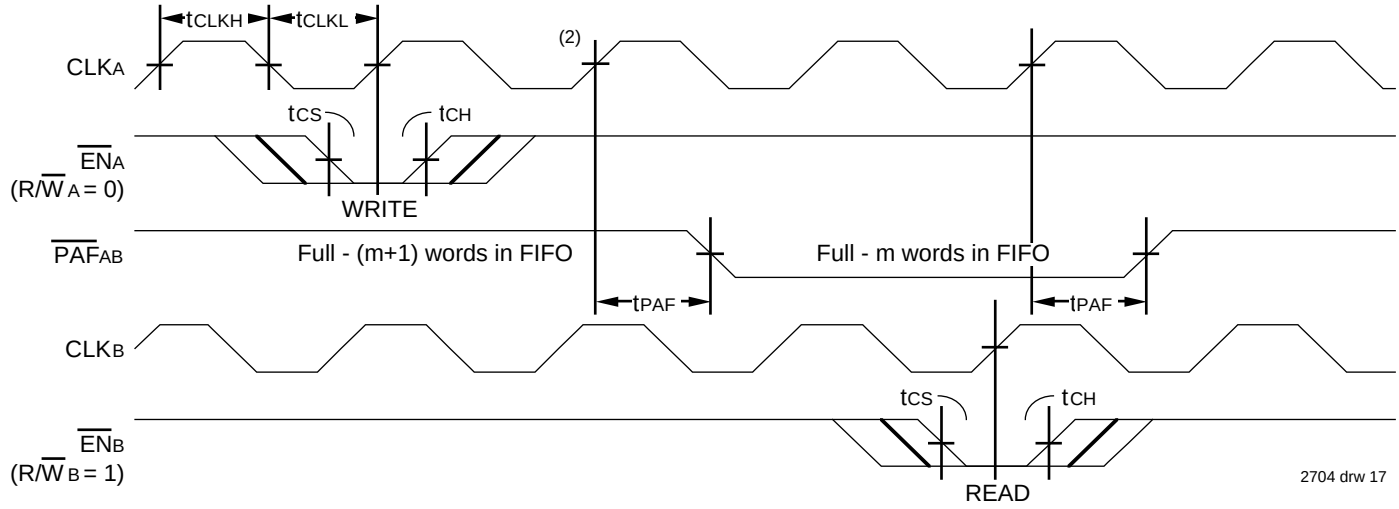
NOTES:
1. When $\overline{CS}_A$ is brought HIGH, A→B Bypass mode will switch to FIFO mode on the following CLK_A going LOW-to-HIGH.
2. After the bypass operation is completed, the $\overline{BYP}_B$ goes from LOW-to-HIGH; this will reset all bypass flags. The bypass path becomes available for the next bypass operation.
3. When A-side changed from bypass mode into FIFO mode, B-side only has one cycle to read the bypass data. On the next cycle, B-side will be forced back to FIFO mode.

Figure 11. B→A Bypass Timing



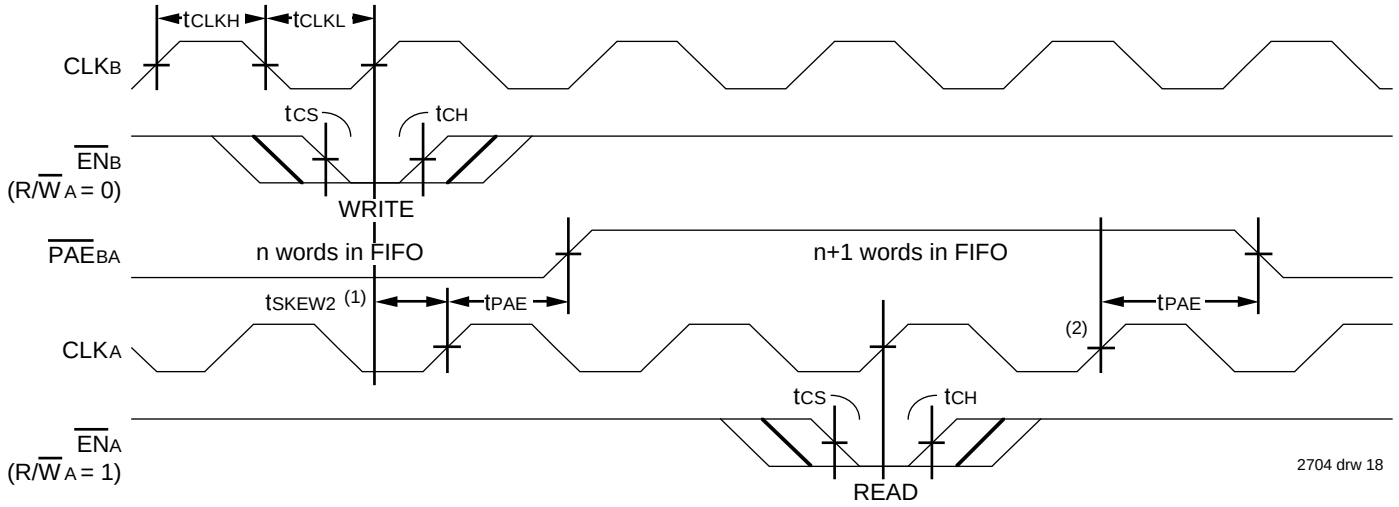
NOTES:
1. t_{SKEW2} the minimum time between a rising CLK_A edge and a rising CLK_B edge for $\overline{PAE}_{AB}$ to change during that clock cycle. If the time between the rising edge of CLK_A and the rising edge of CLK_B is less than t_{SKEW}, then $\overline{PAE}_{AB}$ may not go HIGH until the next CLKB rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n + 1) words in the FIFO when $\overline{PAE}$ goes LOW.

Figure 12. A→B Programmable Almost-Empty Flag Timing



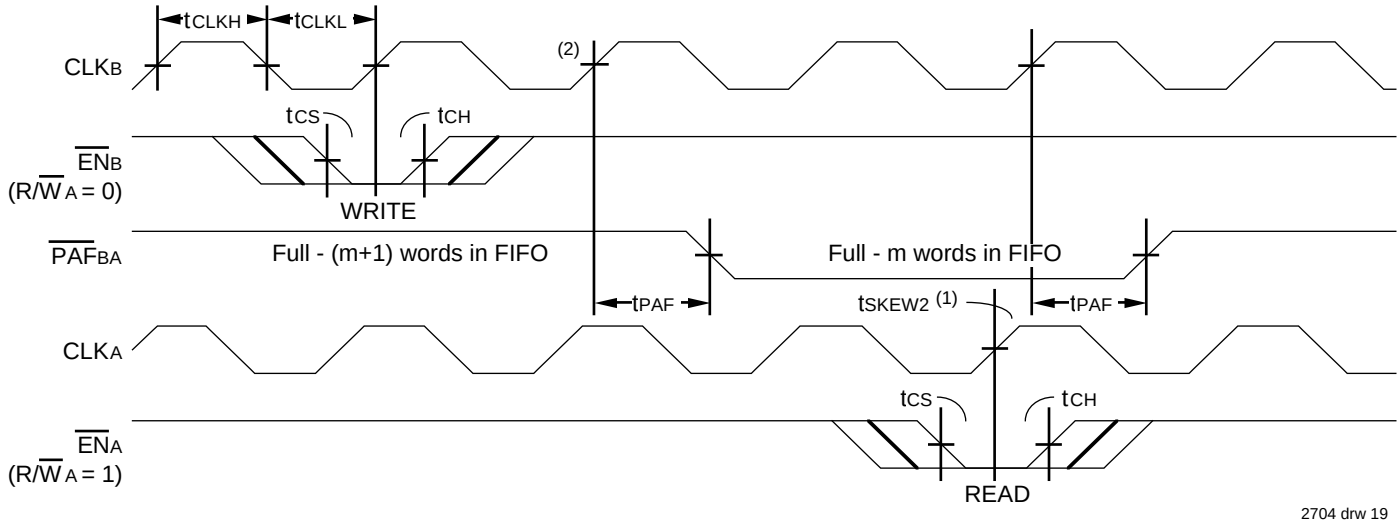
NOTES:
1. t_{SKEW2} is the minimum time between a rising CLK_B edge and a rising CLK_A edge for $\overline{PAF}_{AB}$ to change during that clock cycle. If the time between the rising edge of CLK_B and the rising edge of CLK_A is less than t_{SKEW2}, then $\overline{PAF}_{AB}$ may not go HIGH until the next CLK_A rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when $\overline{PAF}$ goes LOW.

Figure 13. A→B Programmable Almost-Full Flag Timing



NOTES:
1. t_{SKEW2} is the minimum time between a rising CLK_B edge and a rising CLK_A edge for $\overline{PAE}_{BA}$ to change during that clock cycle. If the time between the rising edge of CLK_B and the rising edge of CLK_A is less than t_{SKEW2}, then $\overline{PAE}_{BA}$ may not go HIGH until the next CLK_A rising edge.
2. If a read is performed on this rising edge of the read clock, there will be Empty + (n - 1) words in the FIFO when $\overline{PAE}$ goes LOW.

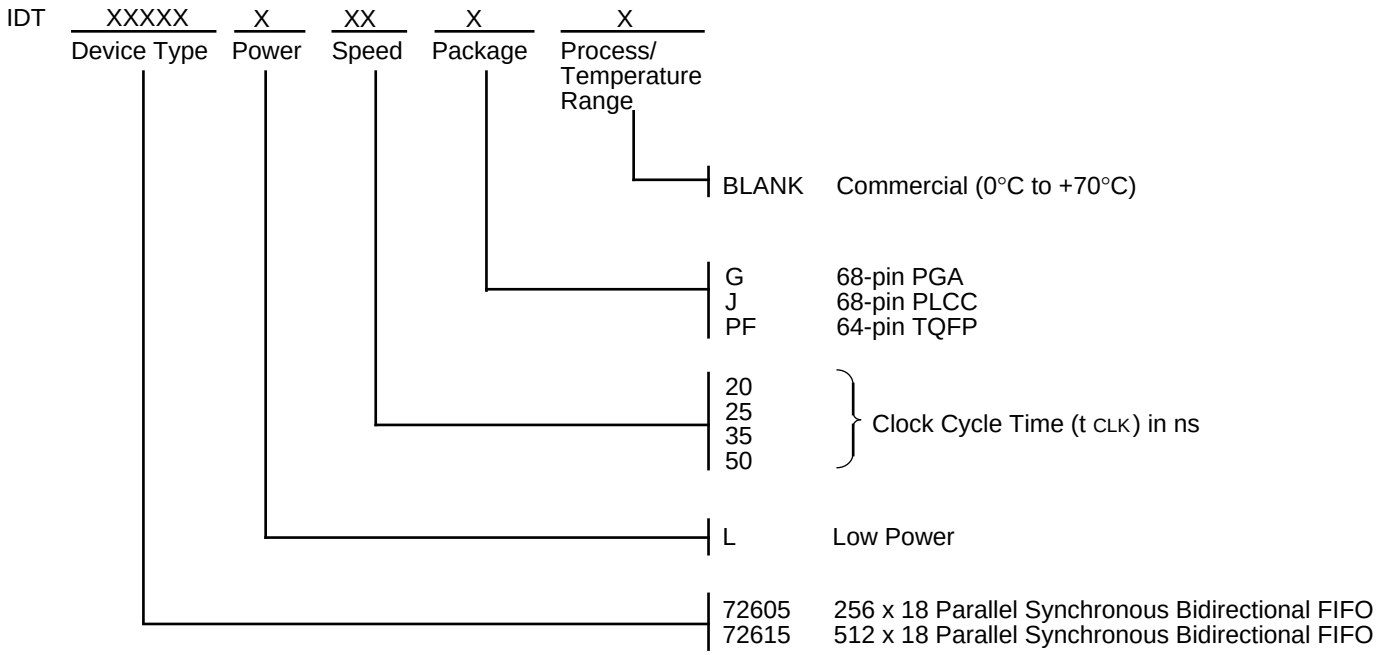
Figure 14. B→A Programmable Almost-Empty Flag Timing



NOTES:
1. t_{SKEW2} is the minimum time between a rising CLK_B edge and a rising CLK_A edge for $\overline{PAF}_{BA}$ to change during that clock cycle. If the time between the rising edge of CLK_B and the rising edge of CLK_A is less than t_{SKEW2}, then $\overline{PAF}_{BA}$ may not go HIGH until the next CLK_A rising edge.
2. If a write is performed on this rising edge of the write clock, there will be Full - (m + 1) words in the FIFO when $\overline{PAF}$ goes LOW.

Figure 15. B→A Programmable Almost-Full Flag Timing

ORDERING INFORMATION



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