

UTC UM602/A LINEAR INTEGRATED CIRCUIT

DUAL OPERATIONAL AMPLIFIER-DUAL COMPARATOR AND ADJUSTABLE VOLTAGE REFERENCE

DESCRIPTION

The UTC UM602/A is a monolithic IC that includes two op-amps, two comparators and a precision voltage reference. This device is offering space and cost saving in many applications like power supply management or data acquisition systems.

OPERATIONAL AMPLIFIERS

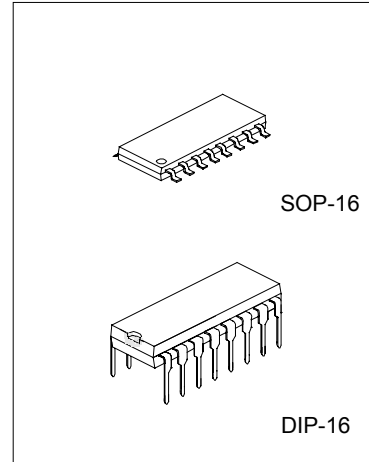
- *Low supply current: 200 μ A/amp.
- *Medium speed: 2.1MHz
- *Low level output voltage close to V_{cc} : 0.1V typ.
- *Input common mode voltage range includes ground

COMPARATORS

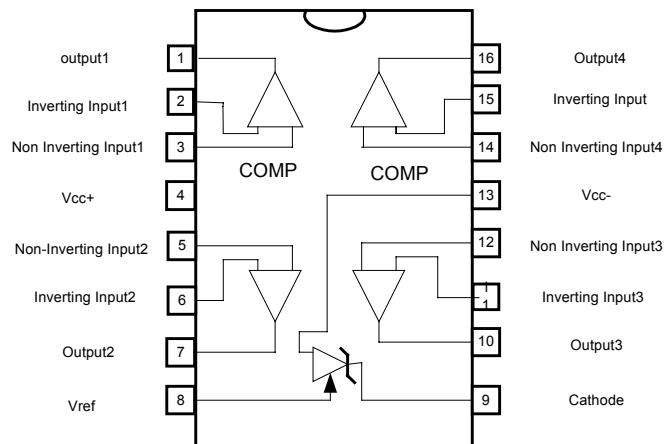
- *Low supply current: 200 μ A/amp. ($V_{cc}=5V$)
- *Input common mode voltage range includes ground
- *Low output saturation voltage: 250mV($I_o=4mA$)

REFERENCE

- *Adjustable output voltage: V_{ref} to 32V
- *Sink current capability: 1 to 100mA
- *1% and 0.4% voltage precision
- *LATCH-UP immunity



PIN CONFIGURATION



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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V _{cc}	36	V
Differential Input Voltage	V _{id}	36	V
Input voltage	V _i	-0.3 to +36	V
Operating Free-air Temperature Range	T _{oper}	-40 to +125	°C
Maximum Junction Temperature	T _j	150	°C
Thermal Resistance Junction to Ambient (SOP package)		150	°C/W

ELECTRICAL CHARACTERISTICS (V_{cc}⁺=5V, V_{cc}⁻=0V, T_{amb}=25°C, unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Total Supply Current T _{min.} < T _{amb} < T _{max.}	I _{cc}		0.8	1.5 2	mA

OPERATIONAL AMPLIFIERS

(V_{cc}⁺=5V, V_{cc}⁻=GND, R₁ connected to V_{cc}/2, T_{amb}=25°C, unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Offset Voltage T _{min.} ≤ T _{amb} ≤ T _{max.}	V _{io}		1	4.5 6.5	mV
Input Offset Voltage Drift	DV _{io}		10		μV/°C
Input Bias Current T _{min.} ≤ T _{amb} ≤ T _{max.}	I _{ib}		20	100 200	nA
Input Offset Current T _{min.} ≤ T _{amb} ≤ T _{max.}	I _{io}		5	20 40	nA
Large Signal Voltage Gain R ₁ =10k, V _{cc} ⁺ =30V V _o =5V to 25V T _{min.} ≤ T _{amb} ≤ T _{max.}	A _{vd}	50 25	100		V/mV
Supply Voltage Rejection Ratio V _{cc} =5V to 30V	SVR	80	100		dB
Input Common Mode Voltage Range T _{min.} ≤ T _{amb} ≤ T _{max.}	V _{icm}	(V _{cc} ⁻) to (V _{cc} ⁺) -1.8 (V _{cc} ⁻) to (V _{cc} ⁺) -2.2			V
Common Mode Rejection Ratio V _{cc} ⁺ =30V, V _{icm} =0V to (V _{cc} ⁺)-1.8V	CMR	70	90		dB
Output Short Circuit Current V _{id} =±1V, V _o =2.5V Source Sink	I _{sc}	3 3	6 6		mA
High Level Output Voltage R _L =10kΩ V _{cc} ⁺ =30V T _{min.} ≤ T _{amb} ≤ T _{max.}	V _{oH}	27 26	28		V
Low Level Output Voltage R _L =10kΩ T _{min.} ≤ T _{amb} ≤ T _{max.}	V _{oL}		100	150 210	mV
Slew Rate V _{cc} =±15V V _i =±10V, R _L =10KΩ, C _L =100pF	SR	1.6	2		V/μs
Gain Bandwidth Product R _L =10KΩ, C _L =100pF, f=100kHz	GBP	1.4	2.1		MHz

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PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Phase Margin $R_L=10K\Omega, C_L=100pF$	Φ_m		45		Degrees
Total Harmonic Distortion	THD		0.05		%
Equivalent Input Noise Voltage $f=1kHz$	en		29		$\frac{nV}{\sqrt{Hz}}$
Channel Separation	Cs		120		dB

COMPARATORS ($V_{CC}^+=+5V$, $V_{CC}=\text{Ground}$, $T_{amb}=25^\circ C$, unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Input Offset Voltage $T_{min.} \leq T_{amb} \leq T_{max.}$	V_{io}			5 9	mV
Input Offset Current $T_{min.} \leq T_{amb} \leq T_{max.}$	I_{io}			50 150	nA
Input Bias Current $T_{min.} \leq T_{amb} \leq T_{max.}$	I_{ib}			250 400	nA
High Level Output Voltage $V_{id}=1V, V_{CC}=V_o+30V$ $T_{min.} \leq T_{amb} \leq T_{max.}$	I_{OH}		0.1	1	nA μA
Low Level Output Voltage $V_{id}=-1V, I_{sink}=4mA$ $T_{min.} \leq T_{amb} \leq T_{max.}$	V_{OL}		250	400 700	mV
Large Signal Voltage Gain $R_1=15K, V_{CC}=15V, V_o=1 \text{ to } 11V$	A_{vd}		200		V/mV
Output Sink Current $V_{id}=-1V, V_o=1.5V$	I_{sink}	6	16		mA
Input Common Mode Voltage Range $T_{min.} \leq T_{amb} \leq T_{max.}$	V_{icm}	0 0		$V_{CC}^+ - 1.5$ $V_{CC}^+ - 2$	V
Differential Input Voltage	V_{id}			V_{CC}^+	V
Response Time –(note1) $R_1=5.1k \text{ to } V_{CC}^+, V_{ref}=1.4V$	t_{re}		1.3		μs
Large Signal Response Time $V_{ref}=1.4V, V_i=TTL, R_1=5.1k \text{ to } V_{CC}^+$	t_{rel}		300		ns

Note1: The response time specified is for 100mV input step with 5mV overdrive.
For larger overdrive signals, 300ns can be obtained.

VOLTAGE REFERENCE

PARAMETER	SYMBOL	VALUE	UNIT
Cathode to Anode Voltage	V_{KA}	V_{ref} to 36	V
Cathode Current	I_K	1 to 100	mA

ELECTRICAL CHARACTERISTICS ($T_{amb}=25^\circ C$, unless otherwise specified)

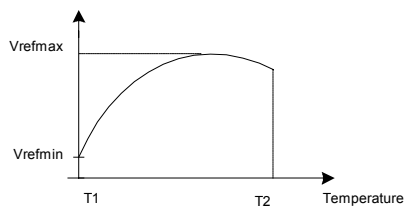
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reference Input Voltage – (figure 1) – $T_{amb}=25^\circ C$	V_{ref}	UM602, $V_{KA}=V_{ref}, I_K=10mA$ UM602A, $V_{KA}=V_{ref}, I_K=10mA$	2.475 2.490	2.500 2.500	2.525 2.510	V

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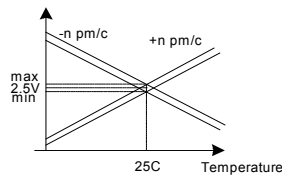
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Reference Input Voltage Deviation Over Temperature Range – (figure 1, note 1)	ΔV_{ref}	$V_{KA}=V_{ref}$, $I_K=10mA$, $T_{min.} \leq T_{amb} \leq T_{max.}$		7	30	mV
Temperature Coefficient of Reference Input Voltage-(note 2)	$\frac{\Delta V_{ref}}{\Delta T}$	$V_{KA}=V_{ref}$, $I_K=10mA$, $T_{min.} \leq T_{amb} \leq T_{max.}$		± 22	± 100	ppm/°C
Ratio of Change in Reference Input Voltage to Change in Cathode to Anode Voltage –(figure2)	$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	$I_K=10mA$, $\Delta V_{KA}=36$ to $3V$		-1.1	-2	mV/V
Reference Input Current –(figure2)	I_{ref}	$I_K=10mA$, $R1=10k\Omega$, $R2=\infty$ $T_{amb}=25^\circ C$ $T_{min.} \leq T_{amb} \leq T_{max.}$		1.5	2.5 3	μA
Reference Input Current Deviation Over Temperature Range-(figure 2)	ΔI_{ref}	$I_K=10mA$, $R1=10k\Omega$, $R2=\infty$, $T_{min.} \leq T_{amb} \leq T_{max.}$		0.5	1	μA
Minimum Cathode Current for Regulation-(figure1)	I_{min}	$V_{KA}=V_{ref}$		0.5	1	mA
Off-State Cathode Current-(figure 3)	I_{off}			180	500	nA

Notes: 1. ΔV_{ref} is defined as the difference between the maximum and minimum values obtained over the full temperature range.

$$\Delta V_{ref} = V_{refmax} - V_{refmin}$$



2. The temperature coefficient is defined as the slopes (positive and negative) of the voltage vs temperature limits within which the reference voltage is guaranteed.



3. The dynamic Impedance is defined as $|Z_{KA}| = \frac{\Delta V_{KA}}{\Delta I_K}$

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Figure 1: Test Circuit for $V_{KA}=V_{ref}$

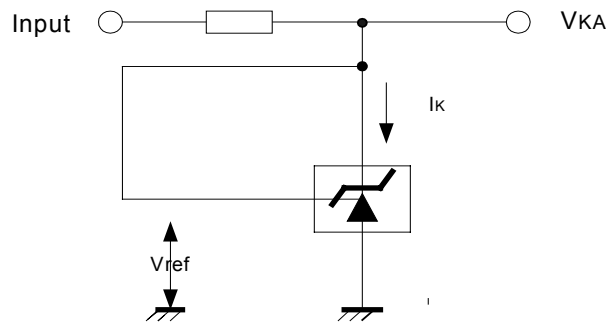


Figure 2: Test Circuit for $V_{KA}>V_{ref}$

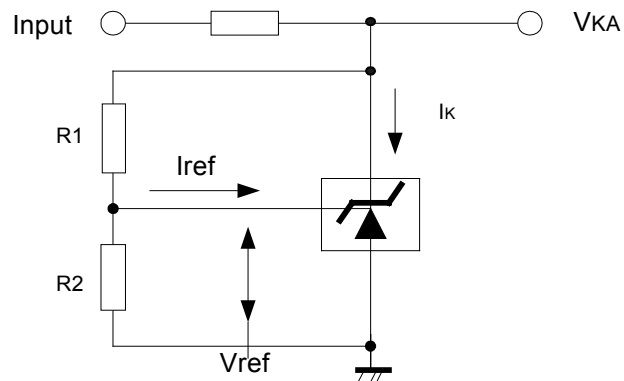
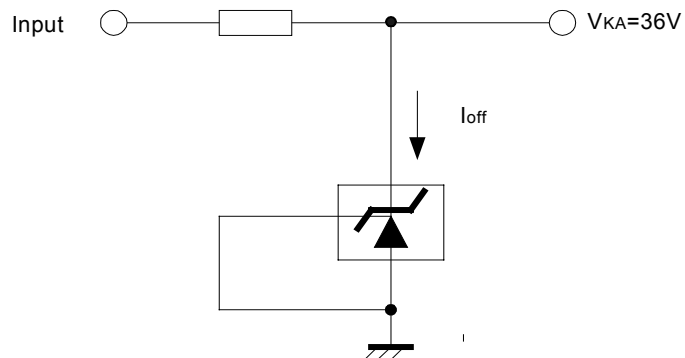


Figure 3: Test Circuit for I_{off}



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