16-Rail Power Supply Sequencer and Monitor with ACPI Support

Check for Samples: UCD90160

FEATURES

- **Monitor and Sequence 16 Voltage Rails**
  - **All Rails Sampled Every 400 µs**
  - **12-bit ADC With 2.5-V, 0.5% Internal V_{REF}**
  - **Sequence Based on Time, Rail and Pin Dependencies**
  - **Four Programmable Undervoltage and Overvoltage Thresholds per Monitor**
- **Nonvolatile Error and Peak-Value Logging per Monitor (up to 12 Fault Detail Entries)**
- **Closed-Loop Margining for 10 Rails**
  - **Margin Output Adjusts Rail Voltage to Match User-Defined Margin Thresholds**
- **Programmable Watchdog Timer and System Reset**
- **Pin Selected Rail States for ACPI Support**
- **Flexible Digital I/O Configuration**
- **Multiphase PWM Clock Generator**
  - **Clock Frequencies From 15.259 kHz to 125 MHz**
  - **Capability to Configure Independent Clock Outputs for Synchronizing Switch-Mode Power Supplies**
- **JTAG and I^2C/SMBus/ PMBus™ Interfaces**

APPLICATIONS

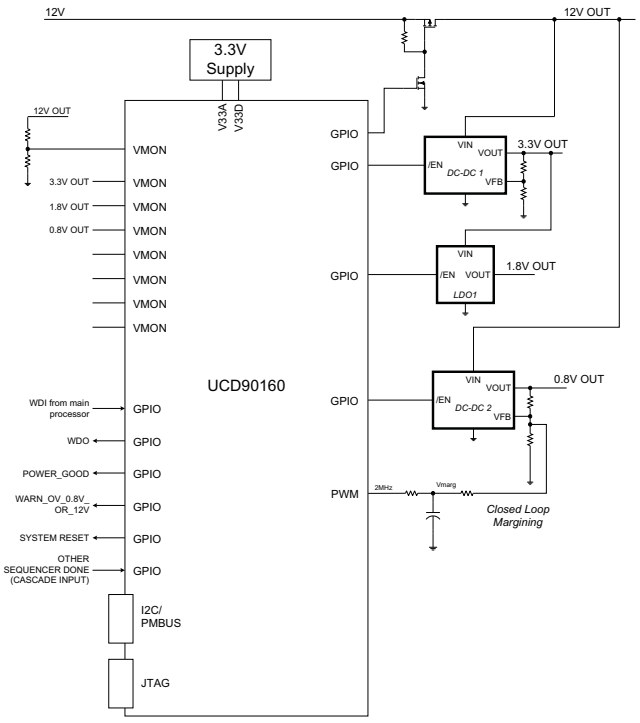
- **Industrial / ATE**
- **Telecommunications and Networking Equipment**
- **Servers and Storage Systems**
- **Any System Requiring Sequencing and Monitoring of Multiple Power Rails**

DESCRIPTION

The UCD90160 is a 16-rail PMBus/I^2C addressable power-supply sequencer and monitor. The device integrates a 12-bit ADC for monitoring up to 16 power-supply voltage inputs. Twenty-six GPIO pins can be used for power supply enables, power-on reset signals, external interrupts, cascading, or other system functions. Twelve of these pins offer PWM functionality. Using these pins, the UCD90160 offers support for margining, and general-purpose PWM functions.

Specific power states can be achieved using the Pin-Selected Rail States feature. This feature allows with the use of up to 3 GPIs to enable and disable any rail. This is useful for implementing system low-power modes and the Advanced Configuration and Power Interface (ACPI) specification that is used for hardware devices.

The TI Fusion Digital Power™ designer software is provided for device configuration. This PC-based graphical user interface (GUI) offers an intuitive interface for configuring, storing, and monitoring all system operating parameters.



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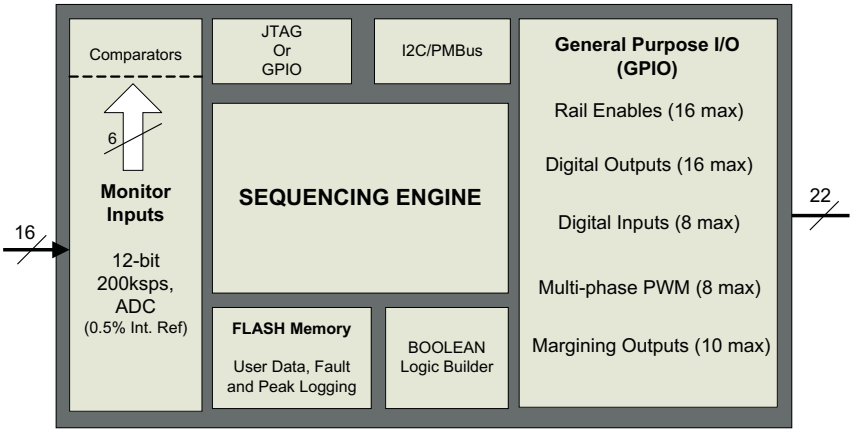
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



64-pin QFN

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
Voltage applied at V33D to DV_{SS}		–0.3 to 3.8	V
Voltage applied at V33A to AV_{SS}		–0.3 to 3.8	V
Voltage applied to any other pin (2)		–0.3 to (V33A + 0.3)	V
Storage temperature (T_{stg})		–40 to 150	°C
ESD rating	Human-body model (HBM)	2.5	kV
	Charged-device model (CDM)	750	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages referenced to V_{SS}

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THERMAL INFORMATION

THERMAL METRIC(1)		UCD90160 RGC 64 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance(2)	26.4	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance (3)	21.2	
θ_{JB}	Junction-to-board thermal resistance (4)	1.7	
ψ_{JT}	Junction-to-top characterization parameter (5)	0.7	
ψ_{JB}	Junction-to-board characterization parameter (6)	8.8	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance (7)	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage during operation (V_{33D}, V_{33DIO}, V_{33A})	3	3.3	3.6	V
Operating free-air temperature range, T_A	–40		110	°C
Junction temperature, T_J			125	°C

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ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SUPPLY CURRENT						
I_{V33A}	Supply current(1)	V_{V33A} = 3.3 V		8		mA
I_{V33DIO}		V_{V33DIO} = 3.3 V		2		mA
I_{V33D}		V_{V33D} = 3.3 V		40		mA
I_{V33D}		V_{V33D} = 3.3 V, storing configuration parameters in flash memory		50		mA
ANALOG INPUTS (MON1–MON16)						
V_{MON}	Input voltage range	MON1–MON13	0		2.5	V
		MON14–MON16	0.2		2.5	V
INL	ADC integral nonlinearity		–4		4	LSB
DNL	ADC differential nonlinearity		-2		2	LSB
I_{lkg}	Input leakage current	3 V applied to pin			100	nA
I_{OFFSET}	Input offset current	1-kΩ source impedance	–5		5	µA
R_{IN}	Input impedance	MON1–MON13, ground reference	8			MΩ
		MON14–MON16, ground reference	0.5	1.5	3	MΩ
C_{IN}	Input capacitance				10	pF
$t_{CONVERT}$	ADC sample period	16 voltages sampled, 3.89 µsec/sample		400		µsec
V_{REF}	ADC 2.5 V, internal reference accuracy	0°C to 125°C	–0.5		0.5	%
		–40°C to 125°C	–1		1	%
ANALOG INPUT (PMBUS_ADDRx)						
I_{BIAS}	Bias current for PMBus Addr pins		9		11	µA
V_{ADDR_OPEN}	Voltage – open pin	PMBUS_ADDR0, PMBUS_ADDR1 open	2.26			V
V_{ADDR_SHORT}	Voltage – shorted pin	PMBUS_ADDR0, PMBUS_ADDR1 short to ground			0.124	V
DIGITAL INPUTS AND OUTPUTS						
V_{OL}	Low-level output voltage	I_{OL} = 6 mA(2), V_{33DIO} = 3 V			Dgnd + 0.25	V
V_{OH}	High-level output voltage	I_{OH} = –6 mA(3), V_{33DIO} = 3 V	V_{33DIO} – 0.6			V
V_{IH}	High-level input voltage	V_{33DIO} = 3 V	2.1		3.6	V
V_{IL}	Low-level input voltage	V_{33DIO} = 3.5 V			1.4	V
MARGINING OUTPUTS						
T_{PWM_FREQ}	MARGINING-PWM frequency	FPWM1-8	15.260		125000	kHz
		PWM3-4	0.001		7800	
$DUTY_{PWM}$	MARGINING-PWM duty cycle range		0		100	%
SYSTEM PERFORMANCE						
V_{DD}Slew	Minimum V_{DD} slew rate	V_{DD} slew rate between 2.3 V and 2.9 V	0.25			V/ms
V_{RESET}	Supply voltage at which device comes out of reset	For power-on reset (POR)			2.4	V
t_{RESET}	Low-pulse duration needed at $\overline{RESET}$ pin	To reset device during normal operation	2			µS
f(PCLK)	Internal oscillator frequency	T_A = 125°C, T_A = 25°C	240	250	260	MHz
$t_{retention}$	Retention of configuration parameters	T_J = 25°C	100			Years
Write_Cycles	Number of nonvolatile erase/write cycles	T_J = 25°C	20			K cycles

(1) Typical supply current values are based on device programmed but not configured, and no peripherals connected to any pins.
(2) The maximum total current, I_{OL}max, for all outputs combined, should not exceed 12 mA to hold the maximum voltage drop specified.
(3) The maximum total current, I_{OH}max, for all outputs combined, should not exceed 48 mA to hold the maximum voltage drop specified.

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PMBus/SMBus/I²C

The timing characteristics and timing diagram for the communications interface that supports I²C, SMBus and PMBus is shown below.

I²C/SMBus/PMBus TIMING REQUIREMENTS

T_A = –40°C to 85°C, 3 V < V_{DD} < 3.6 V; typical values at T_A = 25°C and V_{CC} = 2.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FSMB	SMBus/PMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		400	kHz
FI2C	I²C operating frequency	Slave mode, SCL 50% duty cycle	10		400	kHz
$t_{(BUF)}$	Bus free time between start and stop		4.7			µs
$t_{(HD:STA)}$	Hold time after (repeated) start		0.26			µs
$t_{(SU:STA)}$	Repeated-start setup time		0.26			µs
$t_{(SU:STO)}$	Stop setup time		0.26			µs
$t_{(HD:DAT)}$	Data hold time	Receive mode	0			ns
$t_{(SU:DAT)}$	Data setup time		50			ns
$t_{(TIMEOUT)}$	Error signal/detect	See (1)			35	ms
$t_{(LOW)}$	Clock low period		0.5			µs
$t_{(HIGH)}$	Clock high period	See (2)	0.26		50	µs
$t_{(LOW:SEXT)}$	Cumulative clock low slave extend time	See (3)			25	ms
t_f	Clock/data fall time	See (4)			120	ns
t_r	Clock/data rise time	See (5)			120	ns

(1) The device times out when any clock low exceeds $t_{(TIMEOUT)}$.
(2) $t_{(HIGH)}$, Max, is the minimum bus idle time. SMBC = SMBD = 1 for t > 50 ms causes reset of any transaction that is in progress. This specification is valid when the NC_SMB control bit remains in the default cleared state (CLK[0] = 0).
(3) $t_{(LOW:SEXT)}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
(4) Fall time t_f = 0.9 VDD to (V_{IL}MAX – 0.15)
(5) Rise time t_r = (V_{IL}MAX – 0.15) to (V_{IH}MIN + 0.15)

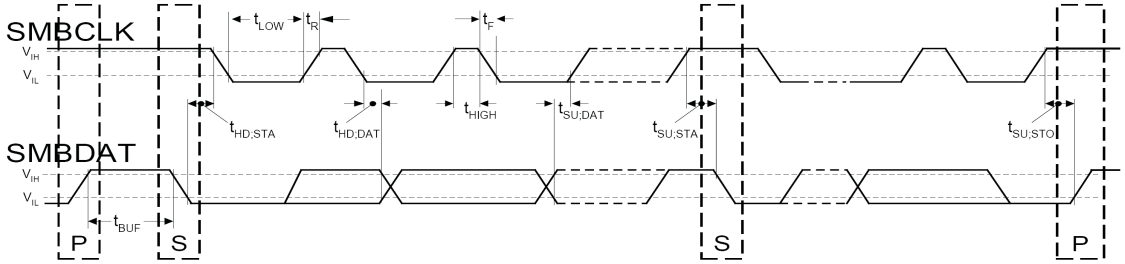

Figure 1. I²C/SMBus Timing Diagram

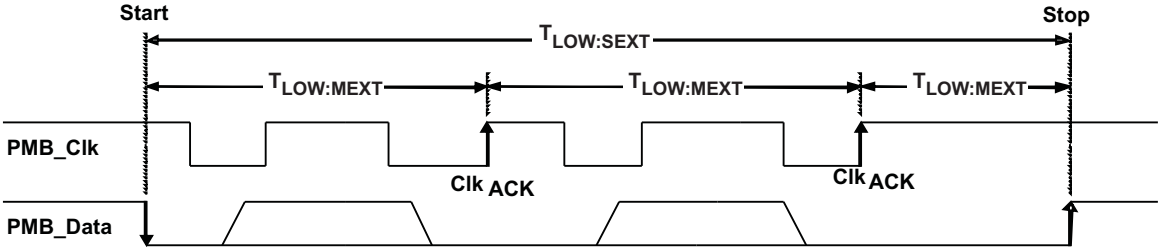

Figure 2. Bus Timing in Extended Mode

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DEVICE INFORMATION

Figure 3. UCD90160 PIN ASSIGNMENT

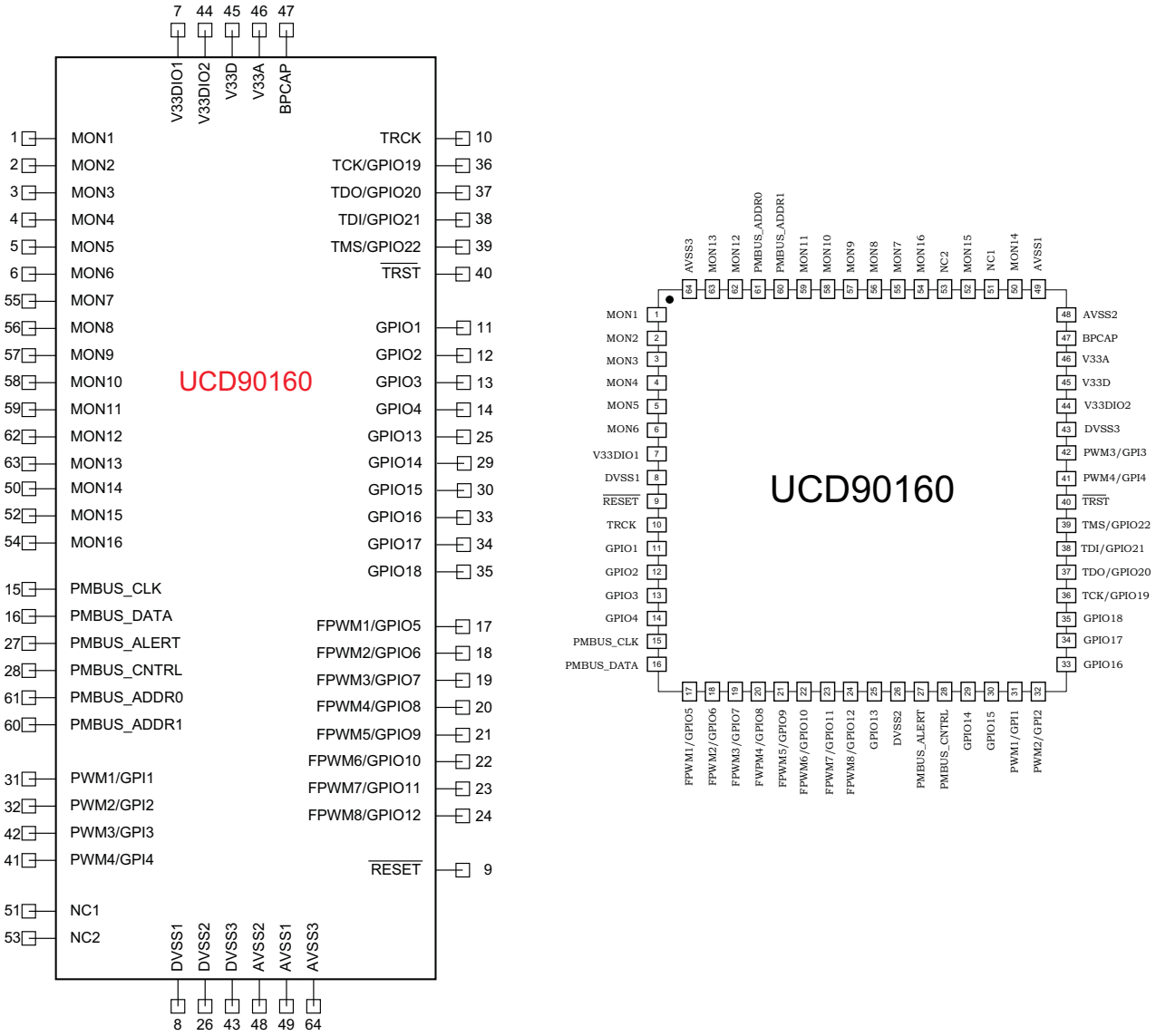

Table 1. PIN FUNCTIONS

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
ANALOG MONITOR INPUTS			
MON1	1	I	Analog input (0 V–2.5 V)
MON2	2	I	Analog input (0 V–2.5 V)
MON3	3	I	Analog input (0 V–2.5 V)
MON4	4	I	Analog input (0 V–2.5 V)
MON5	5	I	Analog input (0 V–2.5 V)
MON6	6	I	Analog input (0 V–2.5 V)
MON7	55	I	Analog input (0 V–2.5 V)
MON8	56	I	Analog input (0 V–2.5 V)

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Table 1. PIN FUNCTIONS (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
MON9	57	I	Analog input (0 V–2.5 V)
MON10	58	I	Analog input (0 V–2.5 V)
MON11	59	I	Analog input (0 V–2.5 V)
MON12	62	I	Analog input (0 V–2.5 V)
MON13	63	I	Analog input (0 V–2.5 V)
MON14	50	I	Analog input (0.2 V–2.5 V)
MON15	52	I	Analog input (0.2 V–2.5 V)
MON16	54	I	Analog input (0.2 V–2.5 V)
GPIO			
GPIO1	11	I/O	General-purpose discrete I/O
GPIO2	12	I/O	General-purpose discrete I/O
GPIO3	13	I/O	General-purpose discrete I/O
GPIO4	14	I/O	General-purpose discrete I/O
GPIO13	25	I/O	General-purpose discrete I/O
GPIO14	29	I/O	General-purpose discrete I/O
GPIO15	30	I/O	General-purpose discrete I/O
GPIO16	33	I/O	General-purpose discrete I/O
GPIO17	34	I/O	General-purpose discrete I/O
GPIO18	35	I/O	General-purpose discrete I/O
PWM OUTPUTS			
FPWM1/GPIO5	17	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM2/GPIO6	18	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM3/GPIO7	19	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM4/GPIO8	20	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM5/GPIO9	21	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM6/GPIO10	22	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM7/GPIO11	23	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
FPWM8/GPIO12	24	I/O/PWM	PWM (15.259 kHz to 125 MHz) or GPIO
PWM1/GPI1	31	I/PWM	Fixed 10-kHz PWM output or GPI
PWM2/GPI2	32	I/PWM	Fixed 1-kHz PWM output or GPI
PWM3/GPI3	42	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PWM4/GPI4	41	I/PWM	PWM (0.93 Hz to 7.8125 MHz) or GPI
PMBus COMM INTERFACE			
PMBUS_CLK	15	I/O	PMBus clock (must have pullup to 3.3 V)
PMBUS_DATA	16	I/O	PMBus data (must have pullup to 3.3 V)
PMBALERT#	27	O	PMBus alert, active-low, open-drain output (must have pullup to 3.3 V)
PMBUS_CNTRL	28	I	PMBus control
PMBUS_ADDR0	61	I	PMBus analog address input. Least-significant address bit
PMBUS_ADDR1	60	I	PMBus analog address input. Most-significant address bit
JTAG			
TRCK	10	O	Test return clock
TCK/GPIO19	36	I/O	Test clock or GPIO
TDO/GPIO20	37	I/O	Test data out or GPIO
TDI/GPIO21	38	I/O	Test data in (tie to V_{dd} with 10-kΩ resistor) or GPIO
TMS/GPIO22	39	I/O	Test mode select (tie to V_{dd} with 10-kΩ resistor) or GPIO
$\overline{\text{TRST}}$	40	I	Test reset – tie to ground with 10-kΩ resistor

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Table 1. PIN FUNCTIONS (continued)

PIN NAME	PIN NO.	I/O TYPE	DESCRIPTION
INPUT POWER AND GROUNDS			
$\overline{\text{RESET}}$	9		Active-low device reset input. Hold low for at least 2 µs to reset the device. Refer to the Device Reset section.
V33A	46		Analog 3.3-V supply. Refer to the Layout Guidelines section.
V33D	45		Digital core 3.3-V supply. Refer to the Layout Guidelines section.
V33DIO1	7		Digital I/O 3.3-V supply. Refer to the Layout Guidelines section.
V33DIO2	44		Digital I/O 3.3-V supply. Refer to the Layout Guidelines section.
BPCap	47		1.8-V bypass capacitor. Refer to the Layout Guidelines section.
AVSS1	49		Analog ground
AVSS2	48		Analog ground
AVSS3	64		Analog ground
DVSS1	8		Digital ground
DVSS2	26		Digital ground
DVSS3	43		Digital ground
QFP ground pad	NA		Thermal pad – tie to ground plane.

FUNCTIONAL DESCRIPTION

TI FUSION GUI

The Texas Instruments *Fusion Digital Power Designer* is provided for device configuration. This PC-based graphical user interface (GUI) offers an intuitive I^2C/PMBus interface to the device. It allows the design engineer to configure the system operating parameters for the application without directly using PMBus commands, store the configuration to on-chip nonvolatile memory, and observe system status (voltage, etc). *Fusion Digital Power Designer* is referenced throughout the data sheet as *Fusion GUI* and many sections include screen shots. The *Fusion GUI* can be downloaded from www.ti.com.

PMBUS INTERFACE

The PMBus is a serial interface specifically designed to support power management. It is based on the SMBus interface that is built on the I^2C physical specification. The UCD90160 supports revision 1.1 of the PMBus standard. Wherever possible, standard PMBus commands are used to support the function of the device. For unique features of the UCD90160, MFR_SPECIFIC commands are defined to configure or activate those features. These commands are defined in the UCD90xxx Sequencer and System Health Controller PMBUS Command Reference (SLVU352). The most current UCD90xxx PMBus Command Reference can be found within the TI Fusion Digital Power Designer software via the Help Menu (Help, Documentation & Help Center, Sequencers tab, Documentation section).

This document makes frequent mention of the PMBus specification. Specifically, this document is *PMBus Power System Management Protocol Specification Part II – Command Language*, Revision 1.1, dated 5 February 2007. The specification is published by the Power Management Bus Implementers Forum and is available from www.pmbus.org.

The UCD90160 is PMBus compliant, in accordance with the *Compliance* section of the PMBus specification. The firmware is also compliant with the SMBus 1.1 specification, including support for the SMBus ALERT function. The hardware can support either 100-kHz or 400-kHz PMBus operation.

THEORY OF OPERATION

Modern electronic systems often use numerous microcontrollers, DSPs, FPGAs, and ASICs. Each device can have multiple supply voltages to power the core processor, analog-to-digital converter or I/O. These devices are typically sensitive to the order and timing of how the voltages are sequenced on and off. The UCD90160 can sequence supply voltages to prevent malfunctions, intermittent operation, or device damage caused by improper power up or power down. Appropriate handling of under- and overvoltage faults can extend system life and improve long term reliability. The UCD90160 stores power supply faults to on-chip nonvolatile flash memory for aid in system failure analysis.

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System reliability can be improved through four-corner testing during system verification. During four-corner testing, the system is operated at the minimum and maximum expected ambient temperature and with each power supply set to the minimum and maximum output voltage, commonly referred to as margining. The UCD90160 can be used to implement accurate closed-loop margining of up to 10 power supplies.

The UCD90160 16-rail sequencer can be used in a PMBus- or pin-based control environment. The TI Fusion GUI provides a powerful but simple interface for configuring sequencing solutions for systems with between one and 16 power supplies using 16 analog voltage-monitor inputs, four GPIs and 22 highly configurable GPIOs. A rail includes voltage, a power-supply enable and a margining output. At least one must be included in a rail definition. Once the user has defined how the power-supply rails should operate in a particular system, analog input pins and GPIOs can be selected to monitor and enable each supply (Figure 4).

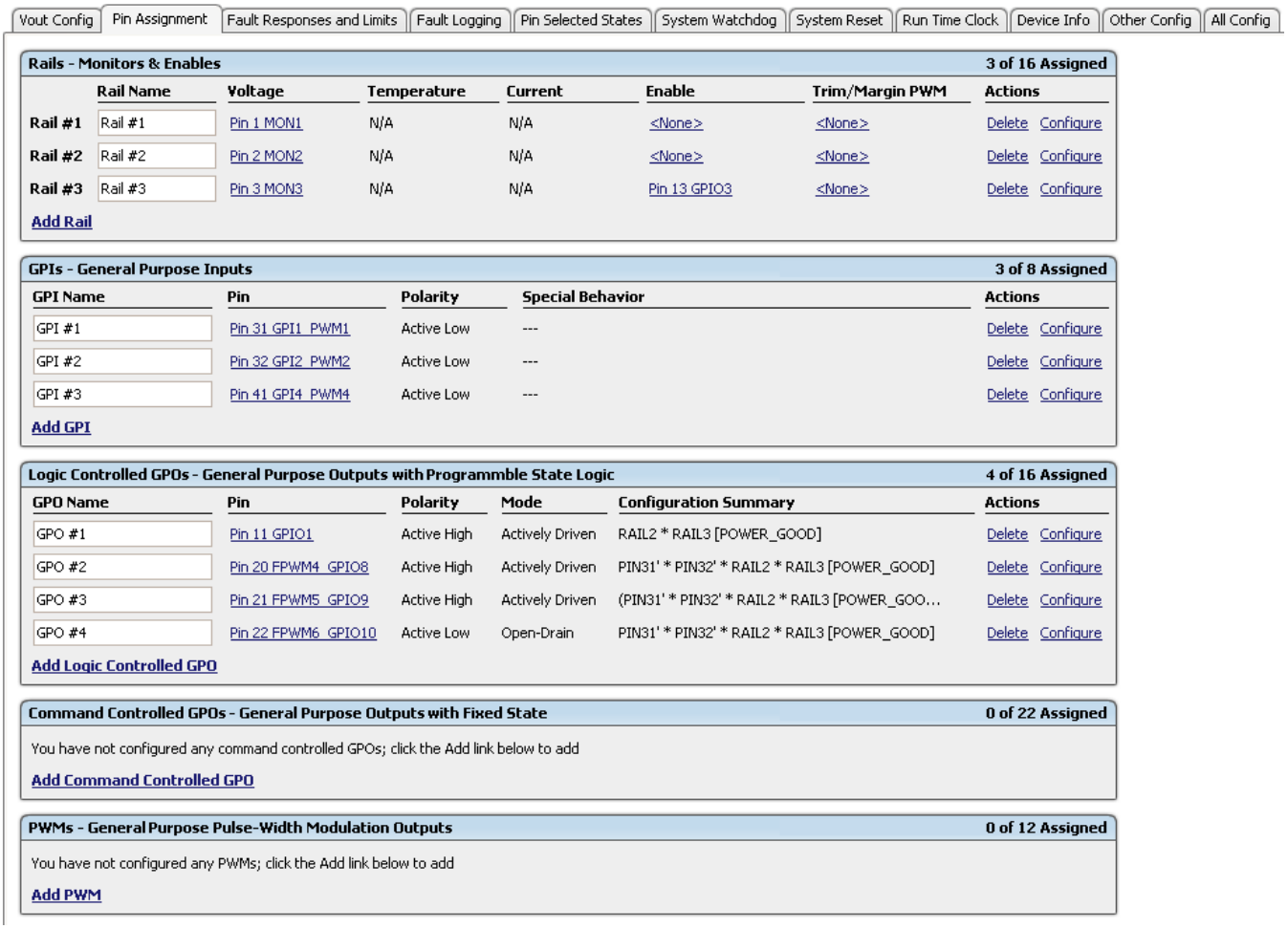

Figure 4. Fusion GUI Pin-Assignment Tab

After the pins have been configured, other key monitoring and sequencing criteria are selected for each rail from the Vout Config tab (Figure 5):

- Nominal operating voltage (Vout)
- Undervoltage (UV) and overvoltage (OV) warning and fault limits
- Margin-low and margin-high values
- Power-good on and power-good off limits
- PMBus or pin-based sequencing control (On/Off Config)
- Rails and GPIs for Sequence On dependencies
- Rails and GPIs for Sequence Off dependencies
- Turn-on and turn-off delay timing

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- Maximum time allowed for a rail to reach POWER_GOOD_ON or POWER_GOOD_OFF after being enabled or disabled
- Other rails to turn off in case of a fault on a rail (fault-shutdown slaves)

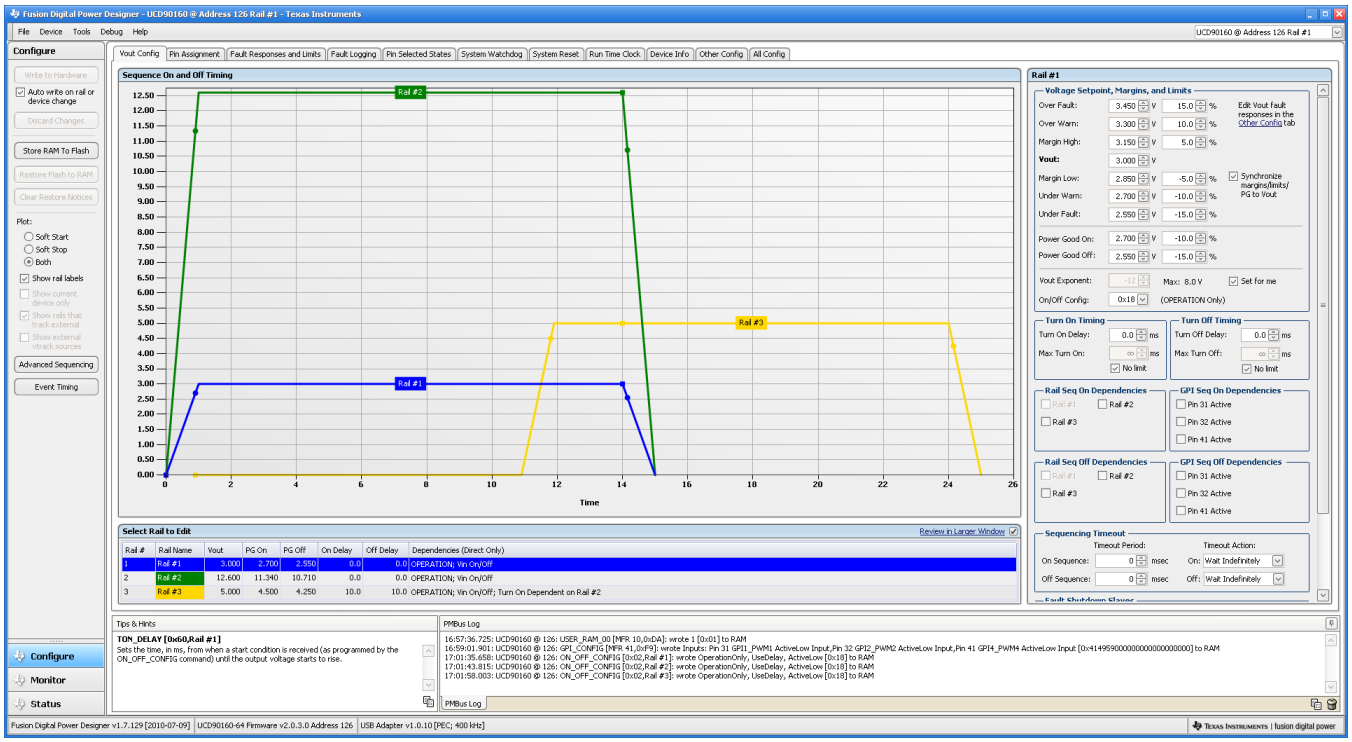

Figure 5. Fusion GUI V_{OUT}-Config Tab

The **Synchronize margins/limits/PG to Vout** checkbox is an easy way to change the nominal operating voltage of a rail and also update all of the other limits associated with that rail according to the percentages shown to the right of each entry.

The plot in the upper left section of Figure 5 shows a simulation of the overall sequence-on and sequence-off configuration, including the nominal voltage, the turnon and turnoff delay times, the power-good on and power-good off voltages and any timing dependencies between the rails.

After a rail voltage has reached its POWER_GOOD_ON voltage and is considered to be in regulation, it is compared against two UV and two OV thresholds in order to determine if a warning or fault limit has been exceeded. If a fault is detected, the UCD90160 responds based on a variety of flexible, user-configured options. Faults can cause rails to restart, shut down immediately, sequence off using turnoff delay times or shut down a group of rails and sequence them back on. Different types of faults can result in different responses.

Fault responses, along with a number of other parameters including user-specific manufacturing information and external scaling and offset values, are selected in the different tabs within the Configure function of the *Fusion GUI*. Once the configuration satisfies the user requirements, it can be written to device SRAM if *Fusion GUI* is connected to a UCD90160 using an I^2C/PMBus. SRAM contents can then be stored to data flash memory so that the configuration remains in the device after a reset or power cycle.

The *Fusion GUI* Monitor page has a number of options, including a device dashboard and a system dashboard, for viewing and controlling device and system status.

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Figure 6. Fusion GUI Monitor Page

The UCD90160 also has status registers for each rail and the capability to log faults to flash memory for use in system troubleshooting. This is helpful in the event of a power-supply or system failure. The status registers (Figure 7) and the fault log (Figure 8) are available in the *Fusion GUI*. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* (SLVU352) and the PMBus Specification for detailed descriptions of each status register and supported PMBus commands.

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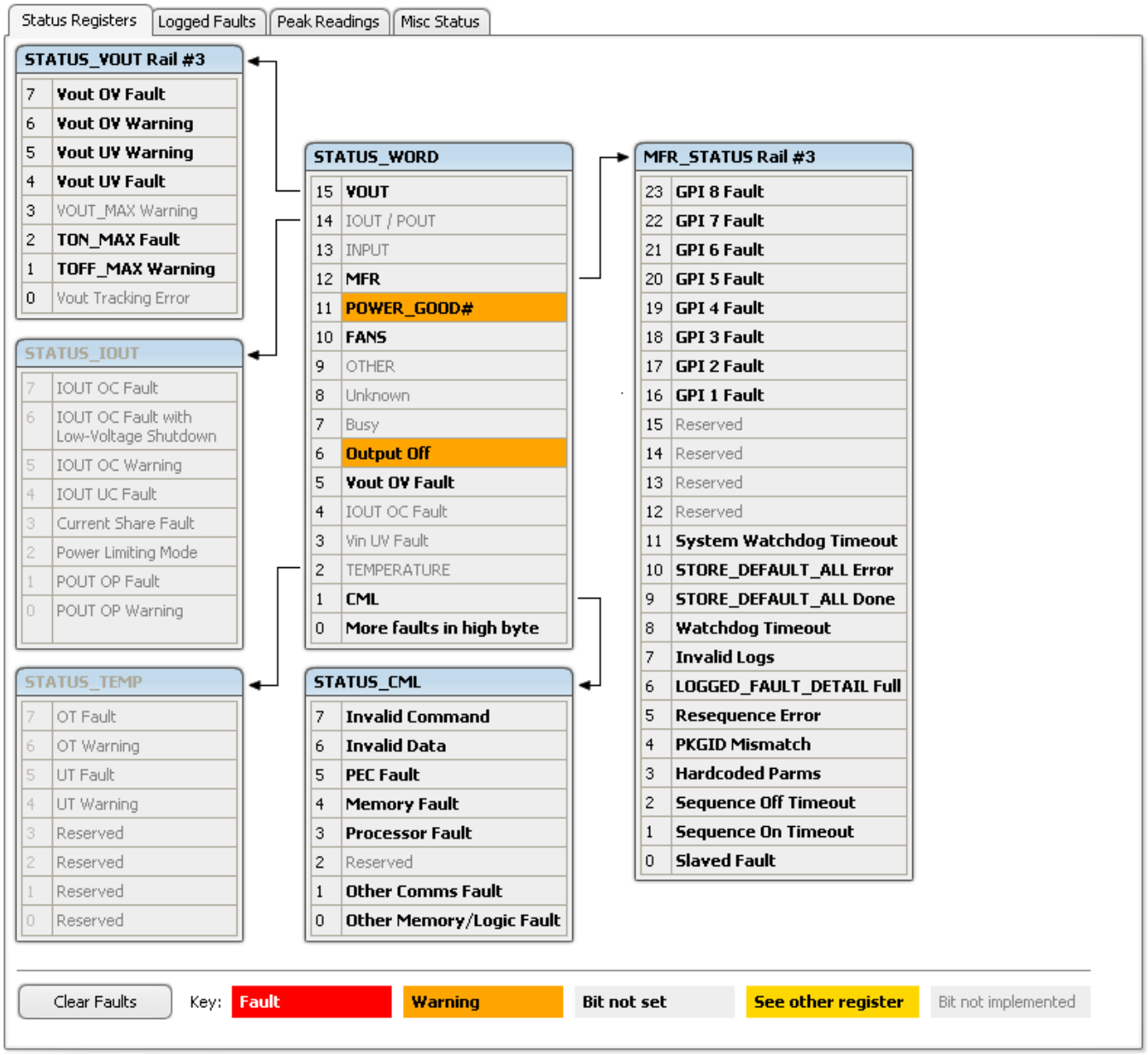

Figure 7. Fusion GUI Rail-Status Register

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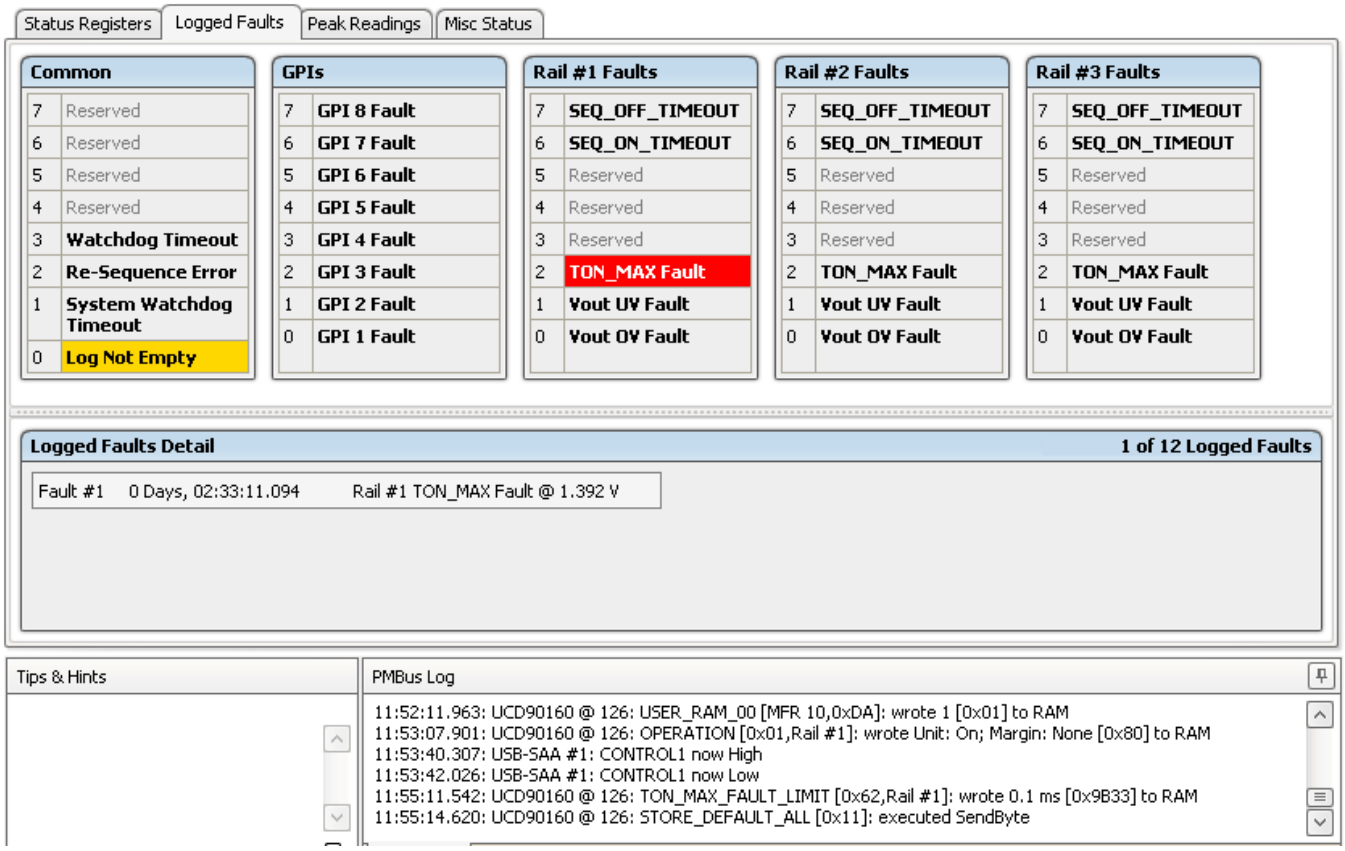

Figure 8. Fusion GUI Flash-Error Log (Logged Faults)

POWER-SUPPLY SEQUENCING

The UCD90160 can control the turn-on and turn-off sequencing of up to 16 voltage rails by using a GPIO to set a power-supply enable pin high or low. In PMBus-based designs, the system PMBus master can initiate a sequence-on event by asserting the PMBUS_CNTRL pin or by sending the OPERATION command over the I^2C serial bus. In pin-based designs, the PMBUS_CNTRL pin can also be used to sequence-on and sequence-off.

The auto-enable setting ignores the OPERATION command and the PMBUS_CNTRL pin. Sequence-on is started at power up after any dependencies and time delays are met for each rail. A rail is considered to be on or within regulation when the measured voltage for that rail crosses the power-good on (POWER_GOOD_ON(1)) limit. The rail is still in regulation until the voltage drops below power-good off (POWER_GOOD_OFF). In the case that there isn't voltage monitoring set for a given rail, that rail is considered ON if it is commanded on (either by OPERATION command, PMBUS CNTRL pin, or auto-enable) and (TON_DELAY + TON_MAX_FAULT_LIMIT) time passes. Also, a rail is considered OFF if that rail is commanded OFF and (TOFF_DELAY + TOFF_MAX_WARN_LIMIT) time passes

(1) In this document, configuration parameters such as Power Good On are referred to using Fusion GUI names. *The UCD90xxx Sequencer and System Health Controller PMBus Command Reference* name is shown in parentheses (POWER_GOOD_ON) the first time the parameter appears.

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Turn-on Sequencing

The following sequence-on options are supported for each rail:

- Monitor only – do not sequence-on
- Fixed delay time (TON_DELAY) after an OPERATION command to turn on
- Fixed delay time after assertion of the PMBUS_CNTRL pin
- Fixed time after one or a group of parent rails achieves regulation (POWER_GOOD_ON)
- Fixed time after a designated GPI has reached a user-specified state
- Any combination of the previous options

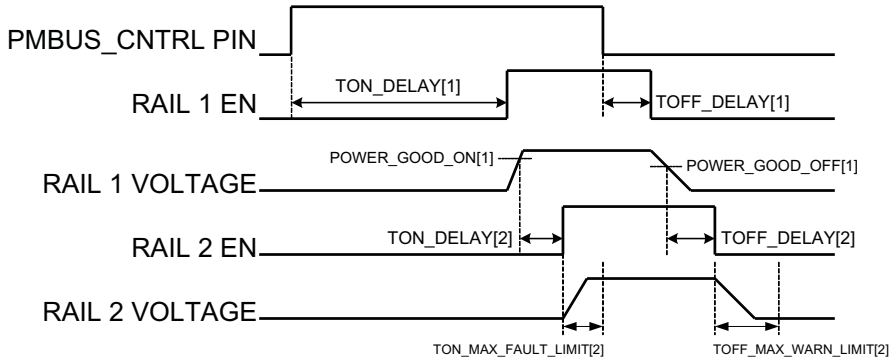
The maximum TON_DELAY time is 3276 ms.

Turn-off Sequencing

The following sequence-off options are supported for each rail:

- Monitor only – do not sequence-off
- Fixed delay time (TOFF_DELAY) after an OPERATION command to turn off
- Fixed delay time after deassertion of the PMBUS_CNTRL pin
- Fixed time after one or a group of parent rails drop below regulation (POWER_GOOD_OFF)
- Fixed delay time in response to an undervoltage, overvoltage, or max turn-on fault on the rail
- Fixed delay time in response to a fault on a different rail when set as a fault shutdown slave to the faulted rail
- Fixed delay time in response to a GPI reaching a user-specified state
- Any combination of the previous options

The maximum TOFF_DELAY time is 3276 ms.



- Rail 1 and Rail 2 are both sequenced “ON” and “OFF” by the PMBUS_CNTRL pin only
- Rail 2 has Rail 1 as an “ON” dependency
- Rail 1 has Rail 2 as an “OFF” dependency

Figure 9. Sequence-on and Sequence-off Timing

Sequencing Configuration Options

In addition to the turn-on and turn-off sequencing options, the time between when a rail is enabled and when the monitored rail voltage must reach its power-good-on setting can be configured using max turn-on (TON_MAX_FAULT_LIMIT). Max turn-on can be set in 1-ms increments. A value of 0 ms means that there is no limit and the device can try to turn on the output voltage indefinitely.

Rails can be configured to turn off immediately or to sequence-off according to rail and GPI dependencies, and user-defined delay times. A sequenced shutdown is configured by selecting the appropriate rail and GPI dependencies, and turn-off delay (TOFF_DELAY) times for each rail. The turn-off delay times begin when the PMBUS_CNTRL pin is deasserted, when the PMBus OPERATION command is used to give a soft-stop command, or when a fault occurs on a rail that has other rails set as fault-shutdown slaves.

Shutdowns on one rail can initiate shutdowns of other rails or controllers. In systems with multiple UCD90160s, it is possible for each controller to be both a master and a slave to another controller.

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PIN SELECTED RAIL STATES

This feature allows with the use of up to 3 GPIs to enable and disable any rail. This is useful for implementing system low-power modes and the Advanced Configuration and Power Interface (ACPI) specification that is used for operating system directed power management in servers and PCs. In up to 8 system states, the power system designer can define which rails are on and which rails are off. If a new state is presented on the input pins, and a rail is required to change state, it will do so with regard to its sequence-on or sequence-off dependencies.

The OPERATION command is modified when this function causes a rail to change its state. This means that the ON_OFF_CONFIG for a given rail must be set to use the OPERATION command for this function to have any effect on the rail state. The first 3 pins configured with the GPI_CONFIG command are used to select 1 of 8 system states. Whenever the device is reset, these pins are sampled and the system state, if enabled, will be used to update each rail state. When selecting a new system state, changes to the status of the GPIs must not take longer than 1 microsecond. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for complete configuration settings of PIN_SELECTED_RAIL_STATES.

Table 2. GPI Selection of System States

GPI 2 State	GPI 1 State	GPI 0 State	System State
NOT Asserted	NOT Asserted	NOT Asserted	0
NOT Asserted	NOT Asserted	Asserted	1
NOT Asserted	Asserted	NOT Asserted	2
NOT Asserted	Asserted	Asserted	3
Asserted	NOT Asserted	NOT Asserted	4
Asserted	NOT Asserted	Asserted	5
Asserted	Asserted	NOT Asserted	6
Asserted	Asserted	Asserted	7

VOLTAGE MONITORING

Up to 16 voltages can be monitored using the analog input pins. The input voltage range is 0 V–2.5 V for MON pins 1-6, 55-59, 62, 63, and 63. Pins 50, 52, and 54 can measure down to 0.2 V. Any voltage between 0 V and 0.2 V on these pins is read as 0.2 V. External resistors can be used to attenuate voltages higher than 2.5 V.

The ADC operates continuously, requiring 3.89 µs to convert a single analog input and 62.2 µs to convert all 16 of the analog inputs. Each rail is sampled by the sequencing and monitoring algorithm every 400 µs. The maximum source impedance of any sampled voltage should be less than 4 kΩ. The source impedance limit is particularly important when a resistor-divider network is used to lower the voltage applied to the analog input pins.

MON1 - MON6 can be configured using digital hardware comparators, which can be used to achieve faster fault responses. Each hardware comparator has four thresholds (two UV (Fault and Warning) and two OV (Fault and Warning)). The hardware comparators respond to UV or OV conditions in about 80 µs (faster than 400 µs for the ADC inputs) and can be used to disable rails or assert GPOs. The only fault response available for the hardware comparators is to shut down immediately.

An internal 2.5-V reference is used by the ADC. The ADC reference has a tolerance of ±0.5% between 0°C and 125°C and a tolerance of ±1% between –40°C and 125°C. An external voltage divider is required for monitoring voltages higher than 2.5 V. The nominal rail voltage and the external scale factor can be entered into the *Fusion GUI* and are used to report the actual voltage being monitored instead of the ADC input voltage. The nominal voltage is used to set the range and precision of the reported voltage according to Table 3.

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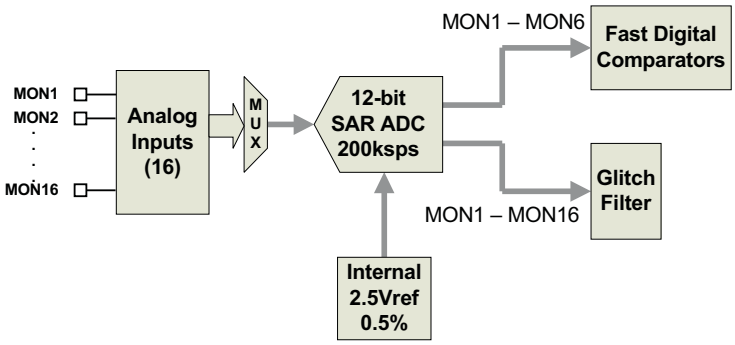

Figure 10. Voltage Monitoring Block Diagram

Table 3. Voltage Range and Resolution

VOLTAGE RANGE (Volts)	RESOLUTION (millivolts)
0 to 127.99609	3.90625
0 to 63.99805	1.95313
0 to 31.99902	0.97656
0 to 15.99951	0.48824
0 to 7.99976	0.24414
0 to 3.99988	0.12207
0 to 1.99994	0.06104
0 to 0.99997	0.03052

Although the monitor results can be reported with a resolution of about 15 µV, the real conversion resolution of 610 µV is fixed by the 2.5-V reference and the 12-bit ADC.

FAULT RESPONSES AND ALERT PROCESSING

Device monitors that the rail stays within a window of normal operation. There are two programmable warning levels (under and over) and two programmable fault levels (under and over). When any monitored voltage goes outside of the warning or fault window, the PMBALERT# pin is asserted immediately, and the appropriate bits are set in the PMBus status registers (see Figure 7). Detailed descriptions of the status registers are provided in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* and the *PMBus Specification.*

A programmable glitch filter can be enabled or disabled for each MON input. A glitch filter for an input defined as a voltage can be set between 0 and 102 ms with 400-µs resolution.

Fault-response decisions are based on results from the 12-bit ADC. The device cycles through the ADC results and compares them against the programmed limits. The time to respond to an individual event is determined by when the event occurs within the ADC conversion cycle and the selected fault response.

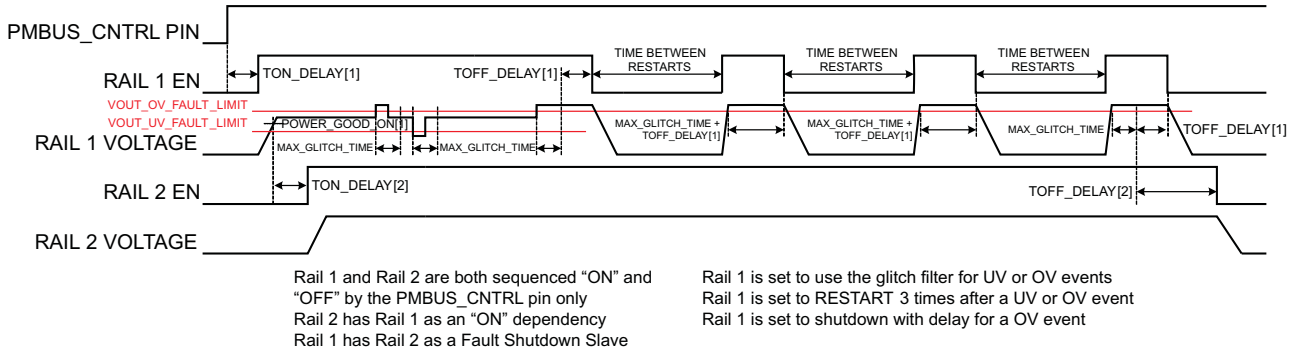

Figure 11. Sequencing and Fault-Response Timing

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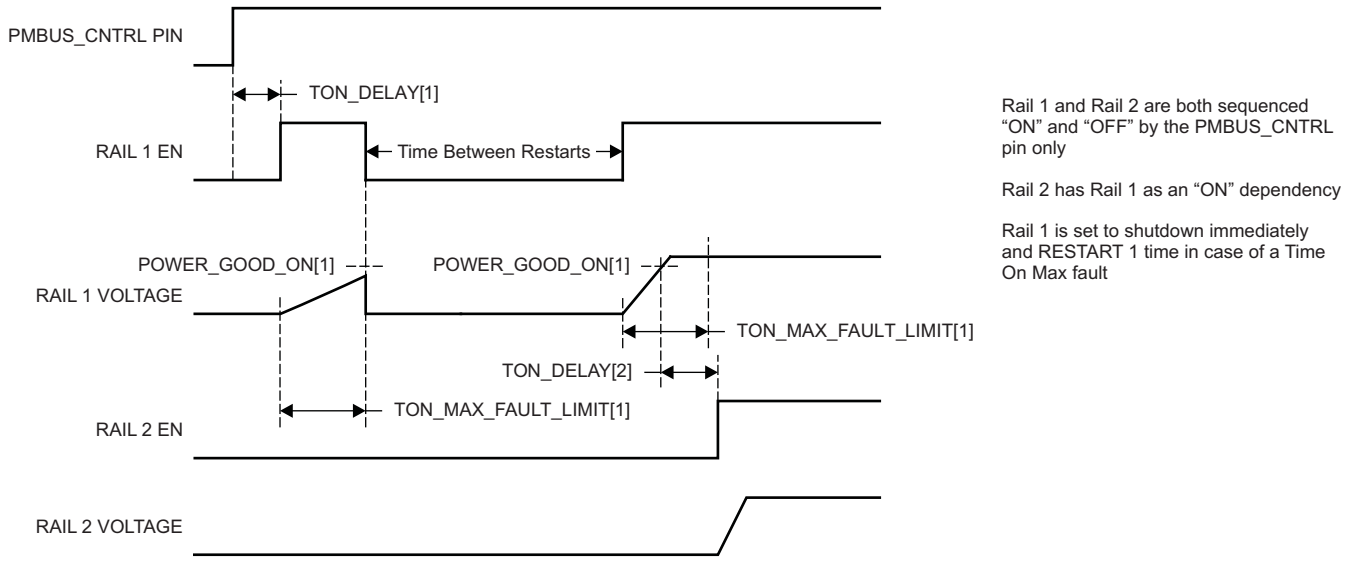

Figure 12. Maximum Turn-on Fault

The configurable fault limits are:

TON_MAX_FAULT – Flagged if a rail that is enabled does not reach the POWER_GOOD_ON limit within the configured time

VOUT_UV_WARN – Flagged if a voltage rail drops below the specified UV warning limit after reaching the POWER_GOOD_ON setting

VOUT_UV_FAULT – Flagged if a rail drops below the specified UV fault limit after reaching the POWER_GOOD_ON setting

VOUT_OV_WARN – Flagged if a rail exceeds the specified OV warning limit at any time during startup or operation

VOUT_OV_FAULT – Flagged if a rail exceeds the specified OV fault limit at any time during startup or operation

TOFF_MAX_WARN – Flagged if a rail that is commanded to shut down does not reach 12.5% of the nominal rail voltage within the configured time

Faults are more serious than warnings. The PMBALERT# pin is always asserted immediately if a warning or fault occurs. If a warning occurs, the following takes place:

Warning Actions

- Immediately assert the PMBALERT# pin
- Status bit is flagged
- Assert a GPIO pin (optional)
- Warnings are not logged to flash

A number of fault response options can be chosen from:

Fault Responses

- *Continue Without Interruption:* Flag the fault and take no action
- *Shut Down Immediately:* Shut down the faulted rail immediately and restart according to the rail configuration

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— *Shut Down using TOFF_DELAY:* If a fault occurs on a rail, exhaust whatever retries are configured. If the rail does not come back, schedule the shutdown of this rail and all fault-shutdown slaves. All selected rails, including the faulty rail, are sequenced off according to their sequence-off dependencies and T_OFF_DELAY times. If Do Not Restart is selected, then sequence off all selected rails when the fault is detected.

Restart

— *Do Not Restart:* Do not attempt to restart a faulted rail after it has been shut down.

— *Restart Up To N Times:* Attempt to restart a faulted rail up to 14 times after it has been shut down. The time between restarts is measured between when the rail enable pin is deasserted (after any glitch filtering and turn-off delay times, if configured to observe them) and then reasserted. It can be set between 0 and 1275 ms in 5-ms increments. Under voltage faults only have a maximum of 1 restart as an option.

— *Restart Continuously:* Same as *Restart Up To N Times* except that the device continues to restart until the fault goes away, it is commanded off by the specified combination of PMBus OPERATION command and PMBUS_CNTRL pin status, the device is reset, or power is removed from the device. This option is not available for under voltage faults.

— *Shut Down Rails and Sequence On (Re-sequence):* Shut down selected rails immediately or after continue-operation time is reached and then sequence-on those rails using sequence-on dependencies and T_ON_DELAY times.

SHUT DOWN ALL RAILS AND SEQUENCE ON (RESEQUENCE)

In response to a fault, or a RESEQUENCE command, the UCD90160 can be configured to turn off a set of rails and then sequence them back on. To sequence all rails in the system, then all rails must be selected as fault-shutdown slaves of the faulted rail. The rails designated as fault-shutdown slaves will do soft shutdowns regardless of whether the faulted rail is set to stop immediately or stop with delay. Shut-down-all-rails and sequence-on are not performed until retries are exhausted for a given fault.

While waiting for the rails to turn off, an error is reported if any of the rails reaches its TOFF_MAX_WARN_LIMIT. There is a configurable option to continue with the resequencing operation if this occurs. After the faulted rail and fault-shutdown slaves sequence-off, the UCD90160 waits for a programmable delay time between 0 and 1275 ms in increments of 5 ms and then sequences-on the faulted rail and fault-shutdown slaves according to the start-up sequence configuration. This is repeated until the faulted rail and fault-shutdown slaves successfully achieve regulation or for a user-selected 1, 2, 3, or 4 times. If the resequence operation is successful, the resequence counter is reset if all of the rails that were resequenced maintain normal operation for one second.

Once shut-down-all-rails and sequence-on begin, any faults on the fault-shutdown slave rails are ignored. If there are two or more simultaneous faults with different fault-shutdown slaves, the more conservative action is taken. For example, if a set of rails is already on its second resequence and the device is configured to resequence three times, and another set of rails enters the resequence state, that second set of rails is only resequenced once. Another example – if one set of rails is waiting for all of its rails to shut down so that it can resequence, and another set of rails enters the resequence state, the device now waits for all rails from both sets to shut down before resequencing.

GPIOs

The UCD90160 has 22 GPIO pins that can function as either inputs or outputs. Each GPIO has configurable output mode options including open-drain or push-pull outputs that can be actively driven to 3.3 V or ground. There are an additional four pins that can be used as either inputs or PWM outputs but not as GPOs. Table 4 lists possible uses for the GPIO pins and the maximum number of each type for each use. GPIO pins can be dependents in sequencing and alarm processing. They can also be used for system-level functions such as external interrupts, power-goods, resets, or for the cascading of multiple devices. GPOs can be sequenced up or down by configuring a rail without a MON pin but with a GPIO set as an enable.

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Table 4. GPIO Pin Configuration Options

PIN NAME	PIN	RAIL EN (16 MAX)	GPI (8 MAX)	GPO (16 MAX)	PWM OUT (12 MAX)	MARGIN PWM (10 MAX)
FPWM1/GPIO5	17	X	X	X	X	X
FPWM2/GPIO6	18	X	X	X	X	X
FPWM3/GPIO7	19	X	X	X	X	X
FPWM4/GPIO8	20	X	X	X	X	X
FPWM5/GPIO9	21	X	X	X	X	X
FPWM6/GPIO10	22	X	X	X	X	X
FPWM7/GPIO11	23	X	X	X	X	X
FPWM8/GPIO12	24	X	X	X	X	X
GPI1/PWM1	31		X		X	
GPI2/PWM2	32		X		X	
GPI3/PWM3	42		X		X	X
GPI4/PWM4	41		X		X	X
GPIO1	11	X	X	X		
GPIO2	12	X	X	X		
GPIO3	13	X	X	X		
GPIO4	14	X	X	X		
GPIO13	25	X	X	X		
GPIO14	29	X	X	X		
GPIO15	30	X	X	X		
GPIO16	33	X	X	X		
GPIO17	34	X	X	X		
GPIO18	35	X	X	X		
TCK/GPIO19	36	X	X	X		
TDO/GPIO20	37	X	X	X		
TDI/GPIO21	38	X	X	X		
TMS/GPIO22	39	X	X	X		

GPO Control

The GPIOs when configured as outputs can be controlled by PMBus commands or through logic defined in internal Boolean function blocks. Controlling GPOs by PMBus commands (GPIO_SELECT and GPIO_CONFIG) can be used to have control over LEDs, enable switches, etc. with the use of an I2C interface. See the UCD90xxx Sequencer and System Health Controller PMBus Command Reference for details on controlling a GPO using PMBus commands.

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GPO Dependencies

GPIOs can be configured as outputs that are based on Boolean combinations of up to two ANDs, all ORed together (Figure 13). Inputs to the logic blocks can include the first 8 defined GPOs, GPIs and rail-status flags. One rail status type is selectable as an input for each AND gate in a Boolean block. For a selected rail status, the status flags of all active rails can be included as inputs to the AND gate. *_LATCH* rail-status types stay asserted until cleared by a MFR PMBus command or by a specially configured GPI pin. The different rail-status types are shown in Table 5. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for complete definitions of rail-status types. The GPO response can be configured to have a delayed assertion or deassertion.

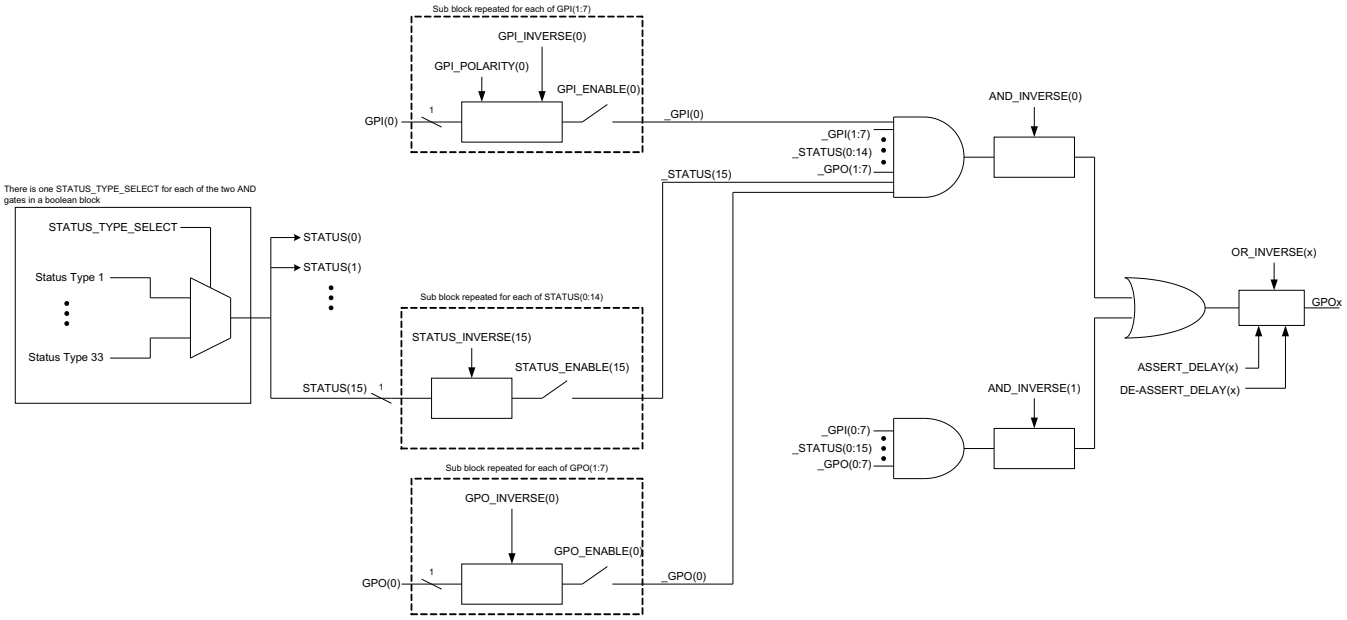

Figure 13. Boolean Logic Combinations

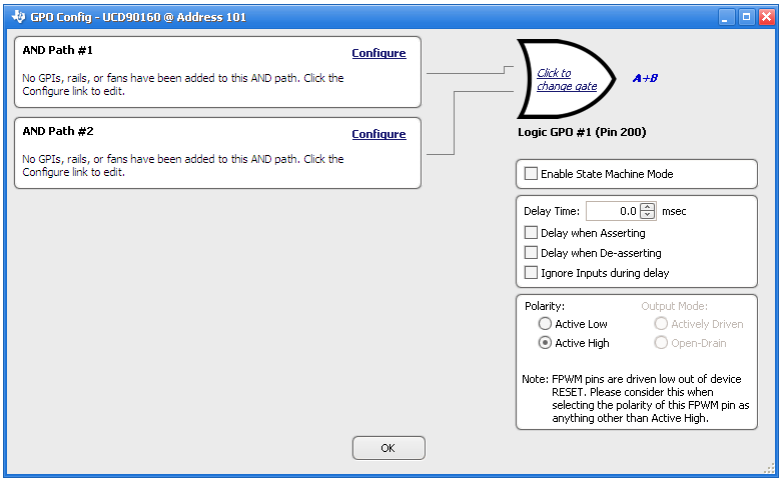

Figure 14. Fusion Boolean Logic Builder

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Table 5. Rail-Status Types for Boolean Logic

Rail-Status Types		
POWER_GOOD	TON_MAX_FAULT	VOUT_UV_WARN_LATCH
MARGIN_EN	TOFF_MAX_WARN	VOUT_UV_FAULT_LATCH
MRG_LOW_nHIGH	SEQ_ON_TIMEOUT	TON_MAX_FAULT_LATCH
VOUT_OV_FAULT	SEQ_OFF_TIMEOUT	TOFF_MAX_WARN_LATCH
VOUT_OV_WARN	SYSTEM_WATCHDOG_TIMEOUT	SEQ_ON_TIMEOUT_LATCH
VOUT_UV_WARN	VOUT_OV_FAULT_LATCH	SEQ_OFF_TIMEOUT_LATCH
VOUT_UV_FAULT	VOUT_OV_WARN_LATCH	SYSTEM_WATCHDOG_TIMEOUT_LATCH

GPO Delays

The GPOs can be configured so that they manifest a change in logic with a delay on assertion, deassertion, both or none. GPO behavior using delays will have different effects depending if the logic change occurs at a faster rate than the delay. On a normal delay configuration, if the logic for a GPO changes to a state and reverts back to previous state within the time of a delay then the GPO will not manifest the change of state on the pin. In Figure 15 the GPO is set so that it follows the GPI with a 3ms delay at assertion and also at de-assertion. When the GPI first changes to high logic state, the state is maintained for a time longer than the delay allowing the GPO to follow with appropriate logic state. The same goes for when the GPI returns to its previous low logic state. The second time that the GPI changes to a high logic state it returns to low logic state before the delay time expires. In this case the GPO does not change state. A delay configured in this manner serves as a glitch filter for the GPO.

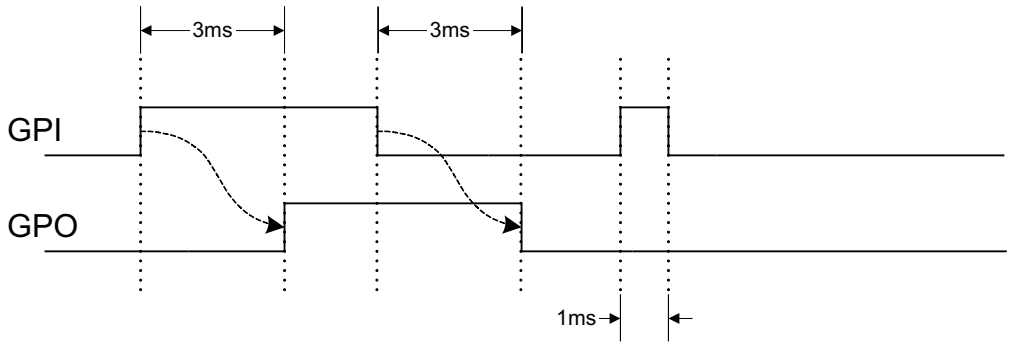

Figure 15. GPO Behavior When Not Ignoring Inputs During Delay

The *Ignore Input During Delay* bit allows to output a change in GPO even if it occurs for a time shorter than the delay. This configuration setting has the GPO ignore any activity from the triggering event until the delay expires. Figure 16 represents the two cases for when ignoring the inputs during a delay. In the case in which the logic changes occur with more time than the delay, the GPO signal looks the same as if the input was not ignored. Then on a GPI pulse shorter than the delay the GPO still changes state. Any pulse that occurs on the GPO when having the *Ignore Input During Delay* bit set will have a width of at least the time delay.

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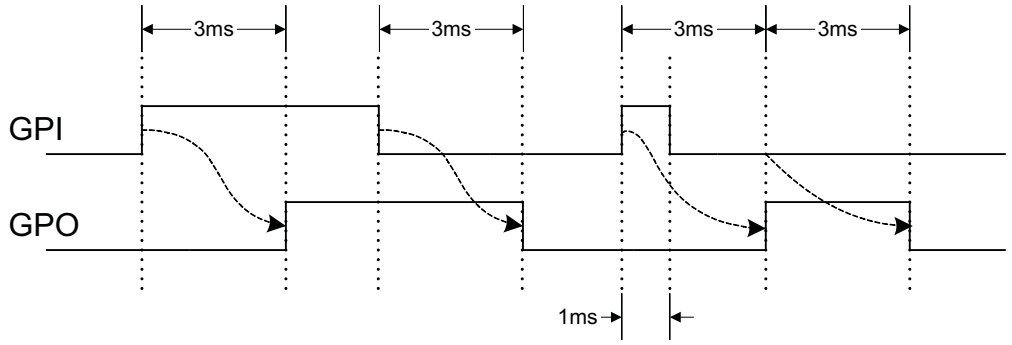

Figure 16. GPO Behavior When Ignoring Inputs During Delay

State Machine Mode Enable

When this bit within the GPO_CONFIG command is set, only one of the AND path will be used at a given time. When the GPO logic result is currently TRUE, AND path 0 will be used until the result becomes FALSE. When the GPO logic result is currently FALSE, AND path 1 will be used until the result becomes TRUE. This provides a very simple state machine and allows for more complex logical combinations.

GPI Special Functions

There are five special input functions for which GPIs can be used. There can be no more than one pin assigned to each of these functions.

- **Sequencing Timeout Source** - If SEQ_TIMEOUT is non-zero on any rail, a fault will occur if this GPI pin does not go active within SEQ_TIMEOUT time after the rail reaches its power good state.
- **Latched Statuses Clear Source** - When a GPO uses a latched status type (_LATCH), you can configure a GPI that will clear the latched status.
- **Input Source for Margin Enable** - When this pin is asserted, all rails with margining enabled will be put in a margined state (low or high).
- **Input Source for Margin Low/Not-High** - When this pin is asserted all margined rails will be set to Margin Low as long as the Margin Enable is asserted. When this pin is de-asserted the rails will be set to Margin High.

The polarity of GPI pins can be configured to be either Active Low or Active High. The first 3 GPIs that are defined regardless of their main purpose will be used for the PIN_SELECTED_RAIL_STATES command.

Power-Supply Enables

Each GPIO can be configured as a rail-enable pin with either active-low or active-high polarity. Output mode options include open-drain or push-pull outputs that can be actively driven to 3.3 V or ground. During reset, the GPIO pins are high-impedance except for FPWM/GPIO pins 17–24, which are driven low. External pulldown or pullup resistors can be tied to the enable pins to hold the power supplies off during reset. The UCD90160 can support a maximum of 16 enable pins.

NOTE

GPIO pins that have FPWM capability (pins 17-24) should only be used as power-supply enable signals if the signal is active high.

Cascading Multiple Devices

A GPIO pin can be used to coordinate multiple controllers by using it as a power good-output from one device and connecting it to the PMBUS_CNTRL input pin of another. This imposes a master/slave relationship among multiple devices. During startup, the slave controllers initiate their start sequences after the master has completed its start sequence and all rails have reached regulation voltages. During shutdown, as soon as the master starts to sequence-off, it sends the shut-down signal to its slaves.

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A shutdown on one or more of the master rails can initiate shutdowns of the slave devices. The master shutdowns can be initiated intentionally or by a fault condition. This method works to coordinate multiple controllers, but it does not enforce interdependency between rails within a single controller.

The PMBus specification implies that the power-good signal is active when ALL the rails in a controller are regulating at their programmed voltage. The UCD90160 allows GPIOs to be configured to respond to a desired subset of power-good signals.

PWM Outputs

FPWM1-8

Pins 17–24 can be configured as fast pulse-width modulators (FPWMs). The frequency range is 15.260 kHz to 125 MHz. FPWMs can be configured as closed-loop margining outputs, fan controllers or general-purpose PWMs.

Any FPWM pin not used as a PWM output can be configured as a GPIO. One FPWM in a pair can be used as a PWM output and the other pin can be used as a GPO. The FPWM pins are actively driven low from reset when used as GPOs.

The frequency settings for the FPWMs apply to pairs of pins:

- FPWM1 and FPWM2 – same frequency
- FPWM3 and FPWM4 – same frequency
- FPWM5 and FPWM6 – same frequency
- FPWM7 and FPWM8 – same frequency

If an FPWM pin from a pair is not used while its companion is set up to function as a PWM, it is recommended to configure the unused FPWM pin as an active-low open-drain GPO so that it does not disturb the rest of the system. By setting an FPWM, it automatically enables the other FPWM within the pair if it was not configured for any other functionality.

The frequency for the FPWM is derived by dividing down a 250MHz clock. To determine the actual frequency to which an FPWM can be set, must divide 250MHz by any integer between 2 and (2^{14}-1).

The FPWM duty cycle resolution is dependent on the frequency set for a given FPWM. Once the frequency is known the duty cycle resolution can be calculated as Equation 1.

$$\text{Change per Step } (\%)_{FPWM} = \text{frequency} \div (250 \times 10^6 \times 16) \quad (1)$$

Take for an example determining the actual frequency and the duty cycle resolution for a 75MHz target frequency.

1. Divide 250MHz by 75MHz to obtain 3.33.
2. Round off 3.33 to obtain an integer of 3.
3. Divide 250MHz by 3 to obtain actual closest frequency of 83.333MHz.
4. Use Equation 1 to determine duty cycle resolution to obtain 2.0833% duty cycle resolution.

PWM1-4

Pins 31, 32, 41, and 42 can be used as GPIs or PWM outputs.

If configured as PWM outputs, then limitations apply:

- PWM1 has a fixed frequency of 10 kHz
- PWM2 has a fixed frequency of 1 kHz
- PWM3 and PWM4 frequencies can be 0.93 Hz to 7.8125 MHz.

The frequency for PWM3 and PWM4 is derived by dividing down a 15.625MHz clock. To determine the actual frequency to which these PWMs can be set, must divide 15.625MHz by any integer between 2 and (2^{24}-1). The duty cycle resolution will be dependent on the set frequency for PWM3 and PWM4.

The PWM3 or PWM4 duty cycle resolution is dependent on the frequency set for the given PWM. Once the frequency is known the duty cycle resolution can be calculated as Equation 2

$$\text{Change per Step } (\%)_{PWM3/4} = \text{frequency} \div (15.625 \times 10^6) \times 100 \quad (2)$$

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To determine the closest frequency to 1MHz that PWM3 can be set to calculate as the following:

1. Divide 15.625MHz by 1MHz to obtain 15.625.
2. Round off 15.625 to obtain an integer of 16.
3. Divide 15.625MHz by 16 to obtain actual closest frequency of 976.563kHz.
4. Use Equation 2 to determine duty cycle resolution to obtain 6.25% duty cycle resolution.

All frequencies below 238Hz will have a duty cycle resolution of 0.0015%.

Programmable Multiphase PWMs

The FPWMs can be aligned with reference to their phase. The phase for each FPWM is configurable from 0° to 360°. This provides flexibility in PWM-based applications such as power-supply controller, digital clock generation, and others. See an example of four FPWMs programmed to have phases at 0°, 90°, 180° and 270° (Figure 17).

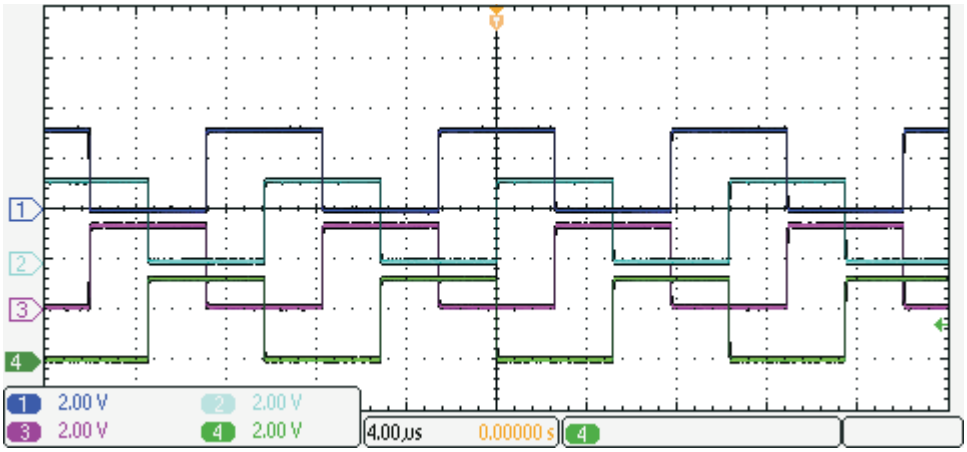

Figure 17. Multiphase PWMs

MARGINING

Margining is used in product validation testing to verify that the complete system works properly over all conditions, including minimum and maximum power-supply voltages, load range, ambient temperature range, and other relevant parameter variations. Margining can be controlled over PMBus using the OPERATION command or by configuring two GPIO pins as margin-EN and margin-UP/DOWN inputs. The MARGIN_CONFIG command in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* describes different available margining options, including ignoring faults while margining and using closed-loop margining to trim the power-supply output voltage one time at power up.

Open-Loop Margining

Open-loop margining is done by connecting a power-supply feedback node to ground through one resistor and to the margined power supply output (V_{OUT}) through another resistor. The power-supply regulation loop responds to the change in feedback node voltage by increasing or decreasing the power-supply output voltage to return the feedback voltage to the original value. The voltage change is determined by the fixed resistor values and the voltage at V_{OUT} and ground. Two GPIO pins must be configured as open-drain outputs for connecting resistors from the feedback node of each power supply to V_{OUT} or ground.

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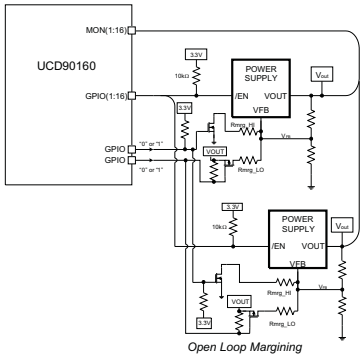

Figure 18. Open-Loop Margining

Closed-Loop Margining

Closed-loop margining uses a PWM or FPWM output for each power supply that is being margined. An external RC network converts the FPWM pulse train into a DC margining voltage. The margining voltage is connected to the appropriate power-supply feedback node through a resistor. The power-supply output voltage is monitored, and the margining voltage is controlled by adjusting the PWM duty cycle until the power-supply output voltage reaches the margin-low and margin-high voltages set by the user. The voltage setting resolutions will be the same that applies to the voltage measurement resolution (Table 3). The closed loop margining can operate in several modes (Table 6). Given that this closed-loop system has feed back through the ADC, the closed-loop margining accuracy will be dominated by the ADC measurement. The relationship between duty cycle and margined voltage is configurable so that voltage increases when duty cycle increases or decreases. For more details on configuring the UCD90160 for margining, see the *Voltage Margining Using the UCD9012x* application note (SLVA375).

Table 6. Closed Loop Margining Modes

Mode	Description
DISABLE	Margining is disabled.
ENABLE_TRI_STATE	When not margining, the PWM pin is set to high impedance state.
ENABLE_ACTIVE_TRIM	When not margining, the PWM duty-cycle is continuously adjusted to keep the voltage at VOUT_COMMAND.
ENABLE_FIXED_DUTY_CYCLE	When not margining, the PWM duty-cycle is set to a fixed duty-cycle.

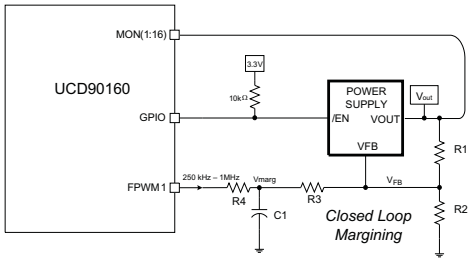

Figure 19. Closed-Loop Margining

SYSTEM RESET SIGNAL

The UCD90160 can generate a programmable system-reset pulse as part of sequence-on. The pulse is created by programming a GPIO to remain deasserted until the voltage of a particular rail or combination of rails reach their respective POWER_GOOD_ON levels plus a programmable delay time. The system-reset delay duration can be programmed as shown in Table 7. See an example of two SYSTEM RESET signals Figure 20. The first

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SYSTEM RESET signal is configured so that it de-asserts on Power Good On and it asserts on Power Good Off after a given common delay time. The second SYSTEM RESET signal is configured so that it sends a pulse after a delay time once Power Good On is achieved. The pulse width can be configured between 0.001s to 32.256s. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for pulse width configuration details.

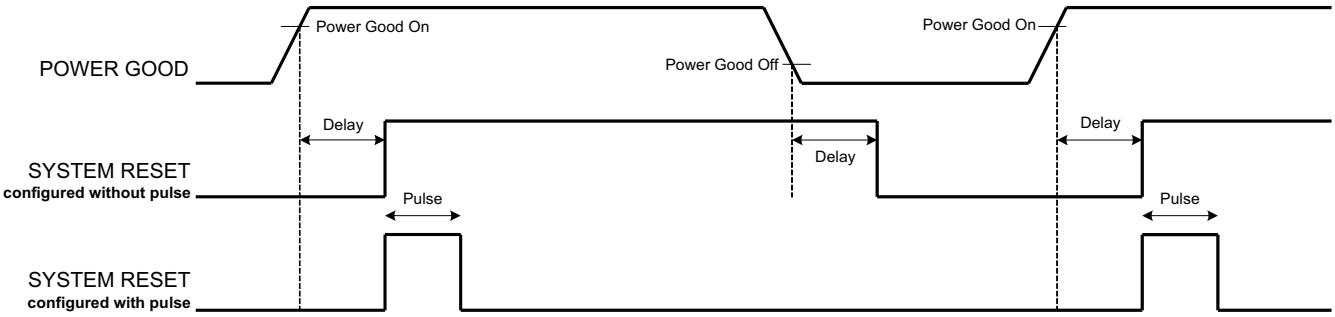

Figure 20. System Reset with and without Pulse Setting

The system reset can react to watchdog timing. In Figure 21 The first delay on SYSTEM RESET is for the initial reset release that would get a CPU running once all necessary voltage rails are in regulation. The watchdog is configured with a Start Time and a Reset Time. If these times expire without the WDI clearing them then it is expected that the CPU providing the watchdog signal is not operating. The SYSTEM RESET is toggled either using a Delay or GPI Tracking Release Delay to see if the CPU recovers.

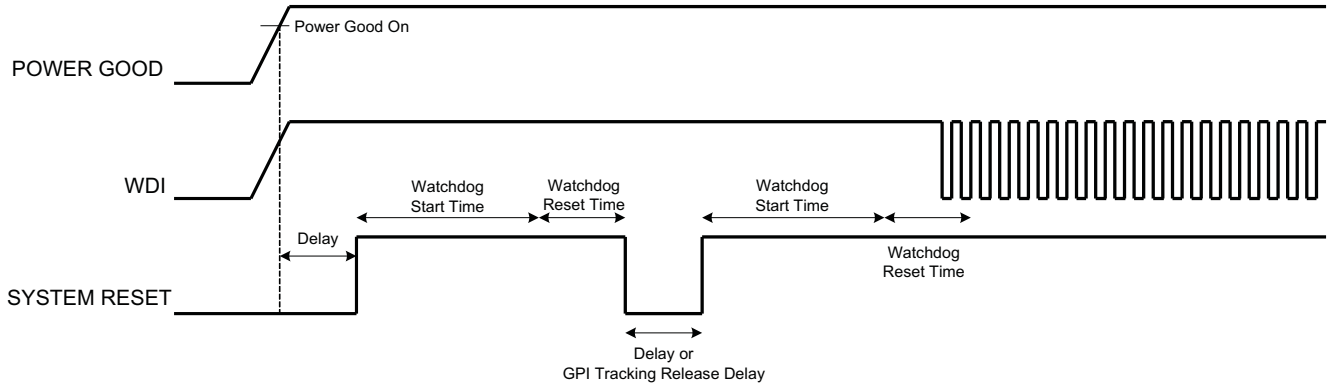

Figure 21. System Reset with Watchdog

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Table 7. System-Reset Delay

Delay
0 ms
1 ms
2 ms
4 ms
8 ms
16 ms
32 ms
64 ms
128 ms
256 ms
512 ms
1.02 s
2.05 s
4.10 s
8.19 s
16.38 s
32.8 s

WATCH DOG TIMER

A GPI and GPO can be configured as a watchdog timer (WDT). The WDT can be independent of power-supply sequencing or tied to a GPIO functioning as a watchdog output (WDO) that is configured to provide a system-reset signal. The WDT can be reset by toggling a watchdog input (WDI) pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C. The WDI and WDO pins are optional when using the watchdog timer. The WDI can be replaced by SYSTEM_WATCHDOG_RESET command and the WDO can be manifested through the Boolean Logic defined GPOs or through the System Reset function.

The WDT can be active immediately at power up or set to wait while the system initializes. Table 8 lists the programmable wait times before the initial timeout sequence begins.

Table 8. WDT Initial Wait Time

WDT INITIAL WAIT TIME
0 ms
100 ms
200 ms
400 ms
800 ms
1.6 s
3.2 s
6.4 s
12.8 s
25.6 s
51.2 s
102 s
205 s
410 s
819 s
1638 s

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The watchdog timeout is programmable from 0.001s to 32.256s. See the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for details on configuring the watchdog timeout. If the WDT times out, the UCD90160 can assert a GPIO pin configured as WDO that is separate from a GPIO defined as system-reset pin, or it can generate a system-reset pulse. After a timeout, the WDT is restarted by toggling the WDI pin or by writing to SYSTEM_WATCHDOG_RESET over I^2C.

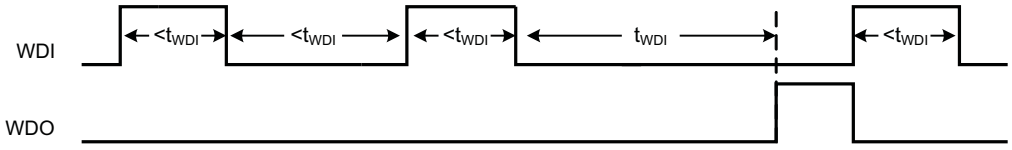

Figure 22. Timing of GPIOs Configured for Watchdog Timer Operation

RUN TIME CLOCK

The Run-Time clock is given in milliseconds and days. Both are 32-bit numbers. This value is saved in nonvolatile memory whenever a STORE_DEFAULT_ALL command is issued. It can also be saved when a power-down condition is detected (See BROWNOUT FUNCTION).

The Run-Time clock may also be written. This allows the clock to be periodically corrected by the host. It also allows the clock to be initialized to the actual, absolute time in years (e.g., March 23, 2010). The user must translate the absolute time to days and milliseconds.

The three usage scenarios for the Run-Time Clock are:

1. **Time from restart (reset or power-on)** – the Run-Time Clock starts from 0 each time a restart occurs
2. **Absolute run-time, or operating time** – the Run-Time Clock is preserved across restarts, so you can keep up with the total time that the device has been in operation (Note: “Boot time” is not part of this. Only normal operation time is captured here.)
3. **Local time** – an external processor sets the Run-Time Clock to real-world time each time the device is restarted.

The Run-Time clock value is used to timestamp any faults that are logged.

DATA AND ERROR LOGGING TO FLASH MEMORY

The UCD90160 can log up to 18 faults and the number of device resets to flash memory. Peak voltage measurements are also stored for each rail. To reduce stress on the flash memory, a 30-second timer is started if a measured value exceeds the previously logged value. Only the highest value from the 30-second interval is written from RAM to flash.

Multiple faults can be stored in flash memory and can be accessed over PMBus to help debug power-supply bugs or failures. Each logged fault includes:

- Rail number
- Fault type
- Fault time since previous device reset
- Last measured rail voltage

The total number of device resets is also stored to flash memory. The value can be reset using PMBus.

There are three settings for handling the fault log once it reaches its maximum capacity. These settings allow to keep the latest faults by using a First In, First Out (FIFO) mode.

- FIFO log disabled - The first 18 faults will be logged. No additional faults will be logged until the fault log is cleared.
- FIFO log for all faults - The most recent 18 faults will be logged. Once 18 faults are logged, any additional faults will cause the oldest fault log entry to be lost.
- FIFO log for last half of faults - The first 9 faults will be logged. The most recent 9 faults will also be logged. In the FIFO portion of the log, once 9 faults are logged, any additional faults will cause the oldest fault entry to be lost.

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With the brownout function enabled, the run-time clock value, peak monitor values, and faults are only logged to flash when a power-down is detected. The device run-time clock value is stored across resets or power cycles unless the brownout function is disabled, in which case the run-time clock is returned to zero after each reset.

It is also possible to update and calibrate the UCD90160 internal run-time clock via a PMBus host. For example, a host processor with a real-time clock could periodically update the UCD90160 run-time clock to a value that corresponds to the actual date and time. The host must translate the UCD90160 timer value back into the appropriate units, based on the usage scenario chosen. See the REAL_TIME_CLOCK command in the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference* for more details.

BROWNOUT FUNCTION

The UCD90160 can be enabled to turn off all nonvolatile logging until a brownout event is detected. A brownout event occurs if V_{CC} drops below 2.9 V. In order to enable this feature, the user must provide enough local capacitance to deliver up to 80 mA (consider additional load based on GPOs sourcing external circuits such as LEDs) on for 5 ms while maintaining a minimum of 2.6 V at the device. If using the brownout circuit (Figure 23), then a schottky diode should be placed so that it blocks the other circuits that are also powered from the 3.3V supply.

With this feature enabled, the UCD90160 saves faults, peaks, and other log data to SRAM during normal operation of the device. Once a brownout event is detected, all data is copied from SRAM to Flash. Use of this feature allows the UCD90160 to keep track of a single run-time clock that spans device resets or system power down (rather than resetting the run time clock after device reset). It can also improve the UCD90160 internal response time to events, because Flash writes are disabled during normal system operation. This is an optional feature and can be enabled using the MISC_CONFIG command. For more details, see the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference*.

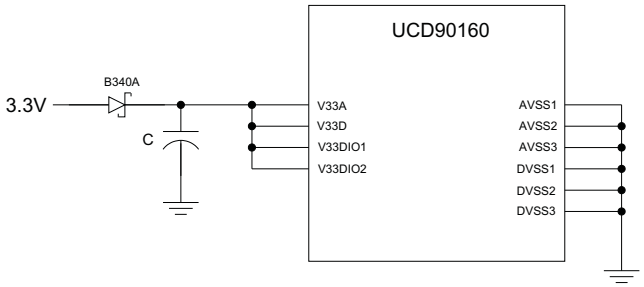

Figure 23. Brownout Circuit

PMBUS ADDRESS SELECTION

Two pins are allocated to decode the PMBus address. At power up, the device applies a bias current to each address-detect pin, and the voltage on that pin is captured by the internal 12-bit ADC. The PMBus address is calculated as follows.

$$\text{PMBus Address} = 12 \times \text{bin}(V_{AD01}) + \text{bin}(V_{AD00})$$

Where $\text{bin}(V_{AD0x})$ is the address bin for one of eight addresses as shown in Table 9. The address bins are defined by the MIN and MAX VOLTAGE RANGE (V). Each bin is a constant ratio of 1.25 from the previous bin. This method maintains the width of each bin relative to the tolerance of standard 1% resistors.

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Table 9. PMBus Address Bins

ADDRESS BIN	RPMBus PMBus RESISTANCE (kΩ)
open	—
11	200
10	154
9	118
8	90.9
7	69.8
6	53.6
5	41.2
4	31.6
short	—

A low impedance (short) on either address pin that produces a voltage below the minimum voltage causes the PMBus address to default to address 126 (0x7E). A high impedance (open) on either address pin that produces a voltage above the maximum voltage also causes the PMBus address to default to address 126 (0x7E).

Address 0 is not used because it is the PMBus general-call address. Addresses 11 and 127 can not be used by this device or any other device that shares the PMBus with it, because those are reserved for manufacturing programming and test. It is recommended that address 126 not be used for any devices on the PMBus, because this is the address that the UCD90160 defaults to if the address lines are shorted to ground or left open. Table 10 summarizes which PMBus addresses can be used. Other SMBus/PMBus addresses have been assigned for specific devices. For a system with other types of devices connected to the same PMBus, see the SMBus device address assignments table in Appendix C of the latest version of the System Management Bus (SMBus) specification. The SMBus specification can be downloaded at http://smbus.org/specs/smbus20.pdf.

Table 10. PMBus Address Assignment Rules

Address	STATUS	Reason
0	Prohibited	SMBus general address call
1-10	Available	
11	Avoid	Causes conflicts with other devices during program flash updates.
12	Prohibited	PMBus alert response protocol
13-125	Available	
126	For JTAG Use	Default value; may cause conflicts with other devices.
127	Prohibited	Used by TI manufacturing for device tests.

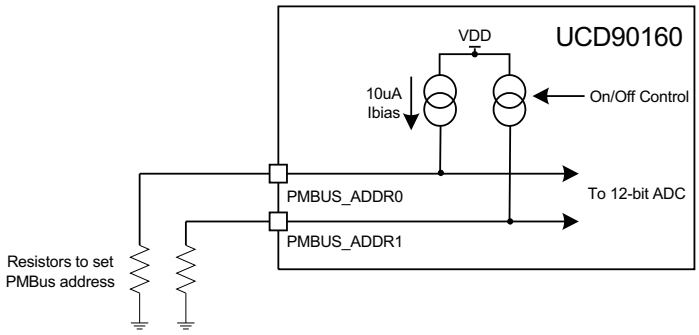

Figure 24. PMBus Address-Detection Method

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CAUTION

Leaving the address in default state as 126 (0x7E) will enable the JTAG and not allow using the JTAG compatible pins (36-39) as GPIOs.

DEVICE RESET

The UCD90160 has an integrated power-on reset (POR) circuit which monitors the supply voltage. At power up, the POR detects the V_{33D} rise. When V_{33D} is greater than V_{RESET}, the device comes out of reset.

The device can be forced into the reset state by an external circuit connected to the $\overline{\text{RESET}}$ pin. A logic-low voltage on this pin for longer than t_{RESET} holds the device in reset. It comes out of reset within 1 ms after $\overline{\text{RESET}}$ is released and can return to a logic-high level. To avoid an erroneous trigger caused by noise, connect $\overline{\text{RESET}}$ to a 10kΩ pullup resistor (from $\overline{\text{RESET}}$ to 3.3 V) and a 1000pF capacitor (from $\overline{\text{RESET}}$ to AVSS).

Any time the device comes out of reset, it begins an initialization routine that lasts about 20 ms. During the initialization routine, the FPWM pins are held low, and all other GPIO and GPI pins are open-circuit. At the end of initialization, the device begins normal operation as defined by the device configuration.

DEVICE CONFIGURATION AND PROGRAMMING

From the factory, the device contains the sequencing and monitoring firmware. It is also configured so that all GPOs are high-impedance (except for FPWM/GPIO pins 17-24, which are driven low), with no sequencing or fault-response operation. See *Configuration Programming of UCD Devices*, available from the *Documentation & Help Center* that can be selected from the *Fusion GUI* Help menu, for full UCD90160 configuration details.

After the user has designed a configuration file using *Fusion GUI*, there are three general device-configuration programming options:

1. Devices can be programmed in-circuit by a host microcontroller using PMBus commands over I^2C (see the *UCD90xxx Sequencer and System Health Controller PMBus Command Reference*). Each parameter write replaces the data in the associated memory (RAM) location. After all the required configuration data has been sent to the device, it is transferred to the associated nonvolatile memory (data flash) by issuing a special command, STORE_DEFAULT_ALL. This method is how the *Fusion GUI* normally reads and writes a device configuration.
2. The *Fusion GUI* (Figure 25) can create a PMBus or I^2C command script file that can be used by the I^2C master to configure the device.

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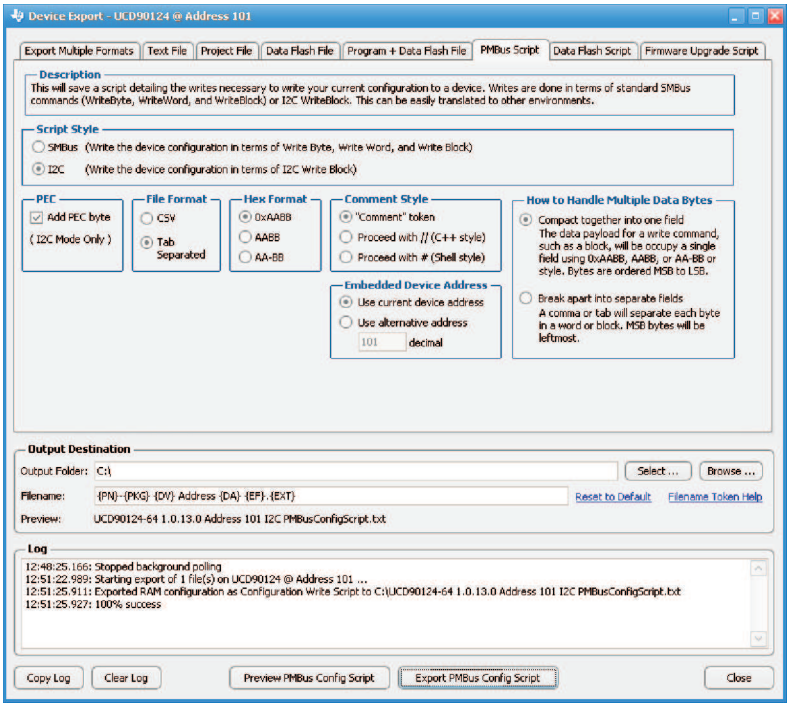

Figure 25. Fusion GUI PMBus Configuration Script Export Tool

3. Another in-circuit programming option is for the *Fusion GUI* to create a data flash image from the configuration file (Figure 26). The configuration files can be exported in Intel Hex, Serial Vector Format (SVF) and S-record. The image file can be downloaded into the device using I^2C or JTAG. The *Fusion GUI* tools can be used on-board if the *Fusion GUI* can gain ownership of the target board I^2C bus.

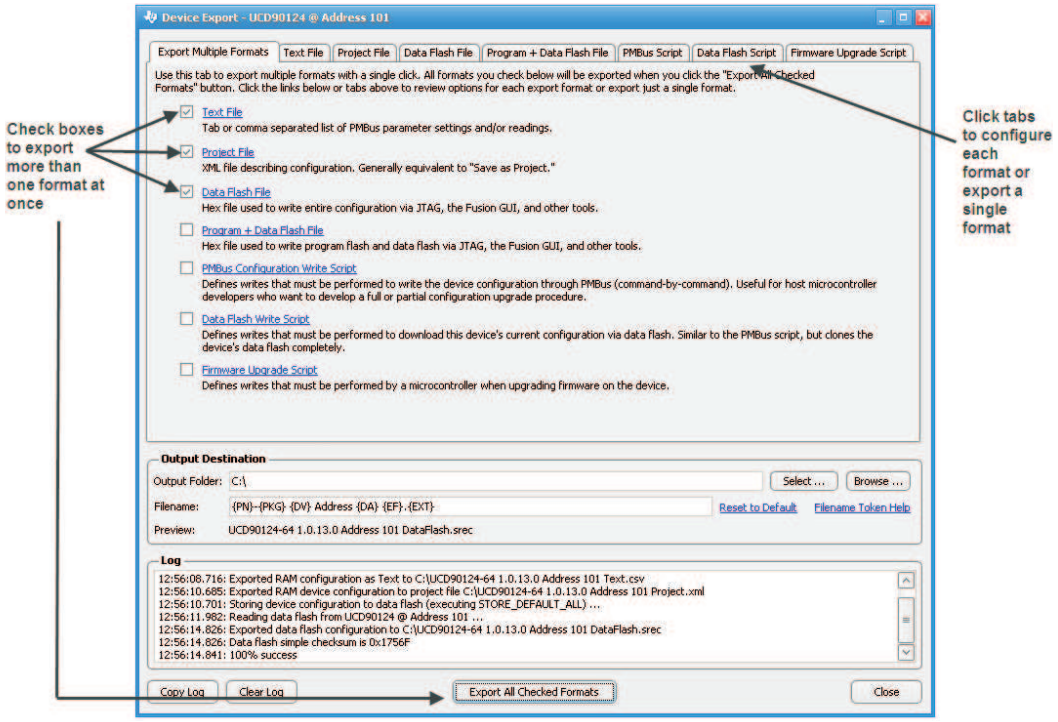

Figure 26. Fusion GUI Device Configuration Export Tool

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Devices can be programmed off-board using the *Fusion GUI* tools or a dedicated device programmer. For small runs, a ZIF socketed board with an I^2C header can be used with the standard *Fusion GUI* or manufacturing GUI. The *Fusion GUI* can also create a data flash file that can then be loaded into the UCD90160 using a dedicated device programmer.

To configure the device over I^2C or PMBus, the UCD90160 must be powered. The PMBus clock and data pins must be accessible and must be pulled high to the same V_{DD} supply that powers the device, with pullup resistors between 1 kΩ and 2 kΩ. Care should be taken to not introduce additional bus capacitance (<100 pF). The user configuration can be written to data flash using a gang programmer via JTAG or I^2C before the device is installed in circuit. To use I^2C, the clock and data lines must be multiplexed or the device addresses must be assigned by socket. The *Fusion GUI* tools can be used for socket addressing. Pre-programming can also be done using a single device test fixture.

Table 11. Configuration Options

	Data Flash via JTAG	Data Flash via I^2C	PMBus Commands via I^2C
Off-Board Configuration	Data Flash Export (.svf type file)	Data Flash Export (.srec or hex type file)	Project file I^2C/PMBus script
	Dedicated programmer	Fusion tools (with exclusive bus access via USB to I^2C adapter)	Fusion tools (with exclusive bus access via USB to I^2C adapter)
On-Board Configuration	Data flash export	Fusion tools (with exclusive bus access via USB to I^2C adapter)	Fusion tools (with exclusive bus access via USB to I^2C adapter)
	IC		

The advantages of off-board configuration include:

- Does not require access to device I^2C bus on board.
- Once soldered on board, full board power is available without further configuration.
- Can be partially reconfigured once the device is mounted.

Full Configuration Update while in Normal Mode

Although performing a full configuration of the UCD90160 in a controlled test setup is recommended, there may be times in which it is required to update the configuration while the device is in an operating system. Updating the full configuration based on methods listed in DEVICE CONFIGURATION AND PROGRAMMING section while the device is in an operating system can be challenging because these methods do not permit the UCD90160 to operate as required by application during the programming. During described methods the GPIOs may not be in the desired states which can disable rails that provide power to the UCD90160. To overcome this, the UCD90160 has the capability to allow full configuration update while still operating in normal mode.

Updating the full configuration while in normal mode will consist of disabling data flash write protection, erasing the data flash, writing the data flash image and reset the device. It is not required to reset the device immediately but make note that the UCD90160 will continue to operate based on previous configuration with fault logging disabled until reset. See *Configuration Programming of UCD Devices*, available from the *Documentation* & *Help Center* that can be selected from the *Fusion GUI* Help menu, for details.

JTAG INTERFACE

The JTAG port can be used for production programming. Four of the six JTAG pins can also be used as GPIOs during normal operation. See the *Pin Functions* table at the beginning of the document and Table 4 for a list of the JTAG signals and which can be used as GPIOs. The JTAG port is compatible with the IEEE Standard 1149.1-1990, IEEE Standard Test-Access Port and Boundary Scan Architecture specification. Boundary scan is not supported on this device.

The JTAG interface can provide an alternate interface for programming the device. It is disabled by default in order to enable the GPIO pins with which it is multiplexed. There are two conditions under which the JTAG interface is enabled:

1. On power-up if the data flash is blank, allowing JTAG to be used for writing the configuration parameters to a programmed device with no PMBus interaction
2. When address 126 (0x7E) is detected at power up. A short to ground or an open condition on either address pin will cause an address 126 (0x7E) to be generated which enables JTAG mode.

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The Fusion GUI can create SVF files (See DEVICE CONFIGURATION AND PROGRAMMING section) based on a given data flash configuration which can be used to program the desired configuration by JTAG. For Boundary Scan Description Language (BSDL) file that supports the UCD90160 see the product folder in www.ti.com.

INTERNAL FAULT MANAGEMENT AND MEMORY ERROR CORRECTION (ECC)

The UCD90160 verifies the firmware checksum at each power up. If it does not match, then the device waits for I^2C commands but does not execute the firmware. A device configuration checksum verification is also performed at power up. If it does not match, the factory default configuration is loaded. The PMBALERT# pin is asserted and a flag is set in the status register. The error-log checksum validates the contents of the error log to make sure that section of flash is not corrupted.

There is an internal firmware watchdog timer. If it times out, the device resets so that if the firmware program is corrupted, the device goes back to a known state. This is a normal device reset, so all of the GPIO pins are open-drain and the FPWM pins are driven low while the device is in reset. Checks are also done on each parameter that is passed, to make sure it falls within the acceptable range.

Error-correcting code (ECC) is used to improve data integrity and provide high-reliability storage of Data Flash contents. ECC uses dedicated hardware to generate extra check bits for the user data as it is written into the Flash memory. This adds an additional six bits to each 32-bit memory word stored into the Flash array. These extra check bits, along with the hardware ECC algorithm, allow for any single-bit error to be detected and corrected when the Data Flash is read.

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APPLICATION INFORMATION

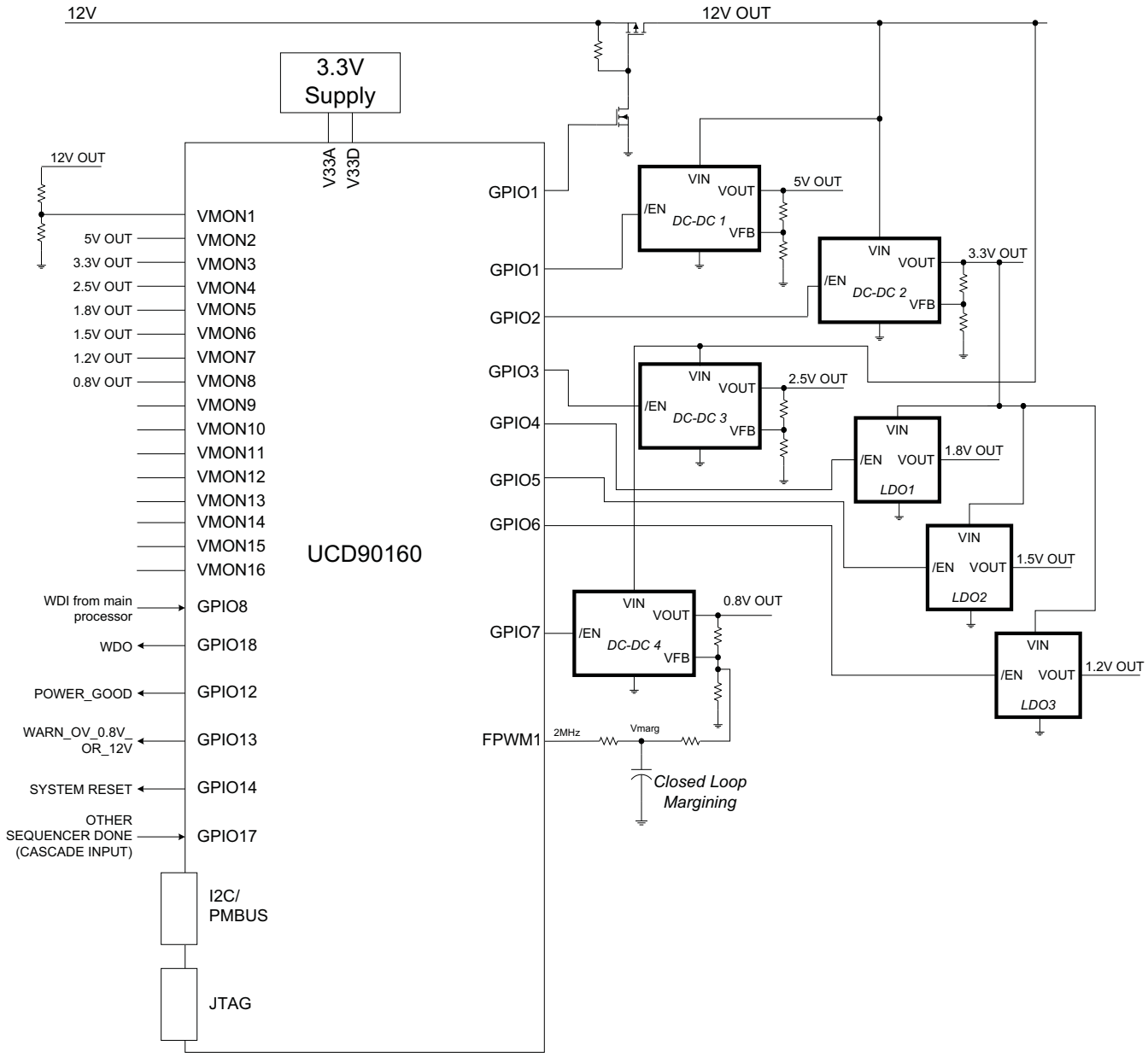

Figure 27. Typical Application Schematic

NOTE

Figure 27 is a simplified application schematic. Voltage dividers such as the ones placed on VMON1 input have been omitted for simplifying the schematic. All VMONx pins which are configured to measure a voltage that exceeds the 2.5V ADC reference are required to have a voltage divider.

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Layout guidelines

The thermal pad provides a thermal and mechanical interface between the device and the printed circuit board (PCB). Connect the exposed thermal pad of the PCB to the device V_{SS} pins and provide at least a 4 × 4 pattern of PCB vias to connect the thermal pad and V_{SS} pins to the circuit ground on other PCB layers.

For supply-voltage decoupling, provide power-supply pin bypass to the device as follows:

- 0.1-µF, X7R ceramic in parallel with 0.01-µF, X7R ceramic at pin 47 (BPCAP)
- 0.1-µF, X7R ceramic in parallel with 4.7-µF, X5R ceramic at pins 44 (V_{33DIO2}) and 45 (V_{33D})
- 0.1-µF, X7R ceramic at pin 7 (V_{33DIO1})
- 0.1-µF, X7R ceramic in parallel with 4.7-µF, X5R ceramic at pin 46 (V_{33A})

Depending on use and application of the various GPIO signals used as digital outputs, some impedance control may be desired to quiet fast signal edges. For example, when using the FPWM pins for fan control or voltage margining, the pin is configured as a digital *clock* signal. Route these signals away from sensitive analog signals. It is also good design practice to provide a series impedance of 20 Ω to 33 Ω at the signal source to slow fast digital edges.

Estimating ADC Reporting Accuracy

The UCD90160 uses a 12-bit ADC and an internal 2.5-V reference (V_{REF}) to convert MON pin inputs into digitally reported voltages. The least significant bit (LSB) value is $V_{LSB} = V_{REF}/2^N$ where N = 12, resulting in a VLSB = 610 µV. The error in the reported voltage is a function of the ADC linearity errors and any variations in VREF. The total unadjusted error (E_{TUE}) for the UCD90160 ADC is ±5 LSB, and the variation of VREF is ±0.5% between 0°C and 125°C and ±1% between –40°C and 125°C. V_{TUE} is calculated as V_{LSB} × E_{TUE}. The total reported voltage error is the sum of the reference-voltage error and V_{TUE}. At lower monitored voltages, V_{TUE} dominates reported error, whereas at higher monitored voltages, the tolerance of V_{REF} dominates the reported error. Reported error can be calculated using Equation 3, where REFTOL is the tolerance of V_{REF}, V_{ACT} is the actual voltage being monitored at the MON pin, and V_{REF} is the nominal voltage of the ADC reference.

$$RPT_{ERR} = \left(\frac{1+REFTOL}{V_{ACT}}\right) \times \left(\frac{V_{REF} \times E_{TUE}}{4096} + V_{ACT}\right) - 1 \quad (3)$$

From Equation 3, for temperatures between 0°C and 125°C, if V_{ACT} = 0.5 V, then RPT_{ERR} = 1.11%. If V_{ACT} = 2.2 V, then RPT_{ERR} = 0.64%. For the full operating temperature range of –40°C to 125°C, if VACT = 0.5 V, then RPT_{ERR} = 1.62%. If V_{ACT} = 2.2 V, then RPT_{ERR} = 1.14%.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
UCD90160RGCR	ACTIVE	VQFN	RGC	64	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	
UCD90160RGCT	ACTIVE	VQFN	RGC	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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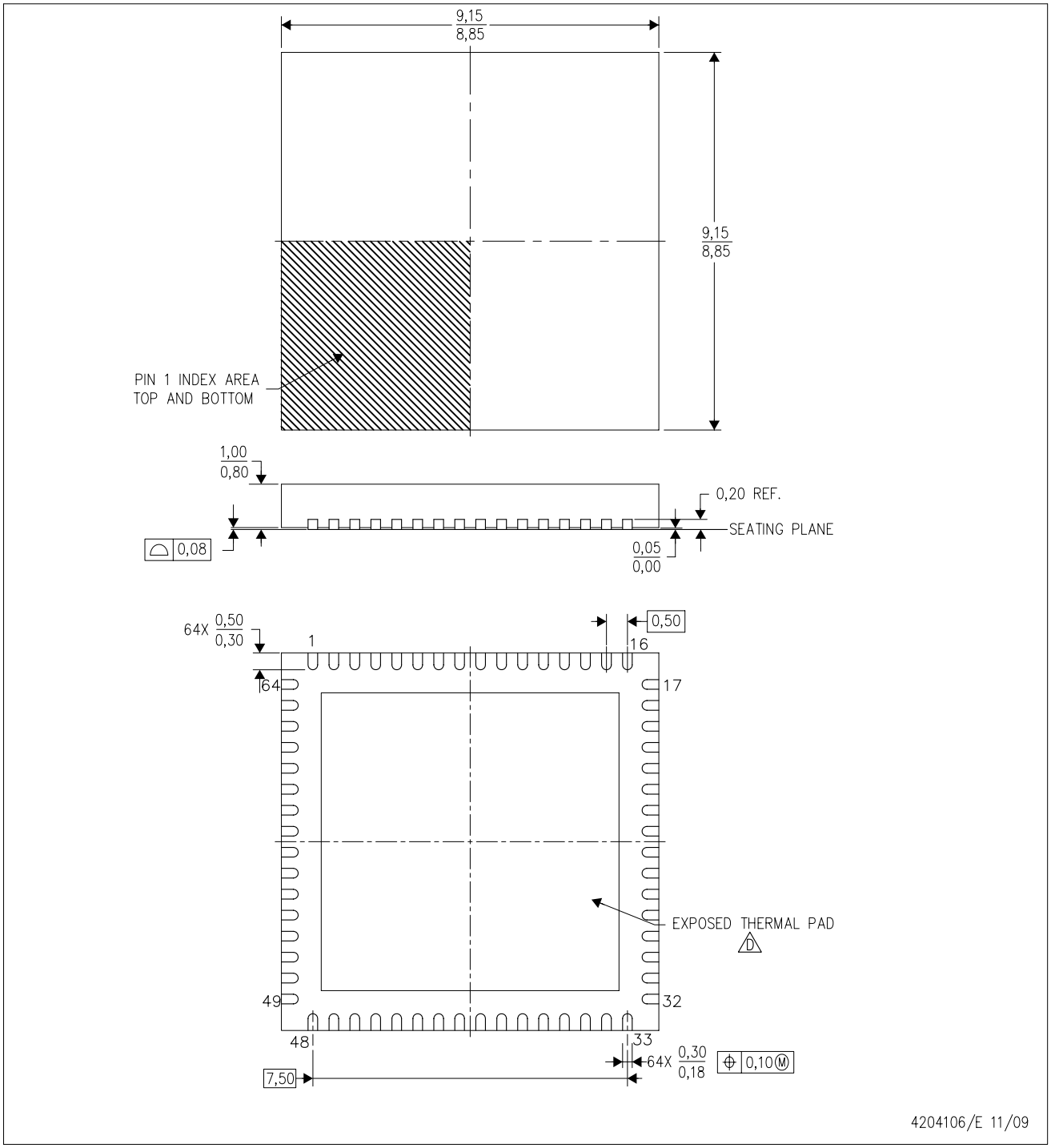
RGC(S–PVQFN–N64) CUSTOM DEVICE PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

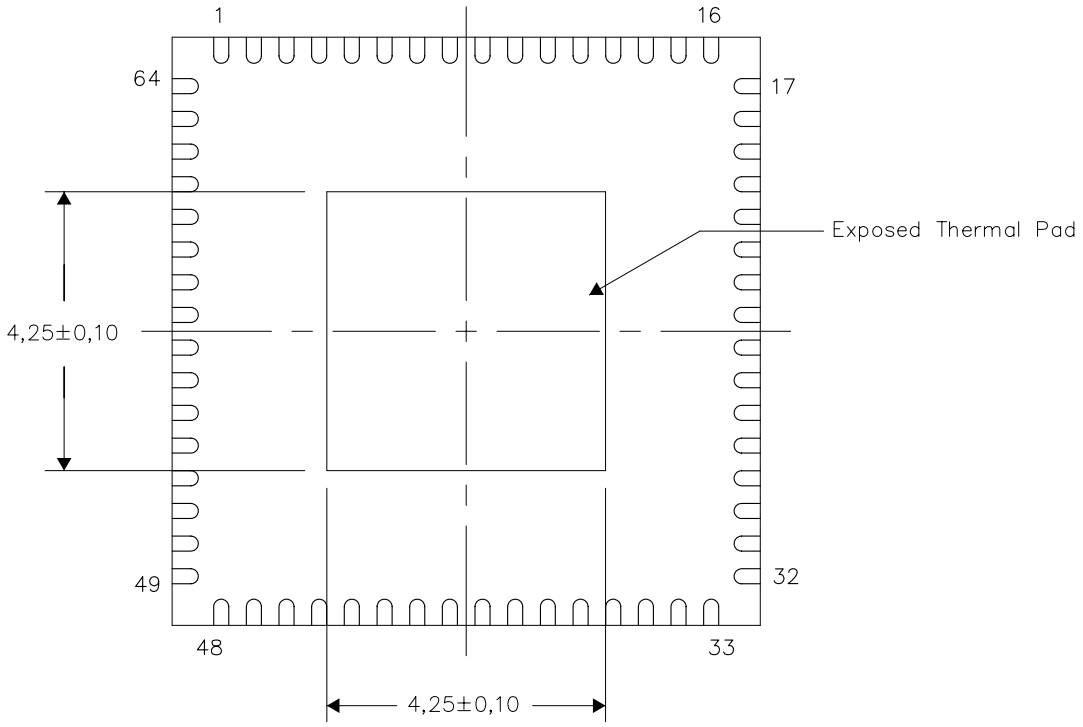
RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



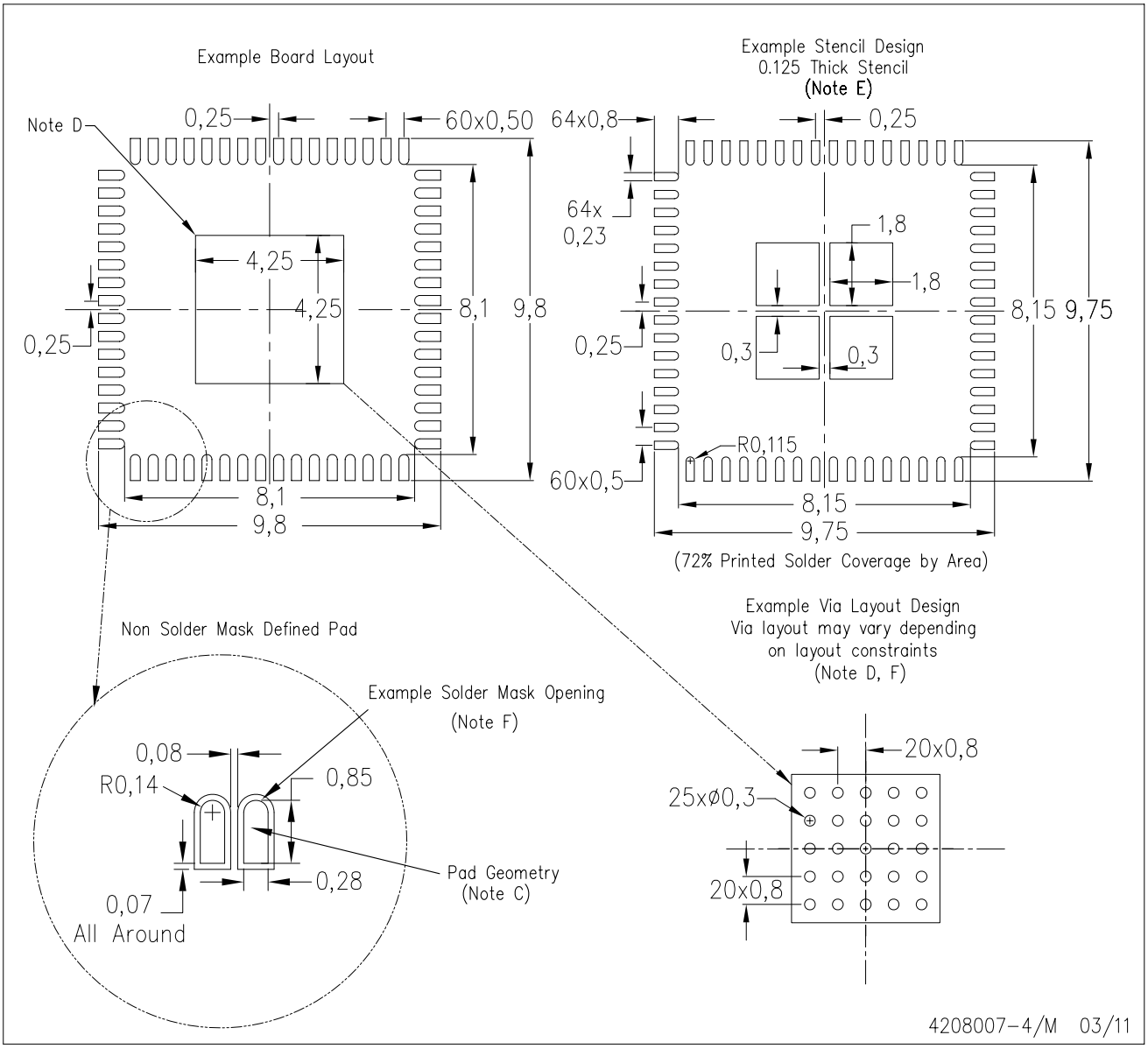
Bottom View

Exposed Thermal Pad Dimensions

4206192–3/0 04/11

NOTE: A. All linear dimensions are in millimeters

RGC (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in thermal pad.

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