NOIM1SM9600A, NOIM2SM9600A

Advance Information

MANO 9600 9.6 MegaPixel Rolling Shutter CMOS Image Sensor

ON Semiconductor®

http://onsemi.com

Features

- 9.6 MegaPixel Resolution in 3840 × 2500 Format
- 2.4 μm × 2.4 μm Square Pixels (Shared 4T Pixel Architecture)
- 2/3 inch Optical Format
- Monochrome (SM) Version
- 20 Frames per Second (fps) at Full Resolution
- 200 mW / 500 mW Power Consumption at 5 fps / 20 fps
- Four Low−Voltage Differential Signaling (LVDS) High Speed Serial Outputs or One 10−bit CMOS Output
- On-chip 10-bit Analog-to-Digital Converter (ADC)
- Windowing to Attain Higher Frame Rate
- Rolling Shutter
- On-chip Fixed Pattern Noise (FPN) Correction
- Serial Peripheral Interface (SPI)
- Automatic Exposure Control (AEC)
- Phase Locked Loop (PLL)
- High Dynamic Range (HDR)
- Dual Power Supply (1.8 V and 3.3 V)
- 0°C to 70°C Operational Temperature Range
- 52-pin LCC
- 500 mW Power Dissipation (LVDS)
- 200 mW Power Dissipation (CMOS)
- These Devices are Pb−Free and are RoHS Compliant



Figure 1. MANO 9600 Package Photograph

Applications

- Biometrics (Fingerprinting)
- Machine Vision
- Inspection
- Microscopy

Description

The MANO9600 is a rolling shutter CMOS image sensor with a resolution of 3840 x 2500 pixels.

The high sensitivity 2.4 μm x 2.4 μm pixels supports correlated double sampling readout reducing noise and increasing dynamic range.

A high level of programmability using a four wire serial peripheral interface enables the user to read out specific regions of interest.

Higher frame rates are achieved with region of interest or sub−sampled readout modes. The sensor has built−in features for bias control and power supply regulation.

The sensor has on−chip programmable gain amplifiers and 10−bit A/D converters. The integration time and gain parameters can be reconfigured without any visible image artifact. Optionally the on−chip automatic exposure control loop (AEC) controls these parameters dynamically. The image's black level is either calibrated automatically or can be adjusted by adding a user programmable offset.

The image data interface of the M1−SM part consists of four LVDS lanes running at 620 Mbps, facilitating frame rates up to 20 frames per second. A separate synchronization and clock channel containing payload information is provided to facilitate the image reconstruction at the receive end. The M2−SM part provides a parallel CMOS output interface at reduced frame rate of 5 frames per second.

The MANO 9600 is packaged in a 52−pin LCC package and is available in a monochrome without micro lens.

Contact your local ON Semiconductor office for more information.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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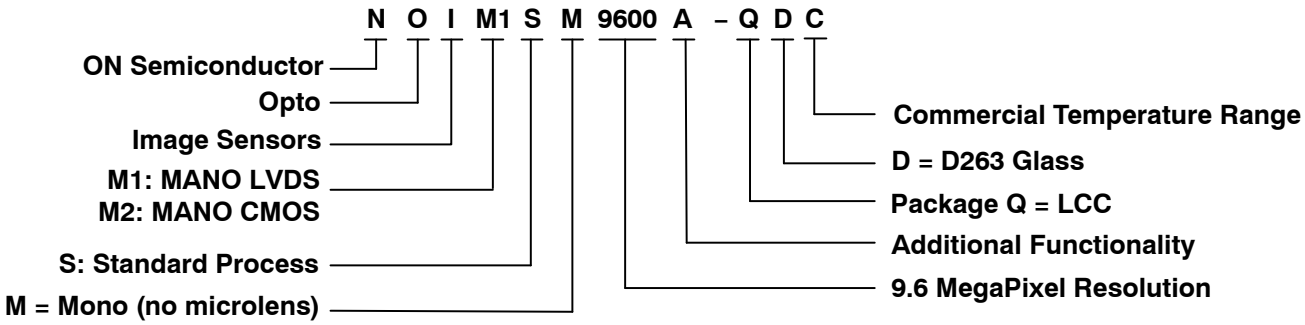
ORDERING INFORMATION

Part Number	Description	Package
NOIM1SM9600A-QDC	LVDS Interface mono	52−pin LCC package
NOIM2SM9600A-QDC	CMOS Interface mono	

The M1-SM base part is used to reference the mono version of the LVDS interface; the M2-SM base part is used to reference the mono version of the CMOS interface.

NOTE: The MANO 9600 does not utilize a micro lens.

ORDERING CODE DEFINITION



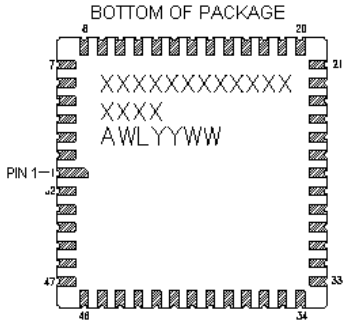
PACKAGE MARK

Following is the mark on the bottom side of the package with Pin 1 to the left center

Line 1: **NOI xx SM9600A** where xx denotes LVDS (M1) / CMOS (M2)

Line 2: **-QDC**

Line 3: **AWLYYWW**; where line 3 is the lot traceability as shown below



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
NNNN = Serial Number

Figure 2. Generic Package Mark

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SPECIFICATIONS

Key Specifications

Table 1. GENERAL SPECIFICATIONS

Parameter	Specification
Active pixels	3840 x 2500
Pixel size	2.4 μm x 2.4 μm (Shared 4T pixel architecture)
Shutter type	Rolling shutter
Master clock	M1-SM: 62 MHz when PLL is used, 310 MHz (10-bit) / 248 MHz (8-bit) when PLL is not used M2-SM: 62 MHz
ADC resolution	10-bit, 8-bit
LVDS outputs	M1-SM: 4 data + sync + clock
CMOS outputs	M2-SM: 10-bit parallel output, frame_valid, line_valid, clock
Data rate	M1-SM: 4 x 620 Mbps (10-bit) / 4 x 496 Mbps (8-bit) M2-SM: 62 MHz
Power dissipation	M1−SM in 10−bit mode: 700 mW at 20 fps frame rate M2−SM: 540 mW at 5 fps frame rate
Package type	52-pin LCC

Table 2. ELECTRO−OPTICAL SPECIFICATIONS

Parameter	Specification
Frame rate at full resolution	M1−SM: 20 fps M2−SM: 5 fps
Optical format	2/3 inch
Conversion gain	0.072 LSB10/e^- 56 μV/e^-
Dark noise	1.5 LSB10, 21 e^-
Responsivity at 550 nm	4 LSB10 /nJ/cm^2
Full well charge	13500 e^-
QE x FF	40% at 550 nm
Pixel FPN	1.3 LSB10
Row FPN	0.07 LSB10
Column FPN	1.3 LSB10
PRNU	< 4% of signal
Dark signal	13.8 e^-/s @ 25°C, 2.4 LSB10/s at +24°C
Dynamic range	54 dB
Signal to Noise Ratio (SNR)	40 dB

Table 3. RECOMMENDED OPERATING RATINGS (Note 1)

Symbol	Description	Min	Max	Units
T_J (Note 2)	Operating temperature range	0	70	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ABSOLUTE MAXIMUM RATINGS (Notes 2 and 3)

Symbol	Parameter	Min	Max	Units
ABS (1.8 V supply group)	ABS rating for 1.8 V supply group	−0.5	2.25	V
ABS (3.3 V supply group)	ABS rating for 3.3 V supply group	−0.5	4.3	V
T_S	ABS storage temperature range	0	150	°C
	ABS storage humidity range at 85°C		85	%RH
Electrostatic discharge (ESD)	Human Body Model (HBM): JS−001−2010	2000		V
	Charged Device Model (CDM): JESD22−C101	500		
LU	Latch-up: JESD−78	200		mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Operating ratings are conditions in which operation of the device is intended to be functional.
2. Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
3. ON Semiconductor recommends that customers become familiar with, and follow the procedures in JEDEC Standard JESD625−A. Refer to Application Note AN52561.

Table 5. ELECTRICAL SPECIFICATIONS

Boldface limits apply for $T_J = T_{MIN}$ to T_{MAX}, all other limits T_J = +30°C. (Notes 4, 5, 6 and 7)

Parameter	Description	Min	Typ	Max	Units
Power Supply Parameters					
Vdd_33	Supply voltage, 3.3 V	**3.1**	3.3	**3.6**	V
Vdd_18	Supply voltage, 1.8 V	**1.6**	1.8	**2**	V
Vdd_pix	Supply voltage, pixel	**3.1**	3.3	**3.6**	V
Idd_pix	Current consumption pixel supply	0.8	1	1.2	mA
Ptot_20fps/5fps	Total power consumption at 20 fps / 5 fps		700 / 540		mW
Pstby	Power consumption in standby mode			50	mW
Pstby_lp	Power consumption in low power standby mode			10	mW
Popt	Power consumption at lower pixel rates		Configurable		
I/O - LVCMOS (JEDEC- JESD8C-01) - Conforming to standard - additional specifications and deviations listed					
fpardata	Data rate on parallel channels			62	Mbps
Cout	Output load			10	pF
tr	Rise time	3	4.5	6	ns
tf	Fall time	2.5	3.5	5	ns
I/O - LVDS (EIA/TIA-644) - Conforming to standard - additional specifications and deviations listed					
fserdata	Data rate on data channels for 20 fps / 5 fps		620 / 150		Mbps
fserclock	Clock rate of output clock for 20 fps / 5 fps		310 / 75		MHz
Vicm	LVDS input common mode level	0.3	1.25	2.2	V
Tccsk	Channel to channel skew			50	ps
Electrical/Interface					
fin	Input clock rate for 20 fps / 5 fps			62 / 15	MHz
tidc	Input clock duty cycle	45	50	55	%
tj	Input clock jitter		20		ps
fspi	SPI clock rate for 20 / 5 fps			10 / 2.5	MHz
ratspi	Ratio: Fin/fspi	6			
Sensor Requirements					
fps	Frame rate at full resolution (CMOS / LVDS)			5 / 20	fps
fps_roi1	Xres x Yres = 3334 x 2500			5.8 / 24	fps
fps_roi2	Xres x Yres = 3840 x 2160			6 / 25	fps
fps_roi3	Xres x Yres = 1024 x 1024			32 / 135	fps
fps_roi4	Xres x Yres = 640 x 480			88 / 366	fps
fps_roi5	Xres x Yres = 512 x 512			91 / 377	fps
fps_roi6	Xres x Yres = 256 x 256			227 / 942	fps
ROT	Row Overhead Time at 20 / 5 fps		1.55 / 6.4		μs
fpix	Pixel rate minimum at 5 fps, maximum at 20 fps	60		248	Mpix/s
I/O - LVCMOS (JEDEC - JESD8C-01) - Conforming to standard - additional specifications and deviations listed					
fpardata	Data rate on parallel channels			62	fps

4. All parameters are characterized for DC conditions after thermal equilibrium is established.
5. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is recommended that normal precautions be taken to avoid application of any voltages higher than the maximum rated voltages to this high impedance circuit.
6. Minimum and maximum limits are guaranteed through test and design.
7. For recommendations on power supply management guidelines, refer to Application Note AN65464: VITA 2000 HSMC Cyclone Reference Board Design Recommendations.

OVERVIEW

Figure 3 and Figure 4 give an overview of the major functional blocks of the M1−SM and M2−SM sensor respectively. The system clock is received by the CMOS clock input. A PLL generates the internal, high speed, clocks, which are distributed to the other blocks. Optionally, the M1−SM can also accept a high speed LVDS clock, in which case the PLL will be disabled.

The sequencer defines the sensor timing and controls the image core. The sequencer is started either autonomously (master mode) or on assertion of an external trigger (slave mode). The image core contains all pixels and readout circuits. The column structure selects pixels for readout and performs correlated double sampling (CDS). The data comes out sequentially and is fed into the analog front end (AFE) block. The programmable gain amplifier (PGA) of the AFE adds the offset and gain. The output is a fully differential analog signal that goes to the ADC, where the analog signal is converted to a 10−bit data stream. Depending on the operating mode, eight or ten bits are fed into the data formatting block. This block adds synchronization information to the data stream based on the frame timing. For the M1−SM version, the data then goes to the low voltage serial (LVDS) interface block which sends the data out through the I/O ring. The M2−SM sensor does not have an LVDS interface but sends out the data through a 10−bit parallel interface.

On-chip programmability is achieved through the Serial Peripheral Interface (SPI). See the Register Map on page 44 for register details.

A bias block generates bias currents and voltages for all analog blocks on the chip. By controlling the bias current, the speed-versus-power of each block can be tuned. All biasing programmability is contained in the bias block.

The sensor can automatically control exposure and gain by enabling the automatic exposure control block (AEC). This block regulates the integration time along with the analog and digital gains to reach the desired intensity.

Image Core

The image core consists of:

- Pixel Array
- Address Decoders and Row Drivers
- Pixel Biasing

The pixel array contains 3840 (H) x 2500 (V) readable pixels with a pixel pitch of 2.4 μm. Four dummy pixel rows and columns are placed at every side of the pixel array to eliminate possible edge effects. The sensor uses a 4T pixel architecture, which makes it possible to read out the pixel array in rolling shutter mode with correlated double sampling (CDS).

The function of the row drivers is to access the image array line by line to reset or read the pixel data. The row drivers are controlled by the on-chip sequencer and can access the pixel array in rolling shutter modes.

The pixel biasing block guarantees that the data on a pixel is transferred properly to the column multiplexer when the row drivers select a pixel line for readout.

Phase Locked Loop

The PLL accepts a (low speed) clock and generates the required high speed clock. Optionally this PLL can be bypassed. Typical input clock frequency is 62 MHz.

LVDS Clock Receiver

The LVDS clock receiver receives an LVDS clock signal and distributes the required clocks to the sensor.

Typical input clock frequency is 310 MHz in 10-bit mode and 248 MHz in 8-bit mode. The clock input needs to be terminated with a 100 Ω resistor.

Column Multiplexer

All pixels of one image row are stored in the column sample-and-hold (S/H) stages. These stages store both the reset and integrated signal levels.

The data stored in the column S/H stages is read out through 8 parallel differential outputs operating at a frequency of 31 MHz.

At this stage, the reset signal and integrated signal values are transferred into an FPN-corrected differential signal.

The column multiplexer also supports read-1-skip-1 and checkerboard subsampling.

Bias Generator

The bias generator generates all required reference voltages and bias currents that the on-chip blocks use. An external resistor of 47 kΩ, connected between pin IBIAS_MASTER and gnd_33, is required for the bias generator to operate properly.

Analog Front End

The AFE contains 8 channels, each containing a PGA and a 10-bit ADC.

For each of the 8 channels, a pipelined 10-bit ADC is used to convert the analog image data into a digital signal, which is delivered to the data formatting block. A black calibration loop is implemented to ensure that the black level is mapped to match the correct ADC input level.

Data Formatting

The data block receives data from two ADCs and multiplexes this data to one data stream. A cyclic redundancy check (CRC) code is calculated on the passing data.

A frame synchronization data block is configured to transmit synchronization codes such as frame start, line start, frame end, and line end indications.

The data block calculates a CRC once per line for every channel. This CRC code can be used for error detection at the receiving end.

Serializer and LVDS Interface (M1−SM only)

The serializer and LVDS interface block receives the formatted (10-bit or 8-bit) data from the data formatting block. This data is serialized and transmitted by the LVDS output driver.

In 10-bit mode, the maximum output data rate is 620 Mbps per channel. In 8-bit mode, the maximum output data rate is 496 Mbps per channel.

In addition to the LVDS data outputs, two extra LVDS outputs are available. One of these outputs carries the output clock, which is skew aligned to the output data channels. The second LVDS output contains frame format synchronization codes to serve system-level image reconstruction.

Output MUX (M2−SM only)

The output MUX multiplexes the four data channels to one channel and transmits the data words using a 10-bit parallel CMOS interface.

Frame synchronization information is communicated by means of frame and line valid strobes.

Sequencer

The sequencer:

- Controls the image core. Starts and stops integration in rolling shutter mode and controls pixel readout.
- Applies the window settings. Organizes readouts so that only the configured window is read.
- Controls the column multiplexer and analog core. Applies gain settings and subsampling modes at the correct time, without corrupting image data.
- Starts up the sensor correctly when leaving standby mode.

Automatic Exposure Control

The AEC block implements a control system to modulate the exposure of an image. Both integration time and gains are controlled by this block to target a predefined illumination level.

Block Diagram

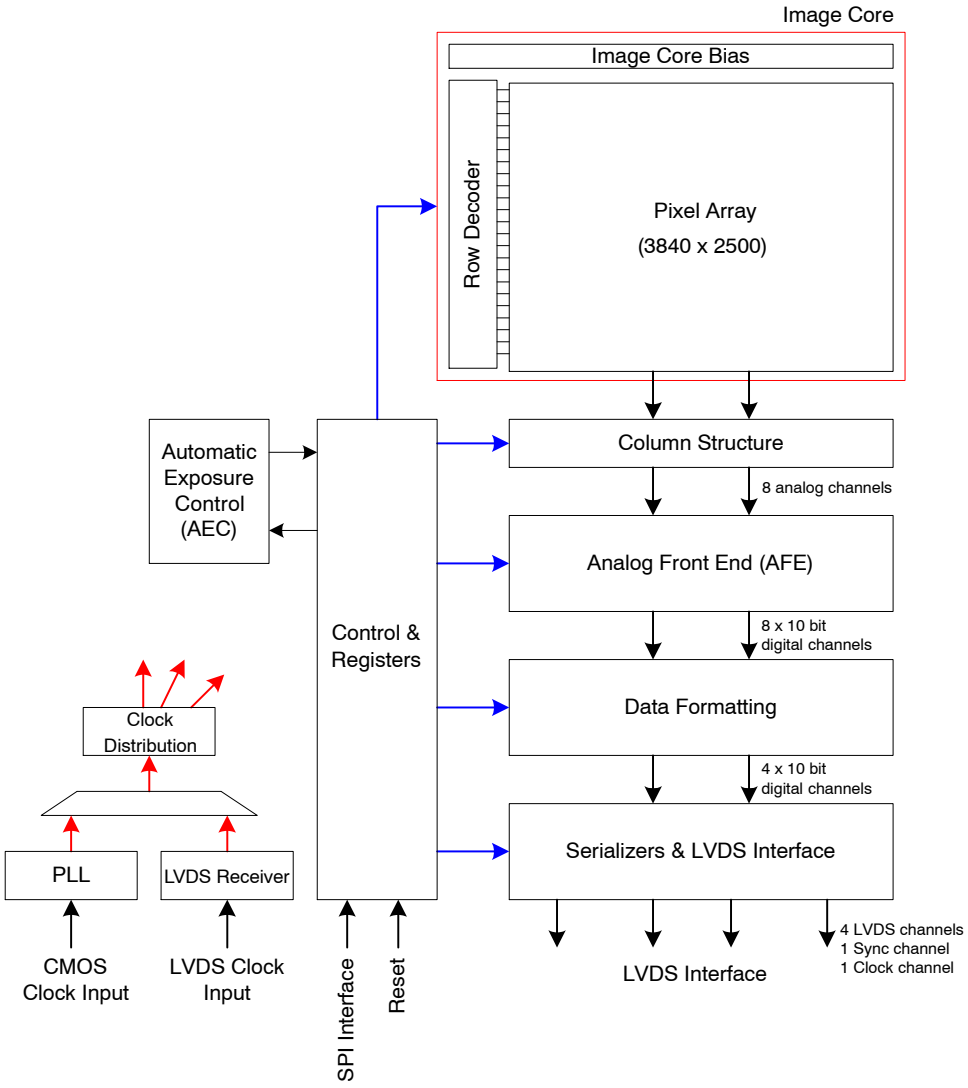


Figure 3. Block Diagram – M1−SM

Block Diagram

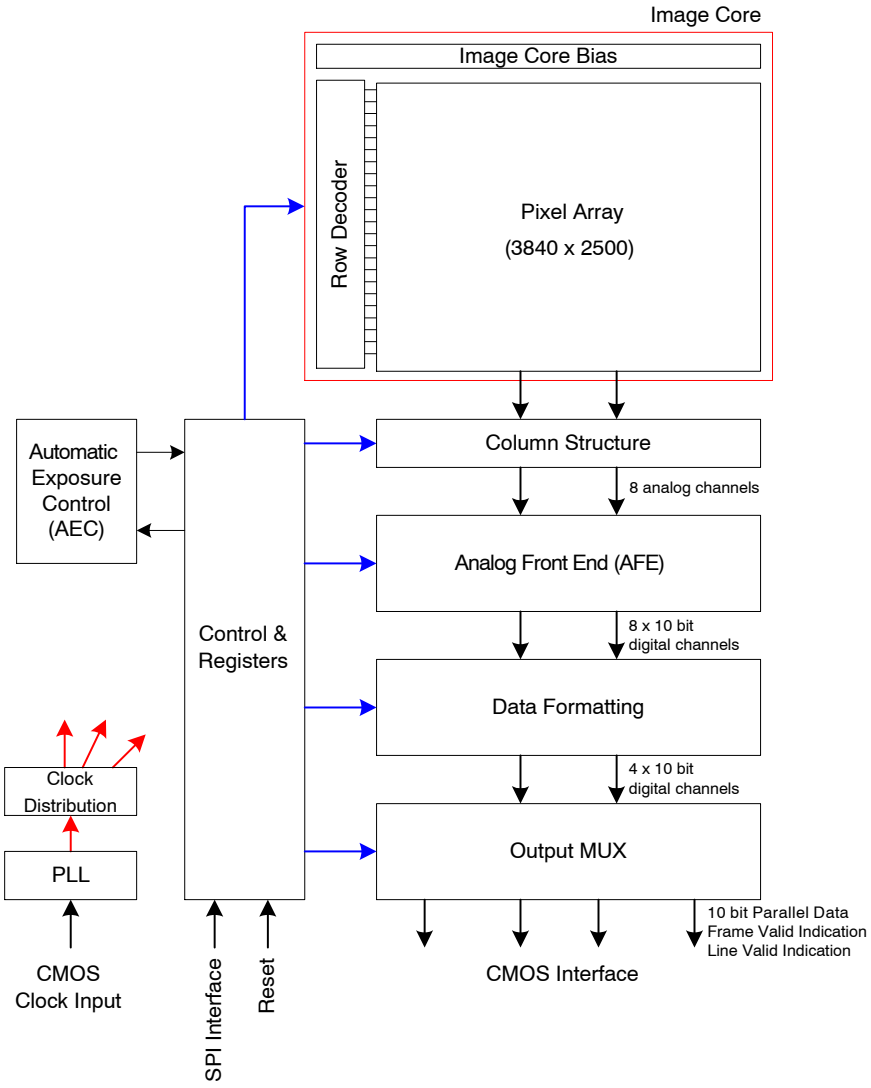


Figure 4. Block Diagram – M2−SM

OPERATING MODES

The MANO 9600 sensor operates in Rolling Shutter Mode

Rolling Shutter Mode

The shutter mechanism is an electronic rolling shutter and the sensor operates in a streaming mode similar to a video. This mechanism is controlled by the on-chip sequencer logic. There are two Y pointers. One points to the row that is to be reset for rolling shutter operation, the other points to the row to be read out. Functionally, a row is reset first and selected for read out sometime later. The time elapsed between these two operations is the exposure time.

Figure 5 schematically indicates the relative shift of the integration times of different lines during the rolling shutter operation. Each row is read and reset in a sequential way. Each row in a particular frame is integrated for the same time, but all lines in a frame 'see' a different stare time. As a consequence, fast horizontal moving objects in the field of view give rise to motion artifacts in the image; this is an unavoidable property of a rolling shutter.

In rolling shutter mode, the pixel Fixed Pattern Noise (FPN) is corrected on-chip by using the CDS technique. After light integration on all pixels in a row is complete, the storage node in the pixel is reset. Afterwards the integrated signal is transferred to that pixel storage node. The difference between the reset level and integrated signal is the FPN corrected signal. The advantage of this technique, compared to the DS technique used in the global shutter modes, is that the reset noise of the pixel storage node is cancelled. This results in a lower temporal noise level.

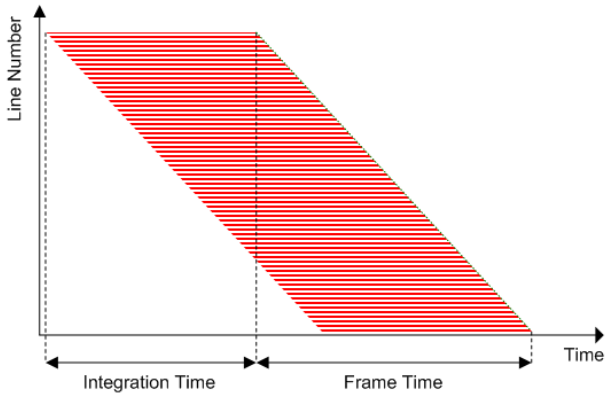


Figure 5. Rolling Shutter Operation

SENSOR OPERATION

Flowchart

Figure 6 shows the sensor operation flowchart. The sensor can be in six different 'states'. Every state is indicated with the oval circle. These states are:

- Power off
- Low power standby
- Standby (1)
- Standby (2)
- Idle
- Running

These states are ordered by power dissipation. In 'power-off' state, the power dissipation is minimal; in 'running' state the power dissipation is maximal.

On the other hand, the lower the power consumption, the more actions (and time) are required to put the sensor in 'running' state and grab images.

This flowchart allows the trade-off between power saving and enabling time of the sensor.

Next to the six 'states' a set of 'user actions', indicated by arrows, are included in the flowchart. These user actions make it possible to move from one state to another.

Sensor States

Power Off

In this state, the sensor is inactive. All power supplies are down and the power dissipation is zero.

Low Power Standby

In low power standby state, all power supplies are on, but internally every block is disabled. No internal clock is running (PLL / LVDS clock receiver is disabled). All register settings are unchanged.

Only a subset of the SPI registers is active for read/write in order to be able to configure clock settings and leave the low power standby state. The only SPI registers that should be touched are the ones required for the 'Enable Clock Management' action described in Enable Clock Management – Part 1 on page 12

Standby (1)

In standby state, the PLL/LVDS clock receiver is running, but the derived logic clock signal is not enabled.

Standby (2)

In standby state, the derived logic clock signal is running. All SPI registers are active, meaning that all SPI registers can be accessed for read or write operations. All other blocks are disabled.

Idle

In the idle state, all internal blocks are enabled, except the sequencer block. The sensor is ready to start grabbing images as soon as the sequencer block is enabled.

Running

In running state, the sensor is enabled and grabbing images.

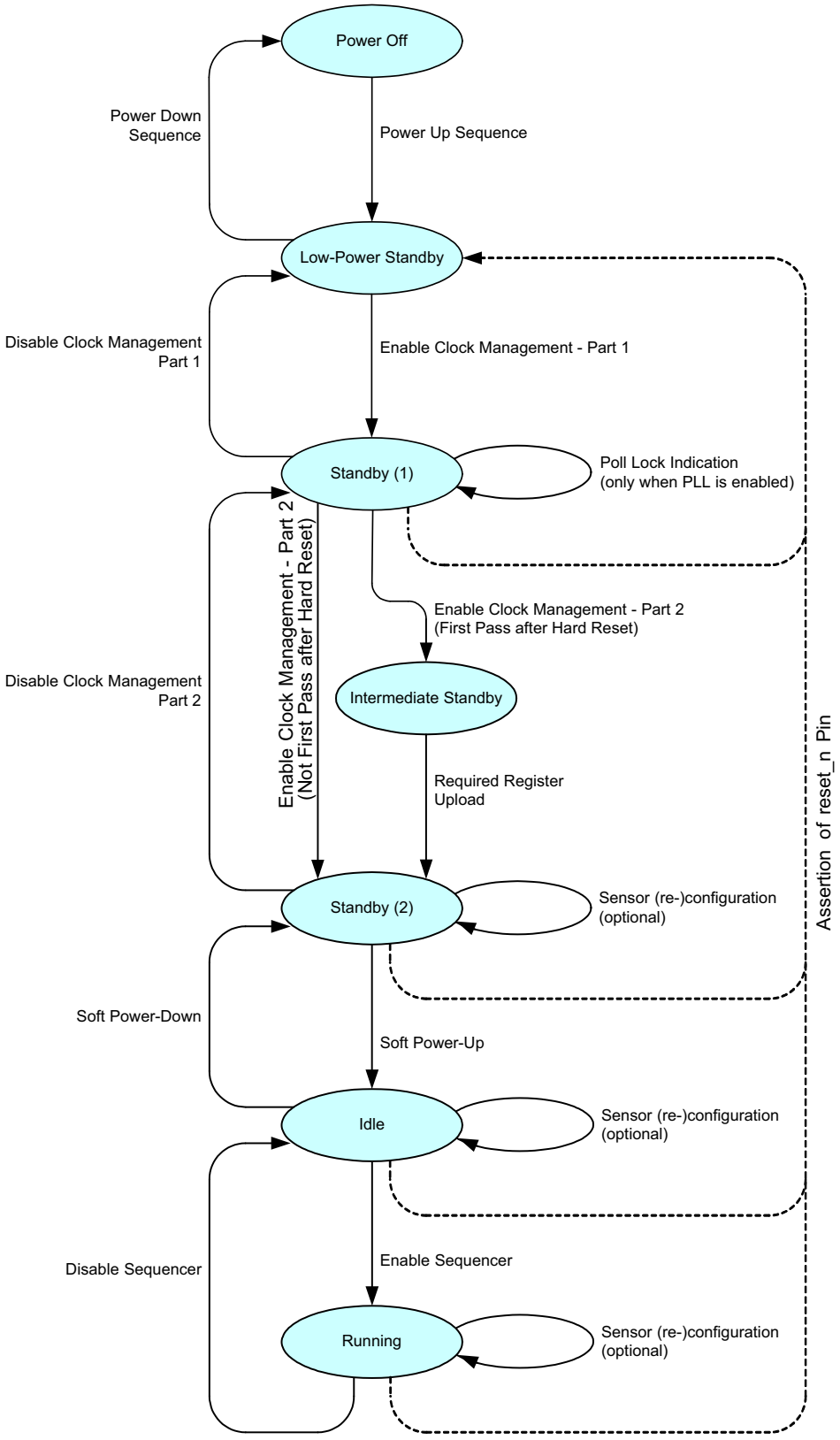


Figure 6. Sensor Operation Flowchart

User Actions: Power Up Functional Mode Sequences

Power Up Sequence

Figure 7 shows the power up sequence of the sensor. The figure indicates that the first supply to ramp-up is the vdd_18 supply, followed by vdd_33 and vdd_pix respectively. It is important to comply with the described sequence. Any other supply ramping sequence may lead to high current peaks and, as consequence, a failure of the sensor power up.

The clock input should start running when all supplies are stabilized. When the clock frequency is stable, the reset_n signal can be de-asserted. After a wait period of 10 μs, the power up sequence is finished and the first SPI upload can be initiated.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

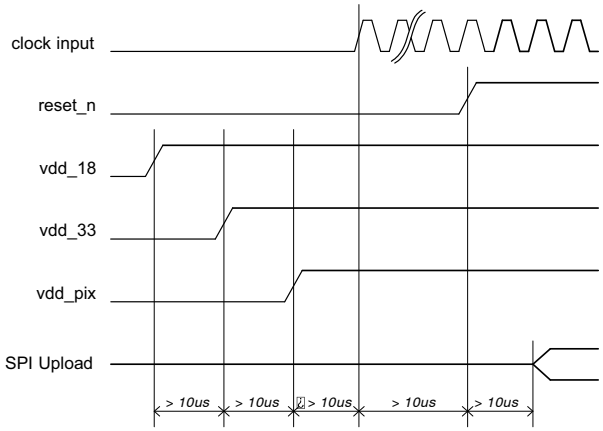


Figure 7. Power Up Sequence

Enable Clock Management − Part 1

The ‘Enable Clock Management’ action configures the clock management blocks and activates the clock generation and distribution circuits in a pre-defined way. First, a set of clock settings must be uploaded through the SPI register. These settings are dependent on the desired operation mode of the sensor.

Table 6 shows the SPI uploads to be executed to configure the sensor for M1-SM 8-bit serial, M1-SM 10-bit serial, or M2-SM 10-bit parallel mode, with and without the PLL.

In the serial modes, if the PLL is not used, the LVDS clock input must be running.

In the M2-SM 10-bit parallel mode, the PLL is bypassed. The clk_pll clock is used as sensor clock.

It is important to follow the upload sequence listed in Table 6.

Use of Phase Locked Loop

If PLL is used, the PLL is started after the upload of the SPI registers. The PLL requires (dependent on the settings) some time to generate a stable output clock. A lock detect circuit detects if the clock is stable. When complete, this is flagged in a status register.

NOTE: The lock detect status must not be checked for the M2-SM sensor.

Check this flag by reading the SPI register. When the flag is set, the ‘Enable Clock Management- Part 2’ action can be continued. When PLL is not used, this step can be bypassed as shown in Figure 6 on page 11.

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD − PART 1

Upload #	Address	Data	Description
M1-SM 8-bit mode with PLL			
1	2	0x0000	Monochrome sensor
2	32	0x200C	Configure clock generator
3	8	0x0000	Release PLL soft reset
4	16	0x0003	Enable PLL
M1-SM 8-bit mode without PLL			
1	2	0x0000	Monochrome sensor
2	32	0x2008	Configure clock management
3	20	0x0001	Enable LVDS clock input
M1-SM 10-bit mode with PLL			
1	2	0x0000	Monochrome sensor
2	32	0x2004	Configure clock generator
7	8	0x0000	Release PLL soft reset
8	16	0x0003	Enable PLL
M1-SM 10-bit mode without PLL			
1	2	0x0000	Monochrome sensor

Table 6. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD − PART 1

Upload #	Address	Data	Description
2	32	0x2000	Configure clock management
3	20	0x0001	Enable LVDS clock input
M2-SM 10-bit mode			
1	2	0x0002	Monochrome sensor parallel mode selection
2	32	0x200C	Configure clock management
3	2	0x0002	Parallel Mode selection
4	16	0x0007	Configure PLL bypass mode

Enable Clock Management - Part 2

The next step to configure the clock management consists of SPI uploads which enables all internal clock distribution. The required uploads are listed in Table 7. Note that it is important to follow the upload sequence listed in Table 7.

Table 7. ENABLE CLOCK MANAGEMENT REGISTER UPLOAD − PART 2

Upload #	Address	Data	Description
M1-SM 8-bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x200E	Enable logic clock
3	34	0x0001	Enable logic blocks
M1-SM 8-bit mode without PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x200A	Enable logic clock
3	34	0x0001	Enable logic blocks
M1-SM 10-bit mode with PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x2006	Enable logic clock
3	34	0x0001	Enable logic blocks
M1-SM 10-bit mode without PLL			
1	9	0x0000	Release clock generator soft reset
2	32	0x2002	Enable logic clock
3	34	0x0001	Enable logic blocks
M2-SM 10-bit mode			
1	9	0x0000	Release clock generator soft reset
2	32	0x200E	Enable logic clock
3	34	0x0001	Enable logic blocks

Required Register Upload

In this phase, the 'reserved' register settings are uploaded through the SPI register. Different settings are not allowed and may cause the sensor to malfunction. The required uploads are listed in Table 8.

NOTE: This table is subject to change.

Table 8. REQUIRED REGISTERED UPLOAD

Upload #	Address	Data
1	192	0x0800
2	42	0x0002
3	128	0x4320
4	205	0x00A0
5	129	0x0001
6	230	0x0044
7	231	0x09CB
8	197	0x2364
9	256	0x0000
10	257	0x01DF
11	258	0x0000
12	259	0x09C3
13	260	0x0000
14	261	0x01DF
15	262	0x0000
16	263	0x09C3
17	201	0x07D0
18	65	0x885B
19	72	0x0000
20	43	0x4701
21	384	0x0900
22	385	0x0BE1
23	386	0x0BC5
24	387	0x0381
25	388	0x0181
26	389	0x218F
27	390	0x2185
28	391	0x2101
29	392	0x0501
30	393	0x07C6
31	394	0x0781
32	395	0x0581
33	396	0x258F
34	397	0x2585
35	398	0x2501
36	399	0x0102
37	400	0x1346
38	401	0x0341
39	402	0x0141
40	403	0x214F
41	404	0x2145
42	405	0x2101
43	406	0x0501
44	407	0x0746
45	408	0x0741
46	409	0x0541
47	410	0x254F
48	411	0x2545
49	412	0x2501
50	413	0x0101
51	414	0x8101
52	415	0x8901
53	416	0x990E
54	417	0x8901
55	418	0x8901
56	419	0xC901
57	420	0xD90E
58	421	0xC901
59	422	0xC900
60	423	0x0900
61	424	0x1BE1
62	425	0x1BC5
63	426	0x1B89
64	427	0x0B82
65	428	0x0381
66	429	0x0181
67	430	0x218F
68	431	0x2185
69	432	0x2101
70	433	0x0501
71	434	0x07C6
72	435	0x0781
73	436	0x0581
74	437	0x258F
75	438	0x2585
76	439	0x2501
77	440	0x0102
78	441	0x1346
79	442	0x0341

REQUIRED REGISTERED UPLOAD
(Table 8. Continued)

Upload #	Address	Data
80	443	0x0141
81	444	0x214F
82	445	0x2145
83	446	0x2101
84	447	0x0501
85	448	0x0746
86	449	0x0741
87	450	0x0541
88	451	0x254F
89	452	0x2545
90	453	0x2501
91	454	0x0101
92	455	0x8101
93	456	0x990E
94	457	0x8901
95	458	0x8901
96	459	0xC901
97	460	0xD90E
98	461	0xC900
99	220	0x2700
100	462	0x0900
101	463	0x1BE1
102	464	0x1BC5
103	465	0x1B89
104	466	0x0B82
105	467	0x0381
106	468	0x0181
107	469	0x218F
108	470	0x2185
109	471	0x2101
110	472	0x0501
111	473	0x07C6
112	474	0x0781
113	475	0x0581
114	476	0x258F
115	477	0x2585
116	478	0x2501
117	479	0x0102
118	480	0x1346
119	481	0x0341
120	482	0x0141
121	483	0x2142
122	484	0x2101
123	485	0x0501
124	486	0x0746
125	487	0x0741
126	488	0x0541
127	489	0x2542
128	490	0x2501
129	491	0x0101
130	492	0x8101
131	493	0x990E
132	494	0x8901
133	495	0x8901
134	496	0xC901
135	497	0xD90E
136	498	0xC900
137	219	0x004E
138	499	0x0010
139	216	0x737F

NOTE: Upload #5: CMOS Mode only. Do NOT show line valid for black lines. [9:1]=0. Uncalibrated black offset
Upload #8: MUX BL coeffs. [13:13] = 1
Upload #20: Select DAC. [7:4]=0

Soft Power Up

During the soft power up action, the internal blocks are enabled and prepared to start processing the image data stream. This action exists of a set of SPI uploads. The soft power up uploads are listed in Table 9.

Table 9. SOFT POWER UP REGISTER UPLOADS FOR MODE DEPENDENT REGISTERS

Upload #	Address	Data	Description
M1-SM 8-bit mode with PLL			
1	32	0x200F	Enable analog clock distribution
2	112	0x0007	Enable LVDS transmitters
M1-SM 8-bit mode without PLL			
1	32	0x200B	Enable analog clock distribution
2	112	0x0007	Enable LVDS transmitters
M1-SM 10-bit mode with PLL			
1	32	0x2007	Enable analog clock distribution
2	112	0x0007	Enable LVDS transmitters
M1-SM 10-bit mode without PLL			
1	32	0x2003	Enable analog clock distribution
2	112	0x0007	Enable LVDS transmitters
M2-SM 10-bit mode			
1	32	0x200F	Enable analog clock distribution

Table 10. SOFT POWER UP FOR LVDS AND CMOS OUTPUTS

Upload #	Address	LVDS	CMOS
1	32	0x400F	0x200F
2	10	0x0000	0x0000
3	64	0x0001	0x0001
4	72	0x0000	0x0000
5	81	0x8880	0x8880
6	42	0x006E	0x006E
7	40	0x0003	0x0003
8	48	0x0001	0x0001
9	112	0x0007	0x0000
10	128	0x4320	

Enable Sequencer

During the ‘Enable Sequencer’ action, the frame grabbing sequencer is enabled. The sensor starts grabbing images in the configured operation mode. Refer to Sensor States on page 10 for an overview of the possible operation modes.

The ‘Enable Sequencer’ action consists of a set of register uploads. The required uploads are listed in Table 11.

Table 11. ENABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data	Description
1	192	0x0003	Enable of Sequencer in rolling shutter mode **Note**: this address contains other configuration bits to select the operation mode

User Actions: Functional Modes to Power Down Sequences

Disable Sequencer

During the ‘Disable Sequencer’ action, the frame grabbing sequencer is stopped. The sensor stops grabbing images and returns to the idle mode.

The ’Disable Sequencer’ action consists of a set of register uploads. as listed in Table 12.

Table 12. DISABLE SEQUENCER REGISTER UPLOAD

Upload #	Address	Data	Description
1	192	0x0002	Disable sequencer. **Note** that this address contains other configuration bits to select the operation mode.

Soft Power Down

During the soft power down action, the internal blocks are disabled and the sensor is put in standby state to reduce the current dissipation. This action exists of a set of SPI uploads. The soft power down uploads are listed in Table 13.

Table 13. SOFT POWER DOWN REGISTER UPLOAD

Upload #	Address	Data	Description
1	112	0x0000	Disable LVDS transmitters
2	48	0x0000	Disable AFE
3	40	0x0000	Disable column multiplexer
4	64	0x0000	Disable biasing block
5	10	0x0999	Soft reset

Disable Clock Management - Part 2

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 14.

Table 14. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
M1-SM 8-bit mode with PLL			
1	34	0x0000	Disable logic blocks
2	32	0x200C	Disable logic clock
3	9	0x0009	Soft reset clock generator
M1-SM 8-bit mode without PLL			
1	34	0x0000	Disable logic blocks
2	32	0x2008	Disable logic clock
3	9	0x0009	Soft reset clock generator
M1-SM 10-bit mode with PLL			
1	34	0x0000	Disable logic blocks
2	32	0x2004	Disable logic clock
3	9	0x0009	Soft reset clock generator
M2-SM 10-bit mode without PLL			
1	34	0x0000	Disable logic blocks
2	32	0x2000	Disable logic clock
3	9	0x0009	Soft reset clock generator
M2-SM 10-bit mode			

Table 14. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 2

Upload #	Address	Data	Description
1	34	0x0000	Disable logic blocks
2	32	0x200C	Disable logic clock
3	9	0x0009	Soft reset clock generator

Disable Clock Management - Part 1

The ‘Disable Clock Management’ action stops the internal clocking to further decrease the power dissipation. This action can be implemented with the SPI uploads as shown in Table 15.

Table 15. DISABLE CLOCK MANAGEMENT REGISTER UPLOAD – PART 1

Upload #	Address	Data	Description
1	16	0x0000	Disable PLL
2	8	0x0099	Soft reset PLL
3	20	0x0000	Configure clock management

Power Down Sequence

Figure 8 illustrates the timing diagram of the preferred power down sequence. It is important that the sensor is in reset before the clock input stops running. Otherwise, the internal PLL becomes unstable and the sensor gets into an unknown state. This can cause high peak currents.

The same applies for the ramp down of the power supplies. The preferred order to ramp down the supplies is first vdd_pix, second vdd_33, and finally vdd_18. Any other sequence can cause high peak currents.

NOTE: The ‘clock input’ can be the CMOS PLL clock input (clk_pll), or the LVDS clock input (lvds_clock_inn/p) in case the PLL is bypassed.

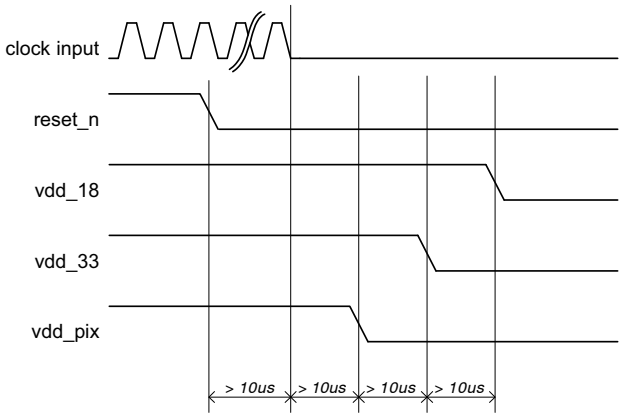


Figure 8. Power Down Sequence

Sensor Reconfiguration

During the standby, idle, or running state several sensor parameters can be reconfigured.

- Frame Rate and Exposure Time: Frame rate and exposure time changes can occur during standby, idle, and running states.
- Signal Path Gain: Signal path gain changes can occur during standby, idle, and running states.
- Windowing: Changes with respect to windowing can occur during standby, idle, and running states. Refer to Window Readout on page 25.
- Subsampling: Changes of the subsampling mode can occur during standby, idle, and running states. Refer to Subsampling and Binning on page 26 for more information.

Sensor Configuration

This device contains multiple configuration registers. Some of these registers can only be configured while the sensor is not acquiring images (while register 192[0] = 0), while others can be configured while the sensor is acquiring images. For the latter category of registers, it is possible to distinguish the register set that can cause corrupted images (limited number of images containing visible artifacts) from the set of registers that are not causing corrupted images.

These three categories are described here.

Static Readout Parameters

Some registers are only modified when the sensor is not acquiring images. Reconfiguration of these registers while images are acquired can cause corrupted frames or even interrupt the image acquisition. Therefore, it is recommended to modify these static configurations while the sequencer is disabled (register 192[0] = 0). The registers shown in Table 16 should not be reconfigured during image acquisition. A specific configuration sequence applies for these registers. Refer to the operation flow and startup description.

Table 16. STATIC READOUT PARAMETERS

Group	Addresses	Description
Clock generator	32	Configure according to recommendation
Image core	40	Configure according to recommendation
AFE	48	Configure according to recommendation
Bias	64–71	Configure according to recommendation
LVDS	112	Configure according to recommendation
All reserved registers		Keep reserved registers to their default state, unless otherwise described in the recommendation

Dynamic Configuration Potentially Causing Image Artifacts

The category of registers as shown in Table 16 consists of configurations that do not interrupt the image acquisition process, but may lead to one or more corrupted images during and after the re-configuration. A corrupted image is an image containing visible artifacts. A typical example of a corrupted image is an image which is not uniformly exposed.

The effect is transient in nature and the new configuration is applied after the transient effect.

Table 17. DYNAMIC CONFIGURATION POTENTIALLY CAUSING IMAGE ARTIFACTS

Group	Addresses	Description
Black level configuration	128–129 197[8]	Reconfiguration of these registers may have an impact on the black-level calibration algorithm. The effect is a transient number of images with incorrect black level compensation.
Sync codes	129[13] 130–135	Incorrect sync codes may be generated during the frame in which these registers are modified.
Datablock test configurations	144–150	Modification of these registers may generate incorrect test patterns during a transient frame.

Dynamic Readout Parameters

It is possible to reconfigure the sensor while it is acquiring images. Frame-related parameters are internally resynchronized to frame boundaries, such that the modified parameter does not affect a frame that has already started. However, there can be restrictions to some registers as shown in Table 18. Some reconfiguration may lead to one frame being blanked. This happens when the modification requires more than one frame to settle. The image is blanked out and training patterns are transmitted on the data and sync channels.

Table 18. DYNAMIC READOUT PARAMETERS

Group	Addresses	Description
Subsampling/binning	232[4:0]	Subsampling or binning is synchronized to a new frame start. Subsampling / binning also required to reconfigure black line address (230[9:5]), last line address 231[12:0] and Y−start offset (230[4:0]) as mentioned in detail in register map given in Table 45 on page 44. Reconfiguration of these parameters cause one frame to be blanked out
Black lines	197	Reconfiguration of these parameters causes one frame to be blanked out as the reset pointers need to be recalculated for the new frame timing.
Dummy lines	198	Reconfiguration of these parameters causes one frame to be blanked out as the reset pointers need to be recalculated for the new frame timing.
ROI configuration	195 256−263	Optionally, it is possible to blank out one frame after reconfiguration of the active ROI in rolling shutter mode. Therefore, register 192[9] must be asserted (blank_roi_switch configuration). A ROI switch is only detected when a new window is selected as the active window (reconfiguration of register 195). Reconfiguration of the ROI dimension of the active window does not lead to a frame blank and can cause a corrupted image.
Exposure reconfiguration	203	Exposure reconfiguration does not cause artifact.
Gain reconfiguration	204	Gains are synchronized at the start of a new frame. Optionally, one frame latency can be incorporated to align the gain updates to the exposure updates (refer to register 199[13] - gain_lat_comp).

Freezing Active Configurations

Though the readout parameters are synchronized to frame boundaries, an update of multiple registers can still lead to a transient effect in the subsequent images, as some configurations require multiple register uploads. For example, to reconfigure sub−sampling / binning scheme we also need to update black line address, Y−start offset and last line address registers. Internally, the sensor synchronizes these configurations to frame boundaries, but it is still possible that the reconfiguration of multiple registers spans over two or even more frames. To avoid inconsistent combinations, freeze the active settings while altering the SPI registers by disabling synchronization for the corresponding functionality before reconfiguration. When all registers are uploaded, re−enable the synchronization. The sensor's sequencer then updates its active set of registers and uses them for the coming frames. The freezing of the active set of registers can be programmed in the sync_configuration registers, which can be found at the SPI address 206.

Figure 9 shows a re-configuration that does not use the sync_configuration option. As depicted, new SPI configurations are synchronized to frame boundaries.

With sync_configuration = '1'. Configurations are synchronized to the frame boundaries.

Figure 10 shows the usage of the sync_configuration settings. Before uploading a set of registers, the corresponding sync_configuration is de-asserted. After the upload is completed, the sync_configuration is asserted again and the sensor resynchronizes its set of registers to the coming frame boundaries.

As seen in the figure, this ensures that the uploads performed at the end of frame N+2 and the start of frame N+3 become active in the same frame (frame N+4).

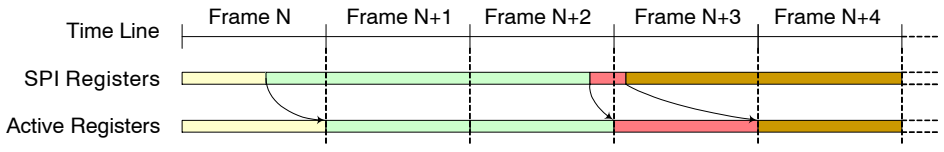


Figure 9. Frame Synchronization of Configurations (no freezing)

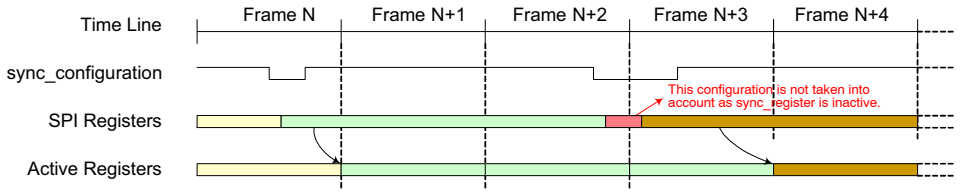


Figure 10. Reconfiguration Using Sync_configuration

NOTE: SPI updates are not taken into account while sync_configuration is inactive. The active configuration is frozen for the sensor. Table 19 lists the several sync_configuration possibilities along with the respective registers being frozen.

Table 19. ALTERNATE SYNC CONFIGURATIONS

Group	Affected Registers	Description
sync_rs_x_length	rs_x_length	Update of x−length configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_black_lines	black_lines	Update of black line configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_dummy_lines	dummy_lines	Update of dummy line configuration is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_exposure	mult_timer fr_length exposure	Update of exposure configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_gain	mux_gainsw afe_gain	Update of gain configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations.
sync_roi	roi_active0[7:0] subsampling binning black line address last line address Y−start offset	Update of active ROI configurations is not synchronized at start of frame when ‘0’. The sensor continues with its previous configurations. **Note:** The window configurations themselves are not frozen. Reconfiguration of active windows is not gated by this setting.

Table 20. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

Group	Addresses	Description
Black Line Generation		
197[7:0]	black_lines	This register configures the number of black lines that are generated at the start of a frame. At least one black line must be generated. The maximum number is 127. **Note:** When the automatic black-level calibration algorithm is enabled, make sure that this register is configured properly to produce sufficient black pixels for the black-level filtering. The number of black pixels generated per line is dependent on the operation mode and window configurations: As the line length is fundamental for rolling shutter operation, the length of a black line is defined by the active window.
197[8:9]	gate_first_line	When asserting this configuration, the first black lines of the frame are blanked out and is not used for black calibration. It is recommended to enable this functionality, because the first black lines can have a different behavior caused by boundary effects. When enabling, the number of black lines must be set to at least two in order to have valid black samples for the calibration algorithm.

Table 20. CONFIGURABLE PARAMETERS FOR BLACK LEVEL ALGORITHM

Group	Addresses	Description
Black Value Filtering		
129[0]	auto_blackcal_enable	Internal black-level calibration functionality is enabled when set to ‘1’. Required black level offset compensation is calculated on the black samples and applied to all image pixels. When set to ‘0’, the automatic black-level calibration functionality is disabled. It is possible to apply an offset compensation to the image pixels, which is defined by the registers 129[10:1]. **Note:** Black sample pixels are not compensated; the raw data is sent out to provide external statistics and, optionally, calibrations.
129[9:1]	blackcal_offset	Black calibration offset that is added or subtracted to each regular pixel value when auto_blackcal_enable is set to ‘0’. The sign of the offset is determined by register 129[10] (blackcal_offset_dec). **Note:** All channels use the same offset compensation when automatic black calibration is disabled. The calculated black calibration factors are frozen when this register is set to 0x1FF (all−‘1’) in auto calibration mode. Any value different from 0x1FF re-enables the black calibration algorithm. This freezing option can be used to prevent eventual frame to frame jitter on the black level as the correction factors are recalculated every frame. It is recommended to enable the black calibration regularly to compensate for temperature changes.
129[10]	blackcal_offset_dec	Sign of blackcal_offset. If set to ‘0’, the black calibration offset is added to each pixel. If set to ‘1’, the black calibration offset is subtracted from each pixel. This register is not used when auto_blackcal_enable is set to ‘1’.
128[10:8]	black_samples	The black samples are low-pass filtered before being used for black level calculation. The more samples are taken into account, the more accurate the calibration, but more samples require more black lines, which in turn affects the frame rate. The effective number of samples taken into account for filtering is 2^ black_samples. **Note:** An error is reported by the device if more samples than available are requested (refer to register 136).

Serial Peripheral Interface

The sensor configuration registers are accessed through an SPI. The SPI consists of four wires:

- sck: Serial Clock
- ss_n: Active Low Slave Select
- mosi: Master Out, Slave In, or Serial Data In
- miso: Master In, Slave Out, or Serial Data Out

The SPI is synchronous to the clock provided by the master (sck) and asynchronous to the sensor's system clock. When the master wants to write or read a sensor's register, it selects the chip by pulling down the Slave Select line (ss_n). When selected, data is sent serially and synchronous to the SPI clock (sck).

Figure 11 shows the communication protocol for read and write accesses of the SPI registers. The MANO 9600 sensor uses 9-bit addresses and 16-bit data words.

Data driven by the system is colored blue in Figure 11, while data driven by the sensor is colored yellow. The data in grey indicates high-Z periods on the miso interface. Red markers indicate sampling points for the sensor (mosi sampling); green markers indicate sampling points for the system (miso sampling during read operations).

The access sequence is:

1. Select the sensor for read or write by pulling down the ss_n line.
2. One SPI clock cycle after selecting the sensor, the 9-bit data is transferred, most significant bit first. The sck clock is passed through to the sensor as indicated in Figure 11. The sensor samples this data on a rising edge of the sck clock (mosi needs to be driven by the system on the falling edge of the sck clock).
3. The tenth bit sent by the master indicates the type of transfer: high for a write command, low for a read command.
4. Data transmission:
   - For write commands, the master continues sending the 16-bit data, most significant bit first.
   - For read commands, the sensor returns the requested address on the miso pin, most significant bit first. The miso pin must be sampled by the system on the falling edge of sck (assuming nominal system clock frequency and maximum 10 MHz SPI frequency).
5. When data transmission is complete, the system deselects the sensor one clock period after the last bit transmission by pulling ss_n high.

Maximum frequency for the SPI depends on the input clock and type of sensor. The frequency is $1/6^{th}$ of the PLL input clock or $1/30^{th}$ (in 10-bit mode) and $1/24^{th}$ (in 8-bit mode) of the LVDS input clock frequency.

At nominal input frequency (62 Mhz / 310 MHz / 248 MHz), the maximum frequency for the SPI is 10 MHz. Bursts of SPI commands can be issued by leaving at least two SPI clock periods between two register uploads. Deselect the chip between the SPI uploads by pulling the ss_n pin high.

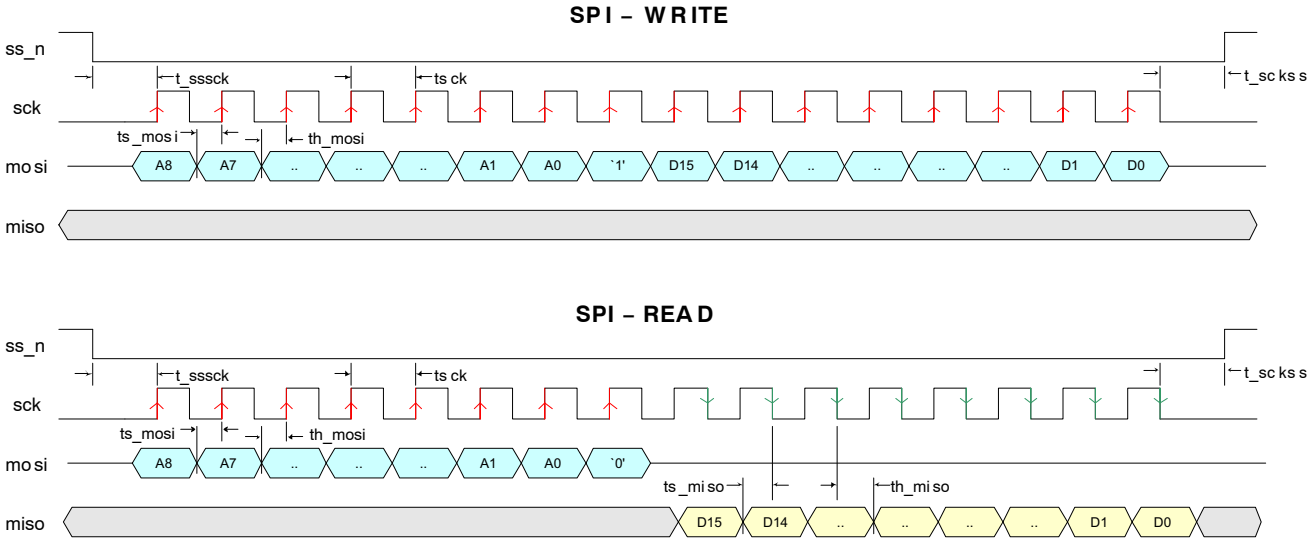


Figure 11. SPI Read and Write Timing Diagram

Rolling Shutter Mode

The exposure time during rolling shutter mode is always an integer multiple of line-times. The exposure time is defined by the register exposure and expressed in number of lines. The register fr_length and mult_timer are not used in this mode.

The maximum exposure time is limited by the frame time. It is possible to increase the exposure time at the cost of the frame rate by adding so called dummy lines. A dummy line lasts for the same time as a regular line, but no pixel data is transferred to the system. The number of dummy lines is controlled by the register dummy_lines. The rolling shutter exposure mechanism is graphically shown in Figure 12.

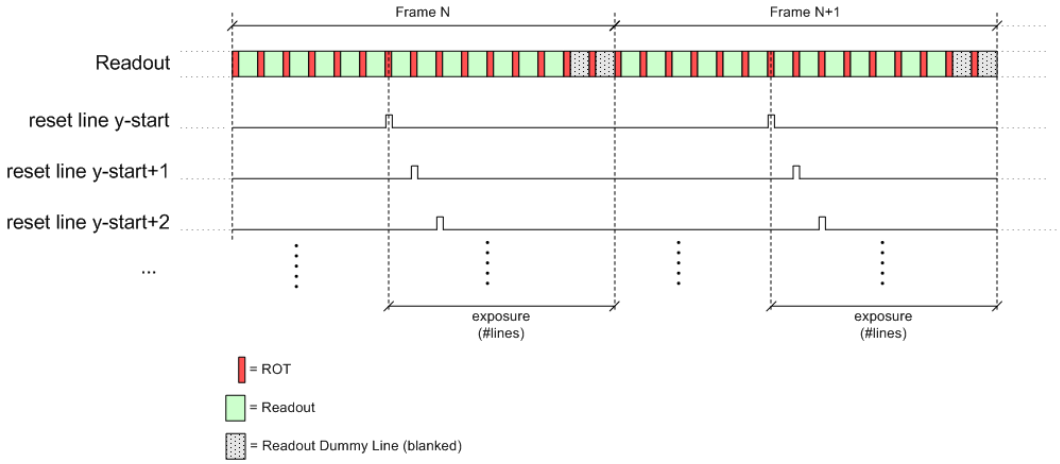


Figure 12. Integration Control in Rolling Shutter Mode

Note:

The duration of one line is the sum of the ROT and the time required to read out one line (depends on the number of active kernels in the window). Optionally, this readout time can be extended by the configuration rs_x_length. This register, expressed in number of periods of the logic clock (16.129 ns for the M1-SM version and 64.516 ns for the M2-SM version), determines the length of the x-readout. However, the minimum for rs_x_length is governed by the window size (x-size).

It is clear that when the number of rows and/or the length of a row are reduced (by windowing or subsampling), the frame time decreases and consequently the frame rate increases.

To be able to artificially increase the frame time, it is possible to:

- add dummy clock cycles to a row time
- add dummy rows to the frame

ADDITIONAL FEATURES

Multiple Window Readout

The MANO9600 sequencer supports windowed readout. The user can limit the data output per frame, which allows increasing the frame rate.

Window Configuration

Only a single window is supported. Do not activate more than one window (register 195). However, it is possible to configure more than one window and dynamically switch between the different window configurations. Note that switching between two different windows might result in a corrupted frame. This is inherent in the rolling shutter mechanism, where each line must be reset sequentially before being read out. This corrupted window can be blanked out by setting register 206[8]. In this case, a dead time is noted on the LVDS interface when the window−switch occurs in the sensor. During this blank out, training patterns are sent out on the data and sync channels for the duration of one frame.

Silicon Restriction when Switching between ROIs

- TRIGGER CONDITION(S)
  - Y_start line is lower than previous y_start line
- SCOPE OF IMPACT
  - Frame_valid fails and sensor stops operating
- RECOMMENDATION
  - Ensure that register 206[8] = 1. (blank_roi_switch)
  - To set a new roi:
    reg 206[5] = 0 // Disable sync_roi
    … // Update roi−settings of the _active_roi here.
    reg 206[5] = 1 // Re−enable sync_roi

Figure 13 shows the four parameters defining a region of interest (ROI).

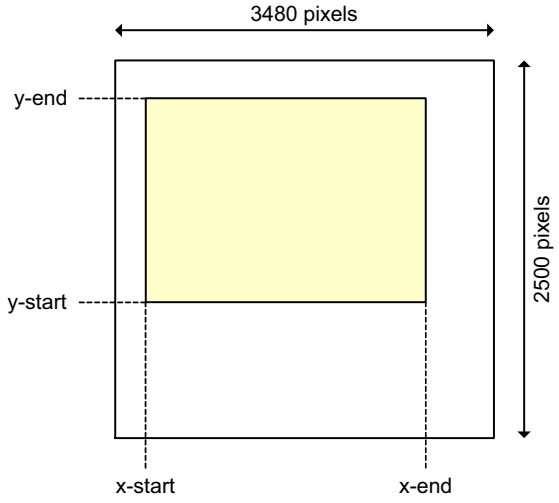


Figure 13. Region of Interest Configuration

- x−start[8:0]

x-start defines the x-starting point of the desired window. The sensor reads out 8 pixels in one single clock cycle. As a consequence, the granularity for configuring the x-start position is also 8 pixels for no sub sampling. The value configured in the x-start register is multiplied by 8 to find the corresponding column in the pixel array when there is no subsampling / binning.

- x-end[8:0]

This register defines the window end point on the x-axis. Similar to x-start, the granularity for this configuration is one kernel. x-end needs to be larger than x-start.

- y-start[12:0]

The starting line of the readout window. The granularity of this setting is one line.

- y-end[12:0]

The end line of the readout window. y-end must be configured larger than y-start. This setting has the same granularity as the y-start configuration.

Pixel array addressing scheme for no−subsampling/ binning.

Address mapping of pixel array rows to on−chip sequencer is shown in Table 21 as per following formula:

Y-address of sequencer = row number

Table 21. SEQUENCER Y-ADDRESS MAPPING FOR NO-SUBSAMPLING / BINNING

Row number	Sequencer Y-address
0	0
1	1
2	2
3	3
4	4
5	5
…	…
…	…
2497	2497
2498	2498
2499	2499

Even columns of pixel array are addressed by the sequencer through following mapping:

X-address of sequencer × 8 + 1 = pixel array column number

Odd columns of pixel array are addressed by sequencer through following mapping:

(X-address of sequencer − 1) × 8 + 1 = pixel array column number

Table 22 shows the column to its read out address mapping in sequencer for even and odd kernels of a row.

Table 22. SEQUENCER X-ADDRESS MAPPING FOR NO-SUBSAMPLING / BINNING

Pixel Array Column No.	Kernel Number	Sequencer X-address
0−14 (every second pixel)	0	0
1−15 (every second pixel)	1	1
16−30 (every second pixel)	2	2
17−31 (every second pixel)	3	3
−	−	−
3808−3822 (every second pixel)	476	476
3809−3823 (every second pixel)	477	477
3824−3838 (every second pixel)	478	478
3825−3839 (every second pixel)	479	479

Subsampling and Binning

Subsampling is used to reduce the image resolution. This allows increasing the frame rate. Two subsampling modes are supported: Read−1−Skip−1 and checkerboard subsampling. Pixel binning is also supported to increase the dynamic range of the sensor. Two binning schemes are supported: 1x2 and 2x2. During these sub−sampling/ binning schemes, address mapping of pixel array rows and columns to on−chip sequencer Y−address and X−address respectively, is different from no−subsampling. So user should configure windows according to the appropriate address mapping explained in detail for each subsampling/ binning scheme in following sections.

Following table shows an example of freezing and releasing of the register updates, to reconfigure subsampling/binning scheme.

Table 23. UPLOAD SEQUENCE FOR SUBSAMPLING / BINNING

Addresses	Data	Description
206[5]	0x0	De−assert sync_roi. The sensor continues with its previous configurations.
232		Enable/disable the required sub−sampling / binning as mentioned in detail in register map, given in Table 45 on page 44
230		Reconfigure Y−start offset and black line address as mentioned in detail in register map, given in Table 45 on page 44 for required subsampling / binning
231		Reconfigure last line address as mentioned in detail in register map, given in Table 45 on page 44 for required subsampling / binning
206[5]	0x1	Assert sync_roi, to enable above uploads for next frame. This Reconfiguration will cause one frame to be blanked out.

Read-1-Skip-1

The read−1−skip−1 subsampling scheme can be enabled. Subsampling occurs both in x− and y− direction. Figure 14 shows which pixels are read and which ones are skipped.

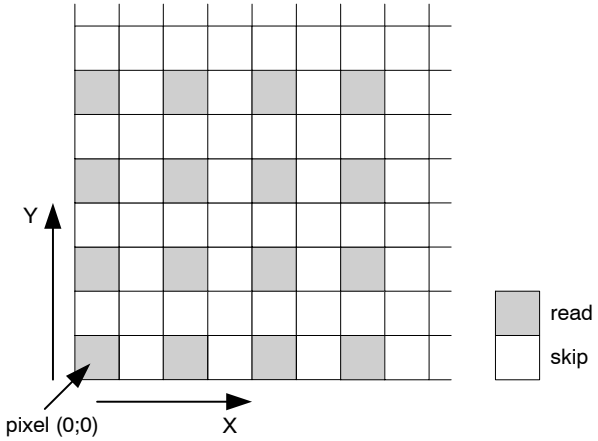


Figure 14. Read-1-Skip-1 Subsampling

2 × 2 Binning

The 2 × 2 binning scheme can also be enabled. During this binning scheme, pixels being readout are charge binned (summed) with pixel adjacent to them in the next row (in Y−direction) and then charge binned pixels of two rows are voltage binned (averaged) with adjacent charge binned pixels in X−direction. (See Table 15).

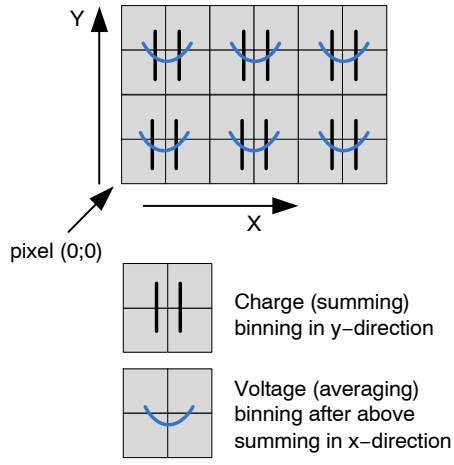


Figure 15. 2 x 2 Binning

Row/column address mapping during read−1−skip−1 subsampling and 2 × 2 binning.

During read−1−skip−1 sub−sampling, only even pixels of every alternative row are read out. These rows are addressed by on−chip sequencer according to the following formula:

Y−sequencer address of a row = row number / 2

For 2 × 2 binning, mapping of binned rows is done to sequencer addresses according to the following formula.

Y−sequencer address of a row = Binning of (row number / 2, row number / 2+1), where Y−address = row number / 2.

Table 24 shows address mapping of rows to be read out in read−1−skip−1subsampling and 2 × 2 binning mode to the sequencer Y−address.

Table 24. SEQUENCER Y-ADDRESS MAPPING FOR READ-1-SKIP-1 SUBSAMPLING AND 2 x 2 BINNING

Row No. (for R1S1 subsampling)	Row No. (for 2 x 2 binning)	Sequencer Y-address
0	(0,1)	0
2	(2,3)	1
4	(4,5)	2
6	(6,7)	3
…	…	…
2494	(2494, 2495)	1247
2496	(2496, 2497)	1248
2498	(2498, 2499)	1249

Table 25 shows the address mapping of pixel array columns to X−address in sequencer for read−1−skip−1 subsampling and 2 × 2 binning schemes.

Table 25. SEQUENCER X-ADDRESS MAPPING FOR READ-1-SKIP-1 SUBSAMPLING AND 2 x 2 BINNING

Pixel Array Even Column No. (for R1S1 subsampling)	Pixel Array Even Column No. (for 2 x 2 binning)	Kernel No.	Sequencer X-address
0−14 (every second pixel)	(0,1) − (14,15)	0	0
16−30 (every second pixel)	(16,17) − (30,31)	1	1
…	…	…	…
3808−3822 (every second pixel)	(3808,3809) − (3822,3823)	238	238
3824−3838 (every second pixel)	(3824,3825) − (3838,3839)	239	239

Checkerboard Subsampling

In this subsampling scheme, read out of even pixels of one row is followed by odd pixels of the next row. Figure 16 shows the pixels that are read and the pixels that are skipped.

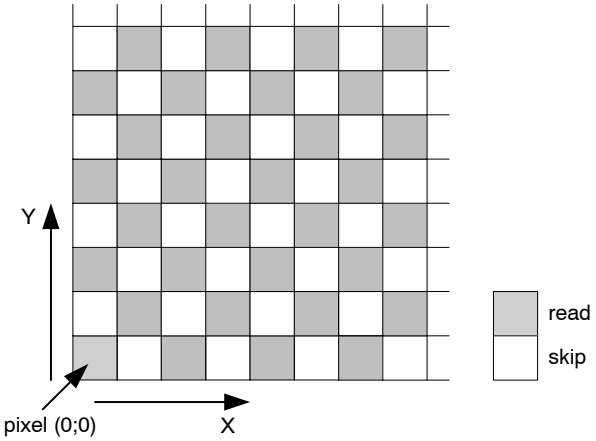


Figure 16. Checkerboard Subsampling

1 × 2 Binning

The 1 × 2 binning can be enabled to increase the dynamic range. During this binning scheme, pixels being read out are charge binned (summed) with adjacent pixels in the same column, as shown in Figure 17.

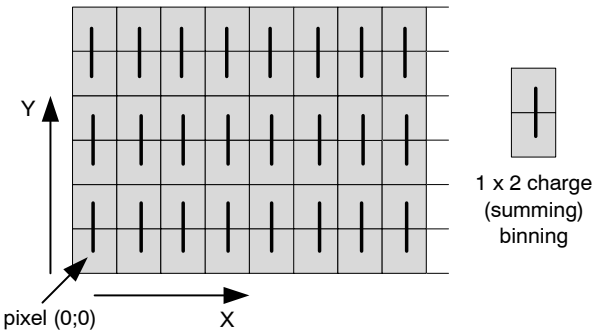


Figure 17. 1 x 2 Binning Scheme

Row/column addressing scheme during checkerboard subsampling and 1 ×2 binning

During check−board pattern subsampling, readout of even pixel segment (only even pixels of row) of a row is followed by odd pixel segment (only odd pixels of row) of next row. These segments are addressed according to following relation:

Y−address of even pixel segment of even row = row number

Y−address of odd pixel segment of odd row = row number

Address mapping of rows to Y−address during checkerboard subsampling is shown in Table 26.

Table 26. SEQUENCER Y-ADDRESS MAPPING FOR CHECKERBOARD SUBSAMPLING

Row No. (checkerboard subsampling)	Row Segment (checkerboard subsampling)	Sequencer Y-address
0	Even	0
1	Odd	1
2	Even	2
3	Odd	3
4	Even	4
5	Odd	5
…	…	…
2494	Even	2494
2495	Odd	2495
2496	Even	2496
2497	Odd	2497
2498	Even	2498
2499	Odd	2499

For 1 × 2 binning, every pixel in one row is binned with adjacent pixel of its next row, so there is one output data row, for every two consecutive rows.

Y−address of sequencer × 2 = binning of (row number, row number + 1), where Y−address = row number/2

For 1 × 2 binning, row address mapping to sequencer is shown in Table 27.

Table 27. SEQUENCER Y-ADDRESS MAPPING FOR 1 x 2 BINNING

Row No. (1 x 2 binning)	Sequencer Y-address
(0, 1)	0
(2, 3)	1
(4, 5)	2
(6, 7)	3
…	…
…	…
(2496, 2497)	1248
(2498, 2499)	1249

For checkerboard subsampling, columns for even pixels of an even row are addressed with mapping shown in Table 28, which is according to the following formula.

X−address of sequencer × 8 × 2 = Pixel array column number

Columns for odd pixels of an odd row are addressed with mapping shown in Table 29, which is according to the following formula.

Table 28. SEQUENCER X-ADDRESS MAPPING FOR EVEN PIXELS OF EVEN ROWS DURING CHECKERBOARD SUBSAMPLING

Pixel Array Even Column No.	Kernel Number	Sequencer X-address
0−14 (every second pixel)	0	0
16−30 (every second pixel)	1	1
−	−	−
3808−3822 (every second pixel)	238	238
3824−3838 (every second pixel)	239	239

Table 29. SEQUENCER X-ADDRESS MAPPING FOR ODD PIXELS OF ODD ROWS DURING CHECKERBOARD SUBSAMPLING

Pixel Array Even Column No.	Kernel Number	Sequencer X-address
0−15 (every second pixel)	0	0
17−31 (every second pixel)	1	1
−	−	−
3809−3823 (every second pixel)	238	238
3825−3839 (every second pixel)	239	239

For 1 × 2 binning, even columns of pixel array are addressed by sequencer with the following mapping:

X−address of sequencer × 8 = pixel array column number

Odd columns of pixel array are addressed by sequencer with the following mapping:

(X−address of sequencer − 1) × 8 + 1 = pixel array column number

Table shows the column to its X−address mapping in sequencer for 1 × 2 binning.

Table 30. SEQUENCER X-ADDRESS MAPPING FOR 1 x 2 BINNING

Pixel Array Column No.	Kernel Number	Sequencer X-address
0−14 (every second pixel)	0	0
1−15 (every second pixel)	1	1
16−30 (every second pixel)	2	2
17−31 (every second pixel)	3	3
−	−	−
3808−3822 (every second pixel)	476	476

3809−3823 (every second pixel)	477	477
3824−3838 (every second pixel)	478	478
3825−3839 (every second pixel)	479	479

Black Calibration

The sensor automatically calibrates the black level for each frame. Therefore, the device generates a configurable number of electrical black lines at the start of each frame. The desired black level in the resulting output interface can be configured and is not necessarily targeted to ‘0’. Configuring the target to a higher level yields some information on the left side of the black level distribution, while the other end of the distribution tail is clipped to ‘0’ when setting the black level target to ‘0’.

The black level is calibrated for the 8 columns contained in one kernel. Configurable parameters for the black−level algorithm are listed in Table 20.

Black Reference

The sensor reads out one or more black lines at the start of every new frame. The number of black lines to be generated is programmable and is minimal equal to 1. The length of the black lines depends on the operation mode. For rolling shutter mode, the length of the black line is equal to the line length configured in the active window.

The black references are used to perform black calibration and offset compensation in the data channels. The raw black pixel data is transmitted over the usual output interface, while the regular image data is compensated (can be bypassed).

On the output interface, black lines can be seen as a separate window, however without Frame Start and Ends (only Line Start/End). The Sync code following the Line Start and Line End indications (“window ID”) contains the active window number for rolling shutter operation. Black reference data is classified by a BL code.

Black line address should be configured through SPI register 230[9:5] according to the following table.

Table 31. BLACK LINE ADDRESS FOR DIFFERENT SUBSAMPLING AND BINNING SCHEMES

Scheme / Pixel Architecture	Black Line Address
Normal	2
R1S1	1
R2S2	1
Checkerboard	2
1 x 2 binning	1
2 x 2 binning	1

Signal Path Gain

Analog Gain Stages

The default settings are optimized for the best performance.

Digital Gain Stage

The digital gain stage allows fine gain adjustments on the digitized samples. The gain configuration is an absolute 5.7 unsigned number (5 digits before and 7 digits after the decimal point).

Automatic Exposure Control

The default settings are optimized for the best performance.

Temperature Sensor

The MANO 9600 has an on-chip temperature sensor which can output a digital code (Tsensor) of the silicon junction temperature. The Tsensor output is a 8-bit digital count between 0 and 255, proportional to the temperature of the silicon substrate. This reading can be translated directly to a temperature reading in °C by calibrating the 8-bit readout at 0°C and 70°C to achieve an output accuracy of ±2°C. The Tsensor output can also be calibrated using a single temperature point (example: room temperature or the ambient temperature of the application), to achieve an output accuracy of ±5°C.

The resolution of the temperature sensor in ºC / bit is made almost constant over process variations by design. Therefore any process variation will result in an offset in the bit count and this offset will remain within ±5°C over the temperature range of 0°C and 70°C.

Tsensor output digital code can be read out through the SPI interface. Refer to the Register Map on page 44.

The output of the temperature sensor to the SPI:

tempd_reg_temp<7:0>: This is the 8-bit N count readout proportional to temperature.

The input from the SPI:

The *reg_tempd_enable* is a global enable and this enables or disables the temperature sensor when logic high or logic low respectively. The temperature sensor is reset or disabled when the input *reg_tempd_enable* is set to a digital low state.

Calibration using one temperature point

The temperature sensor resolution is fixed for a given type of package for the operating range of 0°C to +70°C and hence devices can be calibrated at any ambient temperature of the application, with the device configured in the mode of operation.

Interpreting the actual temperature for the digital code readout:

The formula used is

$$\mathbf{T_J = R\ (Nread - Ncalib) + Tcalib}$$

T_J = junction die temperature

R = resolution in degrees/LSB (typical 0.75 deg/LSB)

Nread = Tsensor output (LSB count between 0 and 255)

Tcalib = Tsensor calibration temperature

Ncalib = Tsensor output reading at Tcalib

Monitor Pins

The internal sequencer has two monitor outputs (Pin 44 and Pin 45) that can be used to communicate the internal states from the sequencer. A three-bit register configures the assignment of the pins.

Table 32. REGISTER SETTING FOR THE MONITOR SELECT PIN

monitor_select [2:0] 192 [13:11]	monitor pin	Description
0x0	monitor0 monitor1	'0' '0'
0x1	monitor0 monitor1	Integration Time ROT Indication ('1' during ROT, '0' outside)
0x2	monitor0 monitor1	Integration Time Dual/Triple Slope Integration (asserted during DS/TS FOT sequence)
0x3	monitor0 monitor1	Start of x-Readout Indication Black Line Indication ('1' during black lines, '0' outside)
0x4	monitor0 monitor1	Frame Start Indication Start of ROT Indication
0x5	monitor0 monitor1	First Line Indication ('1' during first line, '0' for all others) Start of ROT Indication
0x6	monitor0 monitor1	ROT Indication ('1' during ROT, '0' outside) Start of X-Readout Indication
0x7	monitor0 monitor1	Start of X-readout Indication for Black Lines Start of X-readout Indication for Image Lines

DATA OUTPUT FORMAT

The MANO 9600 is available in two different versions:

- M1-SM: Four LVDS output channels, together with an LVDS clock output and an LVDS synchronization output channel.
- M2-SM: A 10-bit parallel CMOS output, together with a CMOS clock output and ‘frame valid’ and ‘line valid’ CMOS output signals.

M1-SM: LVDS Interface Version

LVDS Output Channels

The image data output occurs through four LVDS data channels where a synchronization LVDS channel and an LVDS output clock signal synchronizes the data.

The four data channels are used to output the image data only. The sync channel transmits information about the data sent over these data channels (includes codes indicating black pixels, normal pixels, and CRC codes).

8-bit / 10-bit Mode

The sensor can be used in 8-bit or 10-bit mode.

In 10-bit mode, the words on data and sync channel have a 10-bit length. The output data rate is 620 Mbps.

In 8-bit mode, the words on data and sync channel have an 8-bit length, the output data rate is 496 Mbps.

Note that the 8-bit mode can only be used to limit the data rate at the consequence of image data word depth. It is not supported to operate the sensor in 8-bit mode at a higher clock frequency to achieve higher frame rates.

Frame Format

The frame format is explained by example of the readout of two (overlapping) windows as shown in Figure 18 (a).

The readout of a frame occurs on a line-by-line basis. The read pointer goes from left to right, bottom to top.

Figure 18 indicates that, after the FOT is completed, the sensor reads out a number of black lines for black calibration purposes. After these black lines, the windows are processed. First a number of lines which only includes information of ‘ROI 0’ are sent out, starting at position y0_start. When the line at position y1_start is reached, a number of lines containing data of ‘ROI 0’ and ‘ROI 1’ are sent out, until the line position of y0_end is reached. From there on, only data of ‘ROI 1’ appears on the data output channels until line position y1_end is reached.

During read out of the image data over the data channels, the sync channel sends out frame synchronization codes which give information related to the image data that is sent over the four data output channels.

Each line of a window starts with a Line Start (LS) indication and ends with a Line End (LE) indication. The line start of the first line is replaced by a Frame Start (FS); the line end of the last line is replaced with a Frame End indication (FE). Each such frame synchronization code is followed by a window ID (range 0 to 7). For overlapping windows, the line synchronization codes of the overlapping windows with lower IDs are not sent out (as shown in the illustration: no LE/FE is transmitted for the overlapping part of window 0).

NOTE: In Figure 18, only Frame Start and Frame End Sync words are indicated in (b). CRC codes are also omitted from the figure.

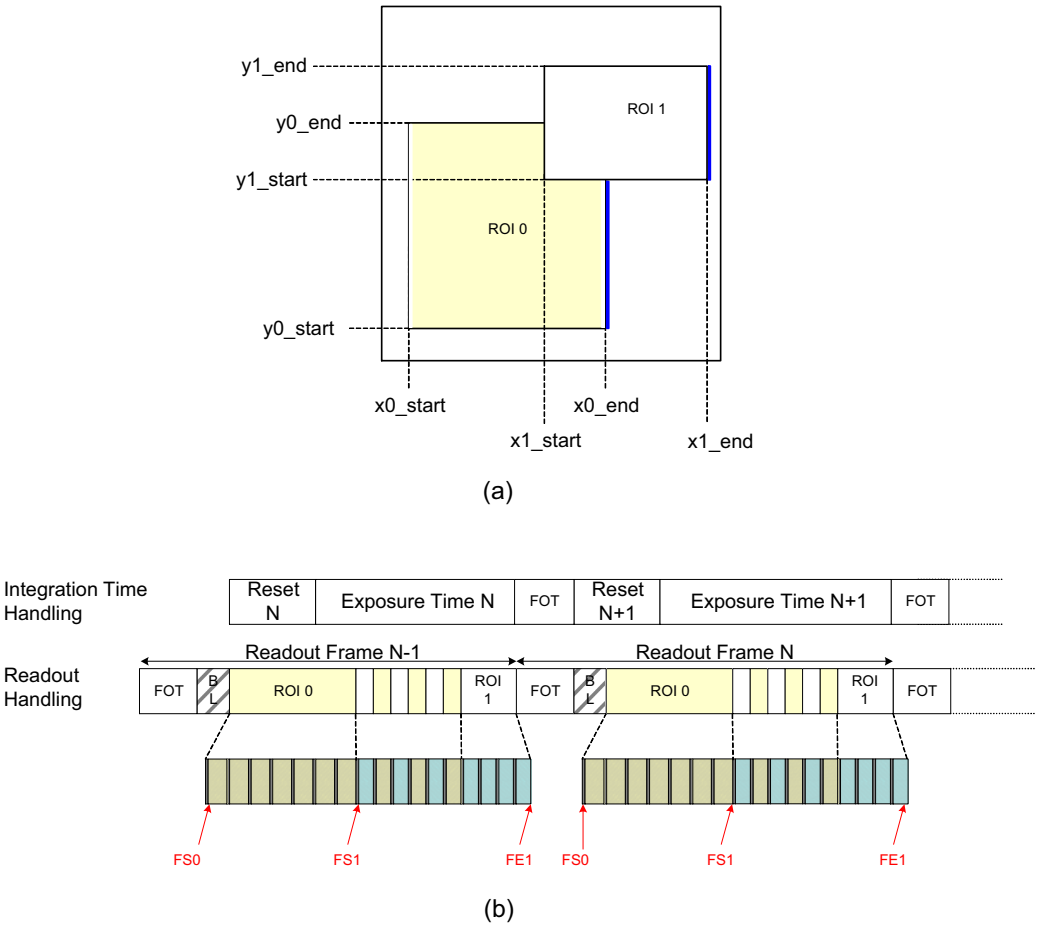


Figure 18. M1−SM: Frame Sync Codes

Figure 19 shows the detail of a black line readout during global or full-frame readout.

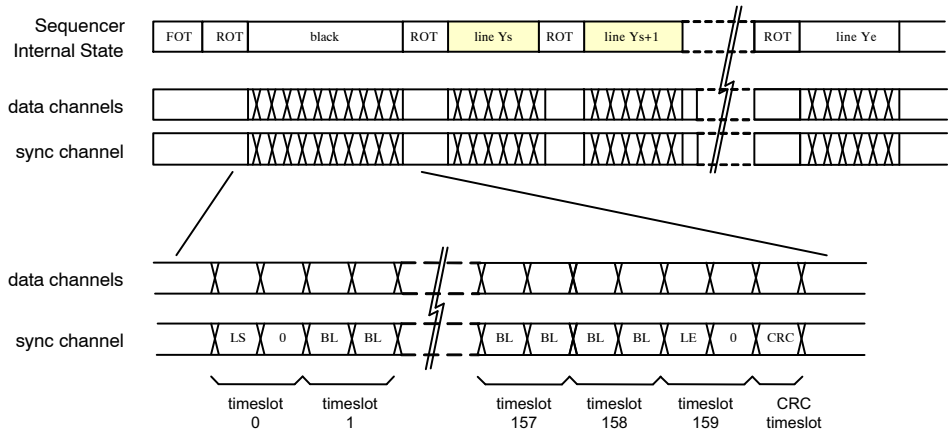


Figure 19. M1−SM: Time Line for Black Line Readout

Figure 20 shows the details of the readout of a number of lines for single window readout, at the beginning of the frame.

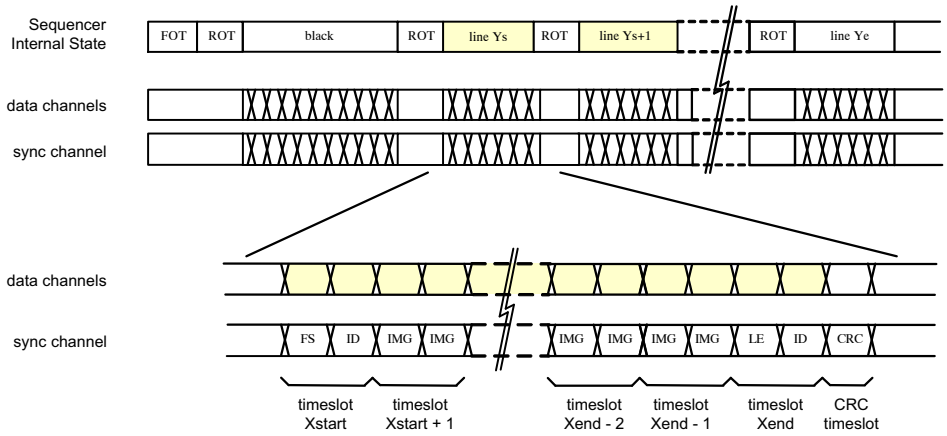


Figure 20. M1−SM: Time Line for Single Window Readout (at the start of a frame)

Figure 21 shows the detail of the readout of a number of lines for readout of two overlapping windows.

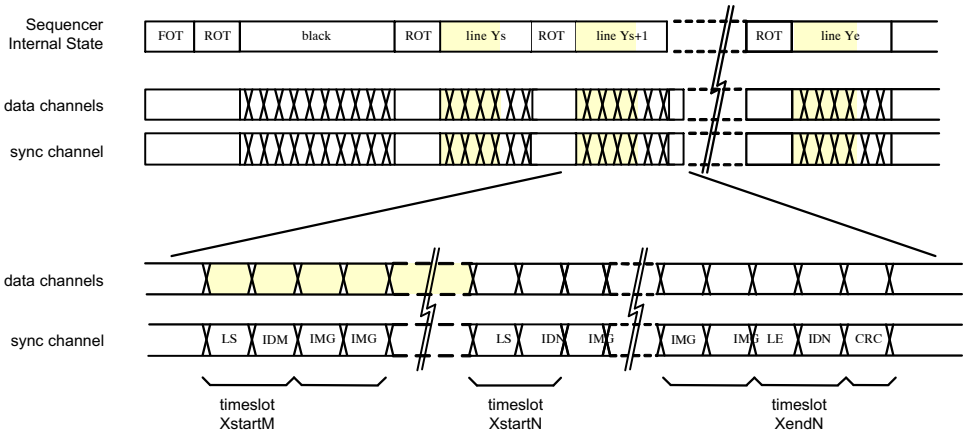


Figure 21. M1−SM: Time Line Showing the Readout of Two Overlapping Windows

Frame Synchronization for 10−bit Mode

Table 33 shows the structure of the frame synchronization code. Note that the table shows the default data word (configurable) for 10-bit mode. If more than one window is active at the same time, the sync channel transmits the frame synchronization codes of the window with highest index only.

Table 33. FRAME SYNCHRONIZATION CODE DETAILS FOR 10-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
9:7	N/A	0x5	Frame start indication
9:7	N/A	0x6	Frame end indication
9:7	N/A	0x1	Line start indication
9:7	N/A	0x2	Line end indication
6:0	131[6:0]	0x2A	These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting

- Window Identification

Frame synchronization codes are always followed by a 3-bit window identification (bits 2:0). This is an integer number, ranging from 0 to 7, indicating the active window. If more than one window is active for the current cycle, the highest window ID is transmitted.

- Data Classification Codes

For the remaining cycles, the sync channel indicates the type of data sent through the data links: black pixel data (BL), image data (IMG), or training pattern (TR). These codes are programmable by a register setting. The default values are listed in Table 31.

Table 34. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 10-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
9:0	132 [9:0]	0x015	Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.
9:0	133 [9:0]	0x035	Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).
9:0	134 [9:0]	0x059	CRC value. The data on the data output channels is the CRC code of the finished image data line.
9:0	135 [9:0]	0x3A6	Training pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.

Frame Synchronization in 8-bit Mode

The frame synchronization words are configured using the same registers as in 10-bit mode. The two least significant bits of these configuration registers are ignored and not sent out. Table 32 shows the structure of the frame synchronization code, together with the default value, as specified in SPI registers. The same restriction for overlapping windows applies in 8-bit mode.

Table 35. FRAME SYNCHRONIZATION CODE DETAILS FOR 8-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
7:5	N/A	0x5	Frame start (FS) indication
7:5	N/A	0x6	Frame end (FE) indication
7:5	N/A	0x1	Line start (LS) indication
7:5	N/A	0x2	Line end (LE) indication
4:0	[6:2]	0x0A	These bits indicate that the received sync word is a frame synchronization code. The value is programmable by a register setting.

- Window Identification

Similar to 10-bit operation mode, the frame synchronization codes are followed by a window identification. The window ID is located in bits 4:2 (all other bit positions are ‘0’). The same restriction for overlapping windows applies in 8-bit mode.

- Data Classification Codes

BL, IMG, CRC, and TR codes are defined by the same registers as in 10-bit mode. Bits 9:2 of the respective configuration registers are used as classification code with default values shown in Table 33.

Table 36. SYNCHRONIZATION CHANNEL DEFAULT IDENTIFICATION CODE VALUES FOR 8-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
7:0	132 [9:2]	0x05	Black pixel data (BL). This data is not part of the image. The black pixel data is used internally to correct channel offsets.
7:0	133 [9:2]	0x0D	Valid pixel data (IMG). The data on the data output channels is valid pixel data (part of the image).
7:0	134 [9:2]	0x16	CRC value. The data on the data output channels is the CRC code of the finished image data line.
7:0	135 [9:2]	0xE9	Training Pattern (TR). The sync channel sends out the training pattern which can be programmed by a register setting.

Training Patterns on Data Channels

In 10-bit mode, during idle periods, the data channels transmit training patterns, indicated on the sync channel by a TR code. These training patterns are configurable independent of the training code on the sync channel as shown in Table 34.

In 8-bit mode, the training pattern for the data channels is defined by the same register as in 10-bit mode, where the lower two bits are omitted; see Table 35.

Table 37. TRAINING CODE ON SYNC CHANNEL IN 10-BIT MODE

Sync Word Bit Position	Register Address	Default Value	Description
[9:0]	130 [9:0]	0x3A6	Data channel training pattern. The data output channels send out the training pattern, which can be programmed by a register setting. The default value of the training pattern is 0x3A6, which is identical to the training pattern indication code on the sync channel.

Table 38. TRAINING PATTERN ON DATA CHANNEL IN 8-BIT MODE

Data Word Bit Position	Register Address	Default Value	Description
[7:0]	130 [9:2]	0xE9	Data Channel Training Pattern (Training pattern).

Cyclic Redundancy Code

At the end of each line, a CRC code is calculated to allow error detection at the receiving end. Each data channel transmits a CRC code to protect the data words sent during the previous cycles. Idle and training patterns are not included in the calculation.

The sync channel is not protected. A special character (CRC indication) is transmitted whenever the data channels send their respective CRC code.

The polynomial in 10-bit operation mode is $x^{10} + x^9 + x^6 + x^3 + x^2 + x + 1$. The CRC encoder is seeded at the start of a new line and updated for every (valid) data word received. The CRC seed is configurable using the crc_seed register. When ‘0’, the CRC is seeded by all-‘0’; when ‘1’ it is seeded with all-‘1’.

In 8-bit mode, the polynomial is $x^8 + x^6 + x^3 + x^2 + 1$. The CRC seed is configured by means of the crc_seed register.

Note The CRC is calculated for every line. This implies that the CRC code can protect lines from multiple windows.

Data Order for M1−SM

To read out the image data through the output channels, the pixel array is organized in kernels. Each row consists of 480 kernels. Even positioned kernel consists of 8 consecutive even pixels and odd positioned kernel consists of 8 consecutive odd kernels. So the kernel size is 8 pixels in x−direction by 1 pixel in y−direction. Figure 22 indicates how the kernels are organized. The first kernel (kernel [0, 0]) is located in the bottom left corner. The data order of this image data on the data output channels depends on the subsampling mode.

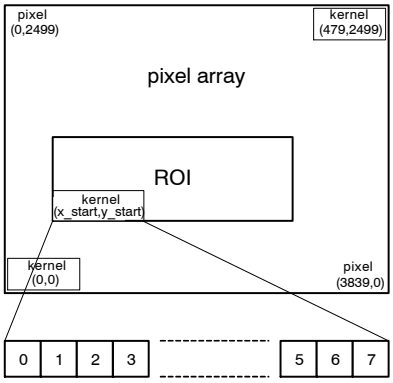


Figure 22. Kernel Organization in Pixel Array

- M1−SM: No Subsampling

The image data is read out in kernels of eight pixels in x−direction by one pixel in y−direction. One data channel output delivers two pixel values of one kernel sequentially.

Figure 23 shows how a kernels are read out over the four output channels. Each row consists of 480 kernels. First pair of kernels is read out ascending, while the next pair of kernels is read out descending. Similarly, all even pairs of kernels are read out in ascending order and odd pairs of kernel are read out in descending order.

Table 39 indicates the pixel data order of each channel for 1st 16 data−outputs. Shaded grey cells shows data order for even pair of kernels and the non−shaded cells shows data order for odd pair of kernels.

Table 39. M1−SM: DATA OUTPUT ORDER WHEN SUBSAMPLING IS DISABLED

Data Number	Pixels on Channel 0	Pixels on Channel 1	Pixels on Channel 2	Pixels on Channel 3
0	0	4	8	12
1	2	6	10	14
2	1	5	9	13
3	3	7	11	15
4	30	26	22	18
5	28	24	20	16
6	31	27	23	19
7	29	25	21	17
8	32	36	40	44
9	34	38	42	46
10	33	37	41	45
11	35	39	43	47
12	62	58	54	50
13	60	56	52	48
14	63	59	55	51
15	61	57	53	49

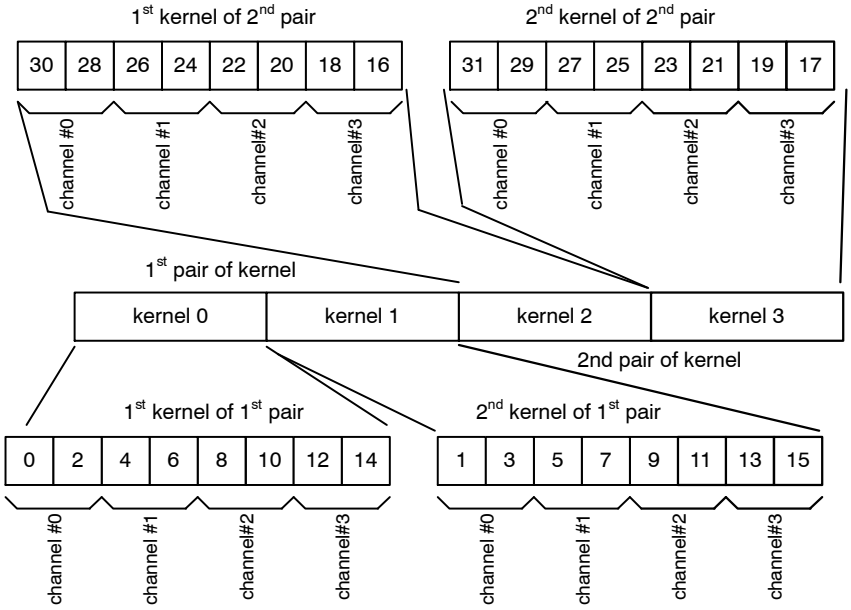


Figure 23. M1−SM: Data Output Order when Subsampling is Disabled

- M1−SM: Read−1−Skip−1 Subsampling

For read−1−skip−1 sub−sampling, only even pixels of a row are readout with next full row of pixels (even/odd pixels of next row) skipped. Hence one line is read out in 240 kernels. Data for even kernels are read out in ascending order and for odd kernels it is read out in descending order as shown in Figure 24. Table 40 shows the data order for first eight data outputs of a row.

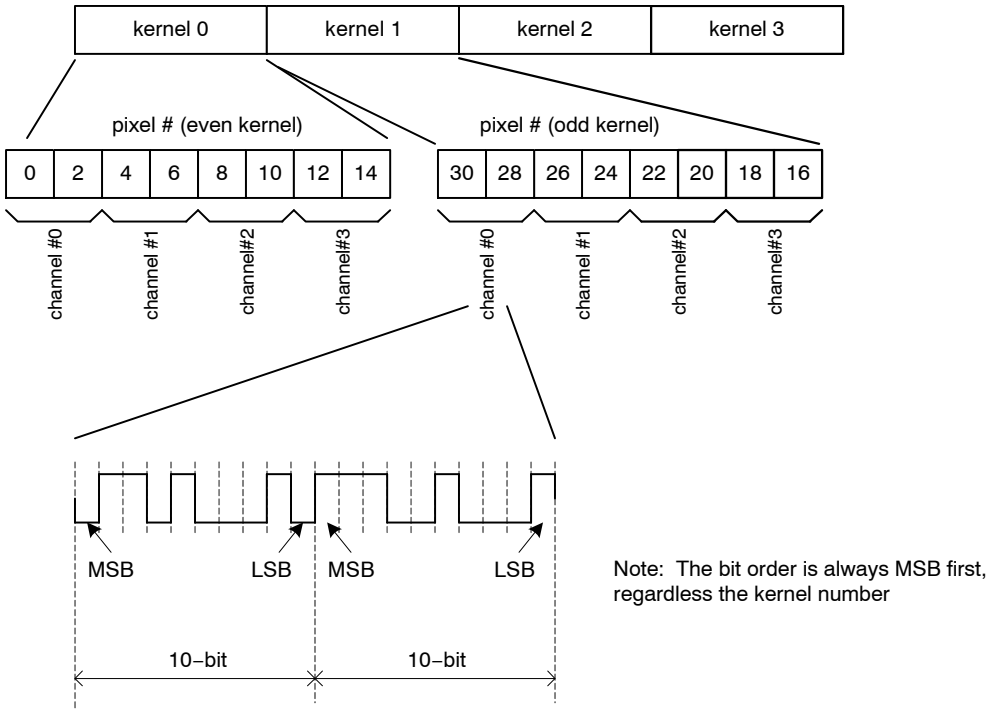


Figure 24. M1−SM: Data Output Order for Read−1−Skip−1 Subsampling

Table 40 shows data order for readout of even and odd kernels for read−1−skip−1 subsampling for first eight data outputs on output channels.

Table 40. M1−SM: DATA OUTPUT ORDER READ−1SKIP−1 SUBSAMPLING

Data Number	Pixels on Channel 0	Pixels on Channel 1	Pixels on Channel 2	Pixels on Channel 3
0	0	4	8	12
1	2	6	10	14
2	30	26	22	18
3	28	24	20	16
4	32	36	40	44
5	34	38	42	46
6	62	58	54	50
7	60	56	52	48

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout.

M1−SM: Checkerboard Subsampling

For checkerboard subsampling, readout of even pixels of one row is followed by readout of odd pixels of the next row.

Figure 25 and Figure 40 show how a even and odd kernels are read out over the four output channels, for even and odd pixels segment of a row respectively. Each segment consists of 240 kernels. For even pixel segment of a row, even positioned kernels are read out ascending, while for odd positioned kernels the data order is reversed (descending). For odd pixel segment of a line also, even positioned kernels are read out ascending, while for odd positioned kernel the data order is reversed (descending).

Note that a window should always start at an even x−address, such that the first kernel of a segment is always at an even position.

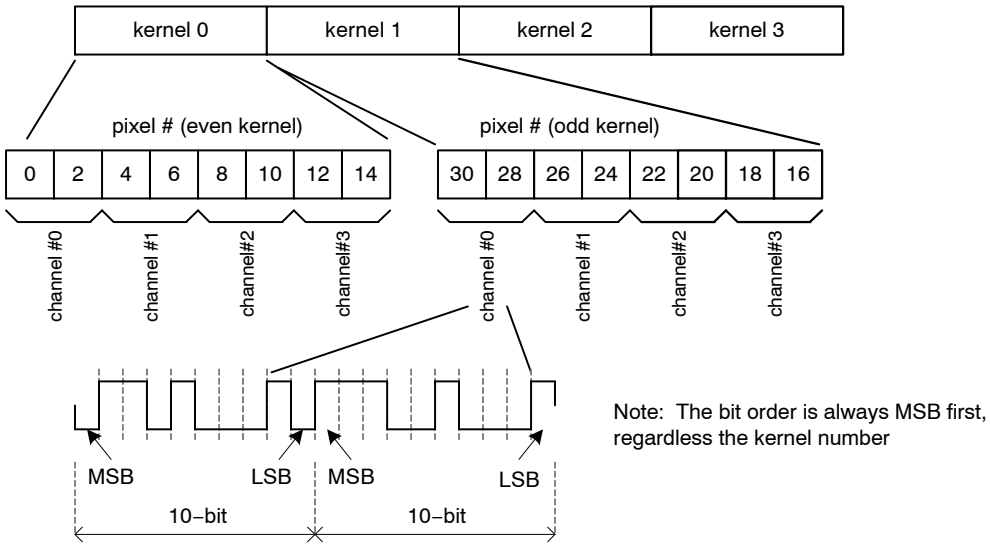


Figure 25. M1−SM: Data Output Order for Even Pixels of Line During Checkerboard Subsampling

Table 41 shows data order for readout of even and odd kernels of even pixels of a line for first eight data outputs on output channels.

Table 41. M1−SM: DATA OUTPUT ORDER FOR EVEN PIXELS OF LINE DURING CHECKERBOARD SUBSAMPLING

Data Number	Pixels on Channel 0	Pixels on Channel 1	Pixels on Channel 2	Pixels on Channel 3
0	0	4	8	12
1	2	6	10	14
2	30	26	22	18
3	28	24	20	16
4	32	36	40	44
5	34	38	42	46
6	62	58	54	50
7	60	56	52	48

Table 42 shows data order for readout of even and odd kernels of odd pixels of a line for first eight data outputs on output channels.

Table 42. M1−SM: DATA OUTPUT ORDER FOR ODD PIXELS OF LINE DURING CHECKERBOARD SUBSAMPLING

Data Number	Pixels on Channel 0	Pixels on Channel 1	Pixels on Channel 2	Pixels on Channel 3
0	1	5	9	13
1	3	7	11	15
2	31	27	23	19
3	29	25	21	17
4	33	37	41	45
5	35	39	43	47
6	63	59	55	51
7	61	57	53	49

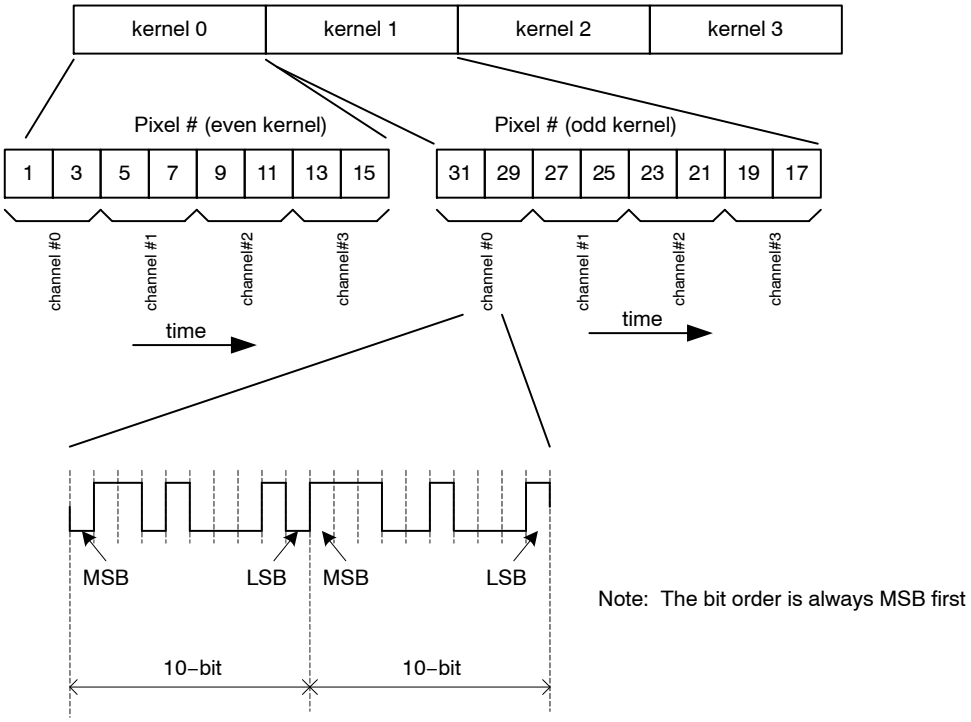


Figure 26. M1−SM: Data Output Order for Odd Pixels of Line During Checkerboard Subsampling

M1−SM: 1 x 2 Binning

For 1 × 2 binning, every pixel in an even row is binned with a similar positioned pixel in the odd row. Data output format is the same as readout of normal row readout with no subsampling. Data order is similar to that shown in Figure 23 and Table 40 on page 37. The only difference is that every pixel in even row is binned with the corresponding pixel in the next odd row.

M1−SM: 2 x 2 Binning

For 2 × 2 binning, data order for even and odd kernel is shown in Figure 27, showing binning between two adjacent pixels in X−direction for row 0 and row 1.

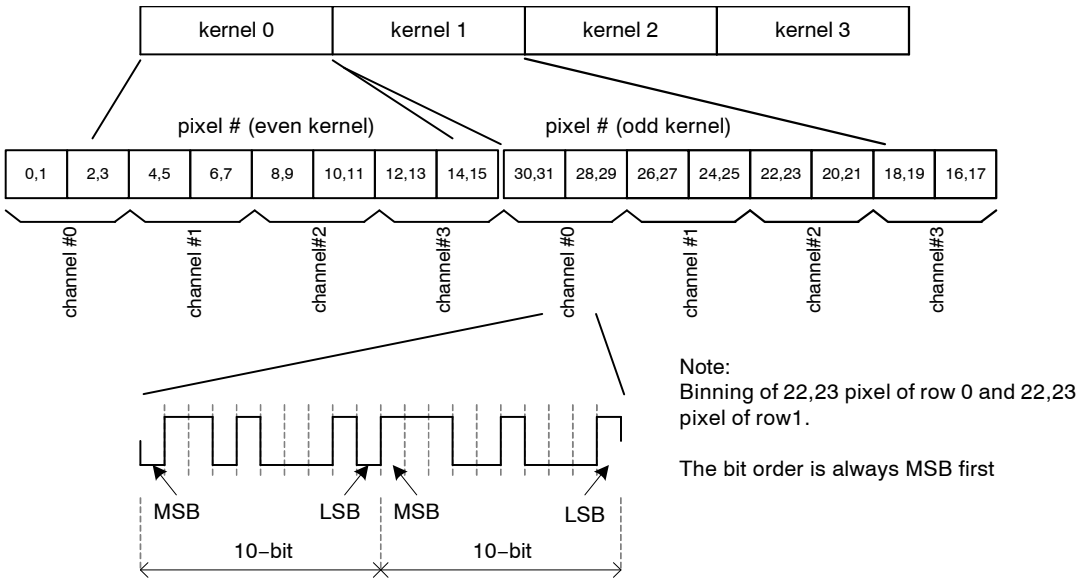


Figure 27. M1−SM: Data Output Order for 2 x 2 Binning

Table 43 shows data order for 2 × 2 binning of two pixels in even row with same pixel# in odd row for first eight data outputs on output channels.

Table 43. M1−SM: DATA OUTPUT ORDER FOR 2 x 2 BINNING

Data Number	Pixels on Channel 0	Pixels on Channel 1	Pixels on Channel 2	Pixels on Channel 3
0	bin(0,1)	bin(4,5)	bin(8,9)	bin(12,13)
1	bin(2,3)	bin(6,7)	bin(10,11)	bin(14,15)
2	bin(30,31)	bin(26,27)	bin(22,23)	bin(18,19)
3	bin(28,29)	bin(24,25)	bin(20,21)	bin(16,17)
4	bin(32,33)	bin(36,37)	bin(40,41)	bin(44,45)
5	bin(34,35)	bin(38,39)	bin(42,43)	bin(46,47)
6	bin(62,63)	bin(58,59)	bin(54,55)	bin(50,51)
7	bin(60,61)	bin(56,57)	bin(52,53)	bin(48,49)

M2−SM: CMOS Interface Version

CMOS Output Signals

The image data output occurs through a single 10-bit parallel CMOS data output, operating at 62 Mbps. The function of the CMOS clock output, ‘frame valid’ and ‘line valid’ signal is to synchronize the output data.

No windowing information is sent out by the sensor.

8-bit/10-bit Mode

The 8-bit mode is not supported when using the parallel CMOS output interface.

Frame Format

Frame timing is indicated by means of two signals: frame_valid and line_valid.

The frame_valid indication is asserted at the start of a new frame and remains asserted until the last line of the frame is completely transmitted.

The line_valid indication serves the following needs:

- While the line_valid indication is asserted, the data channels contain valid pixel data.
- The line valid communicates frame timing as it is asserted at the start of each line and it is de-asserted at the end of the line. Low periods indicate the idle time between lines (ROT).
- The data channels transmit the calculated CRC code after each line. This can be detected as the data words right after the falling edge of the line valid.

The readout of a frame occurs on a line−by−line basis. The read pointer goes from left to right, bottom to top as shown in Figure 29.

Reset handling is shown in Figure 29 (b). The row “y_start” is reset and then after a wait period of one line time, with line length defined by window size in X−direction, reset pointer moves to next row “y_start + 1” and this row is reset. And sequence will continue until row “y_end” is reset. After exposure time, readout happens according to readout handling shown in Figure 29 (c). After ROT, row “y_start” is read out. Then after next ROT, the pixels of the row addressed by “y_start + 1” are read out. And sequence will continue until row “y_end” is read out.

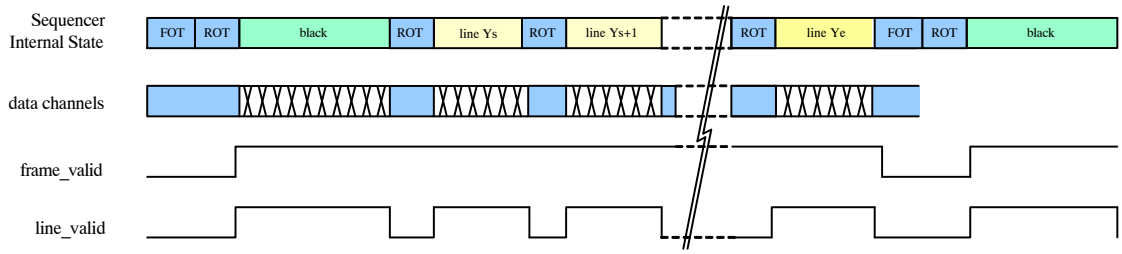


Figure 28. M2−SM: Frame Timing Indication

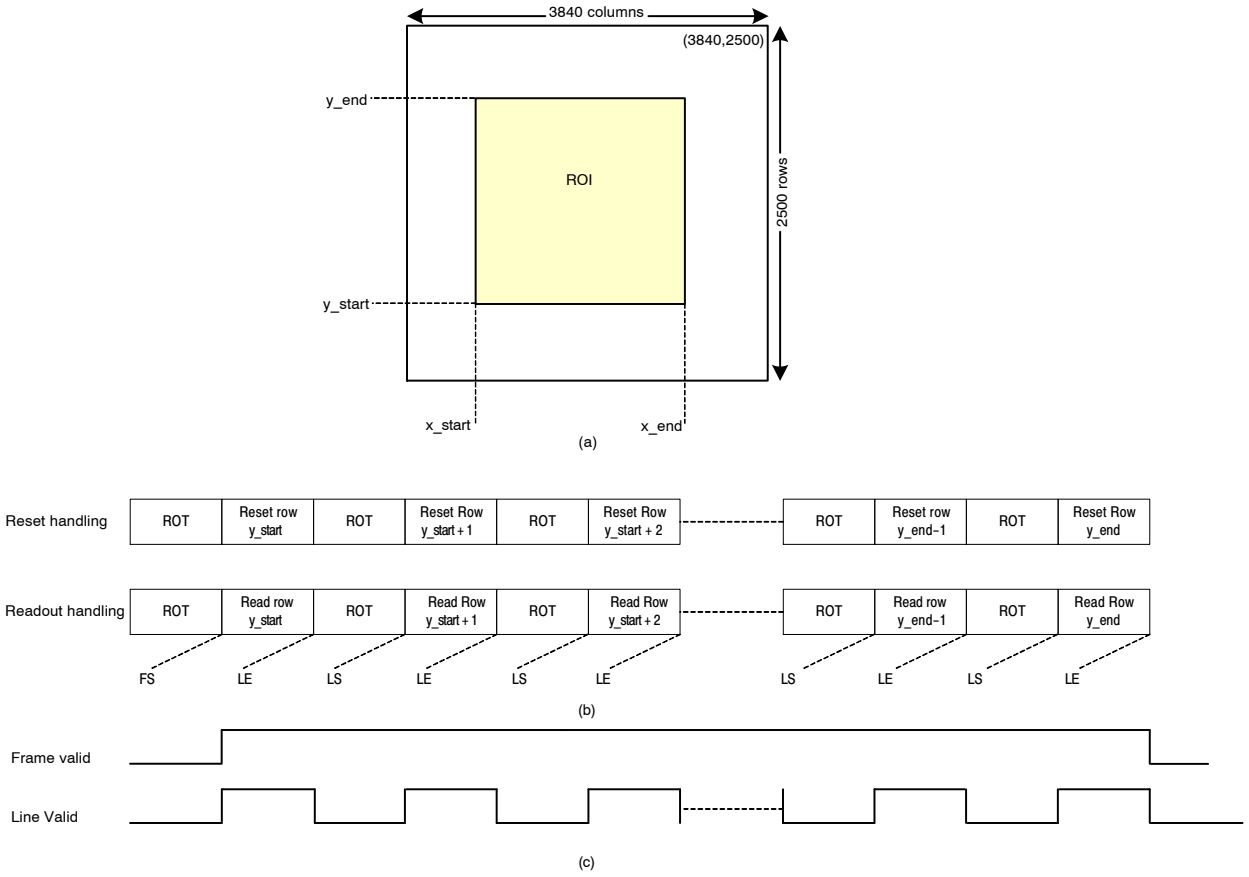


Figure 29. M2−SM: Frame Format to Read Out Image Data

Black Lines: Black pixel data is also sent through the data channels. To distinguish these pixels from the regular image data, it is possible to ‘mute’ the frame and/or line valid indications for the black lines.

Table 44. BLACK LINE FRAME_VALID AND LINE_VALID SETTINGS

bl_frame_valid_enable	bl_line_valid_enable	Description
0x1	0x1	The black lines are handled similar to normal image lines. The frame valid indication is asserted before the first black line and the line valid indication is asserted for every valid (black) pixel.
0x1	0x0	The frame valid indication is asserted before the first black line, but the line valid indication is not asserted for the black lines. The line valid indication indicates the valid image pixels only. This mode is useful when one does not use the black pixels and when the frame valid indication needs to be asserted some time before the first image lines (for example, to precondition ISP pipelines).
0x0	0x1	In this mode, the black pixel data is clearly unambiguously indicated by the line valid indication, while the decoding of the real image data is simplified.
0x0	0x0	Black lines are not indicated and frame and line valid strobes remain de-asserted. Note however that the data channels contains the black pixel data and CRC codes (Training patterns are interrupted).

Data Order

To read out the image data through the parallel CMOS output, the pixel array is divided in kernels. The kernel size is eight pixels in x−direction by one pixel in y−direction. Figure 22 on page 35 indicates how the kernels are organized.

The data order of this image data depends on the subsampling mode.

M2−SM: No Subsampling

The image data is read out in kernels of 8 pixels in x−direction by 1 pixel in y−direction. Figure 30 shows how a kernel is read out over parallel output channel. One row consists of 480 kernels. These kernels are divided further into pairs of two kernels, hence forming 240 pairs. Even pair of kernels is read out in ascending order, while for odd pair of kernels the data order is reversed (descending).

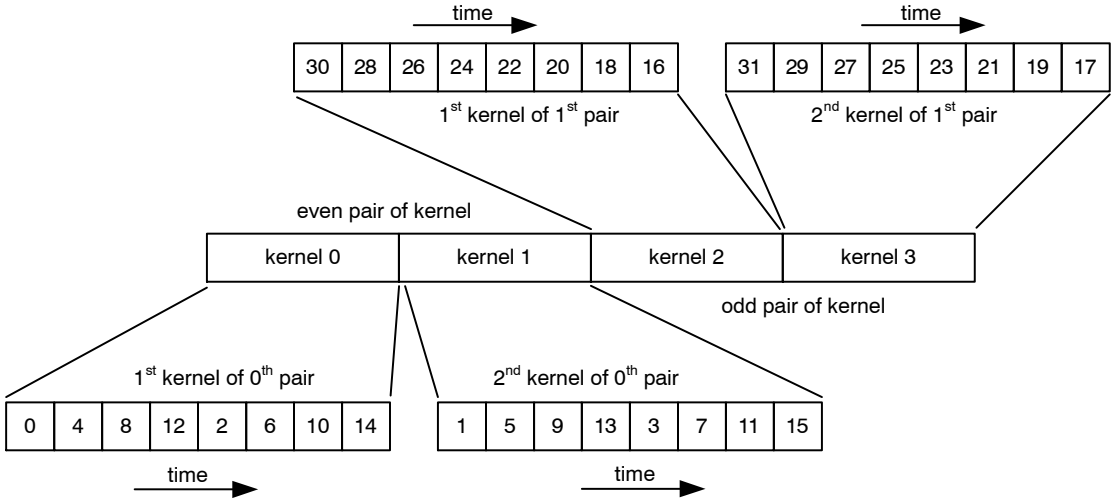


Figure 30. M2−SM: Data Output Order without Subsampling

M2−SM: Read−1−Skip−1 Subsampling

To read out the image data with subsampling enabled on a monochrome sensor, two neighboring kernels are combined to a single kernel of 16 pixels in the x−direction and one pixel in the y−direction. Only the pixels at the even pixel positions inside that kernel are read out. Figure 31 shows the data order.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout.

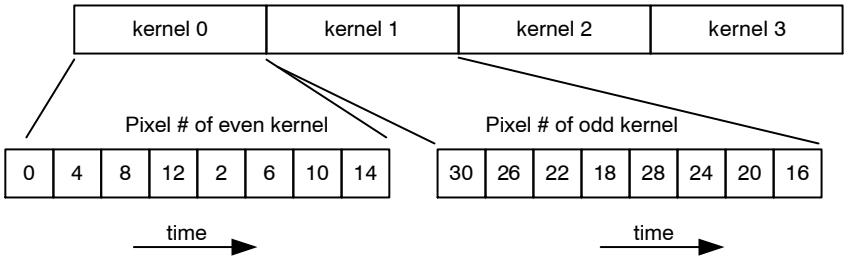


Figure 31. M2−SM: Data Output Order with Read−1−Skip−1 Subsampling

M2−SM: Checkerboard Subsampling

To read out the image data with check−board pattern sub−sampling enabled on a monochrome sensor, readout of even pixels of one row will be followed by readout of odd pixels of next row. Data order for even pixels will be same as read−1−skip−1 as shown in Figure 31. Data order for readout of odd pixels is shown in Figure 32.

Note that there is no difference in data order for even/odd kernel numbers, as opposed to the ‘no−subsampling’ readout.

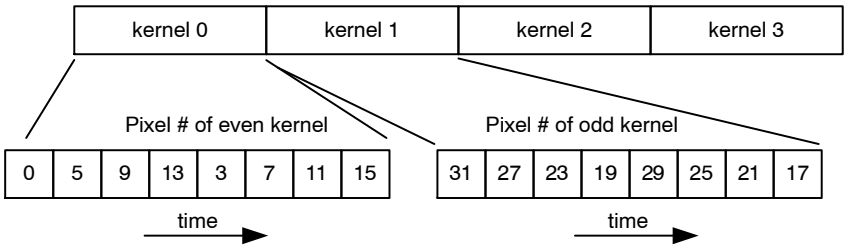


Figure 32. M2−SM: Data Output Order for Odd Pixel during Checkerboard Subsampling

M2−SM: 1 x 2 Binning

For 1 × 2 binning, data output order will be same as no−subsampling as shown in Figure 30. The only difference is that pixels is binned with same positioned pixel in the next row.

M2−SM: 2 x 2 Binning

To read out the image data with 2 × 2 binning enabled on a monochrome sensor, data order will be same as read−1−skip−1sub−sampling but pixel being readout will be binned with odd pixel next to it and same positioned pixels in the next row as shown in Figure 33.

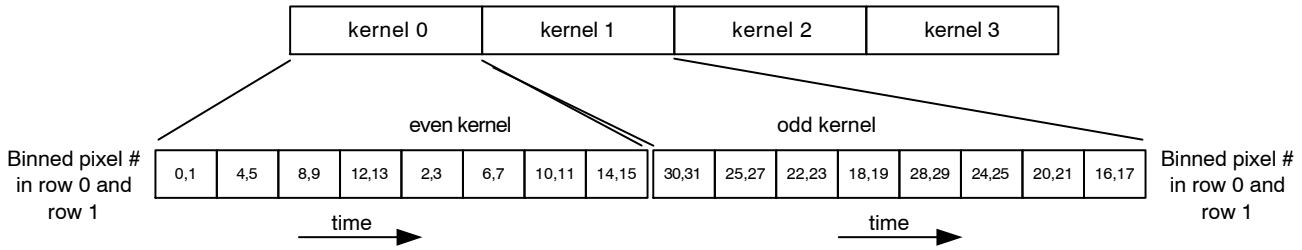


Figure 33. M2−SM: Data Output Order for 2 x 2 Binning

REGISTER MAP

Each functional entity has a dedicated address space, starting at a block offset. The register address is obtained by adding the address offset to the block offset. This address must be used to perform SPI uploads and is shown in the Address column of the register map table.

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
Chip ID [Block Offset: 0]							
0	0		chip_id	0x04D60	19808		RO
		[15:0]	id	0x04D60	19808	ON Semiconductor chip ID	
1	1		reserved	0x0000	0		RO
		[3:0]	reserved	0x0000	0	Reserved	
2	2		chip_configuration	0x0000	0		RW
		[1:0]		0x0	0	Configure as per part number: NOIM1SM9600A-QDC: 0x0 NOIM2SM9600A-QDC: 0x2	
Reset Generator [Block Offset: 8]							
0	8		soft_reset_pll	0x099	153		RW
		[3:0]	pll_soft_reset	0x9	9	PLL Reset 0x9: Soft Reset State Others: Operational	
		[7:4]	pll_lock_soft_reset	0x9	9	PLL Lock Detect Reset 0x9: Soft Reset State Others: Operational	
1	9		soft_reset_cgen	0x09	9		RW
		[3:0]	cgen_soft_reset	0x9	9	Clock Generator Reset 0x9: Soft Reset State Others: Operational	
2	10		soft_reset_analog	0x0999	2457		RW
		[3:0]	mux_soft_reset	0x9	9	Column MUX Reset 0x9: Soft Reset State Others: Operational	
		[7:4]	afe_soft_reset	0x9	9	AFE Reset 0x9: Soft Reset State Others: Operational	
		[11:8]	ser_soft_reset	0x9	9	Serializer Reset 0x9: Soft Reset State Others: Operational	
PLL [Block Offset: 16]							
0	16		power_down	0x0004	4		RW
		[0]	pwd_n	0x0	0	PLL Power Down ‘0’ = Power Down, ‘1’ = Operational	
		[1]	enable	0x0	0	PLL Enable ‘0’ = disabled, ‘1’ = enabled	
		[2]	bypass	0x1	1	PLL Bypass ‘0’ = PLL Active, ‘1’ = PLL Bypassed	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
1	17		config	0x2113	8467		RW
		[7:0]	mdiv	0x13	19	M-divider 19: 10 bit LVDS, 15: 8 bit LVDS	
		[12:8]	ndiv	0x1	1	N-divider	
		[14:13]	pdiv	0x1	1	P-divider	
IO [Block Offset: 20]							
0	20		config	0x0000	0		RW
		[0]	clock_in_pwd_n	0x0	0	Power down Clock Input	
		[10:8]	reserved	0x0	0	Reserved	
PLL lock detector [Block Offset: 24]							
0	24		pll_lock	0x0000	0		RO
		[0]	lock	0x0	0	PLL lock Indication	
Clock Generator [Block Offset: 32]							
0	32		config	0x0004	4		RW
		[0]	enable_analog	0x0	0	Enable analog clocks ‘0’ = disabled, ‘1’ = enabled	
		[1]	enable_log	0x0	0	Enable logic clock ‘0’ = disabled, ‘1’ = enabled	
		[2]	select_pll	0x1	1	Input Clock Selection ‘0’ = Select LVDS clock input, ‘1’ = Select PLL clock input	
		[3]	adc_mode	0x0	0	Set operation mode ‘0’ = 10-bit mode, ‘1’ = 8-bit mode	
		[4]	enable_div_2	0x0	0	Enable the divide by 2 circuit ‘0’ = PLL input direct to cgen ‘1’ = Divide PLL input by 2 before applying it to cgen	
		[11:8]	reserved	0x0	0	Reserved	
		[14:12]	reserved	0x0	0	Reserved	
General Logic [Block Offset: 34]							
0	34		config	0x0000	0		RW
		[0]	enable	0x0	0	Logic General Enable Configuration ‘0’ = Disable ‘1’ = Enable	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
Image Core [Block Offset: 40]							
0	40		image_core_config	0x0000	0		RW
		[0]	imc_pwd_n	0x0	0	Image Core Power Down ‘0’ = powered down, ‘1’ = powered up	
		[1]	mux_pwd_n	0x0	0	Column Multiplexer Power Down ‘0’ = powered down, ‘1’ = powered up	
		[2]	colbias_enable	0x0	0	Bias Enable ‘0’ = disabled ‘1’ = enabled	
AFE [Block Offset:48]							
0	48		power_down	0x0000	0		RW
		[0]	pwd_n	0x0	0	Power down for AFE’s (64 columns) ‘0’ = powered down, ‘1’ = powered up	
Bias [Block Offset: 64]							
0	64		power_down	0x0000	0		RW
		[0]	pwd_n	0x0	0	Power down bandgap ‘0’ = powered down, ‘1’ = powered up	
1	65		configuration	0x888B	34955		RW
		[0]	extres	0x1	1	External Resistor Selection ‘0’ = internal resistor, ‘1’ = external resistor	
		[3:1]	bgrtrim	0x5	5	Bandgap Trim	
		[7:4]	imc_colpc_ibias	0x8	8	Column Precharge ibias Configuration	
		[11:8]	imc_colbias_ibias	0x8	8	Column Bias ibias Configuration	
		[15:12]	cp_ibias	0x8	8	Charge Pump Bias	
2	66		afe_bias	0x53C8	21448		RW
		[3:0]	afe_ibias	0x8	8	AFE ibias Configuration	
		[7:4]	afe_adc_iref	0xC	12	ADC iref Configuration	
		[14:8]	afe_pga_iref	0x53	83	PGA iref Configuration	
3	67		mux_bias	0x08888	34952		RW
		[3:0]	mux_25u_stage1	0x8	8	Column Multiplexer Stage 1 Bias Configuration	
		[7:4]	mux_25u_stage2	0x8	8	Column Multiplexer Stage 2 Bias configuration	
		[11:8]	mux_25u_delay	0x8	8	Column Multiplexer Delay Bias Configuration	
		[15:12]	mux_25u_vcmbuff	0x8	8	Column Multiplexer Vcm Bias Configuration	
4	68		lvds_bias	0x0088	136		RW
		[3:0]	lvds_ibias	0x8	8	LVDS Ibias	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[7:4]	lvds_iref	0x8	8	LVDS Iref	
5	69		fine_trim	0x0000	0		RW
		[1:0]	mux_stage1_fine_trim	0x0	0	fine trim setting for col−mux stage1 bias	
		[3:2]	mux_stage2_fine_trim	0x0	0	fine trim setting for col−mux stage2 bias	
		[5:4]	mux_auxamp_stage1 _fine_trim	0x0	0	fine trim setting for auxiliary amplifier stage1 bias	
		[7:6]	mux_auxamp_stage2 _fine_trim	0x0	0	fine trim setting for auxiliary amplifier stage2 bias	
		[9:8]	afe_5u_fine_trim	0x0	0	fine trim setting for afe bias	
		[11:10]	adcref_5u_fine_trim	0x0	0	fine trim setting for ADC reference bias	
Col−Mux							
1	81		config	0x8881	34945		RW
		[15:0]	reserved	0x8881	34945		
Temperature Sensor [Block Offset: 96]							
0	96		sensor enable	0x0000	0		RW
		[0]	reg_tempd_enable	0x0	0	Temperature Diode Enable ‘0’ = disabled ‘1’ = enabled	
1	97		sensor output	0x0000	0		RO
		[7:0]	tempd_reg_temp	0x00	0	Temperature Readout	
Serializer/LVDS [Block Offset: 112]							
0	112		power_down	0x0000	0		RW
		[0]	clock_out_pwd_n	0x0	0	Power down for Clock Output. ‘0’ = powered down, ‘1’ = powered up	
		[1]	sync_pwd_n	0x0	0	Power down for Sync channel ‘0’ = powered down, ‘1’ = powered up	
		[2]	data_pwd_n	0x0	0	Power down for data channels (4 channels) ‘0’ = powered down, ‘1’ = powered up	
Data Block [Block Offset: 128]							
0	128		blackcal	0x4008	16392		RW
		[7:0]	black_offset	0x08	8	Desired black level at output	
		[10:8]	black_samples	0x0	0	Black pixels taken into account for black calibration. Total samples = 2**black_samples	
		[14:11]	adc_offset	0x8	8	ADC Offset = 2**adc_offset. This setting should correspond to the Calibration DAC setting	
		[15]	crc_seed	0x0	0	CRC Seed ‘0’ = All-0 ‘1’ = All-1	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
1	129		general_configuration	0xC001	49153		RW
		[0]	auto_blackcal_enable	0x1	1	Automatic blackcalibration is enabled when 1, bypassed when 0	
		[9:1]	blackcal_offset	0x00	0	Black Calibration offset used when auto_black_cal_en = '0'.	
		[10]	blackcal_offset_dec	0x0	0	blackcal_offset is added when 0, subtracted when 1	
		[11]	compress_bypass	0x0	0	Bypass compression of 11 bit ADC data to 10 bit output data when 1	
		[12]	bypass	0x0	0	Bypass datablock (test only) when '1'. Use default value for normal operation.	
		[13]	8bit_mode	0x0	0	Shifts window ID indications by 4 cycles. '0' = 10 bit mode, '1' = 8 bit mode	
		[14]	bl_frame_valid_ enable	0x1	1	Assert frame_valid for black lines when '1', gate frame_valid for black lines when '0'. NOIM2SM9600A-QDC	
		[15]	bl_line_valid_enable	0x1	1	Assert line_valid for black lines when '1', gate line_valid for black lines when '0'. NOIM2SM9600A-QDC	
2	130		trainingpattern	0x03A6	934		RW
		[9:0]	trainingpattern	0x3A6	934	Training pattern sent on data channels during idle mode. This data is used to perform word alignment on the LVDS data channels.	
		[10]	reserved	0x0	0	Reserved	
3	131		sync_code0	0x002A	42		RW
		[6:0]	frame_sync	0x02A	42	Frame sync LSBs. Note: The 10^{th} bit indicates frame/ line sync code, 9^{th} bit indicates start, 8^{th} bit indicates end.	
4	132		sync_code1	0x0015	21		RW
		[9:0]	bl	0x015	21	Black Pixel Identification Sync Code	
5	133		sync_code2	0x0035	53		RW
		[9:0]	img	0x035	53	Valid Pixel Identification Sync Code	
6	134		sync_code3	0x0059	89		RW
		[9:0]	crc	0x059	89	CRC Value Identification Sync Code	
7	135		sync_code4	0x03A6	934		RW
		[9:0]	tr	0x3A6	934	Training Value Identification Sync Code	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
Datablock - Test							
16	144		test_configuration	0x0000	0		RW
		[0]	testpattern_en	0x0	0	Insert synthesized testpattern when ‘1’	
		[1]	inc_testpattern	0x0	0	Incrementing testpattern when ‘1’, constant testpattern when ‘0’	
		[2]	prbs_en	0x0	0	Insert PRBS when ‘1’	
		[3]	frame_testpattern	0x0	0	Frame test patterns when ‘1’, unframed testpatterns when ‘0’	
		[4]	test_adc_select	0x0	0	Configures which ADC of selected channels is selected to output ADC data through adc_dout pins	
18	146		test_configuration0	0x0100	256		RW
		[7:0]	testpattern0_lsb	0x00	0	Testpattern used on datapath #0 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern1_lsb	0x01	1	Testpattern used on datapath #1 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
19	147		test_configuration1	0x0302	770		RW
		[7:0]	testpattern2_lsb	0x02	2	Testpattern used on datapath #2 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern3_lsb	0x03	3	Testpattern used on datapath #3 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
20	148		test_configuration2	0x0504	1284		RW
		[7:0]	testpattern4_lsb	0x04	4	Testpattern used on datapath #4 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern5_lsb	0x05	5	Testpattern used on datapath #5 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
21	149		test_configuration3	0x0706	1798		RW
		[7:0]	testpattern6_lsb	0x06	6	Testpattern used on datapath #6 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
		[15:8]	testpattern7_lsb	0x07	7	Testpattern used on datapath #7 when testpattern_en = ‘1’. Note: Most significant bits are configured in register 150.	
22	150		test_configuration16	0x0000	0		RW
		[1:0]	testpattern0_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	
		[3:2]	testpattern1_msb	0x0	0	Testpattern used when testpattern_en = ‘1’	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[5:4]	testpattern2_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[7:6]	testpattern3_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[9:8]	testpattern4_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[11:10]	testpattern5_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[13:12]	testpattern6_msb	0x0	0	Testpattern used when testpattern_en = '1'	
		[15:14]	testpattern7_msb	0x0	0	Testpattern used when testpattern_en = '1'	
AEC[Block Offset: 160]							
0	160		configuration	0x0010	16		RW
		[0]	enable	0x0	0	AEC Enable	
		[1]	restart_filter	0x0	0	Restart AEC filter	
		[2]	freeze	0x0	0	Freeze AEC filter and enforcer gains	
		[3]	pixel_valid	0x0	0	Use every pixel from channel when 0, every 4th pixel when 1	
		[4]	amp_pri	0x1	1	Stage 1 amplifier gets higher priority than stage 2 gain distribution if 1. vice versa if 0	
1	161		intensity	0x60B8	24760		RW
		[9:0]	desired_intensity	0xB8	184	Target average intensity	
		[13:10]	clip-ping_threshold_avg	0x018	24	Clipping threshold for average inc factor 3.3 unsigned	
6	166		exposure	0x03FF	1023		RW
		[15:0]	fixed_exposure	0x03FF	1023	Fixed Exposure Time	
7	167		gain	0x0800	2048		RW
		[1:0]	gain_stage1_select	0x0	0	Fixed Column Amplifier gain	
		[3:2]	gain_stage2_select	0x0	0	Fixed AFE PGA gain	
		[15:4]	fixed_digital_gain	0x080	128	Fixed digital gain 5.7 unsigned	
8	168		min_exposure	0x0001	1		RW
		[15:0]	min_exposure	0x0001	1	Minimum exposure time	
9	169		min_gain	0x0800	2048		RW
		[1:0]	min_gain_stage1	0x0	0	Minimum gain stage 1	
		[3:2]	min_gain_stage2	0x0	0	Minimum gain stage 2	
		[15:4]	min_digital_gain	0x080	128	Minimum digital gain 5.7 unsigned	
10	170		max_exposure	0x03FF	1023		RW
		[15:0]	max_exposure	0x03FF	1023	Maximum exposure time	
11	171		max_gain	0x100D	4109		RW
		[1:0]	max_gain_stage1	0x1	1	Maximum gain stage 1	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[3:2]	max_gain_stage2	0x3	3	Maximum gain stage 2	
		[15:4]	max_digital_gain	0x100	256	Maximum digital gain 5.7 unsigned	
12	172		hysteresis	0x00083	131		RW
		[7:0]	digital_hysteresis	0x083	131	Digital Hysteresis 1.7 unsigned	
		[13:8]	dim_threshold	0x00	0	Dimming Threshold	
		[15:14]	dim_factor	0x0	0	Dimming Factor	
24	184		total_pixels0	0x0000	0		RO
		[15:0]	total_pixels[15:0]	0x0000	0	Total number of pixels sampled for Average, LSB	
25	185		total_pixels1	0x0000	0		RO
		[8:0]	total_pixels[24:16]	0x0	0	Total number of pixels sampled for Average, MSB	
26	186		average_status	0x0000	0		RO
		[9:0]	average	0x000	0	AEC Average Status	
		[12]	locked	0x0	0	AEC Filter Lock Status	
27	187		exposure_status	0x0000	0		RO
		[15:0]	exposure	0x0000	0	AEC Exposure Status	
28	188		gain_status	0x00	0		RO
		[1:0]	gain_stage1	0x0	0	Gain Stage 1 Status	
		[3:2]	gain_stage2	0x0	0	Gain Stage 2 Status	
		[15:4]	digital_gain	0x000	0	AEC Digital Gain Status 5.7 unsigned	
29	189		reserved	0x0000	0		RO
		[12:0]	reserved	0x000	0	Reserved	
Sequencer [Block Offset: 192]							
0	192		general_configuration	0x00	0		RW
		[0]	enable	0x0	0	Enable sequencer ‘0’ = Idle, ‘1’ = enabled	
		[1]	rolling_shutter_enable	0x0	0	Operation Selection ‘0’ = global shutter, ‘1’ = rolling shutter	
		[2]	zero_rot_enable	0x0	0	Zero ROT mode Selection ‘0’ = Normal ROT, ‘1’ = Zero ROT	
		[3]	x_lag	0x0	0	x−lag in Zero ROT mode ‘0’ = No lag, ‘0’ = Lag	
		[4]	reserved	0x0	0	reserved	
		[5]	reserved	0x0	0	reserved	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[6]	nzrot_xsm_delay_ enable	0x0	0	Insert delay between end of ROT and start of readout in normal ROT readout mode if ‘1’. ROT delay is defined by register xsm_delay	
		[7]	reserved	0x0	0	reserved	
		[8]	reserved	0x0	0	reserved	
		[10]	roi_aec_enable	0x0	0	Enable windowing for AEC Statistics. ‘0’ = Subsample all windows ‘1’ = Subsample configured window	
		[13:11]	monitor_select	0x0	0	Control of the monitor pins	
		[14]	pls_mode	0x0	0	Test mode for PLS measurements	
1	193		delay_configuration	0x0000	0		RW
		[7:0]	rs_x_length	0x00	0	X-Readout duration in rolling shutter mode (extends lines with dummy pixels).	
		[15:8]	xsm_delay	0x00	0	Delay between ROT start and X−readout (Zero ROT mode) Delay between ROT end and X−readout (Normal ROT mode with nzrot_xsm_delay_enable=‘1’)	
3	195		roi_active0	0x0001	1		RW
		[7:0]	roi_active[7:0]	0x01	1	Active ROI’s selection	
5	197		black_lines	0x0102	258		RW
		[7:0]	black_lines	0x02	2	Number of black lines. Minimum is 1. Range 1 − 255	
		[8]	gate_first_line	0x1	1	Blank out first line ‘0’: No blank-out ‘1’: Blank-out	
		[11:9]	mask_black_ coefficients	0x0	0	Added for MANO REVB: Can be used to reduce the number of black coefficients used during black calibration. When 000, all 8 coefficients are used	
		[12]	mux_black_ coefficients	0x1	0	Added for MANO REVB: Automatically set number of black coefficients during black calibration according to readout mode	
6	198		dummy_lines	0x0000	0		RW
		[11:0]	dummy_lines	0x000	0	Number of Dummy lines Range 0 − 2047	
9	201		exposure	0x0000	0		RW
		[15:0]	exposure	0x0000	0	Exposure time Rolling shutter: granularity lines	
12	204		gain_configuration	0x0A2	162		RW
		[4:0]	gain_stage1	0x02	2	Gain stage 1	
		[12:5]	gain_stage2	0x5	5	Gain stage 2	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
		[13]	gain_lat_comp	0x0	0	Postpone gain update by 1 frame when '1' to compensate for exposure time updates latency. Gain is applied at start of next frame if '0'	
13	205		digital_gain_ configuration	0x0080	128		RW
		[11:0]	db_gain	0x080	128	Digital gain	
14	206		sync_configuration	0x033F	831		RW
		[0]	sync_rs_x_length	0x1	1	Update of rs_x_length will not be sync'ed at start of frame when '0'	
		[1]	sync_black_lines	0x1	1	Update of black_lines will not be sync'ed at start of frame when '0'	
		[2]	sync_dummy_lines	0x1	1	Update of dummy_lines will not be sync'ed at start of frame when '0'	
		[3]	sync_exposure	0x1	1	Update of exposure will not be sync'ed at start of frame when '0'	
		[4]	sync_gain	0x1	1	Update of gain settings (gain_sw, afe_gain) will not be sync'ed at start of frame when '0'	
		[5]	sync_roi	0x1	1	Update of ROI updates (active_roi) will not be sync'ed at start of frame when '0'	
		[8]	blank_roi_switch	0x1	1	Blank first frame after ROI switching	
		[9]	blank_subsampling_ss	0x1	1	Blank first frame after sub-sampling/binning mode switching in snapshot shutter mode (always blanked out in rolling shutter mode)	
		[10]	exposure_sync_mode	0x0	0	When '0', exposure configurations are sync'ed at the start of FOT. When '1', exposure configurations sync is disabled (continuously syncing). This mode is only relevant for Triggered snapshot – master mode, where the exposure configurations are sync'ed at the start of exposure rather than the start of FOT. For all other modes it should be set to '0'. Note: Sync is still postponed if sync_exposure='0'.	
21	213		gain_status	0x0000	0		RO
		[4:0]	gain_stage1	0x00	0	Current stage 1 gain	
		[12:5]	gain_stage2	0x00	0	Current stage 2 gain	
22	214		digital_gain_status	0x0000	0		RO
		[11:0]	db_gain	0x000	0	Current Digital Gain	
		[12]	reserved	0x0	0	reserved	
		[13]	reserved	0x0	0	reserved	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
38	230		pixel_array_ address_config	0x88	136		RW
		[4:0]	y_address_offset	0x8	8	Offset to y−address to map the actual pixel array *Scheme / Value* normal / 4 R1S1 / 2 R2S2 / 2 chk_board / 4 1x2 binning / 2 2x2 binning / 2	
		[9:5]	black_line_address	0x4	4	Black line address for different pixel arch/readout *Scheme / Value* normal / 2 R1S1 / 1 R2S2 / 1 chk_board / 2 1x2 binning / 1 2x2 binning / 1	
39	231		pixel_array_ address_config	0x1397	5015		RW
		[12:0]	reg_seq_last_line	0x1397	5015	Sequencer last line address for different pixel arch/readouts *Scheme / Value* normal / 2507 R1S1 / 1253 R2S2 / 1253 chk_board / 2507 1x2 binning / 1253 2x2 binning / 1253	
40	232		reg_seq_ subsampling_ binning_modes	0x0	0		RW
		[0]	reg_seq_1x2_binning	0x0	0	Enable/disable 1x2 pixel binning '0' − disable 1x2 pixel binning '1' − enable 1x2 pixel binning	
		[1]	reg_seq_2x2_binning	0x0	0	Enable/disable 2x2 pixel binning '0' − disable 2x2 pixel binning '1' − enable 2x2 pixel binning	
		[2]	reg_seq_check_board _subsample	0x0	0	Enable/disable check board pattern subsampling '0' − disable check board pattern subsampling '1' − enable check board pattern subsampling	
		[3]	reg_seq_r1s1 _subsample	0x0	0	Enable/disable read-1-skip-1 subsampling '0' − disable read-1-skip-1 subsampling '1' − enable read-1-skip-1 subsampling	
		[4]	reg_seq_r2s2 _subsample	0x0	0	Enable/disable read-2-skip-2 subsampling '0' − disable read-2-skip-2 subsampling '1' − enable read-2-skip-2 subsampling	

Table 45. REGISTER MAP

Address Offset	Address	Bit Field	Register Name	Default (Hex)	Default (Dec)	Description	Type
54	246		roi_aec_configuration0	0x0000	0		RW
		[8:0]	x_start	0x00	0	AEC ROI X Start Configuration (used for AEC statistics when roi_aec_enable='1')	
55	247		roi_aec_configuration0	0x0000	0		RW
		[8:0]	x_end	0x000	0	AEC ROI X End Configuration (used for AEC statistics when roi_aec_enable='1')	
56	248		roi_aec_configuration1	0x0000	0		RW
		[12:0]	y_start	0x000	0	AEC ROI Y Start Configuration (used for AEC statistics when roi_aec_enable='1')	
57	249		roi_aec_configuration2	0x0000	0		RW
		[12:0]	y_end	0x0	0	AEC ROI Y End Configuration (used for AEC statistics when roi_aec_enable='1')	
Sequencer ROI [Block Offset: 256]							
0	256		roi0_configuration0	0x00	0		RW
		[8:0]	x_start	0x00	0	X Start Configuration	
1	257		roi0_configuration1	0x0EF	239		RW
		[8:0]	x_end	0x0EF	239	X End Configuration	
2	258		roi0_configuration2	0x0000	0		RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
3	259		roi0_configuration3	0x01387	4999		RW
		[12:0]	y_end	0x01387	4999	Y End Configuration	
4	260		roi1_configuration0	0x00	0		RW
		[8:0]	x_start	0x00	0	X Start Configuration	
5	261		roi1_configuration1	0x0EF	239		RW
		[8:0]	x_end	0x0EF	239	X End Configuration	
6	262		roi1_configuration2	0x0000	0		RW
		[12:0]	y_start	0x0000	0	Y Start Configuration	
7	263		roi1_configuration3	0x01387	4999		RW
		[12:0]	y_end	0x01387	4999	Y End Configuration	

PACKAGE INFORMATION

Pin List

MANO 9600 has two output versions; M1-SM (LVDS) and M2-SM (CMOS). The LVDS I/Os comply to the TIA/EIA-644-A Standard and the CMOS I/Os have a 3.3 V signal level. Table 46 and Table 47 show the pin list for both versions.

Table 46. PIN LIST FOR M1-SM LVDS INTERFACE

Pack Pin No.	Pin Name	I/O Type	Direction	Description
1	gnd_33	Supply		3.3 V ground
2	vdd_33	Supply		3.3 V Supply
3	mosi	CMOS	Input	SPI master out - slave in
4	miso	CMOS	Output	SPI master in - slave out
5	sclk	CMOS	Input	SPI clock
6	gnd_18	Supply		1.8 V ground
7	vdd_18	Supply		1.8 V supply
8	NC			Not connected
9	clock_outn	LVDS	Output	LVDS clock output (Negative)
10	clock_outp	LVDS	Output	LVDS clock output (Positive)
11	doutn0	LVDS	Output	LVDS data output channel #0 (Negative)
12	doutp0	LVDS	Output	LVDS data output channel #0(Positive)
13	doutn1	LVDS	Output	LVDS data output channel #1 (Negative)
14	doutp1	LVDS	Output	LVDS data output channel #1(Positive)
15	doutn2	LVDS	Output	LVDS data output channel #2 (Negative)
16	doutp2	LVDS	Output	LVDS data output channel #2 (Positive)
17	doutn3	LVDS	Output	LVDS data output channel #3 (Negative)
18	doutp3	LVDS	Output	LVDS data output channel #3 (Positive)
19	syncn	LVDS	Output	LVDS sync channel output (Negative)
20	syncp	LVDS	Output	LVDS sync channel output (Positive)
21	vdd_33	Supply		3.3 V supply
22	gnd_33	Supply		3.3 V ground
23	gnd_18	Supply		1.8 V ground
24	vdd_18	Supply		1.8 V supply
25	lvds_clock_inn	LVDS	Input	LVDS clock input (Negative)
26	lvds_clock_inp	LVDS	Input	LVDS clock input (Positive)
27	clk_pll	CMOS	Input	Reference clock input for PLL
28	vdd_18	Supply		1.8 V supply
29	gnd_18	Supply		1.8 V ground
30	ibias_master	Analog	I/O	Master bias reference. Connect 47 k to gnd_33
31	vdd_33	Supply		3.3 V supply
32	gnd_33	Supply		3.3 V ground
33	vdd_pix_low	Supply		1.8 V supply
34	vdd_pix	Supply		Pixel array supply (3.3 V)
35	gnd_colpc	Supply		Pixel array ground (0 V)
36	vdd_pix	Supply		Pixel array supply (3.3 V)
37	gnd_colpc	Supply		Pixel array ground (0 V)

Table 46. PIN LIST FOR M1-SM LVDS INTERFACE

Pack Pin No.	Pin Name	I/O Type	Direction	Description
38	gnd_33	Supply		3.3 V ground
39	vdd_33	Supply		3.3 V supply
40	vdd_pix_low	Supply		1.8 V supply
41	gnd_colpc	Supply		Pixel array ground (0 V)
42	vdd_pix	Supply		Pixel array supply (3.3 V)
43	gnd_colpc	Supply		Pixel array ground (0 V)
44	vdd_pix	Supply		Pixel array supply (3.3 V)
45	NC			Not connected
46	NC			Not connected
47	vdd_pix_low	Supply		1.8 V supply
48	NC			Not connected
49	monitor0	CMOS	Output	Monitor output #0
50	monitor1	CMOS	Output	Monitor output #1
51	reset_n	CMOS	Input	Sensor reset (active low)
52	ss_n	CMOS	Input	SPI slave select (active low)

Table 47. PIN LIST FOR M2-SM CMOS INTERFACE

Pack Pin No.	Pin Name	I/O Type	Direction	Description
1	gnd_33	Supply		3.3 V ground
2	vdd_33	Supply		3.3 V supply
3	mosi	CMOS	Input	SPI master out - slave in
4	miso	CMOS	Output	SPI master in - slave out
5	sclk	CMOS	Input	SPI clock
6	gnd_18	Supply		1.8 V ground
7	vdd_18	Supply		1.8 V supply
8	NC			Not connected
9	dout9	CMOS	Output	Data output bit #9
10	dout8	CMOS	Output	Data output bit #8
11	dout7	CMOS	Output	Data output bit #7
12	dout6	CMOS	Output	Data output bit #6
13	dout5	CMOS	Output	Data output bit #5
14	dout4	CMOS	Output	Data output bit #4
15	dout3	CMOS	Output	Data output bit #3
16	dout2	CMOS	Output	Data output bit #2
17	dout1	CMOS	Output	Data output bit #1
18	dout0	CMOS	Output	Data output bit #0
19	frame_valid	CMOS	Output	Frame valid output
20	line_valid	CMOS	Output	Line valid output
21	vdd_33	Supply		3.3 V supply
22	gnd_33	Supply		3.3 V ground
23	clk_out	Analog		Analog clock output

Table 47. PIN LIST FOR M2-SM CMOS INTERFACE

Pack Pin No.	Pin Name	I/O Type	Direction	Description
24	vdd_18	Supply		1.8 V supply
25	lvds_clock_inn	LVDS	Input	LVDS clock input (Negative)
26	lvds_clock_inp	LVDS	Input	LVDS clock input (Positive)
27	clk_pll	CMOS	Input	Reference clock input for PLL
28	vdd_18	Supply		1.8 V supply
29	gnd_18	Supply		1.8 V ground
30	ibias_master	Analog	I/O	Master bias reference. Connect 47 k to gnd_33
31	vdd_33	Supply		3.3 V supply
32	gnd_33	Supply		3.3 V ground
33	vdd_pix_low	Supply		1.8 V supply
34	vdd_pix	Supply		Pixel array supply (3.3 V)
35	gnd_colpc	Supply		Pixel array ground (0 V)
36	vdd_pix	Supply		Pixel array supply (3.3 V)
37	gnd_colpc	Supply		Pixel array ground (0 V)
38	gnd_33	Supply		3.3 V ground
39	vdd_33	Supply		3.3 V supply
40	vdd_pix_low	Supply		1.8 V supply
41	gnd_colpc	Supply		Pixel array ground (0 V)
42	vdd_pix	Supply		Pixel array supply (3.3 V)
43	gnd_colpc	Supply		Pixel array ground (0 V)
44	vdd_pix	Supply		Pixel array supply (3.3 V)
45	NC			Not connected
46	NC			Not connected
47	vdd_pix_low	Supply		1.8 V supply
48	NC			Not connected
49	monitor0	CMOS	Output	Monitor output #0
50	monitor1	CMOS	Output	Monitor output #1
51	reset_n	CMOS	Input	Sensor reset (Active Low)
52	ss_n	CMOS	Input	SPI slave select (Active Low)

Package Specification

Table 48. MECHANICAL SPECIFICATION FOR MANO 9600 CERAMIC LCC PACKAGE

Parameter	Description	Min	Typ	Max	Units
Die (with Pin 1 to the left center)	Die thickness		750		μm
	Die placement accuracy in package	-50		+50	μm
	Die center, X offset to the center of package	2.5	52.5	102.5	μm
	Die center, Y offset to the center of the package	-268.3	-218.3	-168.3	μm
	Die position, tilt to the Die Attach Plane	-1	0	1	deg
	Die rotation accuracy (referenced to die scribe and lead fingers on package on all four sides)	-1	0	1	deg
	Optical center referenced from the die/package center (X-dir)		-4.4		μm
	Optical center referenced from the die/package center (Y-dir)		-1359.8		μm
	Distance from PCB plane to top of the die surface		1.3		mm
	Distance from top of the die surface to top of the glass lid		0.9		mm
Glass Lid Specification	XY size	(-10%)	19.05 x 19.05	(+10%)	mm^2
	Thickness	0.5	0.55	0.6	mm
	Spectral response range	400		1000	nm
	Transmission of glass lid (refer to Figure 44)			92	%
Mechanical Shock	JESD22-B104C; Condition G			2000	G
Vibration	JESD22-B103B; Condition 1	20		2000	Hz
Mounting Profile	Reflow profile according to J-STD-020D.1			260	°C

Package Outline Drawing

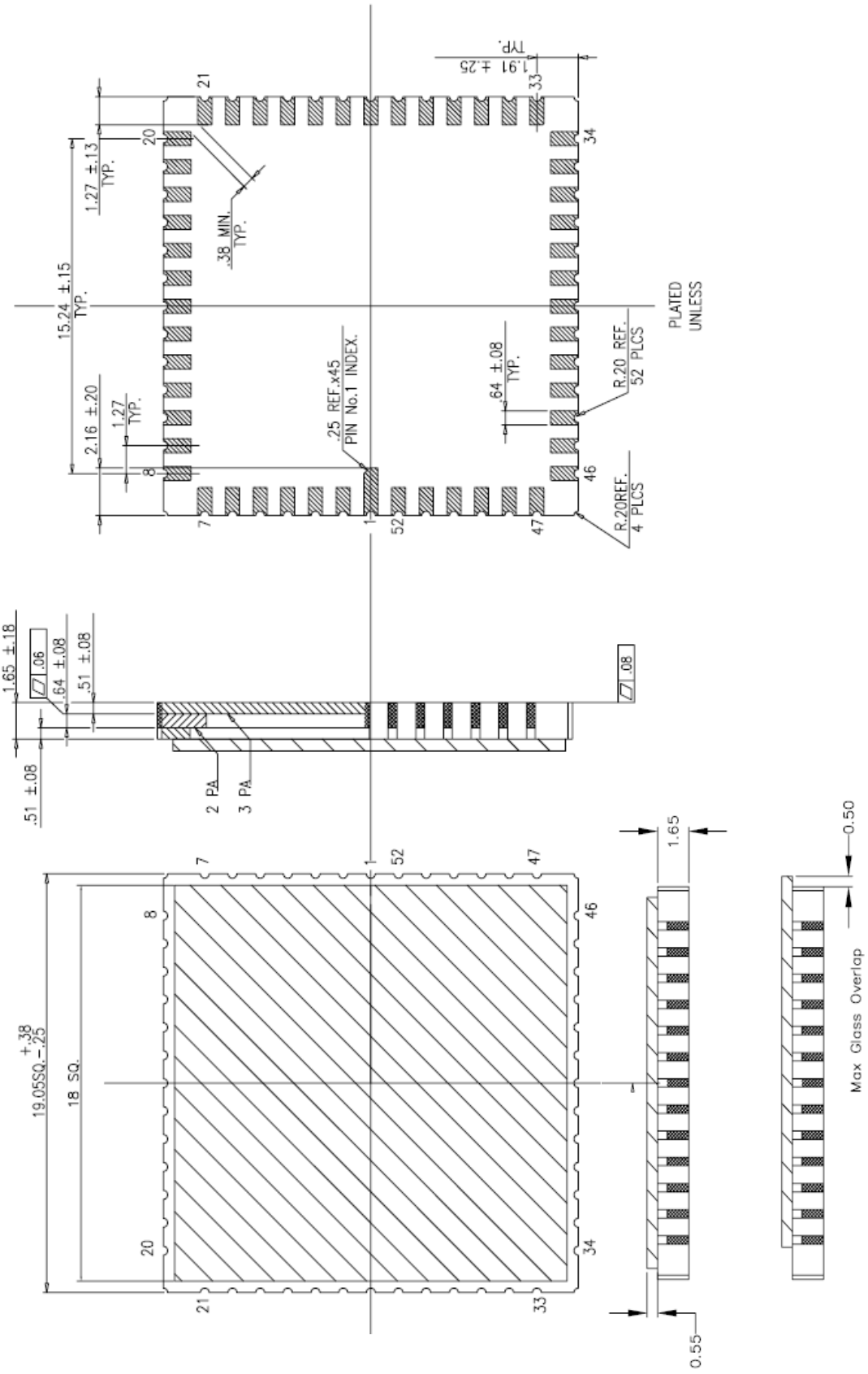


Figure 34. 52−Pin LCC Package (dimensions in mm)

Optical Center Information

The center of the die (CD) is offset from the center of the cavity by (52.5, −218.3) μm.

The center of the cavity is exactly at 50% between the insides of the finger pads.

- Die outer dimensions:
  - B4 is the reference for the Die (0,0) in μm
  - B1 is at (0,10150) μm
  - B2 is at (10900,10150) μm
  - B3 is at (10900,0) μm
- Active Area outer dimensions
  - A1 is the at (785.53, 9663.86) μm
  - A2 is at (10018.33, 9663.86) μm
  - A3 is at (10018.33, 3642.26) μm
  - A4 is at (785.53, 3642.26) μm
- Center of the Active Area
  - AA is at (5401.93, 6653.06) μm
- Center of the Die
  - CD is at (5450, 5075) μm

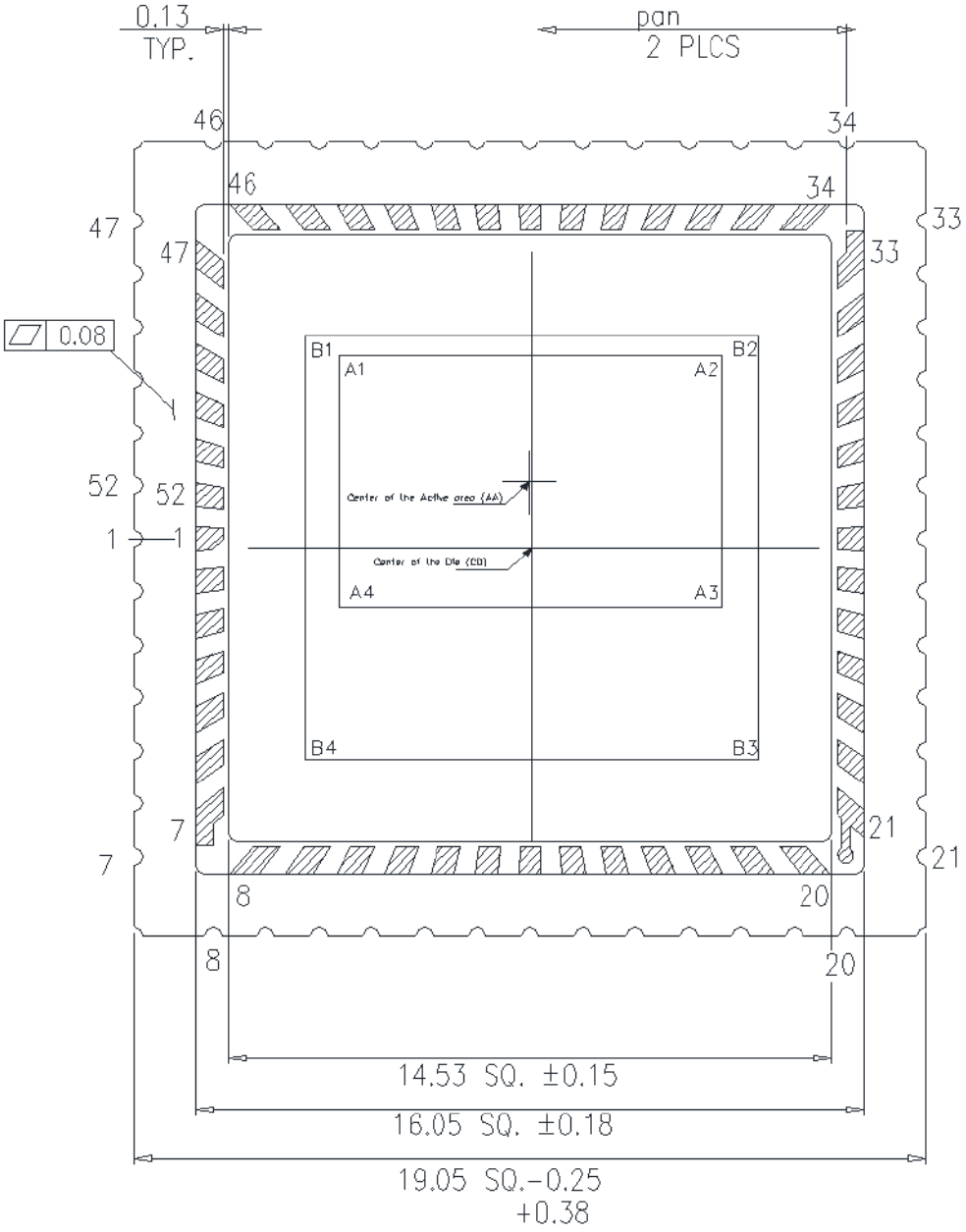


Figure 35. Package Outline Drawing

GLASS LID

The MANO 9600 image sensor uses a glass lid without any coatings. Figure 36 shows the transmission characteristics of the glass lid.

As shown in Figure 36, no infrared attenuating color filter glass is used. (source: http://www.pgo-online.com).

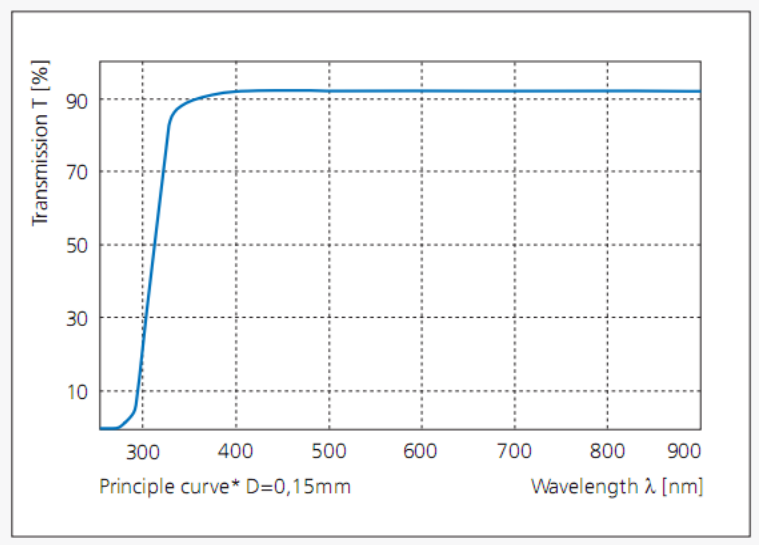


Figure 36. Transmission Characteristics of the Glass Lid

HANDLING PRECAUTIONS

For proper handling and storage conditions, refer to the ON Semiconductor application note AN52561, Image Sensor Handling and Best Practices.

LIMITED WARRANTY

ON Semiconductor's Image Sensor Business Unit warrants that the image sensor products to be delivered hereunder, if properly used and serviced, will conform to Seller's published specifications and will be free from defects in material and workmanship for two (2) years following the date of shipment. If a defect were to manifest itself within 2 (two) years period from the sale date, ON Semiconductor will either replace the product or give credit for the product.

Return Material Authorization (RMA)

ON Semiconductor packages all of its image sensor products in a clean room environment under strict handling procedures and ships all image sensor products in ESD-safe, clean-room-approved shipping containers. Products returned to ON Semiconductor for failure analysis should be handled under these same conditions and packed in its original packing materials, or the customer may be liable for the product.

Refer to the ON Semiconductor RMA policy procedure at http://www.onsemi.com/site/pdf/CAT_Returns_FailureAnalysis.pdf

SPECIFICATIONS AND USER REFERENCES

Specifications, Application Notes and useful resources can be accessible via customer login account at MyOn - CISP Extranet.
https://www.onsemi.com/PowerSolutions/myon/erCispFolder.do

Acceptance Criteria Specification

The Product Acceptance Criteria is available on request. This document contains the criteria to which the MANO 9600 is tested prior to being shipped.

Application Note and References

- AN65464 VITA 2000 HSMC Cyclone Reference Board

ACRONYMS

Acronym	Description
ADC	Analog-to-Digital Converter
AFE	Analog Front End
BL	Black pixel data
CDM	Charged Device Model
CDS	Correlated Double Sampling
CMOS	Complementary Metal Oxide Semiconductor
CRC	Cyclic Redundancy Check
DAC	Digital-to-Analog Converter
DDR	Double Data Rate
DNL	Differential Non-Llinearity
DS	Double Sampling
DSNU	Dark Signal Non-Uniformity
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
FE	Frame End
FF	Fill Factor
FOT	Frame Overhead Time
FPGA	Field Programmable Gate Array
FPN	Fixed Pattern Noise
FPS	Frame per Second
FS	Frame Start
HBM	Human Body Model
IMG	Image data (regular pixel data)
INL	Integral Non-Linearity

Acronym	Description
IP	Intellectual Property
LE	Line End
LS	Line Start
LSB	least significant bit
LVDS	Low-Voltage Differential Signaling
MSB	most significant bit
PGA	Programmable Gain Amplifier
PLS	Parasitic Light Sensitivity
PRBS	Pseudo-Random Binary Sequence
PRNU	Photo Response Non-Uniformity
QE	Quantum Efficiency
RGB	Red-Green-Blue
RMA	Return Material Authorization
rms	Root Mean Square
ROI	Region of Interest
ROT	Row Overhead Time
S/H	Sample and Hold
SNR	Signal-to-Noise Ratio
SPI	Serial Peripheral Interface
TIA	Telecommunications Industry Association
T_J	Junction temperature
TR	Training pattern
% RH	Percent Relative Humidity

GLOSSARY

conversion gain	A constant that converts the number of electrons collected by a pixel into the voltage swing of the pixel. Conversion gain = q/C where q is the charge of an electron (1.602E 19 Coulomb) and C is the capacitance of the photodiode or sense node.
CDS	Correlated double sampling. This is a method for sampling a pixel where the pixel voltage after reset is sampled and subtracted from the voltage after exposure to light.
DNL	Differential non-linearity (for ADCs)
DSNU	Dark signal non-uniformity. This parameter characterizes the degree of non-uniformity in dark leakage currents, which can be a major source of fixed pattern noise.
fill-factor	A parameter that characterizes the optically active percentage of a pixel. In theory, it is the ratio of the actual QE of a pixel divided by the QE of a photodiode of equal area. In practice, it is never measured.
INL	Integral nonlinearity (for ADCs)
IR	Infrared. IR light has wavelengths in the approximate range 750 nm to 1 mm.
Lux	Photometric unit of luminance (at 550 nm, 1lux = 1 lumen/m^2 = 1/683 W/m^2)
pixel noise	Variation of pixel signals within a region of interest (ROI). The ROI typically is a rectangular portion of the pixel array and may be limited to a single color plane.
photometric units	Units for light measurement that take into account human physiology.
PLS	Parasitic light sensitivity. Parasitic discharge of sampled information in pixels that have storage nodes.
PRNU	Photo-response non-uniformity. This parameter characterizes the spread in response of pixels, which is a source of FPN under illumination.
QE	Quantum efficiency. This parameter characterizes the effectiveness of a pixel in capturing photons and converting them into electrons. It is photon wavelength and pixel color dependent.
read noise	Noise associated with all circuitry that measures and converts the voltage on a sense node or photodiode into an output signal.
reset	The process by which a pixel photodiode or sense node is cleared of electrons. ”Soft” reset occurs when the reset transistor is operated below the threshold. ”Hard” reset occurs when the reset transistor is operated above threshold.
reset noise	Noise due to variation in the reset level of a pixel. In 3T pixel designs, this noise has a component (in units of volts) proportionality constant depending on how the pixel is reset (such as hard and soft). In 4T pixel designs, reset noise can be removed with CDS.
responsivity	The standard measure of photodiode performance (regardless of whether it is in an imager or not). Units are typically A/W and are dependent on the incident light wavelength. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
ROI	Region of interest. The area within a pixel array chosen to characterize noise, signal, crosstalk, and so on. The ROI can be the entire array or a small subsection; it can be confined to a single color plane.
sense node	In 4T pixel designs, a capacitor used to convert charge into voltage. In 3T pixel designs it is the photodiode itself.
sensitivity	A measure of pixel performance that characterizes the rise of the photodiode or sense node signal in Volts upon illumination with light. Units are typically V/(W/m^2)/sec and are dependent on the incident light wavelength. Sensitivity measurements are often taken with 550 nm incident light. At this wavelength, 1 683 lux is equal to 1 W/m^2; the units of sensitivity are quoted in V/lux/sec. Note that responsivity and sensitivity are used interchangeably in image sensor characterization literature so it is best to check the units.
spectral response	The photon wavelength dependence of sensitivity or responsivity.
SNR	Signal-to-noise ratio. This number characterizes the ratio of the fundamental signal to the noise spectrum up to half the Nyquist frequency.
temporal noise	Noise that varies from frame to frame. In a video stream, temporal noise is visible as twinkling pixels.

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