

Ultra-low power laser motion sensor for laser mouse applications

Preliminary Data

Features

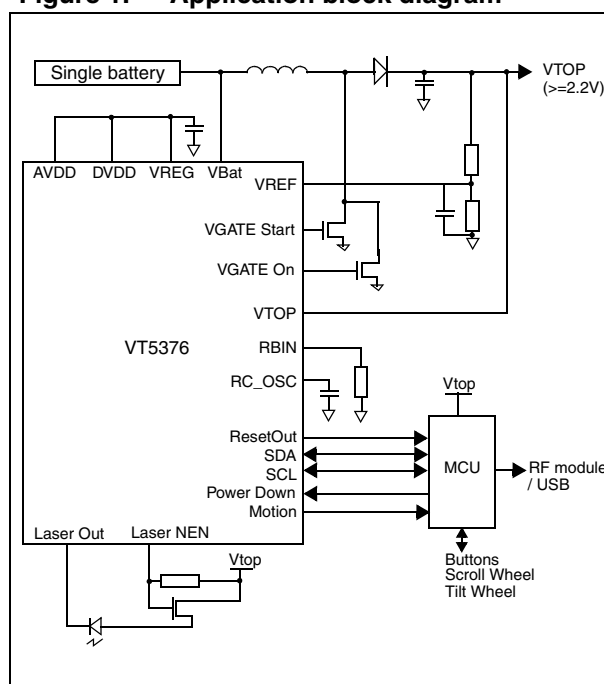
- Ultra-low power performance and high speed/high accuracy motion detection (1 m/s, 20 g)
- Optional on-chip power management scheme (RUN/IDLE1/IDLE2/SLEEP)
- On-chip boost-converter controller enables a complete autonomous single AA/AAA-type battery supply application
- Very low quiescent and operating current mode for battery life saving
- I2C interface, with fast polling rate capability for high end applications (report rate up to 1 per ms)
- Internal oscillator
- CPI programmable up to 3200 CPI
- On-chip ADC for battery level reporting
- Laser drive circuitry, fault detection scheme and safety features
- Versatile usage: the sensor is designed to operate with a companion microcontroller, and can be used for any laser/LED mouse system although it is optimized for wireless applications (27 MHz/2.4 GHz/BT).
- RoHS (lead-free) package

Applications

- Ultra-low power wireless laser mouse, 27 MHz, 2.4 GHz and Bluetooth
- Also suitable for laser USB mouse applications

Description

This device is intended to fit into any 2-chip applications (companion MCU) and offers the best compromise between application cost, power and performance.

Figure 1. Application block diagram


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1 Motion performance

The sensor can operate with a **VCSEL** or **LED** (visible and IR), and when bundled with the appropriate optics subsystem is able to track motion on a wide range of surfaces up to speeds of **1 m/s (40 ips)**, and to detect acceleration of up to **20 g**. The sensor achieves this top speed with very low drift and high accuracy.

Note: Although this device features an UltraLowPower motion detection machine, the power saving has not been achieved by compromising tracking accuracy.

1.1 Technical specifications

Table 1. Technical specifications

Parameter	Description
Resolution	Programmable up to 3200 CPI
Pixel size	30.4µm
Array size	20*20 pixels
Frame rate	up to 4000 fps
Tracking performances	Laser or LED : 1m/s Very low drift.
Supply voltage	1 V to 1.6 V ⁽¹⁾
Operating temperature	0°C to 60°C
Package type	7 mm x 7 mm x 1.4 mm 32 lead LOQFP (Low profile Optical Quad Flat Pack)

1. Using internal boost converter controller. Otherwise, voltage supply ranges from 1.7V to 1.9V.

1.2 Battery life management

The battery life management (in no motion state) can be done manually where the external MCU is the master and controls the sensor state via its POWERDOWN pin (default mode).

Alternatively, the sensor can manage its own power states. In no motion, it cycles through IDLE and SLEEP modes automatically without any intervention from the MCU.

Therefore by using the sensor's automatic power management, the MCU can be fully switched OFF in the case of no motion allowing for extra power savings, and resulting in a very simple driver firmware design.

1.2.1 Manual power management via POWERDOWN pin

In this mode the chip is woken-up by de-asserting the POWERDOWN pin. When doing so both the analog and DCDC engines are woken up in a programmed sequence. The POWERDOWN pin can be re-asserted straight away as the sensor undergoes just a single frame sequence.

1.2.2 Automatic power management via internal timer

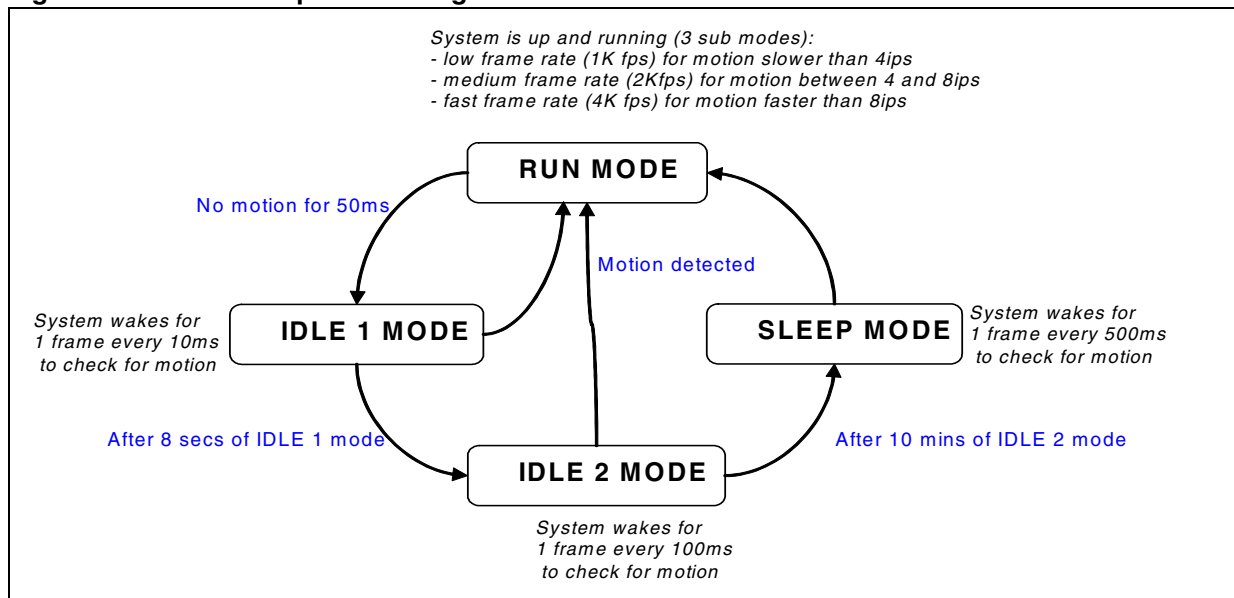
In this mode, after having written the initialization I2C command, the POWERDOWN pin must be left high at all times.

In running mode the motion engine operation is basically the same as the manual power management mode, however, in the case of no motion (after a set time) the chip now has the ability to put itself to sleep for a determined period of time. This mode features the usual modes: RUNNING, IDLE1, IDLE2 and SLEEP, with on-chip preprogrammed time constants (firmware).

If no motion is detected the VT5376 will in turn cycle to IDLE1/IDLE2 then SLEEP. In each of these modes, the behavior is a single frame operation; the RC timer is programmed to wake up for the next period then the sensor goes to sleep. The MOTION pin will go high if motion is detected. The sensor will remain in RUN mode until the host has polled ALL motion data.

In this automatic power management mode the external MCU can set itself to STDBY and just wait for the MOTION pin to come up, hence saving power in the no motion condition. This enables the application MCU firmware to be simplified as much as possible.

Figure 2. Automatic power management



The VT5376 automatic power management has a four state power scheme; RUN, IDLE1, IDLE2 and SLEEP.

RUN mode is the mode where the whole system is up and running. This mode has three sub-modes, dependant on the mouse velocity: 1K fps (for motion slower than 4 ips), 2K fps (for motion between 4 ips and 8 ips) and 4K fps (for motion faster than 8 ips). As long as there is motion the mouse will remain in this state.

After 50 ms of mouse inactivity the mouse goes into the IDLE 1 mode. In this mode, the system wakes up every 10 ms for 1 frame and checks for motion; if the mouse has not moved the system automatically goes back to its low power state otherwise the system will go into RUN mode.

After 8 seconds of IDLE 1 mode, the system then goes into IDLE 2 mode where it wakes up for 1 frame every 100 ms. After 10 minutes of no activity the system falls into SLEEP mode,

which is exactly the same as the IDLE modes except that the system wakes up only every 500 ms to check motion activity.

2 Power supply options and power consumption

The sensor includes a DCDC controller to supply the laser / LED. This allows the overall sensor system to operate from a single AA or AAA battery supply voltage (from 1.6V down to 1V), allowing for a simple and low power / low cost system design. Two power supply schemes can be used.

2.1 Low cost application

The internal DCDC controller and voltage regulators are used so that the overall application can be supplied from a single AA/AAA battery cell, without the need for an external step-up convertor device. This approach is extremely economical.

Table 2. Typical power supply and power consumption

	Run			IDLE1	IDLE2	SLEEP
	4000 fps	2000 fps	1000 fps			
Total @ ITop (chip + Laser/LED)	5.8 mA	3.5 mA	2.4 mA	0.3 mA	0.15 mA	0.1 mA
Total chip @Vbat	0.04 mA	0.04 mA	0.04 mA	0.04 mA	0.04 mA	0.04 mA

- Note: 1 DCDC efficiency from single battery cell to Vtop (typical 2.2V) is around 70%.
 2 Maximum load on Vtop is 25mA

2.2 External supply application

In this instance, the internal DCDC controller and voltage regulators are turned off and bypassed. The sensor then needs to be supplied with a single regulated 1.8V +/- 0.1V.

Table 3. Power supply and typical power consumption

	Run			IDLE1	IDLE2	SLEEP
	4000 fps	2000 fps	1000 fps			
Total @Vtop/Vbat/Dvdd/Avdd (1.8V) Chip + Laser/LED	5.8 mA	3.5 mA	2.4 mA	0.3 mA	0.15 mA	0.1 mA

3 Electrical characteristics

3.1 Supply voltages (using internal DC/DC controller)

Table 4. Supply voltages using DC/DC controller

Symbol	Parameter	Min.	Typ.	Max.	Unit
VTOP	Boosted supply ⁽¹⁾	2.0	2.2	2.6	V
VBAT	Supply from single AA cell	1.0	1.25	1.6	V

1. Value defined by resistors ratio

3.2 Supply voltages (direct drive, bypassing DC/DC controller)

Table 5. Supply voltage values (direct drive, bypassing DC/DC controller)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VTOP	Boosted supply	1.7	1.8	1.9	V
VBAT	Supply from single AA cell	1.0	1.8	1.9	V
AVDD	Analog supply	1.7	1.8	1.9	V
DVDD	Digital core supply	1.7	1.8	1.9	V
VREG	Digital core supply	1.7	1.8	1.9	V

3.3 Logic IO

Table 6. Digital IO electrical characteristics

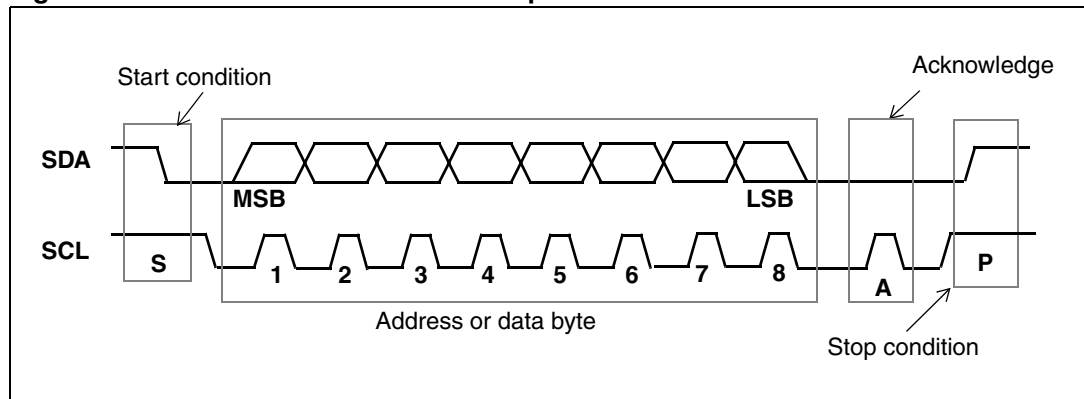
Symbol	Parameter	Min.	Typ.	Max.	Unit
CMOS digital inputs (Reset_Out, Motion, PowerDown, SDA and SCL)					
V _{IL}	Low level input voltage	0		0.3*VDD	V
V _{IH}	High level input voltage	0.7*VDD		VDD + 0.3	V
I _{IL}	Low level input current			-1	μA
I _{IH}	High level input current			1	μA
CMOS digital outputs					
V _{OL}	Low level output voltage (4mA load)			0.3*VDD	V
V _{OH}	High level output voltage (4mA load)	0.7*VDD			V

4 Interface

The interface is 400 kHz I2C, with very fast polling rate for high CPI applications (down to 1 ms period).

4.1 Protocol

Figure 3. Serial interface data transfer protocol

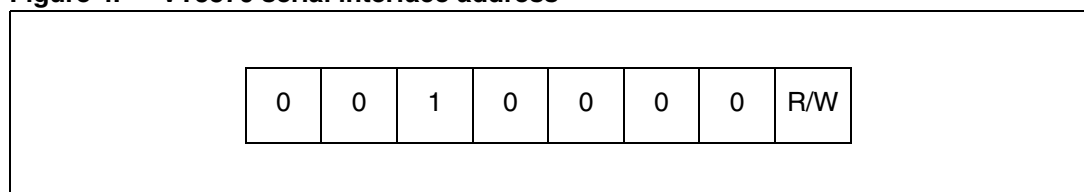


4.2 Data format

Information is packed in 8-bit packets (bytes) always followed by an acknowledge bit. The internal data is produced by sampling *sda* at a rising edge of *scl*. The external data must be stable during the high period of *scl*. The exceptions to this are *start* (S) or *stop* (P) conditions when *sda* falls or rises respectively, while *scl* is high.

The first byte contains the device address byte which includes the data direction *read*, (*r*), *~write*, (*~w*), bit.

Figure 4. VT5376 serial interface address



The byte following the address byte contains the address of the first data byte (also referred to as the *index*).

4.3 Message interpretation

All serial interface communications with the sensor must begin with a *start* condition. If the *start* condition is followed by a valid address byte then further communications can take place. The sensor will acknowledge the receipt of a valid address by driving the *sda* wire low. The state of the *read/-write* bit (lsb of the address byte) is stored and the next byte of data, sampled from *sda*, can be interpreted.

During a write sequence the second byte received is an address index and is used to point to one of the internal registers. The serial interface will automatically increment the index address by one location after each slave acknowledge. The master can therefore send data bytes continuously to the slave until the slave fails to provide an acknowledge or the master terminates the write communication with a *stop* condition or sends a *repeated start*, (*Sr*).

As data is received by the slave it is written bit by bit to a serial/parallel register. After each data byte has been received by the slave, an acknowledge is generated, the data is then stored in the internal register addressed by the current index.

During a read message, the content of the addressed register is then parallel loaded into the serial/parallel register and clocked out of the device by *scl*.

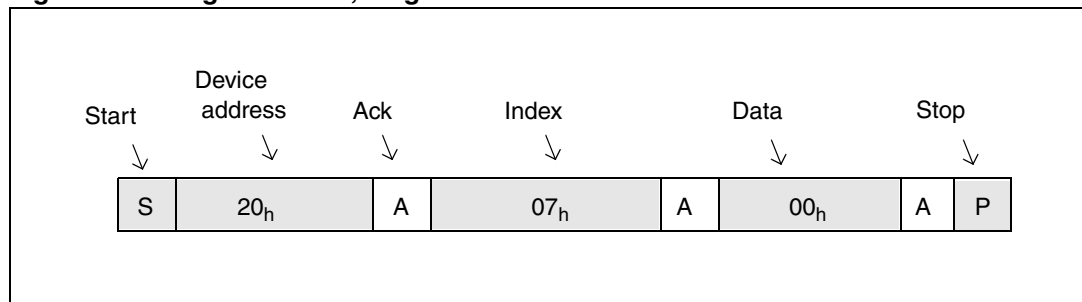
At the end of each byte, in both read and write message sequences, an acknowledge is issued by the receiving device. A message can only be terminated by the bus master, either by issuing a stop condition, a repeated start condition or by a negative acknowledge (NACK) after reading a complete byte during a read operation.

4.4 Type of messages

Single location, single data write

When a random value is written to the sensor, the message will look like this:

Figure 5. Single location, single write

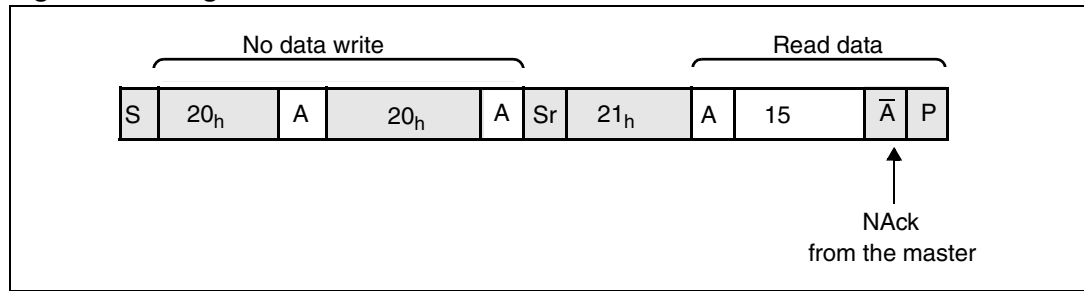


The r/w bit is set to zero for writing. The write message is terminated with a stop condition from the master.

Single location read

When a location is to be read, but the value of the stored index is not known, a write message with no data byte must be written first, specifying the index. The read message then completes the message sequence. To avoid relinquishing the serial to bus to another master a repeated start condition is asserted between the write and read messages.

Figure 6. Single read



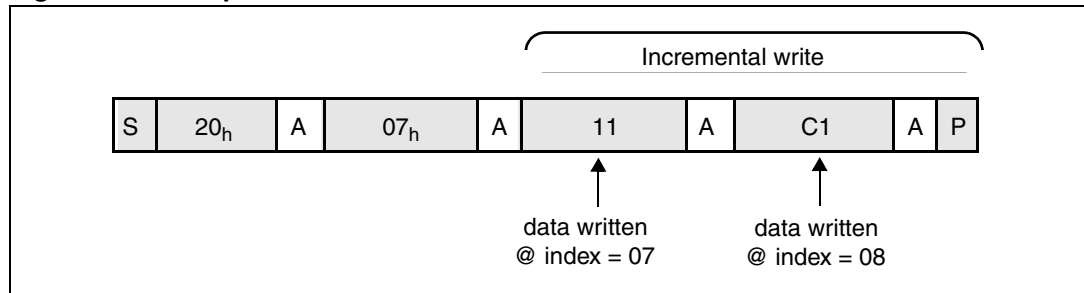
As mentioned in the previous example, the read message is terminated with a negative acknowledge (\bar{A}) from the master.

Multiple location write

It is possible to write data bytes to consecutive adjacent internal registers without having to send explicit indexes prior to sending each data byte.

Note: An auto-increment write is assumed if no stop condition occurs.

Figure 7. Multiple location write

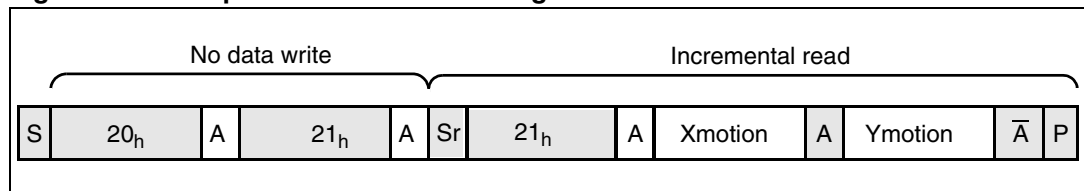


Multiple location read: reading motion value example

Multiple locations can be read within a single read message. An auto-increment write is assumed.

Note: Registers are read until the master Nacks the data.

Figure 8. Multiple location read: reading motion



5 I2C control register map

Table 7. I2C control register map

Address	Bits	Name	R/W	Default	Description
0x00	[7:0]	Device Hardware revision	RO	00h	HW revision: set by the mask set revision
0x01	[7:0]	Device Soft revision	RW	01h	FW revision: is updated every time internal firmware of minor revision is done.
0x05	[0]	Automatic Power management	RW	0h	When set, the device controls its own power mode state machine in no motion condition. If not set, POWERDOWN controls the state of the device (standby/run)
	[1]	Laser Selected	RW	0h	When set, the device sets all internal variables to optimize the system for laser illumination. If set, LASER_OUT is activated to direct drive a VCSEL, and LASER_NEN controls its power supply switch. If not set, LASER_NEN becomes the LED_ON signal, toggling at frame rate.
	[2]	Use External Supply	RW	0h	1: The device switches its internal 1.8 V regulator off, and assumes 1.8 V will be supplied at all times to Vtop, DVDD and AVDD. VBat can also be supplied by the same 1.8V or from a single battery. 0: Device uses internal regulators (Vtop must be set >= 2.2V).
	[3]	Host Config Done	RW	0h	This bit must be set to 1 to indicate to the chip that the boot configuration of the sensor (mainly this register) is complete, and it can start motioning.
	[5]	Led dac driven	RW	0h	If set to 1, and the chip is set in LED mode, then the LED is direct driven by the internal DAC.
	[7]	fw idle state	RW	0h	If enabled the MCU firmware will go into an idle mode (I2C commands still available).

Table 7. I2C control register map (continued)

Address	Bits	Name	R/W	Default	Description
0x0A	[7]	Force Laser Out ON	RW	0h	If set to 1, this sets the LASER_OUT DAC always ON (instead of toggling normally). This mode is provided in case the DAC current needs calibrating. To confirm this mode, register 0x0D will also need to be written to (complement data).
	[6:0]	DAC current setting	RW	7Fh	Sets DAC current setting. To validate the setting, register 0x0D will also need to be written to (complement data). With Rbin = 12K ohms, 0x7F: 3.4mA 0x00: 10mA.
0x0B	[0]	Laser Drive Enable	RW	0h	0: Current source OFF 1: Enable current source
	[1]	Laser NEN Out	RW	1h	Laser NEN pin state Note: This command is only valid if bit [5] is 1
	[2]	Laser NEN OD Enable	RW	1h	0: LASER_NEN 1.8V capable CMOS 1: LASER_NEN - OpenDrain 5V tolerant Note: This command is only valid if bit [5] is 1
	[3]	Force Laser Out High	RW	0h	0: Normal operation, LASEROUT set by DAC 1: Set to 1 to detect short to GND on LASER_OUT
	[4]	Laser comp Enable	RW	0h	0: Disable fault detection comparators 1: Enable fault detection comparators
	[5]	Laser NEN trk led n	RW	0h	0: LASER_NEN replaced by TRK_LED pulse (LED) 1: LASER_NEN controlled by bits [1] and [2] (Laser)
	[6]	Laser Bias Enable	RW	0h	0: Disable bias current source 1: Enable bias current source Note: valid only if bit [7] is high
	[7]	Laser Bias Ctrl	RW	0h	0 : Laser bias is driven the same way as laser drive (DAC) 1 : Laser bias is controlled with laser_bias_enable signal (bit [6])

Table 7. I2C control register map (continued)

Address	Bits	Name	R/W	Default	Description
0x0C	[5]	Rbin Low	RO	0h	0: Rbin above threshold 1: Rbin below threshold (shorted to GND) Note: if Laser_Comp_Enable (reg 0x0B, bit [4]) = 0, Rbin_Low=1
	[6]	Laser Low	RO	0h	0: Laser OUT above LOW threshold 1: Laser OUT below LOW threshold (shorted to GND). Note: if Laser_Comp_Enable = 0, Laser_Low = 1
	[7]	Laser High	RO	0h	0: Laser OUT below HIGH threshold 1: Laser OUT above HIGH threshold (shorted to VDD). Note: if Laser_Comp_Enable = 0, Laser_High = 1
0x0D	[7]	Force Laser Out ON (Compl)	RW	1h	If set to 0, this sets the LASER_OUT DAC always ON (instead of toggling normally). This mode is provided in case the DAC current needs calibrating. To confirm this mode, register 0x0A will also need to be written to (complement data).
	[6:0]	DAC current setting (Compl)	RW	00h	Sets DAC current setting. To validate the setting, register 0x0A will also need to be written to (complement data). With Rbin = 12K ohms, 0x00: 3.4mA 0x7F: 10mA
0x21	[7:0]	X_motion	RO		This register holds the overall X movement data since last polling was done. Value is 8 bit 2's complement. ⁽¹⁾
0x22	[7:0]	Y_motion	RO		This register holds the overall Y movement data since last polling was done. Value is 8 bit 2's complement. ⁽¹⁾
0x23	[0]	X Overflow	RO	0h	This register records if the X-motion integrator has reached its limit.
	[1]	Y Overflow	RO	0h	This register records if the Y-motion integrator has reached its limit.
	[3]	No Motion	RO	0h	This bit is asserted if both X/Y integrators are empty

Table 7. I2C control register map (continued)

Address	Bits	Name	R/W	Default	Description
0x27	[0]	Invert X	RW	0h	Allows X to be inverted ⁽²⁾
	[1]	Invert Y	RW	0h	Allows Y to be inverted ⁽²⁾
	[3]	Swap XY	RW	1h	Replaces X with Y and Y with X
	[5]	Test Pattern Enabled	RW	0h	0: Normal mode 1: Diamond shape pattern
	[7]	Test Pattern Speed	RW	0h	Diamond test pattern speed - 0x0 : motion = 127 max speed 0x1 : motion = 64 0x2 : motion = 32 0x3 : motion = 16
0x29	[7:0]	Min_features[13:6]	RW	0000_0100	This register represents the feature threshold below which motion is no longer valid (in this case, the device reports "0" motion). This is linked to the value reported in registers 0x31/0x32
0x2A	[7:0]	Scaling for X motion vectors	RW	0001_0000	Sets resolution as CPI: 8: 400 CPI 16: 800 CPI Assuming lens magnification of x0.5
0x2B	[7:0]	Scaling for Y motion vectors	RW	0001_0000	Sets resolution as CPI: 0x08: 400 CPI 0x10: 800 CPI Assuming lens magnification of x 0.5
0x31	[15:8]	Features count	RO		Feature count report: the higher the value, the more distinctive features the surface requires, for the motion detection machine to operate reliably.
0x32	[7:0]		RO		
0x41	[7:0]	Exposure [8:1]	RW	80h	Exposure value in 2 x CLK12 period units
0x43	[4]	Auto Expo En	RW	1h	Auto exposure enable
0x47	[7:0]	Vbat converted data	RO		This register holds the current converted data from the Vbat input voltage. The data range is as follows: 0000_0000: Vbat = 0.6 V 1111_1111: Vbat = 1.6 V The response is linear for each value in between. ADC step: 1V/256 = 3.9mV
0x4F	[7:0]	Exp max value	RO		This registers holds the maximum pixel value (before CDS) for the current frame. It shows if some pixels are saturated or not.

Table 7. I2C control register map (continued)

Address	Bits	Name	R/W	Default	Description
0x61	[7:0]	IMAGE[7:0]	RO		This register contains the pixel value when the frame dump feature has been activated (reg 0x62, bit 0). To read the 400 pixels from the captured frame, the register must be read 400 consecutive times.
0x62	[0]	Frame dump mode enable	RW	0h	If set to 1, the device will capture a single frame. When the frame is captured and ready to be downloaded via reg 0x61, bit 2 (frame ready) is set.
	[1]	Frame dump start	RO	0h	Bit is set at start of frame dump
	[2]	Frame ready for download		0h	This bit is asserted when the captured frame is ready to be downloaded via reg 0x61. When frame download is complete, bit 3 is reset
	[3]	Frame upload complete	0h	This flag is set when all 400 pixels have been read by I2C host.	
	[4]	PCI Test enable	R/W	0h	If set Motion, Laser_NEN, Reset_Out and VGate_On become PCI data outputs (QCLK, FST and 2 bits serial data)
0x82	[1]	Timer ITR enable	R/W	1h	Timer interrupt enable.

1. Internal ACCUMULATOR is reduced from this value every time it is read.
2. Default changes to 1 for a laser system after *host_config_done* (that is, system set up for optics without a lens)

6 Laser

6.1 Direct laser drive and calibration

The sensor includes a 7-bit DAC and an output current source.

The DAC value must be set via two I2C commands after power-up (default is MIN = 3.4mA, with Rbin = 12K).

To allow VCSEL output power measurements to be done, the user can set the laser out (normally strobed during operation) to continuously on via an I2C command. This feature is optional and is designed to offer maximum flexibility.

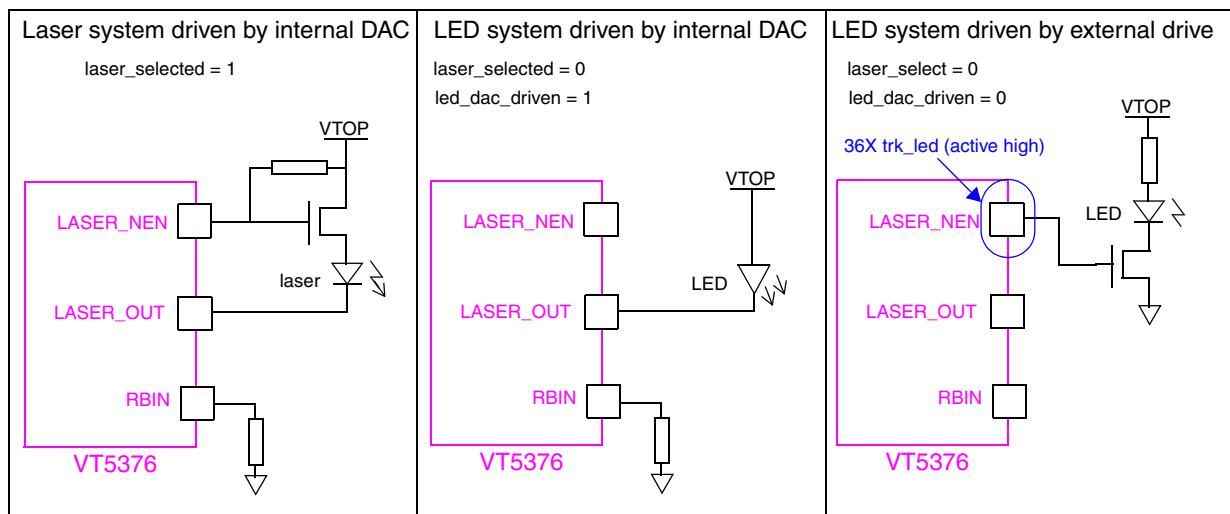
Alternatively, the Idac maximum (up to a max = 13mA) and minimum values can be changed by adjusting the Rbin value (for example, with Rbin = 24K, Idac max = 5mA and Idac min = 1.7mA).

Idac max is set by the formula:

$$I_{dac} \text{ (max)} = 120/R_{bin} \text{ (result in mA, Rbin in kohms)}$$

No external driver is required, just a FET power switch controlled by LASER_NEN signal.

Figure 9. Application schematics using Laser or LED (driven with internal DAC or external current source)



6.2 Laser or led system managed by host (external micro)

The host must first select **LED** or **LASER** (bit [1] of register 0x05).

- **LED**

The host must select if the LED is to be driven by the internal DAC or an external current supply using bit [5] of register 0x05 (*led_dac_driven*). Bit [3] of register 0x05 (*host_config_done*) then needs to be set.

- **Case internal DAC drive:** VT5376 sets the maximum current from the DAC and the system starts running.
- **Case external drive:** VT5376 powers down its laser_drive and the led_on signal is present on the LASER_NEN pin.

- **LASER**

The host must first decide whether to perform LASER fault detection (described in [Section 6.3](#)) then set bit [3] of register 0x05 (*host_config_done*).

If the system passes the laser fault detection (or *laser_fault_detect* was not performed), the host can then adjust the LASER DAC current by writing a value to bits [0-6] in register 0x0A AND writing its complementary value to bits [0-6] of register 0x0D, if the values are not compatible the VT5376 applies the minimum DAC current.

6.3 Laser fault detection and safety feature

The sensor includes a set of diagnostic features that can be carried out at power-up (before setting *host_config_done*). The tests listed below can be selected.

- Check LASER_OUT is not shorted to VDD ($LASER_OUT < 1.2V$).
 - Enable DAC and disable OUT_HIGH switch by writing 0xF7 to register 0x0B (*Top_laser_setting*), then make *force_laser_out_on* = 1, by writing 0x01 to bit 7 of register 0x0A (*Top_laser_DAC_setting*), and 0 to its complementary bit (bit 7) in register 0x0D (*Top_laser_Dac_setting_C*). Finally read bit 6 of register 0xC to ensure that *laser_low* = 1.
External LASER_NEN switch must be fitted in order to make LASER_OUT go below 0.4V.
- Check LASER_OUT and RBIN are not shorted to GND ($LASER_OUT$ and $RBIN > 0.4V$).
 - Disable DAC and enable OUT_HIGH switch (*force_laser_out_high* = 1) by writing 0xFE to register 0x0B (*Top_laser_setting*). Then read register 0x0C (*Top_laser_diagnostics*) to ensure that bit 7 (*laser_high*) is set to 1 and bit 5 (*Rbin_low*) is set to 0.

If the result of these tests is a pass then the MCU can set the laser system as follows:

1. Set bit [3] of register 0x05 (*host_config_done*).
2. Write 0x25 (*laser_drive* and *laser_nen_enable*) in register 0x0B (*Top_laser_setting*).
3. Write the required DAC value (bits 0-6) in register 0x0A (*Top_laser_DAC_setting*) ensuring that *force_laser_out_on* = 0. Write the 1's complement value of the above setting in register 0x0D (*Top_laser_Dac_setting_C*).

7 General features

7.1 Device clocking

The device integrates its own oscillator. It does not require an external Xtal or resonator, instead it requires only an external capacitor of 33 pF. The accuracy of this cap will determine the accuracy of the internal clock. Ignoring the capacitor accuracy, the frequency will be accurate within 10% range.

7.2 Battery level monitoring

The device includes an 8-bit ADC that translates the VBAT voltage into an 8-bit value that can be read via I2C. The external MCU can upload this value and take any action required.

7.3 Resolution setting (counts/inch)

Due to an accurate on-chip interpolation process, the device operates below the pixel resolution. This enables the user to easily select any desired resolution via a simple register write.

Note: Different resolutions can be applied to X and Y. This could be useful in case of optical non-symmetry or distortion.

7.4 Image (frame) capture

It is possible to capture an image and download it using a simple I2C write/read sequence. This is useful to calibrate optics during pre-production or to perform basic tests.

In order to achieve this, the user must:

1. Put the firmware into IDLE by setting bit 7 of register 0x05 (*fw_idle_state*).
2. Disable the motion engine controller by clearing bit 1 of register 0x82 (*timer_itr_enable*).
3. Enable frame dump mode by setting bit 0 of register 0x62 (*frame_dump_mode_enable*).

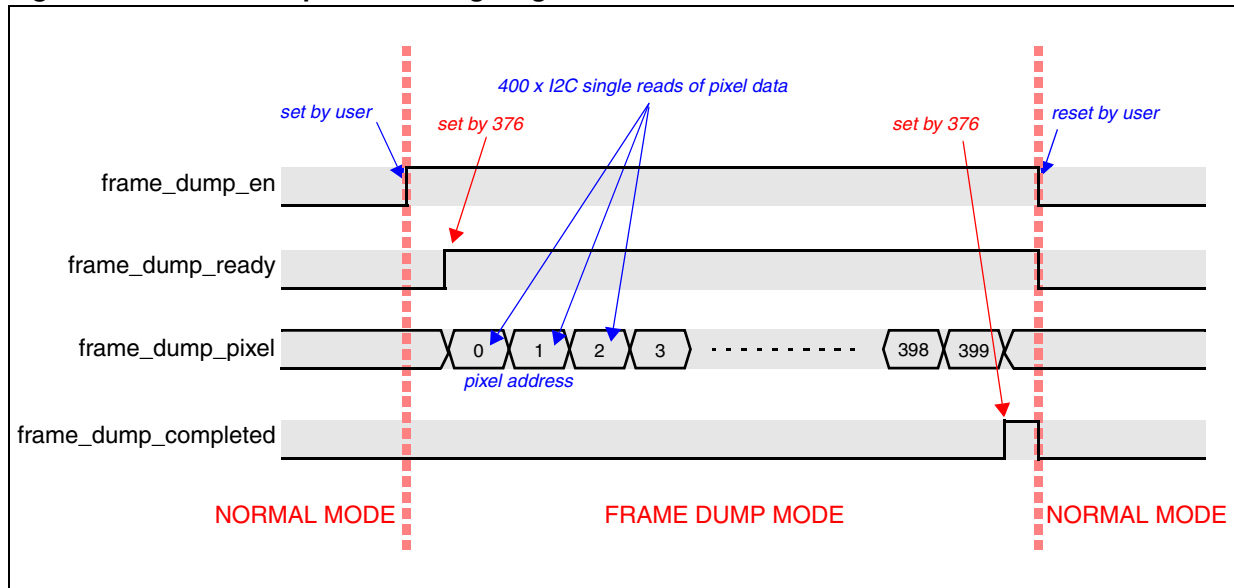
The VT5376 resets the sensor, enables the DCDC, runs a single frame sequence and stores it into an internal RAM. Once this process is complete, the VT5376 signals that the image is ready for download, by asserting bit 2 in register 0x62 (*frame_ready_for_download*).

When this flag is asserted, the user can download the 400 consecutive pixels by reading register 0x61 (*image*) 400 consecutive times.

When all the pixels have been read, the VT5376 signals the end of the process by setting bit 3 in register 0x62 (*frame_upload_complete*).

To resume normal operation the user should reset bit 0 in register 0x62 to exit the frame dump mode, take the firmware out of Idle by resetting bit 7 of register 0x05 and set bit 1 of register 0x82 to enable the motion controller.

Figure 10. Frame dump mode timing diagram



7.5 Image streaming

To enter this test mode, set bit 4 of registry 0x62 to 1 (*PCI_test_enable*).

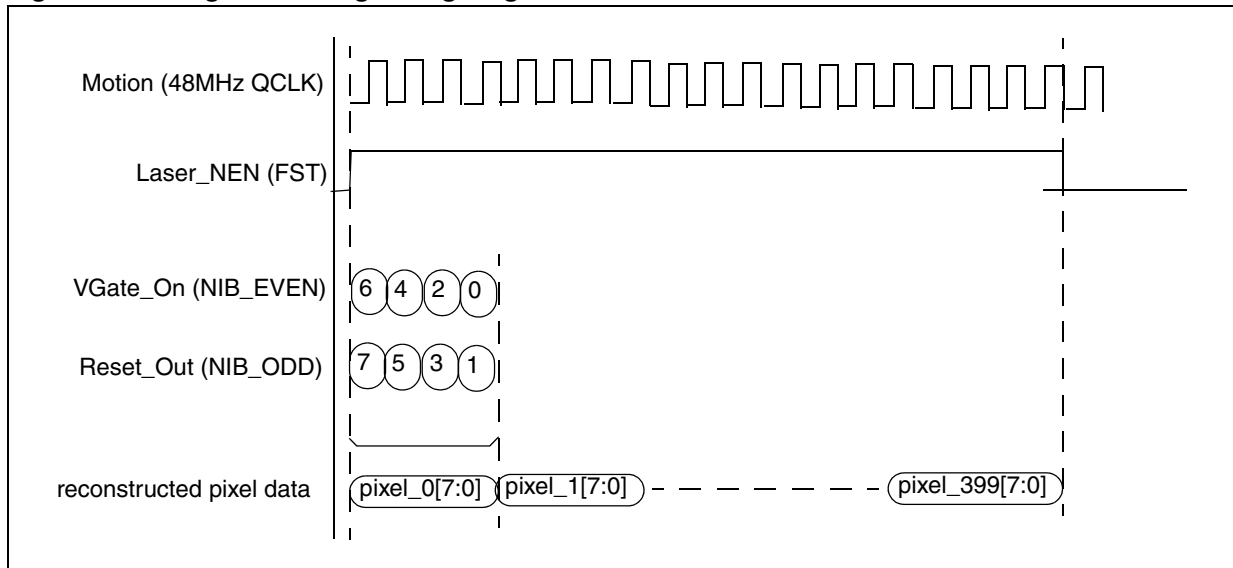
In this mode, the pins VGATE_ON, RESET_OUT, LASER_NEN and MOTION are used to output serially fast video data in the form of 2 bits nibble + FST and QCLK.

Upon receipt of an FST (LASER_NEN) rising edge, NIB_EVEN (VGATE_ON) and NIB_ODD (RESET_OUT) output data every 48 MHz clock cycle. The signals should be sampled 10 ns after the FST rising edge, and then every 20.8 ns exactly, during $400 \times 4 = 1600$ cycles.

Groups of four consecutive NIB_EVEN and NIB_ODD must then be repackaged together to form a single 8-bit pixel data. This format enables the pixels to be output at the same frame rate as normal operation, and keeps I2C available to access the usual register settings.

For more details on image streaming please refer to the VT5376 image system user manual.

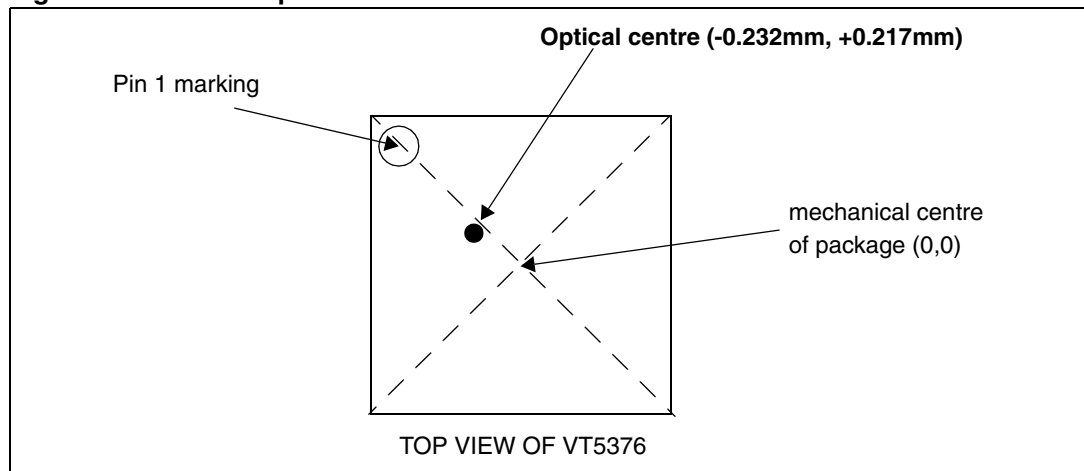
Figure 11. Image streaming timing diagram



7.6 Optical centre

The optical centre of the VT5376 is NOT in the centre of the package. It is offset by -0.232 mm in the X axis and +0.217 mm in the Y axis with respect to the centre of the package as shown in [Figure 12](#). The PCB designer must take this into account when laying out the PCB.

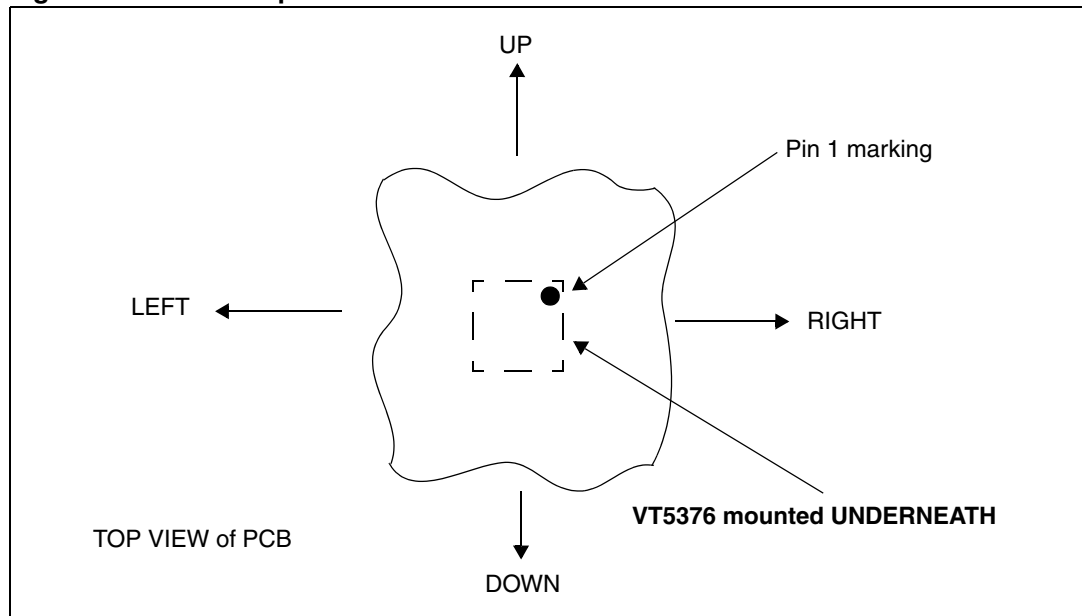
Figure 12. VT5376 optical centre



7.7 Sensor orientation on PCB (with lens)

The VT5376 must be orientated correctly on the PCB in order to move the cursor in the correct directions when the mouse is moved. This is shown in [Figure 13](#).

Figure 13. VT5376 optical centre



8.1 Overall 2.4 GHz mouse power consumption example

Assumptions

- VCSEL, MCU and 2.4 GHz Tx operate from 2.2 V
- MCU consumes 1 mA in running mode and 50 uA in standby mode. In no motion period, it remains in standby until it receives an interrupt from the VT5376, indicating that MOTION has been detected.
- 2.4 GHz Tx consumes 10 mA, but data is sent by bursts of 500 μs every 5 ms (that is Nordic nRF2402).
- Maximum current is delivered to VCSEL (10 mA strobed).
- DCDC efficiency is 70%
- Ambient temperature

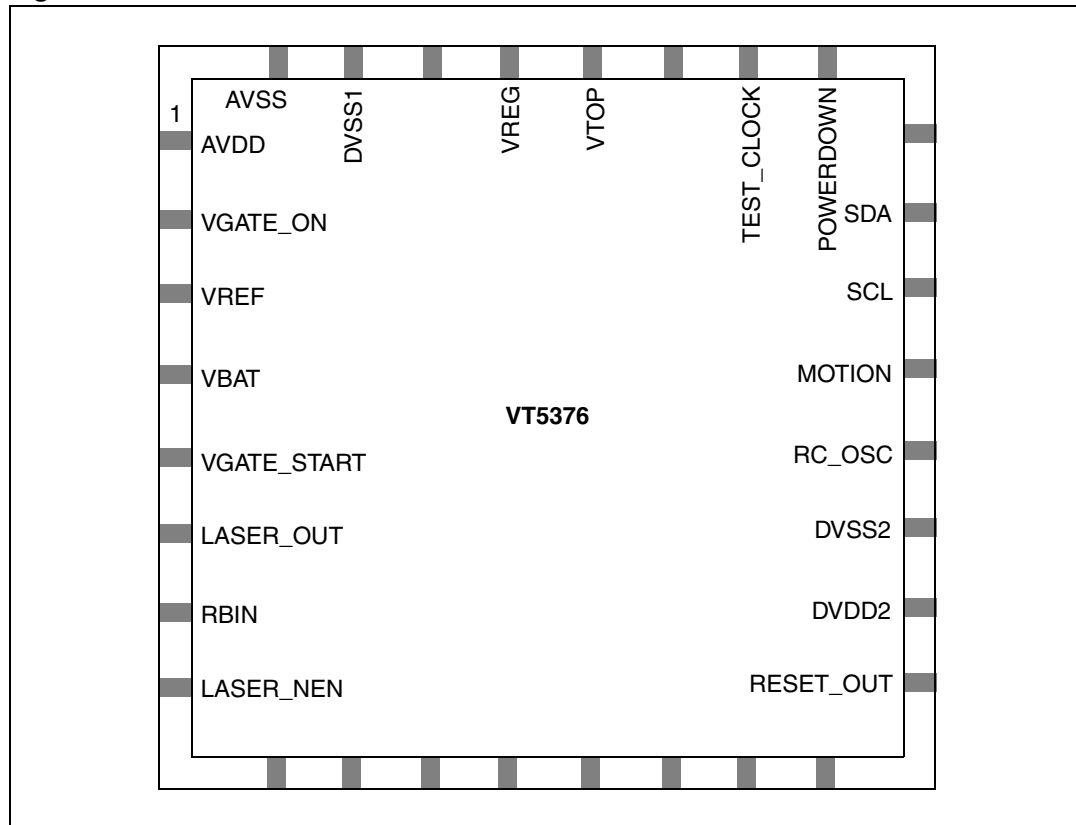
Table 8. Power supply and typical power consumption

	Run			IDLE1	IDLE2	SLEEP
	4000 fps	2000 fps	1000 fps			
Total @ Vbat (1.25 V)	18 mA	12 mA	9.3 mA	0.59 mA	0.29 mA	0.24 mA

Using STMicroelectronics battery life model, these values would enable the mouse to operate for 12 months from two AA batteries in parallel.

9 Pinout

Figure 15. Pinout



9.1 Pin description

Table 9. VT5376 pin description

Pin	Pin name	Type	Description	Comment
1	AVDD	PWR	1.8 V regulated and analog supply	Connect to VREG/DVDD
2	VGATE_ON	I/O	Digital IO	Supplied by VTOP
3	VREF	ANA	Analog ref input	To set VTOP
4	VBAT	PWR	Single battery supply	int DCDC: 1.0 V to 1.6 V ext: 1.0 V to 1.9 V
5	VGATE_START	ANA	Output	Supplied by Vbat
6	LASER_OUT	ANA	Laser drive set by internal DAC	
7	RBIN	ANA	Sets maximum laser/led current	Typical 12K ohms
8	LASER_NEN	I/O	Laser enable	Active low
17	RESET_OUT	I/O	Digital IO	1.8V only
18	DVDD2	PWR	1.8 V regulated and digital supply	Connect to VREG
19	DVSS2	PWR	Digital Ground	
20	RC_OSC	ANA	6 MHz Oscillator	Connect 33pF to ground
21	MOTION	I/O	Digital IO	1.8V only
22	SCL	I/O	Digital IO	5V tolerant
23	SDA	I/O	Digital IO	5V tolerant
25	POWERDOWN	I/O	Digital IO	Active high
26	TEST_CLOCK	I/O	Digital IO	Connect to ground
28	VTOP	PWR	Power supply for internal regulators	int DCDC: 2.0 V to 2.6 V Ext: 1.8 V +/-0.1 V
29	VREG	PWR	1.8 V regulated supply	Connect to DVDD/AVDD
31	DVSS1	PWR	Digital ground	
32	AVSS	PWR	Analog ground	

Note: All other pins are NOT CONNECTED.

10 Package mechanical data

Figure 16. TQFP32 clear resin body 7.0 x 7.0 x 1.40 footprint 1.0

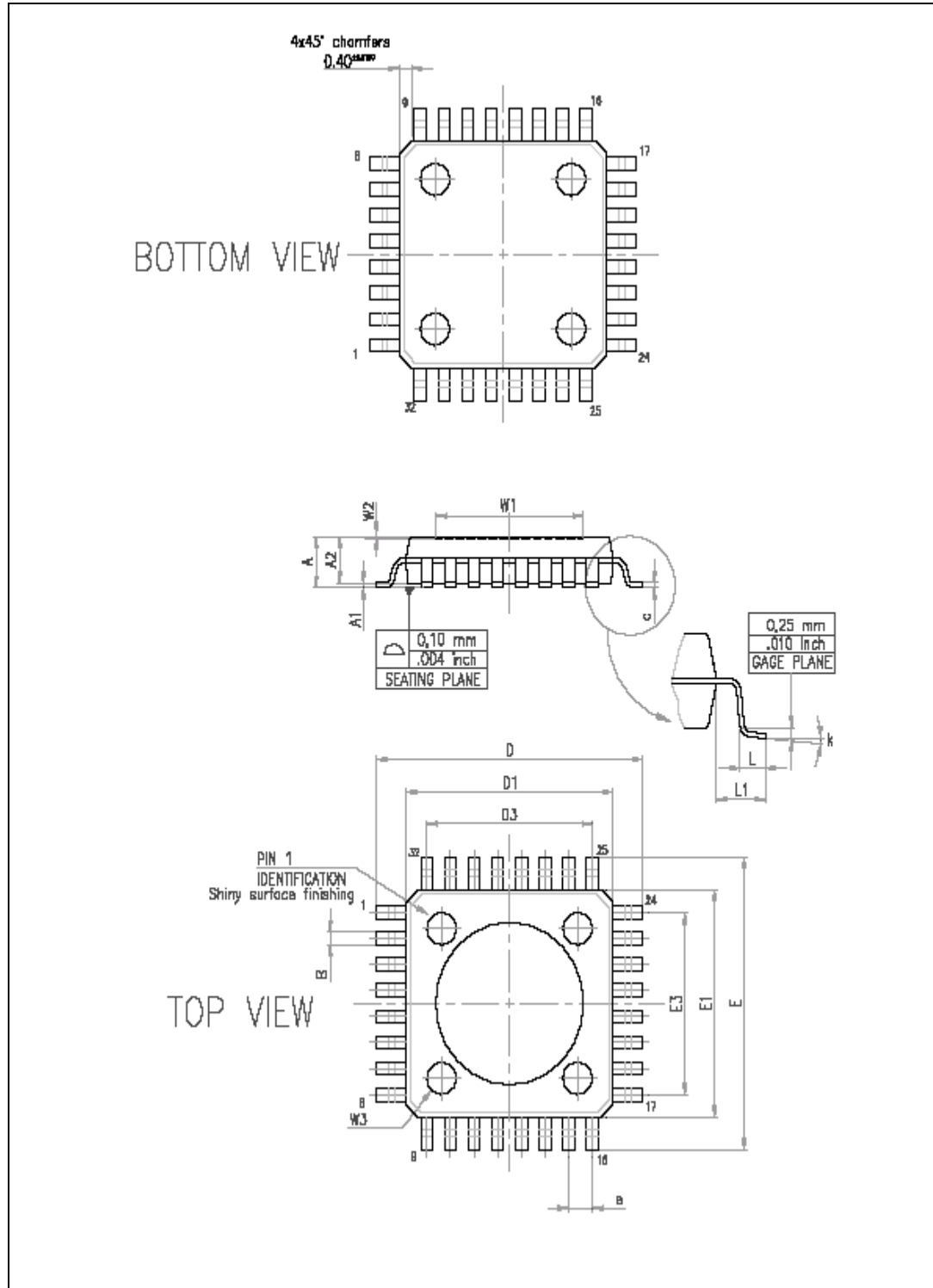


Table 10. TQFP dimensions (mm)

Reference	Minimum (mm)	Typical (mm)	Maximum (mm)
A			1.600
A1	0.050		0.150
A2	1.350	1.400	1.450
B	0.300	0.370	0.450
c	0.090		0.200
D		9.000	
D1		7.000	
D3		5.600	
e		0.800	
E		9.000	
E1		7.000	
E3		5.600	
L	0.450	0.600	0.750
L1		1.000	
k	0d	3.5d	7d
W1		5.000	
W2		0.650	

- Note:
- 1 Surface finish W1 is 0.07 Ra.
 - 2 Ejectors are on 5.2 mm square for both top and bottom package.
 - 3 On top package, only the pin 1 identification is not an engraved ejector.

10.1 TQFP package guidelines

The IC can be exposed a maximum of two times to an IR/Convection reflow solder process having a temperature profile peak of no higher than 240 °C.

The package/chip are lead free and is ROHS compliant.

For full handling guidelines please contact ST (document reference 7310263).

11 Ordering information

Table 11. Ordering information

Order code	Package	Packing
VT5376V032	TQFP32 OPTO 7 mm x 7 mm x 1.4 mm	Tray

Table 12. Evaluation boards ordering information

Order code	Description
STV-376-E01	USB2 VT5376 high-speed imaging system evaluation board
STV-376-E02	VT5376 sensor in a full-speed wired laser mouse evaluation board
STV-376-E03	VT5376 sensor in a low-speed wireless laser mouse evaluation board

12 Revision history

Table 13. Document revision history

Date	Revision	Changes
27-Sep-2007	1	Initial release.
09-Sep-2008	2	Updated <ul style="list-style-type: none"> – Chapter 1: Motion performance – Chapter 2: Power supply options and power consumption – Chapter 3: Electrical characteristics – Chapter 5: I2C control register map – Chapter 6: Laser – Chapter 7: General features – Chapter 8: Typical application – Chapter 9: Pinout – Chapter 10: Package mechanical data – Chapter 11: Ordering information – Image download sections (Section 7.4 and Section 7.5)

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