74ABT657

Octal transceiver with parity generator/checker; 3-state

Rev. 03 — 15 March 2010 Product data sheet

1. General description

The 74ABT657 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT657 is an octal transceiver featuring non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 64 mA. The Transmit/Receive input (pin T/$\overline{R}$) determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (active LOW) enables data from B ports to A ports.

When Output Enable input (pin $\overline{OE}$) is HIGH, both A and B ports are high-impedance. The parity select input (pin ODD/$\overline{EVEN}$) allows the user to generate either an odd or even parity output, depending on the system. Pin PARITY is an output from the generator/checker when transmitting from port A to port B (pin T/$\overline{R}$ = HIGH) and an input when receiving from port B to port A port (pin T/$\overline{R}$ = LOW).

In transmit mode (pin T/$\overline{R}$ = HIGH) port A is polled to determine the number of HIGH inputs on port A. Pin PARITY output goes to the logic state determined by the setting of pin ODD/$\overline{EVEN}$ and by the number of HIGH inputs on port A. For example, if pin ODD/$\overline{EVEN}$ is set LOW (even parity) and the number of HIGH inputs on port A is odd, pin PARITY output goes HIGH, transmitting even parity. If the number of HIGH inputs on port A is even, pin PARITY output goes LOW, keeping even parity.

In receive mode (pin T/$\overline{R}$ = LOW) port B is polled to determine the number of HIGH inputs on port B. If pin ODD/$\overline{EVEN}$ is LOW (even parity) and the number of HIGH inputs on port B is:

- Odd and pin PARITY input is HIGH, pin $\overline{ERROR}$ is HIGH, indicating no error
- Even and pin PARITY input is HIGH, pin $\overline{ERROR}$ goes LOW, indicating an error

2. Features and benefits

- Combinational functions in one package
- Low static and dynamic power dissipation with high speed and high output drive
- Output capability: +64 mA and –32 mA
- Power-up 3-state
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT657D	–40 °C to +85 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74ABT657DB	–40 °C to +85 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74ABT657PW	–40 °C to +85 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1

4. Functional diagram

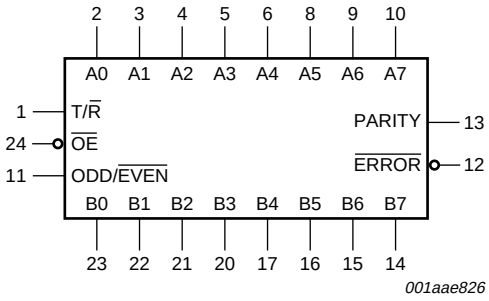


Fig 1. Logic symbol

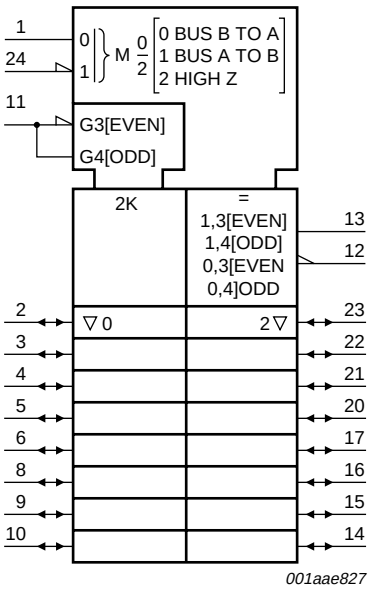


Fig 2. IEC logic symbol

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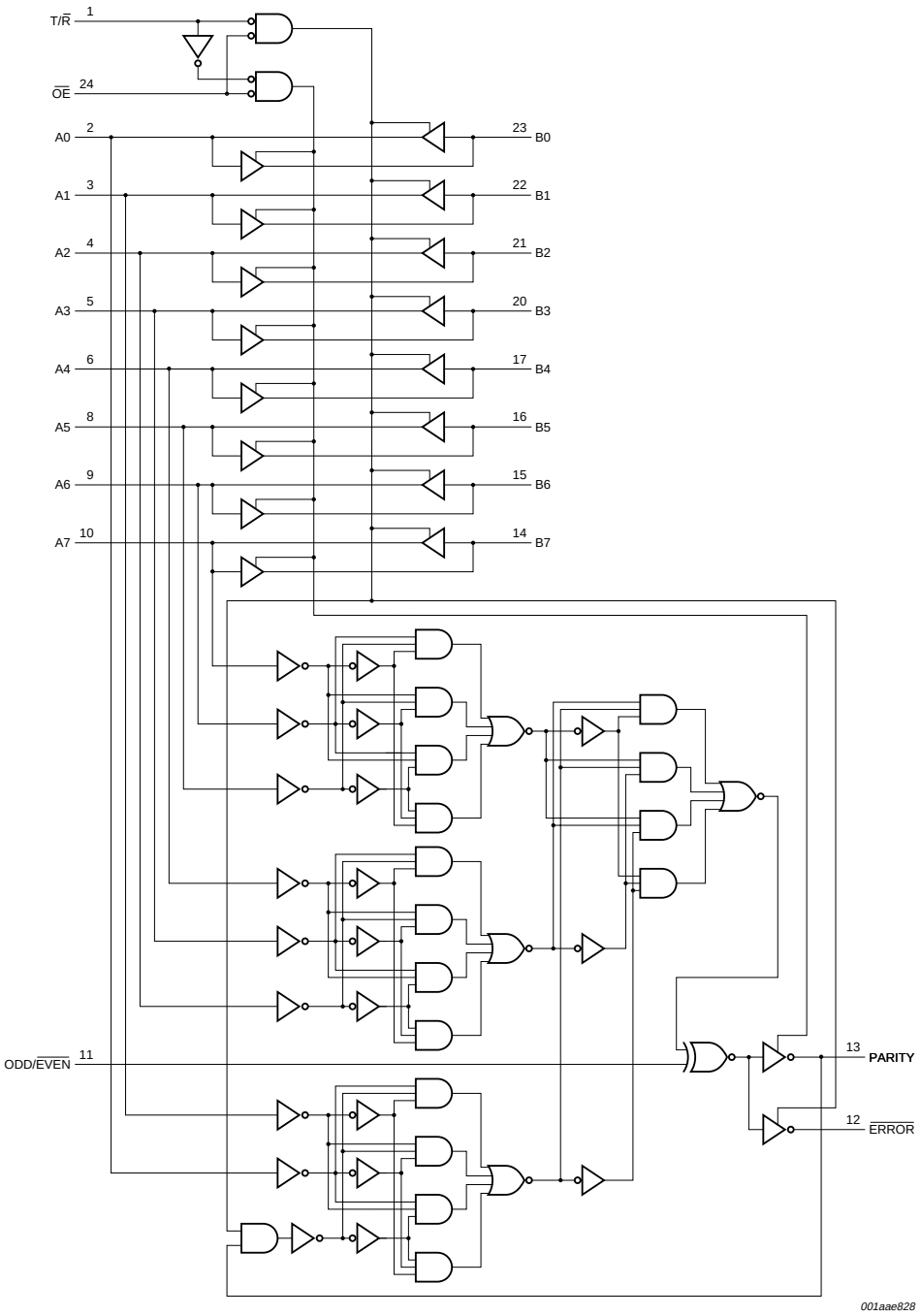


Fig 3. Logic diagram

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5. Pinning information

5.1 Pinning

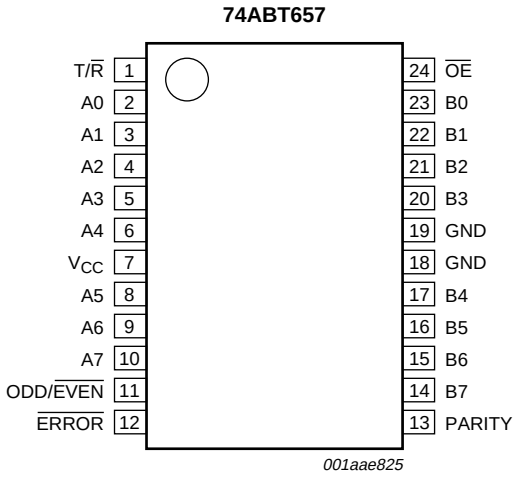


Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
T/$\overline{R}$	1	transmit/receive input
A0 to A7	2, 3, 4, 5, 6, 8, 9, 10	A port input/3-state output
V_{CC}	7	positive supply voltage
ODD/$\overline{EVEN}$	11	parity select input
$\overline{ERROR}$	12	error output in receive mode
PARITY	13	parity output in transmit mode/input in receive mode
B0 to B7	23, 22, 21, 20, 17, 16, 15, 14	B port input/3-state output
GND	18, 19	ground (0 V)
$\overline{OE}$	24	output enable input (active LOW)

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6. Functional description

6.1 Function selection

Table 3. Function selection[1]

Number of inputs HIGH	Inputs			Data I/O	Output	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	Mode
0, 2, 4, 6 and 8 (even)	L	H	H	H	Z	transmit
	L	H	L	L	Z	transmit
	L	L	H	H	H	receive
	L	L	H	L	L	receive
	L	L	L	H	L	receive
	L	L	L	L	H	receive
1, 3, 5 and 7 (odd)	L	H	H	L	Z	transmit
	L	H	L	H	Z	transmit
	L	L	H	H	L	receive
	L	L	H	L	H	receive
	L	L	L	H	H	receive
	L	L	L	L	L	receive
Don't care	H	X	X	Z	Z	3-state

[1] H = HIGH voltage level;
L = LOW voltage level;
X = don't care;
Z = high-impedance OFF-state.

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7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			–0.5	+7.0	V
V_I	input voltage		[1]	–1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	–0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V		–18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V		–50	-	mA
I_O	output current	output in LOW-state		-	128	mA
T_j	junction temperature		[2]	-	150	°C
T_{stg}	storage temperature			–65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		–32	-	-	mA
I_{OL}	LOW-level output current		-	-	64	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	5	ns/V
T_{amb}	ambient temperature	in free air	–40	-	+85	°C

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9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions		25 °C			–40 °C to +85 °C		Unit
				Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = –18 mA		–1.2	–0.9	-	–1.2	-	V
V_{OH}	HIGH-level output voltage	V_I = V_{IL} or V_{IH}							
		V_{CC} = 4.5 V; I_{OH} = –3 mA		2.5	3.5	-	2.5	-	V
		V_{CC} = 5.0 V; I_{OH} = –3 mA		3.0	4.0	-	3.0	-	V
		V_{CC} = 4.5 V; I_{OH} = –32 mA		2.0	2.6	-	2.0	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 64 mA; V_I = V_{IL} or V_{IH}		-	0.42	0.55	-	0.55	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V							
		control pins		-	±0.01	±1.0	-	±1.0	µA
		data pins		-	±5	±100	-	±100	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O ≤ 4.5 V		-	±5.0	±100	-	±100	µA
$I_{O(pu/pd)}$	power-up/power-down output current	V_{CC} = 2.0 V; V_O = 0.5 V; V_I = GND or V_{CC}; $\overline{OE}$ HIGH	[1]	-	±5.0	±50	-	±50	µA
I_{OZ}	OFF-state output current	V_{CC} = 5.5 V; V_I = V_{IL} or V_{IH}							
		V_O = 2.7 V		-	5.0	50	-	50	µA
		V_O = 0.5 V		-	–5.0	–50	-	–50	µA
I_{LO}	output leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}		-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V	[2]	–180	–100	–50	–180	–50	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}							
		outputs HIGH-state		-	0.5	250	-	250	µA
		outputs LOW-state		-	20	30	-	30	mA
		outputs disabled		-	0.5	250	-	250	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND	[3]						
		outputs enabled		-	0.5	1.5	-	1.5	mA
		outputs 3-state, one data input		-	50	250	-	250	µA
		outputs 3-state; one enable input		-	0.5	1.5	-	1.5	mA
C_I	input capacitance	V_I = 0 V or V_{CC}		-	4	-	-	-	pF
$C_{I/O}$	input/output capacitance	outputs disabled; V_O = 0 V or V_{CC}		-	7	-	-	-	pF

[1] This parameter is valid for any V_{CC} between 0 V and 2.1 V with a transition time of up to 10 ms. For V_{CC} = 2.1 V to V_{CC} = 5 V ± 10 %, a transition time of up to 100 µs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

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10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Figure 9.

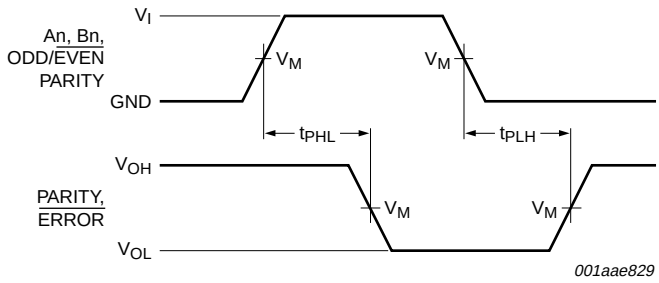
Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			−40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
t_{PLH}	LOW to HIGH propagation delay	An to Bn or Bn to An; see Figure 6	1.1	2.5	4.1	1.1	4.6	ns
		An to PARITY; see Figure 5 and 6	2.5	5.1	6.7	2.5	8.1	ns
		ODD/$\overline{\text{EVEN}}$ to PARITY and $\overline{\text{ERROR}}$; see Figure 5 and 6	1.7	3.5	4.6	1.7	5.3	ns
		Bn to $\overline{\text{ERROR}}$; see Figure 5 and 6	3.9	7.3	10.2	3.9	12.3	ns
		PARITY to $\overline{\text{ERROR}}$; see Figure 5 and 6	2.7	4.5	5.9	2.7	7.7	ns
t_{PHL}	HIGH to LOW propagation delay	An to Bn or Bn to An; see Figure 6	1.2	3.0	3.9	1.2	4.3	ns
		An to PARITY; see Figure 5 and 6	2.8	5.0	7.4	2.8	8.9	ns
		ODD/$\overline{\text{EVEN}}$ to PARITY and $\overline{\text{ERROR}}$; see Figure 5 and 6	1.9	3.7	5.1	1.9	5.8	ns
		Bn to $\overline{\text{ERROR}}$; see Figure 5 and 6	4.0	7.9	10.5	4.0	12.9	ns
		PARITY to $\overline{\text{ERROR}}$; see Figure 5 and 6	3.2	5.2	6.7	3.2	8.1	ns
t_{PZH}	OFF-state to HIGH propagation delay	see Figure 7 and 8 [1]	1.3	3.6	5.5	1.3	6.5	ns
t_{PZL}	OFF-state to LOW propagation delay	see Figure 7 and 8 [1]	1.9	4.2	5.3	1.9	6.5	ns
t_{PHZ}	HIGH to OFF-state propagation delay	see Figure 7 and 8	2.4	3.6	5.6	2.4	6.2	ns
t_{PLZ}	LOW to OFF-state propagation delay	see Figure 7 and 8	2.2	3.4	7.3	2.2	7.8	ns

[1] These delay times reflect the 3-state recovery time only and do not include the delay through the buffers and the parity check circuitry which affect the $\overline{\text{ERROR}}$ output. To ensure **valid** information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output. **Valid** data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to PARITY).

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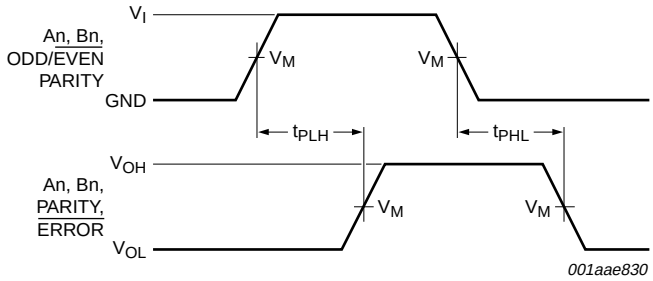
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11. Waveforms



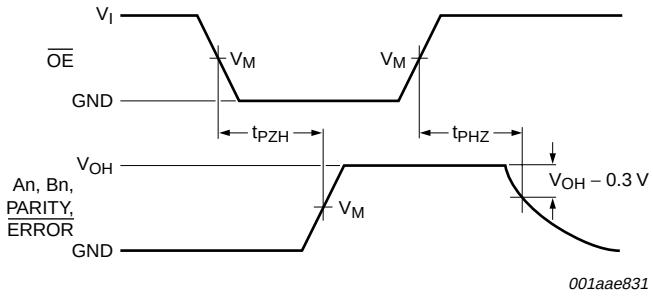
V_M = 1.5 V

Fig 5. Propagation delay for inverting output



V_M = 1.5 V

Fig 6. Propagation delay for non-inverting output

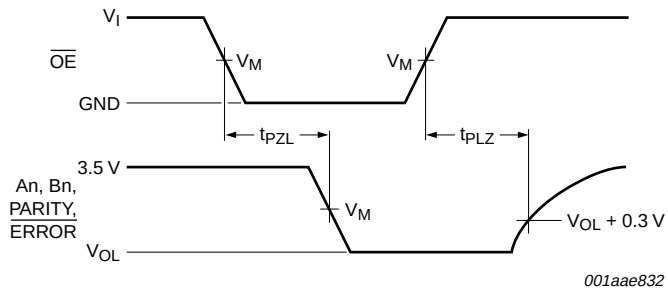


V_M = 1.5 V

Fig 7. 3-state output enable time to HIGH-level and output disable time from HIGH-level

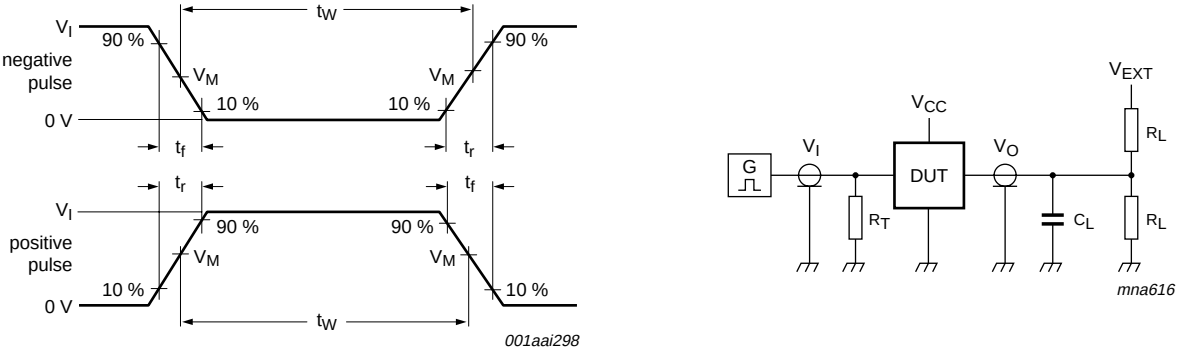
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V_M = 1.5 V

Fig 8. 3-state output enable time to LOW-level and output disable time from LOW-level



a. Input pulse definition

b. Test circuit

Test data and V_{EXT} levels are given in Table 8.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = Test voltage for switching times.

Fig 9. Test circuit for measuring switching times

Table 8. Test data

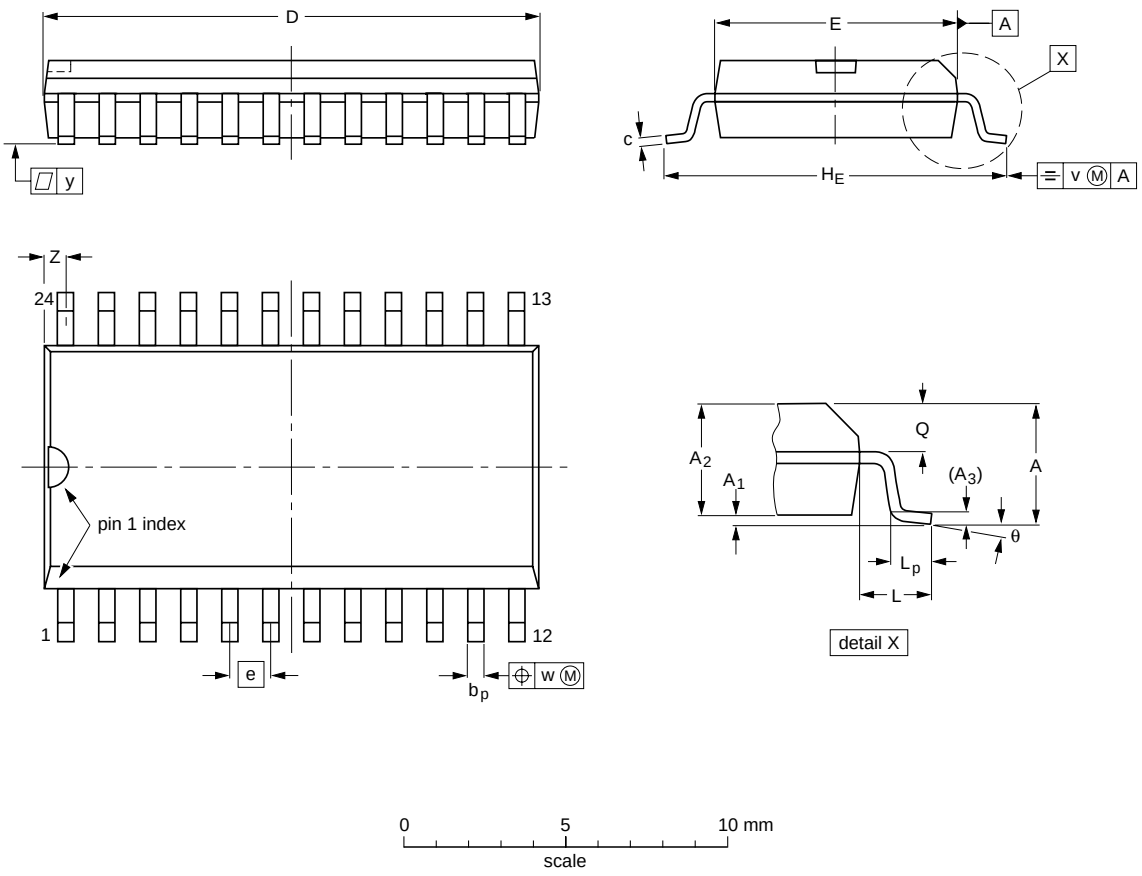
Input				Load		V_{EXT}		
V_I	f_I	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

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12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

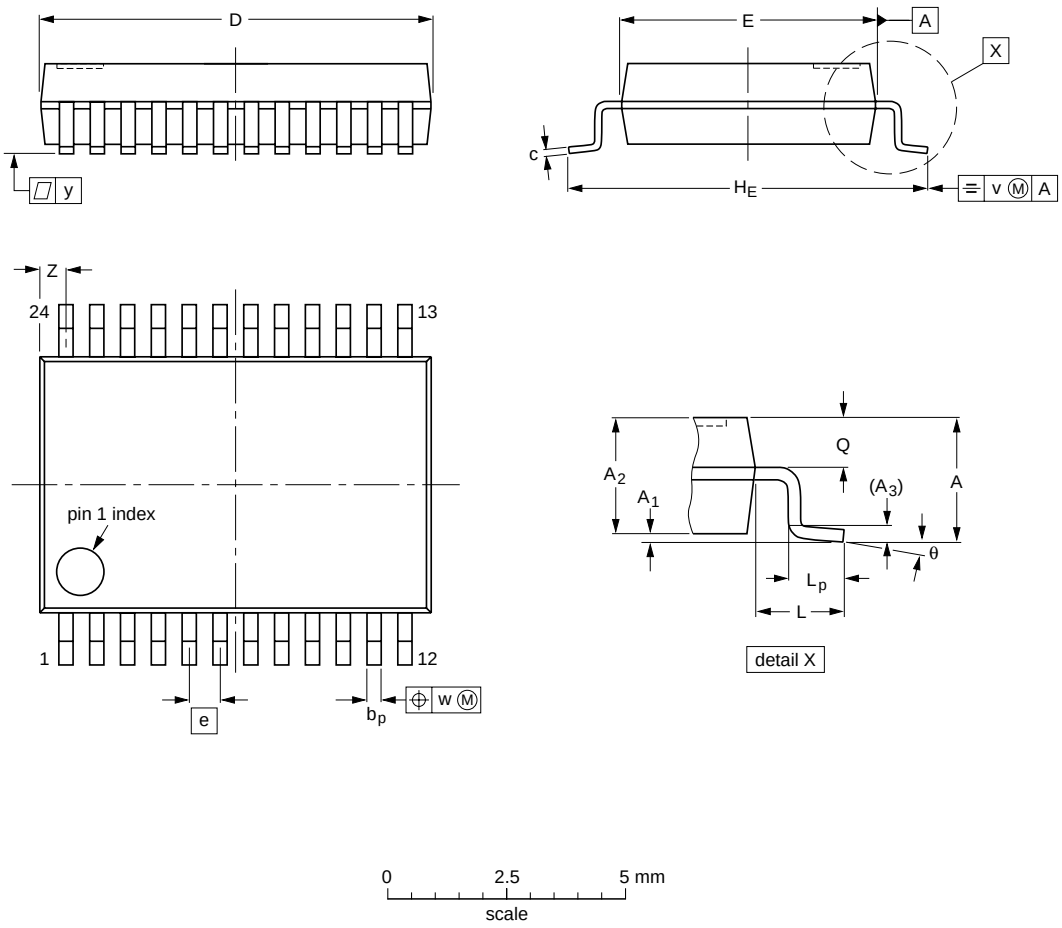
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT137-1 (SO24)

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SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

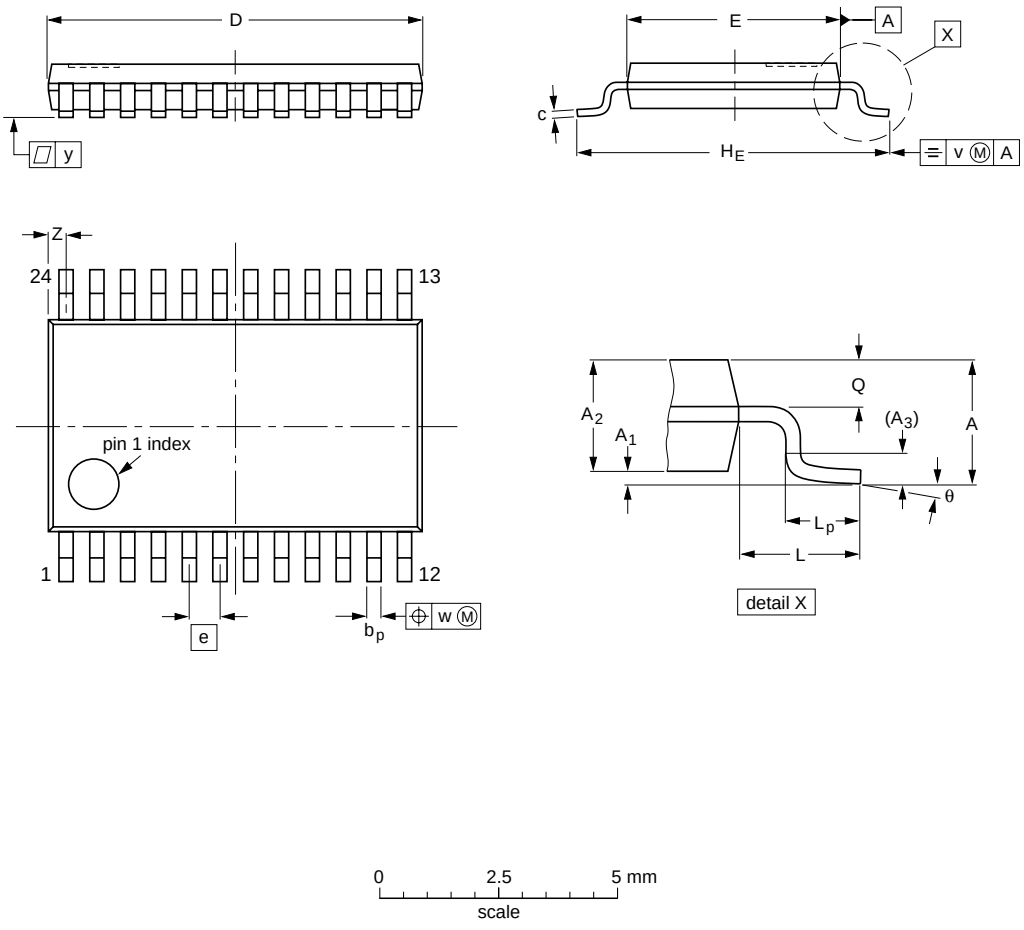
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT340-1		MO-150				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT340-1 (SSOP24)

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TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT355-1 (TSSOP24)

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13. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT657_3	20100315	Product data sheet	-	74ABT657_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • DIP 24 (SOT222-1) package removed from Section 3 “Ordering information” and Section 12 “Package outline”.			
74ABT657_2	20041027	Product specification	-	74ABT657
74ABT657	19951211	Product specification	-	-

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15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

1	**General description**	**1**
2	**Features and benefits**	**1**
3	**Ordering information**	**2**
4	**Functional diagram**	**2**
5	**Pinning information**	**4**
5.1	Pinning	4
5.2	Pin description	4
6	**Functional description**	**5**
6.1	Function selection	5
7	**Limiting values**	**6**
8	**Recommended operating conditions**	**6**
9	**Static characteristics**	**7**
10	**Dynamic characteristics**	**8**
11	**Waveforms**	**9**
12	**Package outline**	**11**
13	**Abbreviations**	**14**
14	**Revision history**	**14**
15	**Legal information**	**15**
15.1	Data sheet status	15
15.2	Definitions	15
15.3	Disclaimers	15
16	**Contact information**	**16**
17	**Contents**	**17**

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