

Description

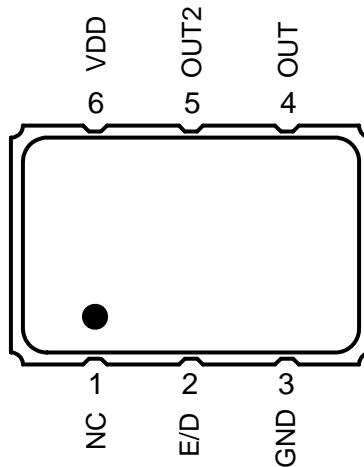
The XUQ is an Ultra Precision LVPECL crystal oscillator with 300fs typical phase jitter over 12kHz to 20MHz bandwidth. Available in a wide frequency range from 16kHz to 670MHz, the IDT XUQ series crystal oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 4th order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XUQ is an excellent choice over the conventional technologies. The XUQ has stabilities as tight as $\pm 20\text{ppm}$ with extremely quick delivery for both standard and custom frequencies.

Features

- Frequency range: 0.016 to 670MHz
- Output type: LVPECL
- Frequency stability: $\pm 20\text{ppm}$, $\pm 25\text{ppm}$, $\pm 50\text{ppm}$, or $\pm 100\text{ppm}$
- Supply voltage: 1.8V, 2.5V, or 3.3V
- Phase jitter (1.875MHz to 20MHz): 100fs typical
- Phase jitter (12kHz to 20MHz): 300fs typical
- Package options: 5.0mm x 3.2mm x 1.2mm (JS6)
7.0mm x 5.0mm x 1.3mm (JU6)
- Operating temperatures: -20°C to $+70^{\circ}\text{C}$ or -40°C to $+85^{\circ}\text{C}$

Pin Assignment



6-pin CLCC

Pin Descriptions

Pin Number	Pin Name	Description
1	NC	No connect
2	E/D	Enable/Disable ¹ (0=Output Disabled)
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary output
6	VDD	Supply Voltage

1. Pulled high internally.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XUQ. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0V
E/D	-0.5V to VDD + 0.5V
OUT	-0.5V to VDD + 0.5V
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

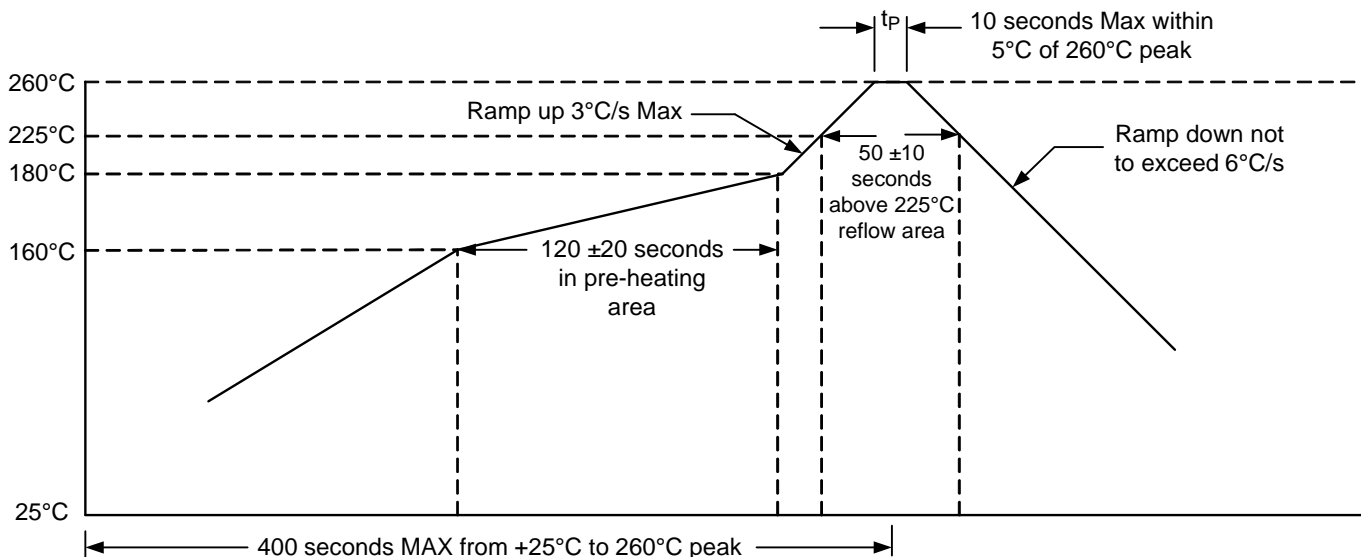
ESD Compliance

Human Body Model (HBM)	1000V
Machine Model (MM)	150V

Mechanical Testing

Parameter	Test Method
Mechanical Shock	Half-Sine wave with 0.3ms 3000G X, Y, Z each direction 1 time
Mechanical Vibration	Frequency: 10 to 55 MHz Amplitude: 1.5mm Frequency: 55~2000Hz Peak value: 20G Duration time: 4H for each X,Y,Z axis Total 12hours
High Temp Operating Life (HTOL)	2000 Hours 125°C (under power)
Hermetic Seal	Gross leak (Air leak test) Fine leak (Helium leak test) He-pressure: 6kgf/cm ² 2 hours

Solder Reflow Profile



DC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	$\leq 212.5MHz$ $> 212.5MHz$			115 128	mA
Output HIGH Voltage	V_{OH}	Std LVPECL load	1.85		2.3	V
Output LOW Voltage	V_{OL}	Std LVPECL load	1.1		1.65	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				$30\%V_{DD}$	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

($V_{DD} = 3.3V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.016		670	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	± 20		± 100	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	± 25		± 100	ppm
Aging (1 st year)		$T_a = 25^\circ C$			3	ppm
Aging (10 years)		$T_a = 25^\circ C$			10	ppm
Output Load		To $V_{DD}-2.0V$		50		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP} , Std frequencies			400	ps
Output Fall Time		80% to 20% V_{PP} , Std frequencies			400	ps
Output Clock Duty Cycle	T_{DTCY}	$50\% V_{PP}$ $\leq 312.5MHz$ $> 312.5MHz$	45 40		55 60	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		1.8	7	ps
Random Jitter	R_J	Frequency = 156.25MHz		0.7	1.8	ps
Deterministic Jitter	D_J	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		8	24	ps
Total Jitter	T_J			18	42	ps
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	Standard frequencies at $25^\circ C$, 3.3V		300	400	fs
Phase Noise Performance Frequency = 156.25MHz	ϕ_{NOISE}	100Hz of Carrier		-95		dBc/Hz
		1kHz of Carrier		-115		dBc/Hz
		10kHz of Carrier		-120		dBc/Hz
		100kHz of Carrier		-129		dBc/Hz
		1MHz of Carrier		-149		dBc/Hz
		10MHz of Carrier		-156		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at $25^\circ C$. We do not recommend hand soldering the devices.

DC Characteristics

($V_{DD} = 2.5V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	$\leq 156.25\text{MHz}$ $> 156.25\text{MHz}$			102 112	mA
Output HIGH Voltage	V_{OH}	Std LVPECL load	1.1		1.45	V
Output LOW Voltage	V_{OL}	Std LVPECL load	0.035		0.085	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				$30\%V_{DD}$	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

($V_{DD} = 2.5V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.750		670	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	± 20		± 100	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	± 25		± 100	ppm
Output Load		To $V_{DD}-2.0V$		50		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP}		250	630	ps
Output Fall Time		80% to 20% V_{PP}		360	630	ps
Output Clock Duty Cycle	T_{DTCY}	50% V_{PP} $\leq 156.25\text{MHz}$ $> 156.25\text{MHz}$	45 40		55 60	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		2	5	ps
Random Jitter	R_J	Frequency = 156.25MHz		0.7	1.6	ps
Deterministic Jitter	D_J	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		8	22	ps
Total Jitter	T_J			18	38	ps
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	Frequency = 156.25MHz at $25^\circ C$, 2.5V		350	500	fs
Phase Noise Performance Frequency = 156.25MHz	ϕ_{NOISE}	100Hz of Carrier		-94		dBc/Hz
		1kHz of Carrier		-113		dBc/Hz
		10kHz of Carrier		-120		dBc/Hz
		100kHz of Carrier		-128		dBc/Hz
		1MHz of Carrier		-147		dBc/Hz
		10MHz of Carrier		-155		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at $25^\circ C$. We do not recommend hand soldering the devices.

DC Characteristics

($V_{DD} = 1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	I_{DD}	$\leq 250MHz$ $> 250MHz$			75 90	mA
Output HIGH Voltage	V_{OH}	Std LVPECL load	0.5		0.8	V
Output LOW Voltage	V_{OL}	Std LVPECL load	0		0.25	V
Enable/Disable Input HIGH Voltage (Output enabled)*	V_{IH}		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	V_{IL}				$30\%V_{DD}$	V

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

AC Characteristics

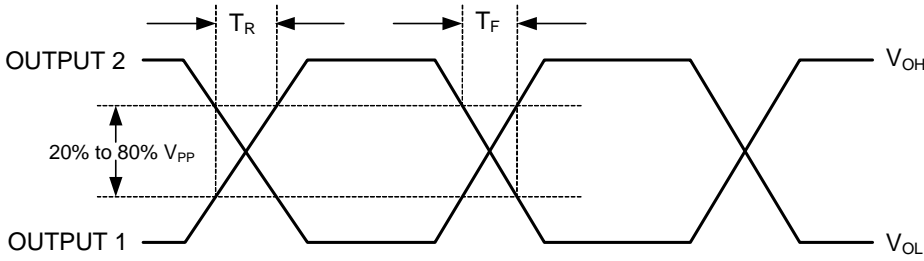
($V_{DD} = 1.8V \pm 5\%$, $T_A = -20^\circ C$ to $+70^\circ C$; -40° to $+85^\circ C$). Below are guaranteed for listed standard frequencies.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	F_{OUTR}		0.016		670	MHz
Frequency Stability STD Frequencies		Temperature = $-20^\circ C$ to $+70^\circ C$	± 20		± 100	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	± 25		± 100	ppm
Output Load		To GND		50		Ohms
Start-up Time	T_{ST}	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% V_{PP}		250	350	ps
Output Fall Time		80% to 20% V_{PP}		250	350	ps
Output Clock Duty Cycle	T_{DTCY}	At 50% V_{PP} $\leq 312.5MHz$ $> 312.5MHz$	45 40		55 60	%
Output Enable/ Disable Time	T_{OE}				100	ns
Period Jitter, RMS	J_{PER}	Frequency = 156.25MHz		1.8	4.2	ps
Random Jitter	R_J	Frequency = 156.25MHz		0.75	1.6	ps
Deterministic Jitter	D_J	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		8	25	ps
Total Jitter	T_J			20	45	ps
Phase Jitter (12kHz – 20MHz)	ϕ_{JITTER}	Frequency = 156.25MHz at $25^\circ C$, 1.8V		750	1200	fs
Phase Noise Performance Frequency = 156.25MHz	ϕ_{NOISE}	100Hz of Carrier		-90		dBc/Hz
		1kHz of Carrier		-101		dBc/Hz
		10kHz of Carrier		-109		dBc/Hz
		100kHz of Carrier		-122		dBc/Hz
		1MHz of Carrier		-144		dBc/Hz
		10MHz of Carrier		-149		dBc/Hz
Output Frequency (Standards)	F_{OUT}	100MHz, 106.25MHz, 125MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

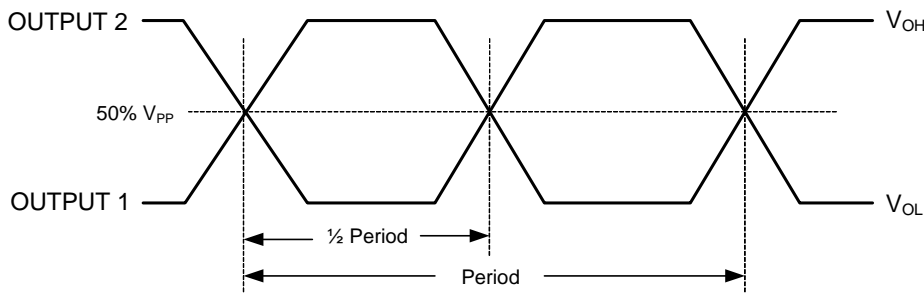
Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at $25^\circ C$. We do not recommend hand soldering the devices.

Output Waveform

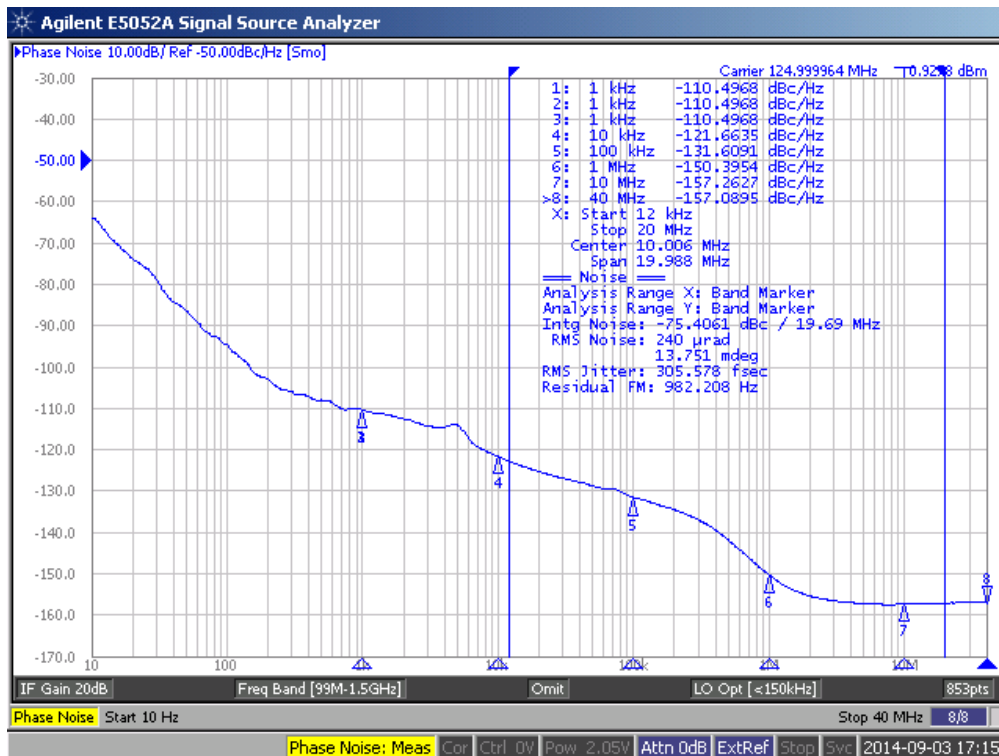
Rise Time/Fall Time Measurements



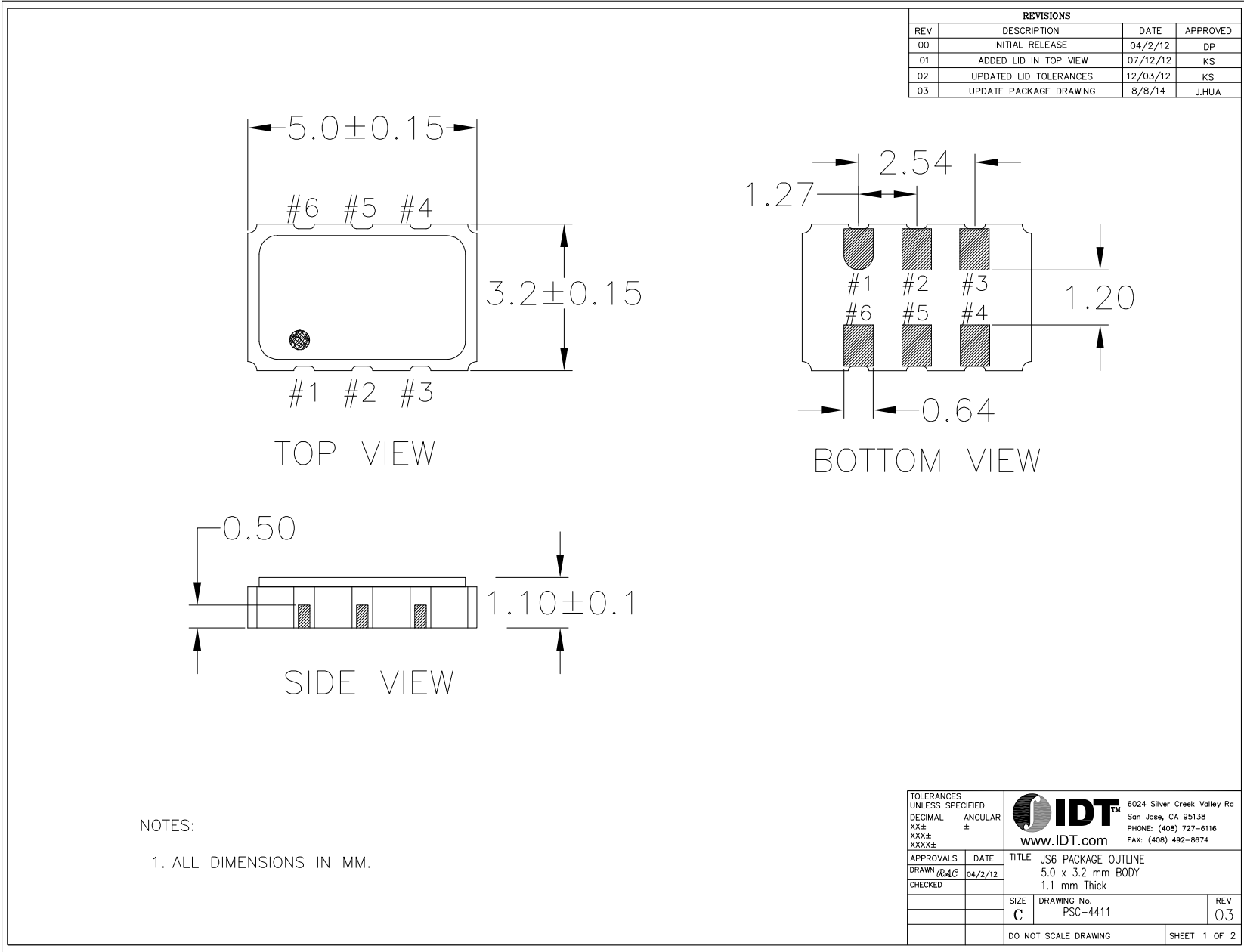
Oscillator Symmetry



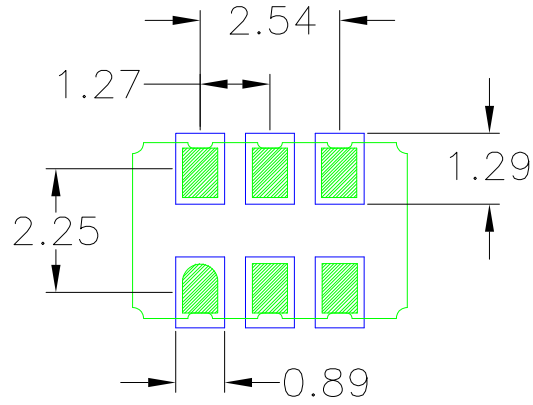
Typical Phase Noise



JS6 Package Outline and Dimensions



JS6 Package Outline and Dimensions (cont.)



RECOMMENDED LAND PATTERN

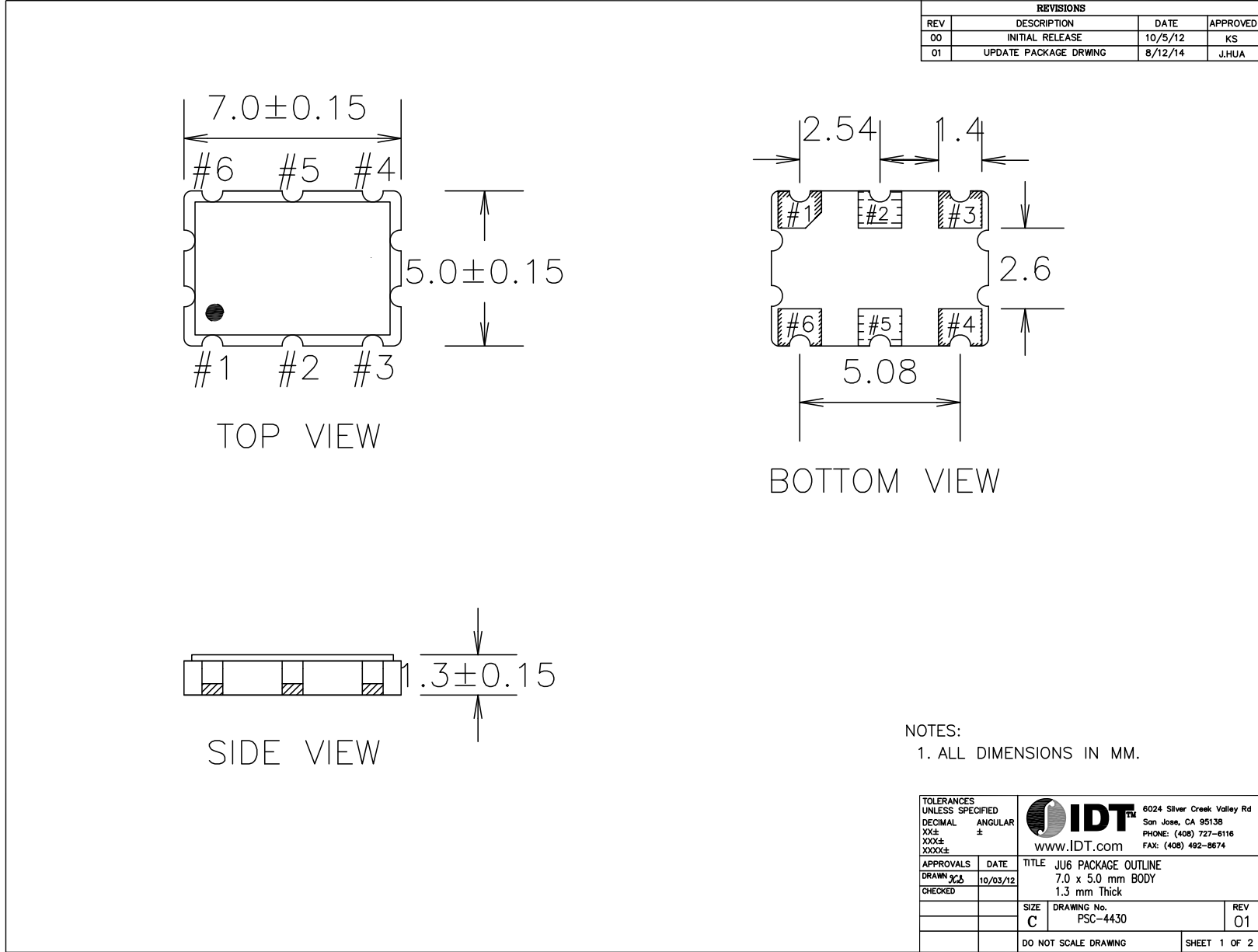
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

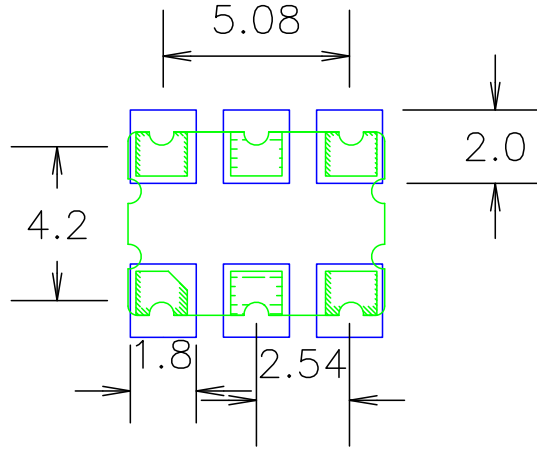
REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	J.HUA

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XXX± ± XXXX± ±		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674 www.IDT.com
APPROVALS	DATE	
DRAWN <i>pac</i>	04/2/12	TITLE JS6 PACKAGE OUTLINE 5.0 x 3.2 mm BODY 1.1 mm Thick
CHECKED		SIZE C DRAWING No. PSC-4411 REV 0.3
DO NOT SCALE DRAWING		SHEET 2 OF 2

JU6 Package Outline and Dimensions



JU6 Package Outline and Dimensions (cont.)



RECOMMENDED LAND PATTERN

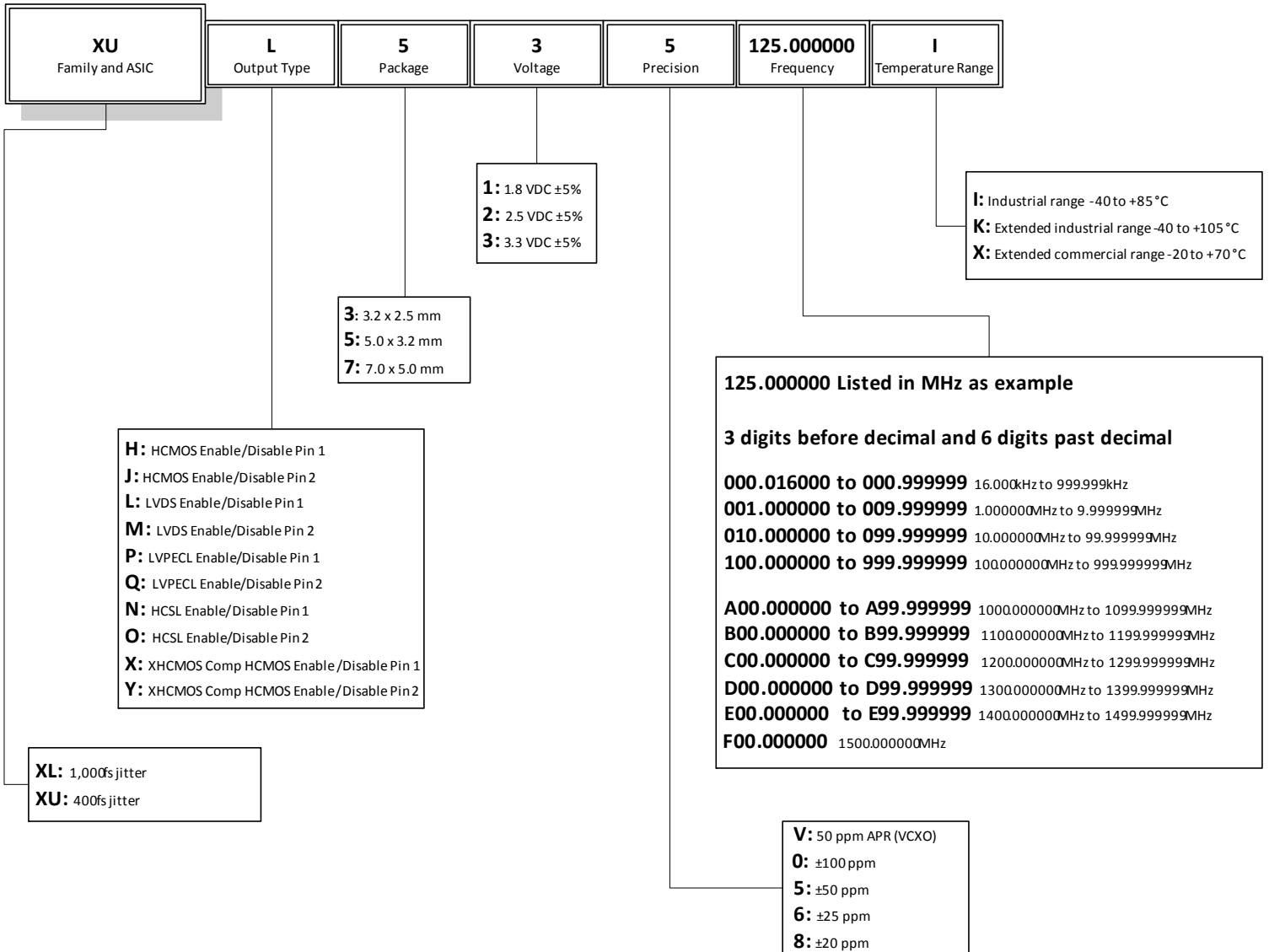
NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW, AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

REVISIONS			
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	J.HUA

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XXX± ± XXXX± XXXXX±		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8674 www.IDT.com
APPROVALS DRAWN: [signature] CHECKED: [signature]	DATE 10/03/12	
TITLE JU6 PACKAGE OUTLINE 7.0 x 5.0 mm BODY 1.3 mm Thick		SIZE C
DRAWING No. PSC-4430		REV 01
DO NOT SCALE DRAWING		SHEET 2 OF 2

IDT Ordering Information



Revision History

Date	Originator	Description of Change
01/09/15	B. Chandhoke	Initial release.
10/28/16	P. Jenkins	Update ordering information decoder tables by separating them into Scheme 1 and Scheme 2; add note to distinguish the two tables.
06/13/17	L.S.	Removed "Ordering Information Scheme #1 (for reference only)". Replaced with a single ordering information table.
06/20/17	L.S.	Corrected frequency errors in Ordering Information table.



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