19-2536; Rev 0; 7/02

MAXIM

±15kV ESD-Protected, Fail-Safe, 20Mbps, Slew-Rate-Limited RS-485/RS-422 Transceivers in a SOT

General Description

The MAX3060E/MAX3061E/MAX3062E high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted. This means that the receiver output is a logic high if all transmitters on a terminated bus are disabled (high impedance). These devices also feature hot-swap circuitry that eliminates data glitches during hot insertion.

The MAX3060E features slew-rate-limited drivers that minimize EMI and reduce reflections caused by improperly terminated cables, allowing error-free data transmission up to 115kbps. The MAX3061E, also slew-rate limited, transmits up to 500kbps. The MAX3062E driver is not slew-rate limited, allowing transmit speeds up to 20Mbps. All transmitter outputs are protected to ±15kV using the Human Body Model.

These transceivers typically draw 910µA of supply current when unloaded, or 790µA when fully loaded with the drivers disabled.

All devices have a 1/8-unit-load receiver input impedance that allows up to 256 transceivers on the bus. These devices are intended for half-duplex communication.

Applications

RS-422/RS-485 Communications

Level Translators

Transceivers for EMI-Sensitive Applications

Industrial-Control Local-Area Networks

Features

- ♦ **True Fail-Safe Receiver While Maintaining EIA/TIA-485 Compatibility**
- ♦ **Enhanced Slew-Rate Limiting Facilitates Error-Free Data Transmission (MAX3060E and MAX3061E)**
- ♦ **1nA Low-Current Shutdown Mode**
- ♦ **Hot-Swappable for Telecom Applications**
- ♦ **ESD Protection: ±15kV Human Body Model**
- ♦ **Allow Up to 256 Transceivers on the Bus**
- ♦ **Space-Saving 8-Pin SOT23 Package**

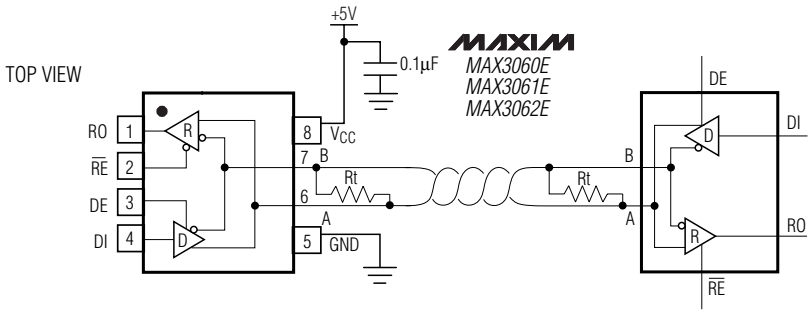
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX3060EEKA-T	-40°C to +85°C	8 SOT23-8	AAKI
MAX3061EEKA-T	-40°C to +85°C	8 SOT23-8	AAKJ
MAX3062EEKA-T	-40°C to +85°C	8 SOT23-8	AAKK

Selector Guide

PART	DATA RATE (Mbps)	SLEW-RATE LIMITED	TRANSCEIVERS ON BUS
MAX3060E	0.115	Yes	256
MAX3061E	0.5	Yes	256
MAX3062E	20	No	256

Typical Operating Circuit/Pin Configuration



For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to GND
Supply Voltage (V_{CC}) .....+7V
Input Voltage ($\overline{RE}$, DE, DI).....-0.3V to (V_{CC} + 0.3V)
Driver Output/Receiver Input Voltage (A, B) .....-7.5V to +12.5V
Receiver Output Voltage (RO).....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
8-Pin SOT23 (derate 8.9mW/°C above +70°C).....714mW

Operating Temperature Range
MAX306_EE_ _ .....-40°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Junction Temperature .....+150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DRIVER							
Differential Driver Output (No Load)	V_{OD1}	V_{CC} = 5V				5	V
Differential Driver Output	V_{OD2}	Figure 1, R = 50Ω (RS-422)		2.0			V
		Figure 1, R = 27Ω (RS-485)		1.5			
Change in Magnitude of Differential Output Voltage	ΔV_{OD}	Figure 1, R = 50Ω or R = 27Ω (Note 3)				0.2	V
Driver Common-Mode Output Voltage	V_{OC}	Figure 1, R = 50Ω or R = 27Ω				3	V
Change in Magnitude of Common-Mode Voltage	ΔV_{OC}	Figure 1, R = 50Ω or R = 27Ω (Note 3)				0.2	V
Input High Voltage	V_{IH}	DE, DI, $\overline{RE}$		2.0			V
Input Low Voltage	V_{IL}	DE, DI, $\overline{RE}$				0.8	V
DI Input Hysteresis	V_{HYS}				100		mV
Input Current	I_{IN1}	DE, DI, $\overline{RE}$				±1	µA
Hot-Swap Driver Input Current	$I_{HOTSWAP}$	DE, $\overline{RE}$ (Note 4)				±200	µA
Input Current (A and B)	I_{IN2}	DE = GND, V_{CC} = GND or 5.25V	V_{IN} = +12V			125	µA
			V_{IN} = -7V	-100			
Driver Short-Circuit Output Current	V_{OD1}	-7V ≤ V_{OUT} ≤ +12V, T_A = +25°C (Note 5)		±15		±250	mA
ESD Protection for A, B		IEC 1000-4-2 Air-Gap Discharge			±7		kV
		IEC 1000-4-2 Contact Discharge			±7		
		Human Body Model			±15		

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
RECEIVER							
Receiver Differential Threshold Voltage	V_{TH}	-7V ≤ VCM ≤ +12V		-200	-125	-50	mV
Receiver Input Hysteresis	ΔV_{TH}				25		mV
Receiver Output High Voltage	V_{OH}	I_O = -4mA, V_{ID} = -50mV		V_{CC} - 1.5			V
Receiver Output Low Voltage	V_{OL}	I_O = 4mA, V_{ID} = -200mV				0.4	V
Three-State Output Current at Receiver	I_{OZR}	0V ≤ V_O ≤ V_{CC}			0.01	±1	µA
Receiver Input Resistance	R_{IN}	-7V ≤ V_{CM} ≤ +12V		96			kΩ
Receiver Output Short-Circuit Current	I_{OSR}	0V ≤ V_{RO} ≤ V_{CC}		±8		±80	mA
SUPPLY CURRENT							
Supply Current	I_{CC}	No load, DI = GND or V_{CC}	DE = $\overline{RE}$ = GND		790	1400	µA
			DE = $\overline{RE}$ = V_{CC}		910	1500	
Supply Current in Shutdown Mode	I_{SHDN}	DE = GND, $\overline{RE}$ = V_{CC}			0.001	1	µA

SWITCHING CHARACTERISTICS—MAX3060E

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}, t_{DPHL}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF	1.0	1.7	2.4	µs
Driver Output Skew (t_{DPLH} - t_{DPHL})	t_{DSKEW}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF	-200	-7	+200	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF	1.3	1.85	2.5	µs
Maximum Data Rate	f_{MAX}		115			kbps
Driver Enable to Output High	t_{DZH}	Figures 4 and 6, C_L = 100pF, S2 closed		0.6	1.5	µs
Driver Enable to Output Low	t_{DZL}	Figures 4 and 6, C_L = 100pF, S1 closed		0.5	1.5	µs
Driver Disable Time from Low	t_{DLZ}	Figures 4 and 6, C_L = 15pF, S1 closed		60	200	ns
Driver Disable Time from High	t_{DHZ}	Figures 4 and 6, C_L = 15pF, S2 closed		85	200	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 7 and 9; $\lvert V_{ID} \rvert \geq 2.0V$; rise and fall time of $V_{ID} \leq 4ns$, C_L = 15pF		47	80	ns
Differential Receiver Skew (t_{RPLH} - t_{RPHL})	t_{RSKD}	Figures 7 and 9; $\lvert V_{ID} \rvert \geq 2.0V$; rise and fall time of $V_{ID} \leq 4ns$, C_L = 15pF	-10	-3	+10	ns
Receiver Enable to Output Low	t_{RZL}	Figures 2 and 8, C_L = 15pF, S1 closed			50	ns
Receiver Enable to Output High	t_{RZH}	Figures 2 and 8, C_L = 15pF, S2 closed			50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 2 and 8, C_L = 15pF, S1 closed			50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 2 and 8, C_L = 15pF, S2 closed			50	ns
Time to Shutdown	t_{SHDN}	(Note 6)	50	180	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 4 and 6, C_L = 100pF, S2 closed			2	µs
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 4 and 6, C_L = 100pF, S1 closed			2	µs
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 2 and 8, C_L = 15pF, S2 closed			1.5	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 2 and 8, C_L = 15pF, S1 closed			1.5	µs

SWITCHING CHARACTERISTICS—MAX3061E

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}, t_{DPHL}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF	250	470	800	ns
Driver Output Skew (t_{DPLH} - t_{DPHL})	t_{DSKEW}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF	-100	-4	+100	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF	200	530	750	ns
Maximum Data Rate	f_{MAX}		500			kbps
Driver Enable to Output High	t_{DZH}	Figures 4 and 6, C_L = 100pF, S2 closed		330	1000	ns
Driver Enable to Output Low	t_{DZL}	Figures 4 and 6, C_L = 100pF, S1 closed		200	1000	ns
Driver Disable Time from Low	t_{DLZ}	Figures 4 and 6, C_L = 15pF, S1 closed		60	200	ns
Driver Disable Time from High	t_{DHZ}	Figures 4 and 6, C_L = 15pF, S2 closed		80	200	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 7 and 9; $\lvert V_{ID} \rvert \geq 2.0V$; rise and fall time of $V_{ID} \leq 4ns$, C_L = 15pF		47	80	ns
Differential Receiver Skew (t_{RPLH} - t_{RPHL})	t_{RSKD}	Figures 7 and 9; $\lvert V_{ID} \rvert \geq 2.0V$; rise and fall time of $V_{ID} \leq 4ns$, C_L = 15pF	-10	-3	+10	ns
Receiver Enable to Output Low	t_{RZL}	Figures 2 and 8, C_L = 15pF, S1 closed			50	ns
Receiver Enable to Output High	t_{RZH}	Figures 2 and 8, C_L = 15pF, S2 closed			50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 2 and 8, C_L = 15pF, S1 closed			50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 2 and 8, C_L = 15pF, S2 closed			50	ns
Time to Shutdown	t_{SHDN}	(Note 6)	50	180	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN}$	Figures 4 and 6, C_L = 100pF, S2 closed			1.5	µs
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 4 and 6, C_L = 100pF, S1 closed			1.5	µs
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 2 and 8, C_L = 15pF, S2 closed			1.5	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 2 and 8, C_L = 15pF, S1 closed			1.5	µs

SWITCHING CHARACTERISTICS—MAX3062E

(V_{CC} = +5V ±5%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Input to Output	t_{DPLH}, t_{DPHL}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF		20	30	ns
Driver Output Skew (t_{DPLH} - t_{DPHL})	t_{DSKEW}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF	-10	+1	+10	ns
Driver Rise or Fall Time	t_{DR}, t_{DF}	Figures 3 and 5, R_{DIFF} = 54Ω, C_{DIFF} = 50pF		8	15	ns
Maximum Data Rate	f_{MAX}		20			Mbps
Driver Enable to Output High	t_{DZH}	Figures 4 and 6, C_L = 100pF, S2 closed		250	500	ns
Driver Enable to Output Low	t_{DZL}	Figures 4 and 6, C_L = 100pF, S1 closed		250	500	ns
Driver Disable Time from Low	t_{DLZ}	Figures 4 and 6, C_L = 15pF, S1 closed		100	200	ns
Driver Disable Time from High	t_{DHZ}	Figures 4 and 6, C_L = 15pF, S2 closed		100	200	ns
Receiver Input to Output	t_{RPLH}, t_{RPHL}	Figures 7 and 9; $\lvert V_{ID} \rvert \geq 2.0V$; rise and fall time of $V_{ID} \leq 4ns$, C_L = 15pF		45	80	ns
Differential Receiver Skew (t_{RPLH} - t_{RPHL})	t_{RSKD}	Figures 7 and 9; $\lvert V_{ID} \rvert \geq 2.0V$; rise and fall time of $V_{ID} \leq 4ns$, C_L = 15pF	-10	-4	+10	ns
Receiver Enable to Output Low	t_{RZL}	Figures 2 and 8, C_L = 15pF, S1 closed			50	ns
Receiver Enable to Output High	t_{RZH}	Figures 2 and 8, C_L = 15pF, S2 closed			50	ns
Receiver Disable Time from Low	t_{RLZ}	Figures 2 and 8, C_L = 15pF, S1 closed			50	ns
Receiver Disable Time from High	t_{RHZ}	Figures 2 and 8, C_L = 15pF, S2 closed			50	ns
Time to Shutdown	t_{SHDN}	(Note 6)	50	180	600	ns
Driver Enable from Shutdown to Output High	$t_{DZH(SHDN)}$	Figures 4 and 6, C_L = 100pF, S2 closed			100	ns
Driver Enable from Shutdown to Output Low	$t_{DZL(SHDN)}$	Figures 4 and 6, C_L = 100pF, S1 closed			100	ns
Receiver Enable from Shutdown to Output High	$t_{RZH(SHDN)}$	Figures 2 and 8, C_L = 15pF, S2 closed			1.5	µs
Receiver Enable from Shutdown to Output Low	$t_{RZL(SHDN)}$	Figures 2 and 8, C_L = 15pF, S1 closed			1.5	µs

Note 1: Overtemperature limits are guaranteed by design and are not production tested. Devices are tested at T_A = +25°C.

Note 2: All currents into the device are positive; all currents out of the device are negative. All voltages are referred to device ground, unless otherwise noted.

Note 3: ΔV_{OD} and ΔV_{OC} are the changes in V_{OD} and V_{OC}, respectively, when the DI input changes state.

Note 4: This input current level is for the hot-swap enable (DE, $\overline{RE}$) inputs and is present until the first transition only. After the first transition, the input reverts to a standard high-impedance CMOS input with input current I_{IN1}. For the first 10µs, the input current can be as high as 1mA. During this period the input is disabled.

Note 5: Maximum current level applies to peak current just prior to foldback-current limiting; minimum current level applies during current limiting.

Note 6: The device is put into shutdown by bringing $\overline{RE}$ high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 600ns, the device is guaranteed to have entered shutdown.

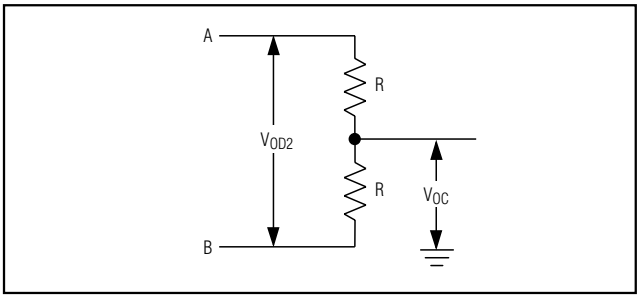


Figure 1. Driver DC Test Load

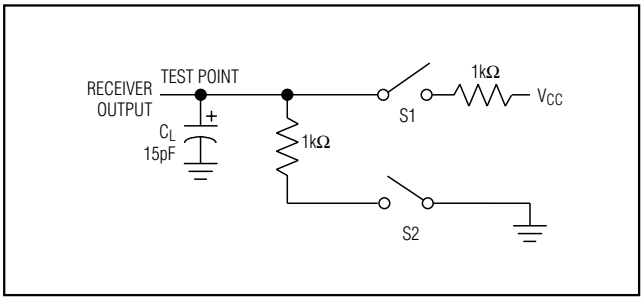


Figure 2. Receiver Enable/Disable Timing Test Load

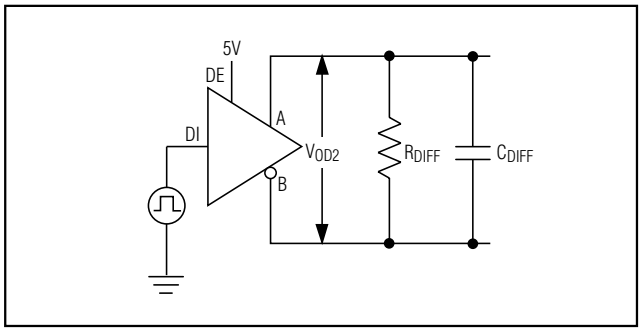


Figure 3. Driver Timing Test Circuit

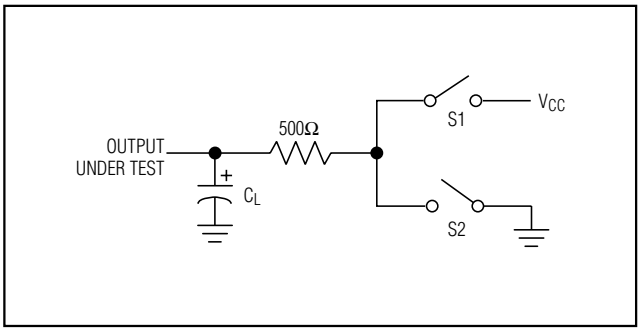


Figure 4. Driver Enable/Disable Timing Test Load

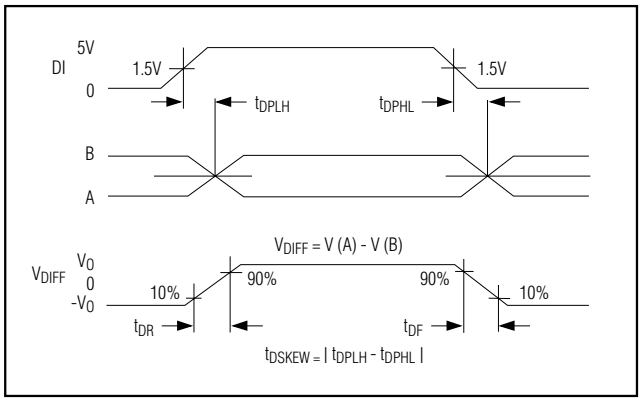


Figure 5. Driver Propagation Delays

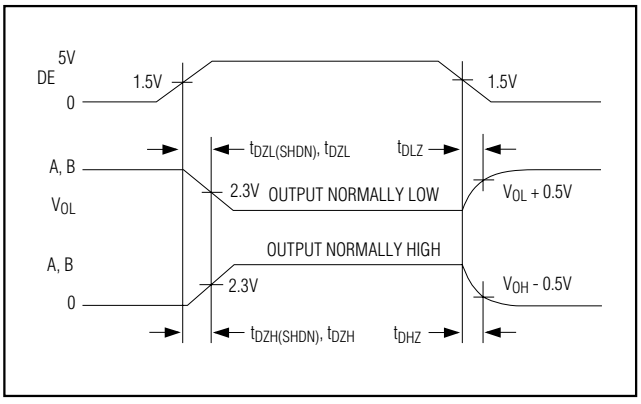


Figure 6. Driver Enable and Disable Times

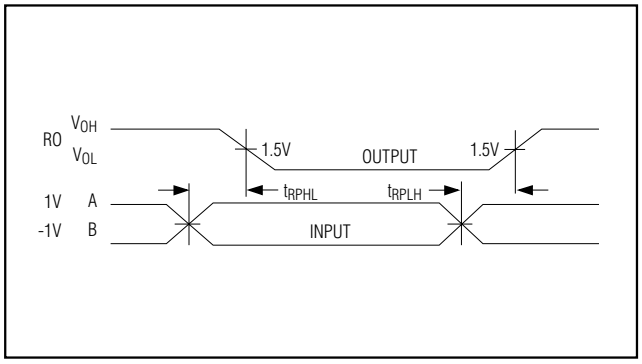


Figure 7. Receiver Propagation Delays

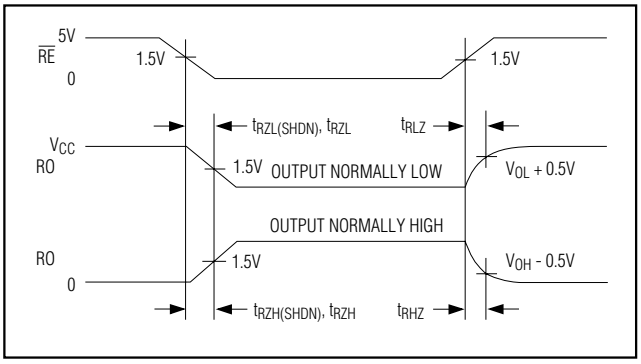


Figure 8. Receiver Enable and Disable Times

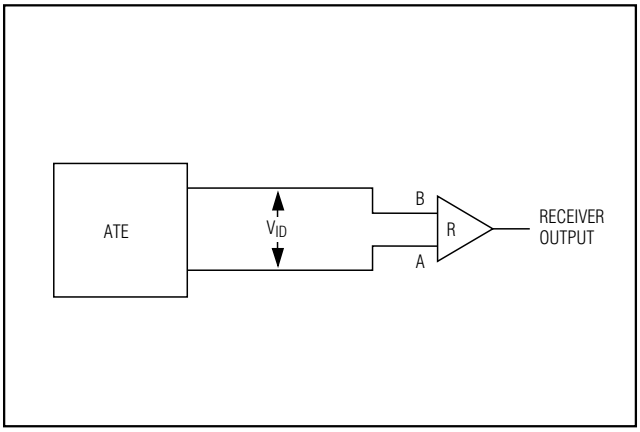
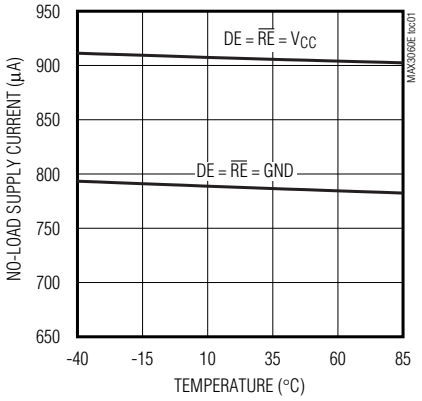


Figure 9. Receiver Propagation Delay Test Circuit

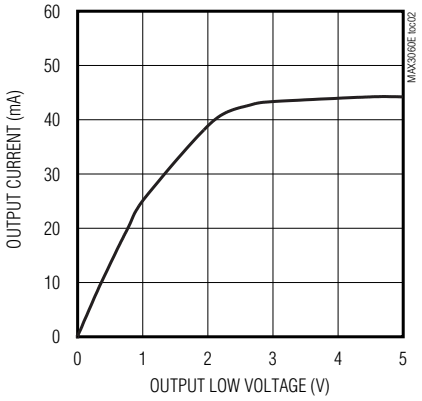
Typical Operating Characteristics

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

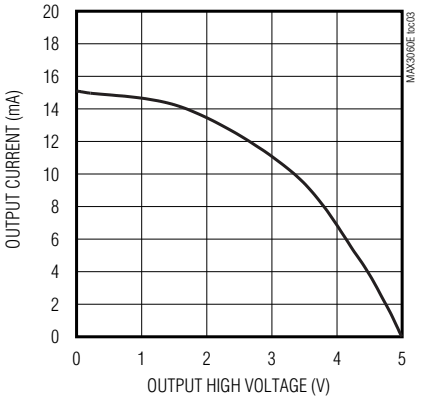
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



RECEIVER OUTPUT CURRENT vs. RECEIVER OUTPUT LOW VOLTAGE



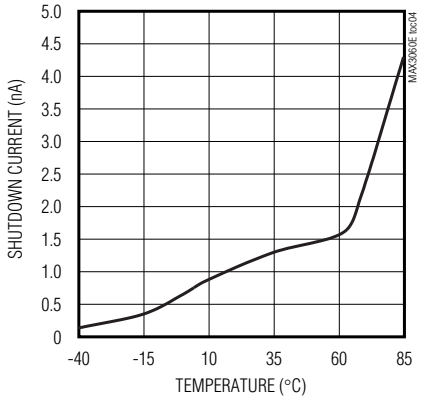
RECEIVER OUTPUT CURRENT vs. RECEIVER OUTPUT HIGH VOLTAGE



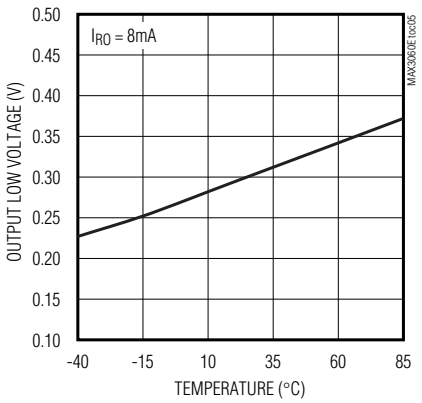
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

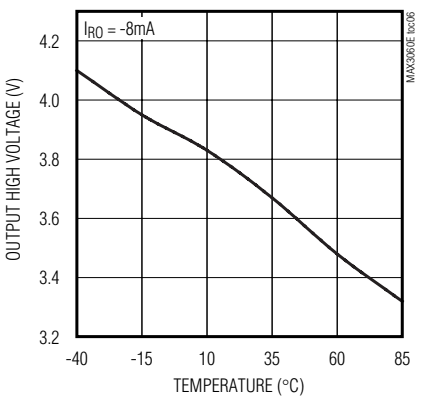
SHUTDOWN CURRENT vs. TEMPERATURE



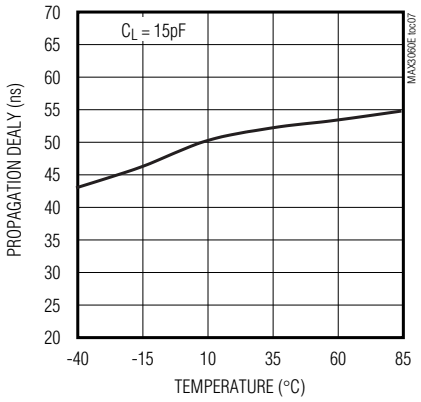
RECEIVER OUTPUT LOW VOLTAGE vs. TEMPERATURE



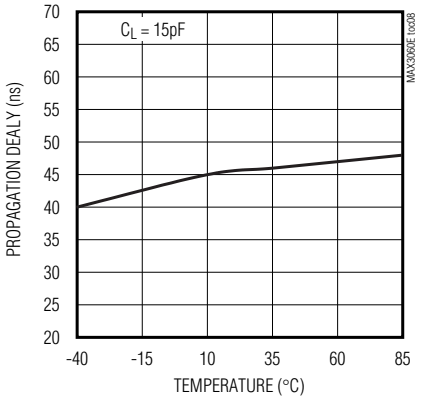
RECEIVER OUTPUT HIGH VOLTAGE vs. TEMPERATURE



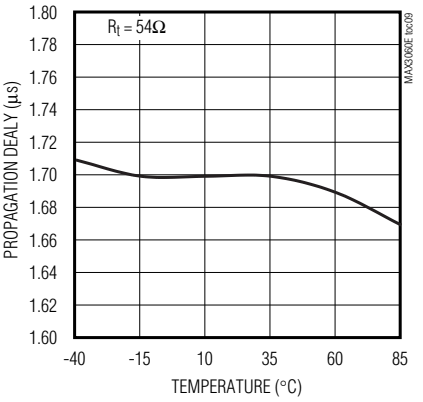
RECEIVER PROPAGATION DELAY (MAX3060E/MAX3061E) vs. TEMPERATURE



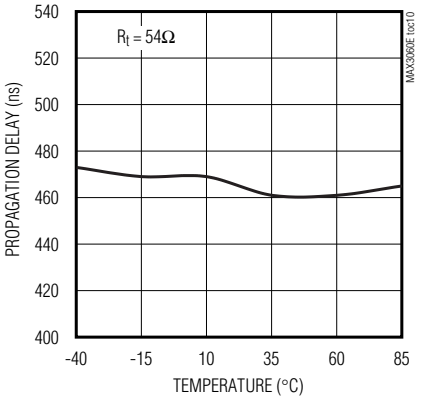
RECEIVER PROPAGATION DELAY (MAX3062E) vs. TEMPERATURE



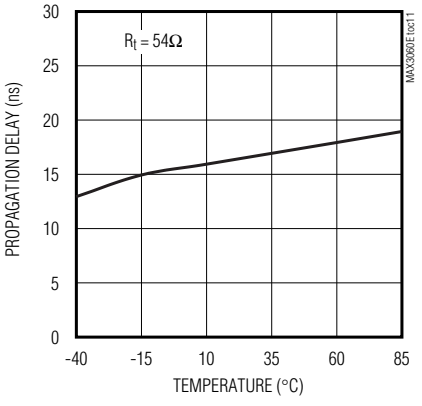
DRIVER PROPAGATION DELAY (MAX3060E) vs. TEMPERATURE



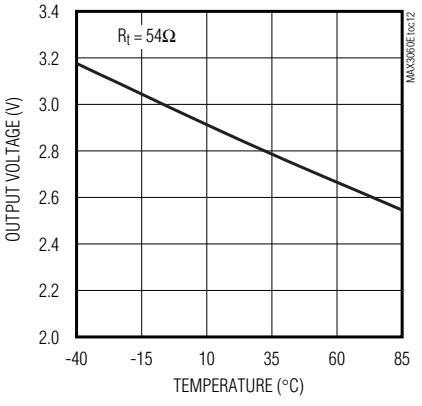
DRIVER PROPAGATION DELAY (MAX3061E) vs. TEMPERATURE



DRIVER PROPAGATION DELAY (MAX3062E) vs. TEMPERATURE



DRIVER DIFFERENTIAL OUTPUT VOLTAGE vs. TEMPERATURE

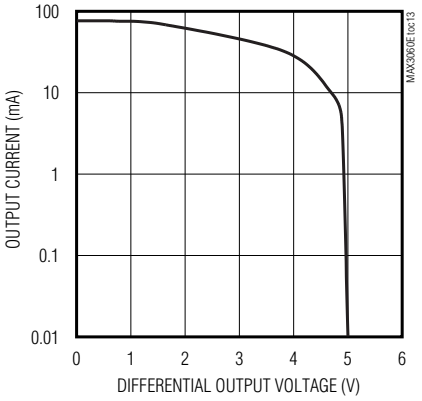


±15kV ESD-Protected, Fail-Safe, 20Mbps, Slew-Rate-Limited RS-485/RS-422 Transceivers in a SOT

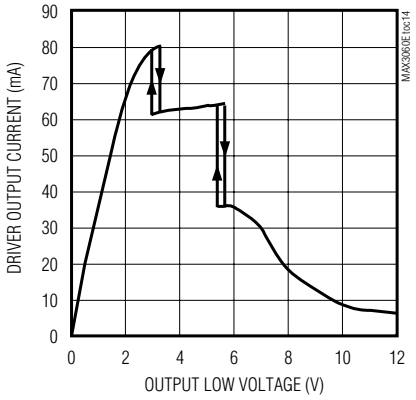
Typical Operating Characteristics (continued)

(V_{CC} = +5V, T_A = +25°C, unless otherwise noted.)

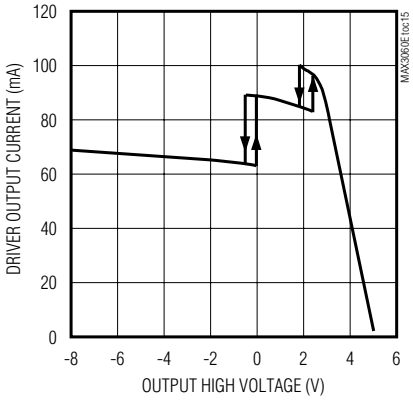
DRIVER OUTPUT CURRENT vs. DIFFERENTIAL OUTPUT VOLTAGE



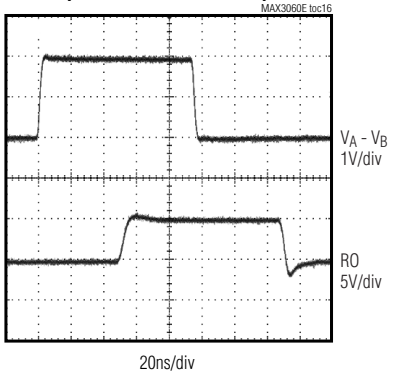
DRIVER OUTPUT CURRENT vs. OUTPUT LOW VOLTAGE



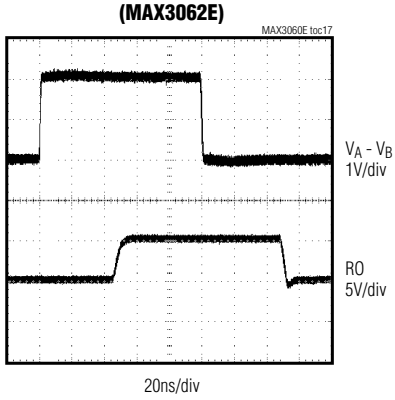
DRIVER OUTPUT CURRENT vs. OUTPUT HIGH VOLTAGE



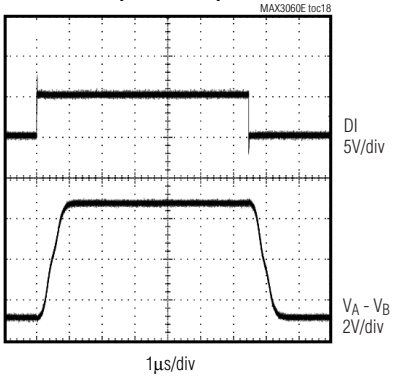
RECEIVER PROPAGATION DELAY (MAX3060E/MAX3061E)



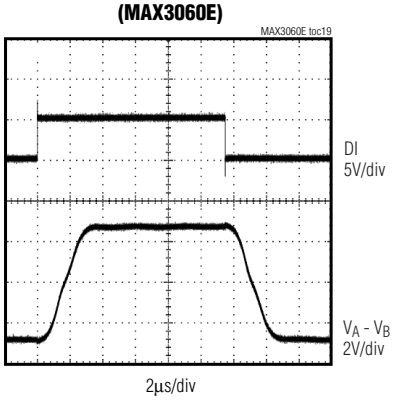
RECEIVER PROPAGATION DELAY (MAX3062E)



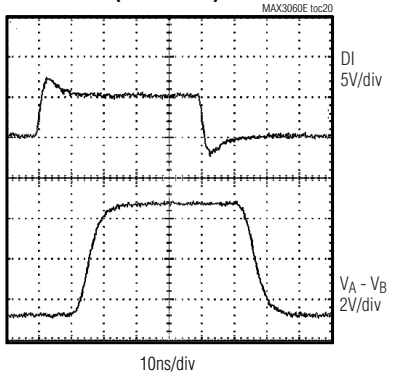
DRIVER PROPAGATION DELAY (MAX3061E)



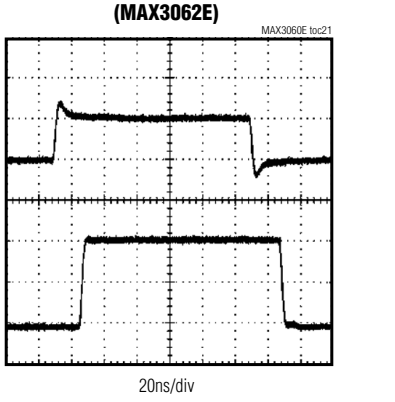
DRIVER PROPAGATION DELAY (MAX3060E)



DRIVER PROPAGATION DELAY (MAX3061E)



DRIVER PROPAGATION DELAY (MAX3062E)



Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. When $\overline{RE}$ is low and when A - B ≥ -50mV, RO is high; if A - B ≤ -200mV, RO is low. RO is high impedance when $\overline{RE}$ is high.
2	$\overline{RE}$	Receiver Output Enable. Drive $\overline{RE}$ low to enable RO; RO is high impedance when $\overline{RE}$ is high. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. $\overline{RE}$ is a hot-swap input and reverts to a standard CMOS input after the first low transition.
3	DE	Driver Output Enable. Drive DE high to enable driver outputs. Driver outputs are high impedance when DE is low. Drive $\overline{RE}$ high and DE low to enter low-power shutdown mode. DE is a hot-swap input and reverts to a standard CMOS input after the first high transition.
4	DI	Driver Input. With DE high, a low on DI forces the noninverting output low and the inverting output high. Similarly, a high on DI forces the noninverting output high and the inverting output low.
5	GND	Ground
6	A	Noninverting Receiver Input and Noninverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	V_{CC}	Positive Supply. Bypass with a 0.1µF capacitor to GND.

Detailed Description

The MAX3060E/MAX3061E/MAX3062E high-speed transceivers for RS-485/RS-422 communication contain one driver and one receiver. These devices feature fail-safe circuitry, which guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the *Fail Safe* section). All devices have a hot-swap input structure that prevents disturbances on the differential signal lines when a circuit board is plugged into a hot backplane (see the *Hot-Swap Capability* section). The MAX3060E features a reduced slew-rate driver that minimizes EMI and reduces reflections caused by improperly terminated cables, allowing error-free data transmission up to 115kbps (see the *Reduced EMI and Reflections* section). The MAX3061E is also slew-rate limited, transmitting up to 500kbps. The MAX3062E driver is not slew-rate limited, allowing transmit speeds up to 20Mbps. The MAX3060E/MAX3061E/MAX3062E are half-duplex transceivers.

All of these parts operate from a single +5V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state.

Receiver Input Filtering

The receivers of the MAX3060E and MAX3061E incorporate input filtering in addition to input hysteresis. This filtering enhances noise immunity with differential signals that have very slow rise and fall times. Receiver propagation delay increases by 2ns due to this filtering.

Fail-Safe

The MAX3060E family of devices guarantee a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by setting the receiver threshold between -50mV and -200mV. If the differential receiver input voltage (A - B) is greater than or equal to -50mV, RO is logic high. If A - B is less than or equal to -200mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. In the case of an unterminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the receiver's input resistors. With the receiver thresholds of the MAX3060E family, this results in a logic high output with a 50mV minimum input noise margin. Unlike previous fail-safe devices, the -50mV to -200mV threshold complies with the ±200mV EIA/TIA-485 standard.

Functional Tables

Table 1. Transmitter Functional Table

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{RE}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	Shutdown*	

X = Don't care.

**Shutdown mode, driver and receiver outputs are high impedance.*

Table 2. Receiver Functional Table

RECEIVING			
INPUTS			OUTPUT
$\overline{RE}$	DE	A-B	RO
0	X	≥ -0.05V	1
0	X	≤ -0.2V	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	Shutdown

Hot-Swap Capability

Hot-Swap Input

When circuit boards are inserted into a hot or powered backplane, differential disturbances to the data bus can lead to data errors. Upon initial circuit board insertion, the data communication processor undergoes its own power-up sequence. During this period, the processor's logic-output drivers are high impedance and are unable to drive the DE and $\overline{RE}$ inputs of the MAX306_E to a defined logic level. Leakage currents up to ±10µA from the high-impedance state of the processor's logic drivers could cause standard CMOS enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to the enable inputs. Without the hot-swap capability, these factors could improperly enable the transceiver's driver or receiver.

When V_{CC} rises, an internal pulldown circuit holds DE low for at least 10µs and until the current into DE exceeds 200µA. After the initial positive transition, the pulldown circuit becomes transparent, resetting the hot-swap tolerable input.

Hot-Swap Input Circuitry

These devices' enable inputs feature hot-swap capability. At the input there are two NMOS devices, M1 and M2 (Figure 10). When V_{CC} ramps from zero, an internal 10µs timer turns on M2 and sets the SR latch, which also turns on M1. Transistors M2, a 300µA current sink, and M1, a 30µA current sink, pull DE to GND through an 8kΩ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After 10µs, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{RE}$, there is a complementary circuit employing two PMOS devices pulling $\overline{RE}$ to V_{CC}.

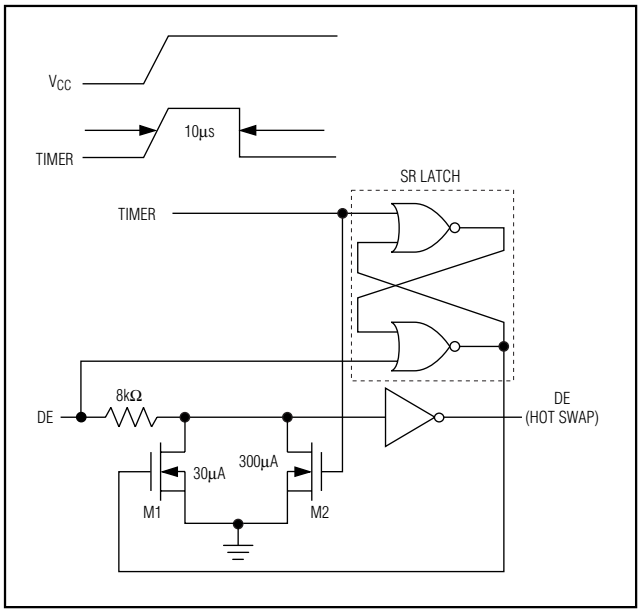


Figure 10. Simplified Structure of the Driver Enable Input (DE)

Hot-Swap Line Transient

The circuit of Figure 11 shows a typical offset termination used to guarantee a greater than 200mV offset when a line is not driven (the 50pF represents the minimum parasitic capacitance that would exist in a typical application). During a hot-swap event when the driver is connected to the line and is powered up, the driver must not cause the differential signal to drop below 200mV. Figures 12, 13, and 14 show the results of the MAX3060E during power-up for three different V_{CC} ramp rates (0.1V/µs, 1V/µs, and 10V/µs). The photos show the V_{CC} ramp, the single-ended signal on each side of the 100Ω termination, as well as the differential signal across the termination.

±15kV ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against ESD encountered during handling and assembly. The MAX3060E family's receiver inputs/driver outputs (A, B) have extra protection against static electricity found in normal operation. Maxim's engineers developed state-of-the-art structures to protect these pins against ±15kV ESD without damage. After an ESD event, the devices continue working without latchup.

ESD protection can be tested in several ways. The receiver inputs are characterized for protection to the following:

- ±15kV using the Human Body Model
- ±7kV using the Contact Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)
- ±7kV using the Air-Gap Discharge method specified in IEC 1000-4-2 (formerly IEC 801-2)

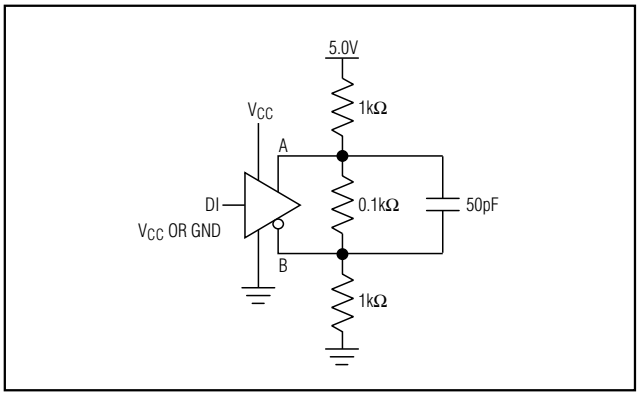


Figure 11. Typical Offset Termination

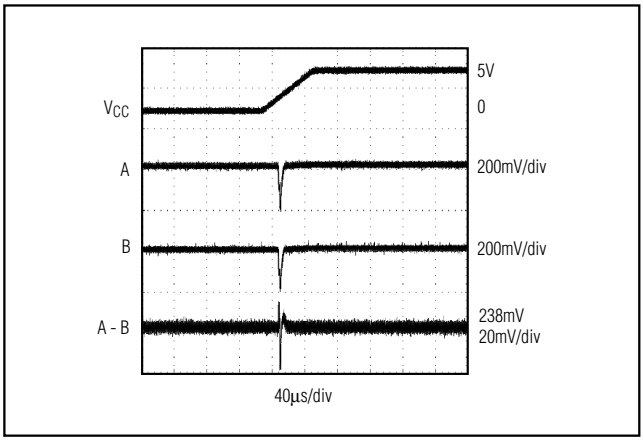


Figure 12. Differential Power-Up Glitch (0.1V/µs)

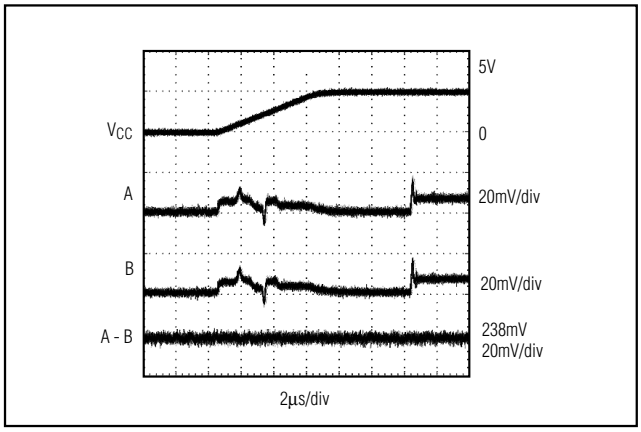


Figure 13. Differential Power-Up Glitch (1V/µs)

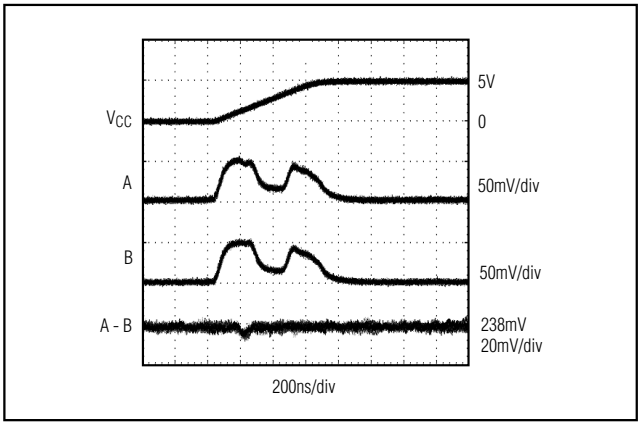


Figure 14. Differential Power-Up Glitch (10V/µs)

ESD Test Conditions

ESD performance depends on a number of conditions. Contact Maxim for a reliability report that documents test setup, methodology, and results.

Human Body Model

Figure 15a shows the Human Body Model, and Figure 15b shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

IEC 1000-4-2

The IEC 1000-4-2 standard covers ESD testing and performance of finished equipment; it does not specifically refer to integrated circuits.

The main difference between tests done using the Human Body Model and IEC 1000-4-2 is higher peak current in IEC 1000-4-2. Because series resistance is lower in the IEC 1000-4-2 ESD test model (Figure 16), the ESD withstand voltage measured to this standard is generally lower than that measured using the Human Body Model. The Air-Gap test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Machine Model

The Machine Model for ESD testing uses a 200pF storage capacitor and zero-discharge resistance. It mimics the stress caused by handling during manufacturing and assembly. All pins (not just RS-485 inputs) require this protection during manufacturing. Therefore, the Machine Model is less relevant to the I/O ports than are the Human Body Model and IEC 1000-4-2.

Applications Information

256 Transceivers on the Bus

The standard RS-485 receiver input impedance is 12kΩ (one-unit load), and the standard driver can drive up to 32-unit loads. The MAX3060E family of transceivers have a 1/8-unit-load receiver input impedance (96kΩ), allowing up to 256 transceivers to be connected in parallel on one communication line. Any combination of these devices and/or other RS-485 transceivers with a total of 32 unit loads or less can be connected to the line.

Reduced EMI and Reflections

The MAX3060E and MAX3061E are slew-rate limited, minimizing EMI and reducing reflections caused by improperly terminated cables. Figure 17 shows the driver output waveform and its Fourier analysis of a 25kHz signal transmitted by a MAX3062E. High-frequency harmonic components with large amplitudes are evident. Figure 18 shows the same signal displayed for a MAX3061E transmitting under the same conditions.

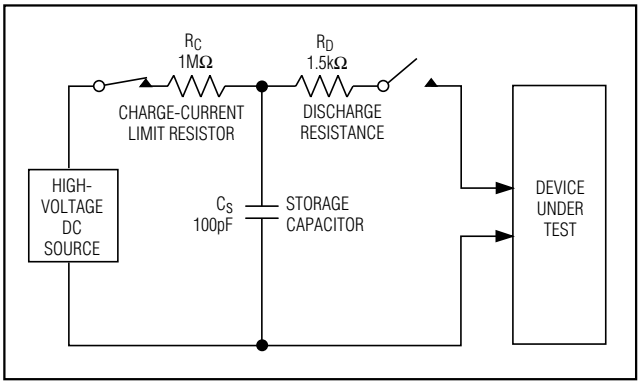


Figure 15a. Human Body ESD Test Model

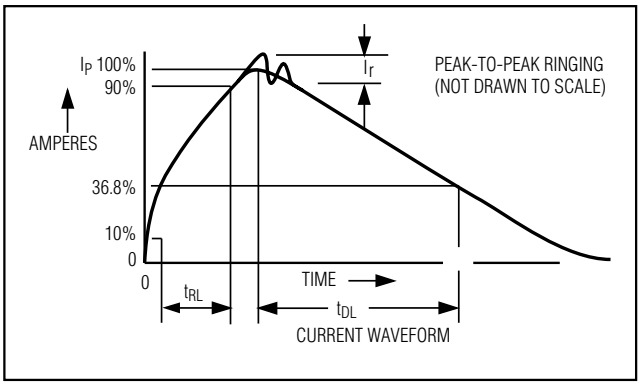


Figure 15b. Human Body Current Waveform

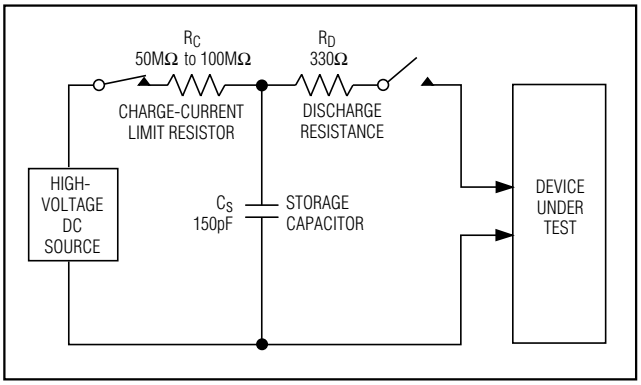


Figure 16. IEC 1000-4-2 ESD Test Model

Figure 18's high-frequency harmonic components are much lower in amplitude, compared with Figure 17's, and the potential for EMI is significantly reduced. Figure 19 shows the same signal displayed for a MAX3060E transmitting under the same conditions. Figure 19's high-frequency harmonic components are even lower.

In general, a transmitter's rise time relates directly to the length of an unterminated stub, which can be driven with only minor waveform reflections. The following equation expresses this relationship conservatively:

$$\text{Length} = t_{RISE} / (10 \times 1.5\text{ns/ft})$$

where t_{RISE} is the transmitter's rise time.

For example, the MAX3060E's rise time is typically 1850ns, which results in excellent waveforms with a stub length up to 123ft. A system can work well with longer unterminated stubs, even with severe reflections, if the waveform settles out before the UART samples them.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both $\overline{RE}$ high and DE low. In shutdown, the devices typically draw only 1nA of supply current.

$\overline{RE}$ and DE can be driven simultaneously. The parts are guaranteed not to enter shutdown if $\overline{RE}$ is high and DE is low for less than 50ns. If the inputs are in this state for at least 600ns, the parts are guaranteed to enter shutdown.

Enable times $t_{_ZH}$ and $t_{_ZL}$ in the *Switching Characteristics* tables assume the part was not in a low-power shutdown state. Enable times $t_{_ZH(SHDN)}$ and $t_{_ZL(SHDN)}$ assume the parts were shut down. It takes drivers and receivers longer to become enabled from low-power shutdown mode ($t_{_ZH(SHDN)}$, $t_{_ZL(SHDN)}$) than from driver/receiver-disable mode ($t_{_ZH}$, $t_{_ZL}$).

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides protection after a 20µs delay against short circuits over the whole common-mode voltage range (see *Typical Operating Characteristics*). The second, a thermal shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature becomes excessive.

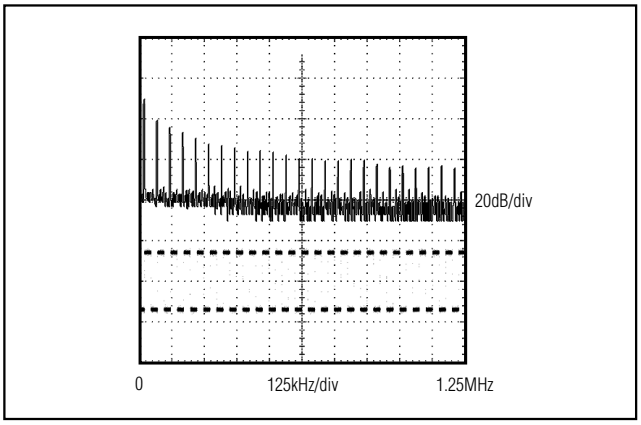


Figure 17. Driver Output Waveform and FFT Plot of MAX3062E Transmitting a 25kHz Signal

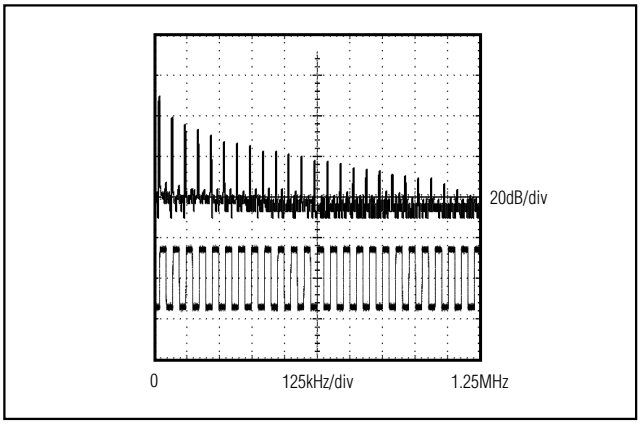


Figure 18. Driver Output Waveform and FFT Plot of MAX3061E Transmitting a 25kHz Signal

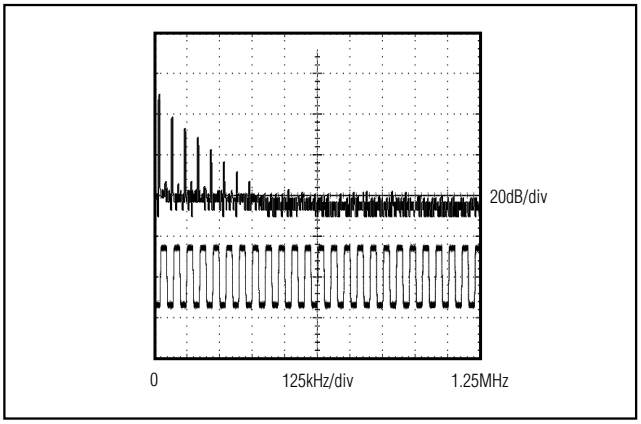


Figure 19. Driver Output Waveform and FFT Plot of MAX3060E Transmitting a 25kHz Signal

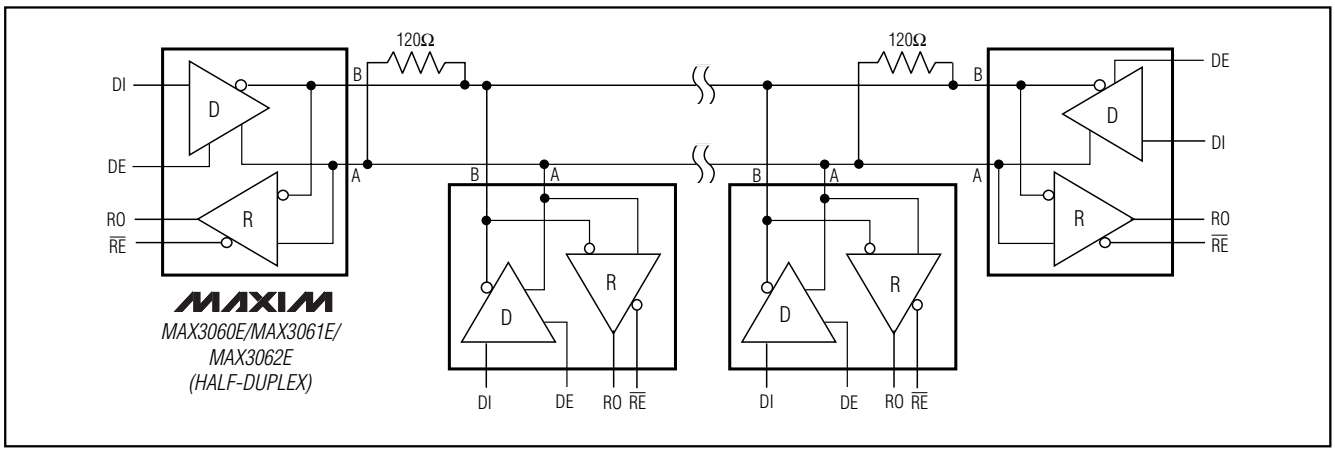


Figure 20. Typical Half-Duplex RS-485 Network

Typical Applications

The MAX3060E family of transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 20 shows a typical network application circuit.

To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible. The slew-rate-limited MAX3060E and MAX3061E are more tolerant of imperfect termination.

Chip Information

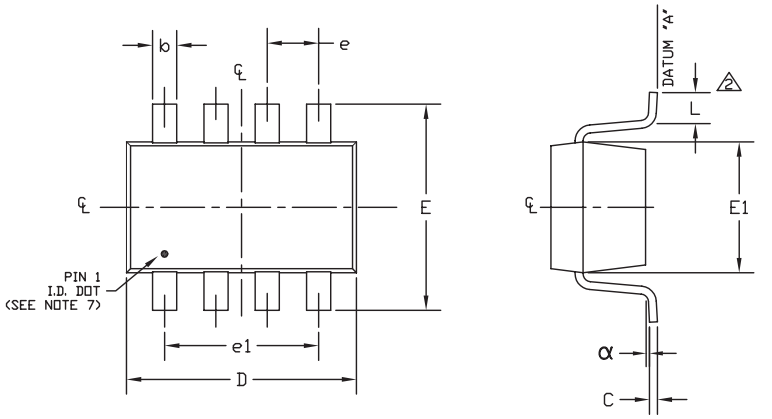
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PROCESS: CMOS

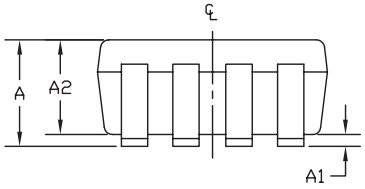
Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SOT23, 8L.EPS



SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.28	0.45
C	0.09	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.10	0.60
e	0.65 ref	
e1	1.95 ref	
α	0°	10°



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. FOOT LENGTH MEASURED REFERENCE TO FLAT FOOT SURFACE PARALLEL TO DATUM "A".
3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.
5. EIAJ REF. NUMBER" SC-74 (6 LEAD VERSION)
6. COPLANARITY 4 MILS. MAX.
7. PIN 1 I.D. DOT IS 0.3 MM Ø MIN. LOCATED ABOVE PIN 1.
8. MEETS JEDEC MO178.

MAXIM

PROPRIETARY INFORMATION

TITLE:

PACKAGE OUTLINE, SOT-23, 8L

APPROVAL	DOCUMENT CONTROL NO.	REV	
	21-0078	C	1/1

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