

DUAL SWITCHER AND LINEAR REGULATORS

Check for Samples: [TPS43331-Q1](#)

FEATURES

- Input Operating Range 5 V to 30 V (VBAT), With Transients Up to 40 V
- Two, Adjustable Output Voltage, Step-Down Switching Voltage Regulators
- External Clock Input
- Soft-Start Control for Step-Down Regulators
- Programmable, Linear Regulator (VSTBY), Low Quiescent Current (65uA typ.)
- Programmable, Linear Regulator (VLR)
- Overvoltage Detection and Shutdown
- Protected, High-Side Drive Output (HSD)
- Power-On Reset for Standby Regulator (VSTBY)
- Serial Communication, I2C Interface
- Low Voltage Warning Detection With Programmable Input Threshold (LVWIN, VBATW)
- Enable Feature, Controls VBUCK 1
- Programmable Power Good Delay Time (PGDLY) for VSTBY
- Current-Limit and Independent Thermal Detection and Shutdown Protection on All Regulators and High-Side Driver Output
- Operating Junction Temperature Range: -40°C to 150°C
- Thermally Enhanced 38-Pin DAP PowerPAD™ Package

APPLICATIONS

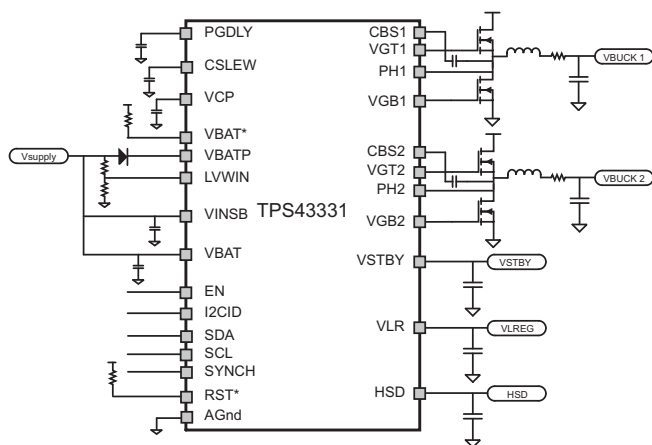
- Qualified for Automotive Applications
- Power Supply for Microcontrollers and DSPs

DESCRIPTION

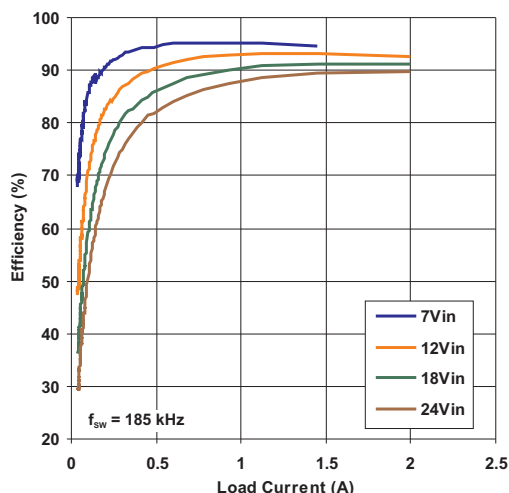
The TPS43331 is a multi-rail output voltage regulator, with two synchronous switch mode controllers and two linear regulators. In addition, there is a reverse protected high side switch and voltage supervisor for monitoring the standby regulator and input voltage. The regulator outputs and high side switch are controlled either by discrete inputs for certain outputs and serial interface using the I2C configuration for outputs not controlled by discrete inputs.

The standby linear regulator (VSTBY) is high voltage tolerant and can be connected directly to the vehicle battery, the quiescent current is typically 65 μ A to maintain a regulated output with light loads.

SIMPLIFIED SCHEMATIC



EFFICIENCY vs LOAD CURRENT ($V_{OUT} = 5$ V)



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|--------------|-----------------------|------------------|
| -40°C to 125°C | HTSSOP – DAP | Reel of 2000 | TPS43331QDAPRQ1 | TPS43331Q1 |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
- (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS^{(1) (2)}

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|----------|-----|------|
| Unregulated Input ⁽³⁾ | VBAT, VBATP | -0.3 | 40 | V |
| Unregulated power supply ⁽³⁾ | VINSB, VINLR | -0.3 | 40 | V |
| High side output ⁽⁴⁾ | HSD | -0.3 | 40 | V |
| Low voltage warning input | LVWIN | -0.3 | 40 | V |
| Switched linear regulator | VLR | -0.3 | 15 | V |
| Bootstrap capacitor | VCP | -0.3 | 18 | V |
| Logic level or low voltage signals | PGDLY, CSLEW, $\overline{\text{VBATW}}$, $\overline{\text{RST}}$, EN, VSTBYS, VLRS, SYNCH, I2CID, SCL, SDA, VCMP1, VCMP2, VFB1, VFB2 ⁽³⁾ | -0.3 | 5.5 | V |
| | ISHI1, ISHI2, ISLO1, ISLO2 ⁽³⁾ | -0.3 | 10 | |
| | CBS1, CBS2, VGT1, VGT2 | -0.3 | 40 | |
| | VGB1, VGB2 | -0.3 | 10 | |
| | PH1, PH2 ⁽⁴⁾ | -1 | 40 | |
| θ_{JC} | Thermal impedance junction to case ⁽⁵⁾ | | 10 | °C/W |
| θ_{JA} | Thermal impedance junction to ambient ⁽⁶⁾ | | 25 | °C/W |
| ESD | Electrostatic discharge ⁽⁷⁾ | All pins | 2 | kV |
| T _J | Operating junction temperature range | -40 | 150 | °C |
| T _{STG} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Absolute negative voltage on these pins not to go below -0.5 V
- (4) Absolute negative voltage on these pins not to go below -1.0 V, and transients of -2 V due to recirculation of an inductive load for < 100ns
- (5) This assumes junction to exposed thermal pad.
- (6) This assumes a JEDEC JESD 51-5 standard board with thermal vias – See PowerPAD section and the application report *PowerPAD Thermally Enhanced Package (SLMA002)* for more information.
- (7) The human body model is a 100-pF capacitor discharged through a 1.5-k Ω resistor into each pin

RECOMMENDED OPERATING CONDITIONS

| | | MIN | MAX | UNIT |
|---|---|-----|-----|------|
| Unregulated Input | VBAT, VBATP | 5 | 30 | V |
| Unregulated power supply | VINSB, VINLR | 1.8 | 30 | V |
| High side output | HSD | 5 | 30 | V |
| Low voltage warning input | LVWIN | 5 | 30 | V |
| Switched linear regulator and standby regulator | VLR, VSTBY | 3 | 16 | V |
| Bootstrap capacitor | VCP | | 16 | V |
| Logic level or low voltage signals | PGDLY, CSLEW, $\overline{\text{VBATW}}$, RST, EN, VSTBYS, VLRS, SYNCH, I2CID, SCL, SDA, VCMP1, VCMP2, VFB1, VFB2 | 4.5 | 5.3 | V |
| | ISH1, ISH2, ISLO1, ISLO2 | 1.2 | 9 | V |
| | CBS1, CBS2, VGT1, VGT2 | 5 | 38 | V |
| | VGB1, VGB2 | 3 | 8 | V |
| | PH1, PH2 | -1 | 30 | V |
| T _A Operating ambient temperature ⁽¹⁾ | | -40 | 125 | °C |

(1) Assumes T_A = T_J – Power dissipation × θ_{JA}

DC ELECTRICAL CHARACTERISTICS

VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|--|------|------|------|
| VBAT Battery input | | | | |
| V _{NOV} Normal operating voltage | | 6 | 18 | V |
| V _{JSV} Jump start voltage | T _A = -40°C to 50°C | 18 | 26.5 | V |
| V _{OVSD} Overvoltage shutdown | All outputs except standby reg are disabled, | 27 | | V |
| V _{HYS} Hysteresis | | 0.5 | | V |
| V _{UVLO} Undervoltage lockout | VSTBY ref disabled, Verify < V _{OL(max)} | 2 | 5.2 | V |
| I _Q Battery input leakage current | Standby mode, Battery = 14 V, I _{VSTBY} = 100 μA, I _{Battery} - I _{VSTBY} , EN = 0 V | | 100 | μA |
| | Standby mode, V _{UVLO} < Battery < 18 V, I _{VSTBY} = -100 μA, I _{Battery} - I _{VSTBY} , EN = 0 V | | 130 | |
| | Standby mode, 18 V < Battery < 40 V, I _{VSTBY} = -100 μA, I _{Battery} - I _{VSTBY} , EN = 0 V | | 200 | |
| I _B Battery input bias current | VBAT = 6V to 18V, HSDEN = VLREN = SW2EN = 1, VGT2 = VGB2 = open, I _{VSTBY} = I _{VLR} = I _{HSD} = 100 μA, I _{Battery} - I _{VSTBY} - I _{VLR} - I _{HSD} | | 25 | mA |
| I _B VBAT input bias current | VBAT = 6 V to 18 V, HSDEN = 1, I _{HSD} = 100 μA, I _{VBAT} - I _{HSD} | | 1 | mA |
| | VBAT = 40 V | | 5 | |
| | VBAT = -20 V | | -2 | |
| LVWIN Low voltage warning input | | | | |
| V _{TH} Input high threshold | | 1.10 | 1.20 | V |
| V _{HYS} Hysteresis | On rising edge on input signal | 70 | 120 | mV |
| I _{LKG} Input leakage current | LVWIN = 1 V to 18 V | -1 | 1 | μA |
| | LVWIN = 40 V | -1 | 1.0 | |

DC ELECTRICAL CHARACTERISTICS (continued)

VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|--------------------------------|--|------|-------|------|
| VBATP Consumption current | | | | | |
| I _B | Supply current from VBATP line | I _{VSTBY} = 50 mA | | 10 | mA |
| | | SW2EN = 1, VGTX = VGBX = open | | 15 | |
| | | V _{LREN} = 1, I _{VLR} = 100 μA | | 10 | |
| | | I _{VBATP} = I _{VLR} | | 10 | |
| | | VBAT = 40 V, I _{VSTBY} = 50 mA | | 6 | |
| | | VBAT = VINLR = Open, V _{UVLO} < VBATP = VINSB < 18 V, V _{LREN} = SW2EN = HSDEN = 1, I _{VLR} = I _{HSD} = -100 μA, VGTX = VGBX = Open, I _{VBATP} = I _{VSTBY} + I _{VLR} + I _{HSD} | | 20 | |
| CSLEW Slew rate control on standby regulator VSTBY | | | | | |
| I _{CSLEW} | Soft-start rate on VSTBY reg | C _{CSLEW} = 0.01 μF | -2.9 | -1.45 | μA |
| EN Enable/disable input | | | | | |
| V _{IH} | Enable | | 2 | | V |
| V _{IL} | Disable | | | 0.8 | V |
| V _{HYS} | Hysteresis | | 300 | 800 | mV |
| I _{LKG} | Input leakage current | | -1 | 1 | μA |
| SYNCH Synchronization input voltage threshold | | | | | |
| V _{IH} | Enable | Switch enabled going from low to high 20% to 80% | 2 | | V |
| V _{IL} | Disable | Switch disabled going from high to low 80% to 20% | | 0.8 | V |
| V _{HYS} | Hysteresis | | 300 | 800 | mV |
| R _{PD} | Input pulldown resistance | | 20 | 100 | kΩ |
| PGDLY Power good delay | | | | | |
| I _{OH} | Power delay output current | PGDLY = 0, 100 pF ≤ C _{PGDLY} ≤ 0.01 μF | -2.6 | -1.5 | μA |
| V _{TH} | Input threshold | Verify $\overline{\text{RST}}$ de-asserted | 1.5 | 2.5 | V |
| V _{SAT} | PGDLY saturation voltage | 100 pF ≤ C _{PGDLY} ≤ 0.01 μF | | 0.4 | V |
| RST Reset output | | | | | |
| V _{OL} | Reset output | 0.5 V ≤ VSTBY ≤ VTH_min (VSTBY), I _{OL} = 1.6 mA, active mode | | 0.4 | V |
| | | 0.5 V ≤ VSTBY ≤ VTH_min (VSTBY), I _{OL} = 1.6 mA, standby mode | | 0.4 | V |
| | | 0.5 V ≤ VBATP ≤ VUVLO_min, I _{OL} = 100 μA | | 0.4 | V |
| I _{Leakage} | Output leakage current | $\overline{\text{RST}}$ = VSTBY, active and standby modes | -10 | 10 | μA |
| VBATW Low input voltage warning (Battery input) | | | | | |
| V _{OL} | Warning output voltage | I _{OL} = 1.6mA, active and standby modes | | 0.4 | V |
| I _{Leakage} | Output leakage current | $\overline{\text{VBATW}}$ = VSTBY, active and standby modes | -10 | 10 | μA |

AC SWITCHING CHARACTERISTICS

VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted) (see Figure 1 and Figure 2)

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|---------------------|--|--|-----|------|
| RST Reset timing | | | | | |
| 1 | t _{enrst} | Reset enable time | 0 | | μs |
| 2 | t _{PGDLY} | Reset delay time | CPGDLY(nom) = 100 pF | | μs |
| 3 | t _{por} | Internal power on reset | VSTBY in regulation to RST de-asserted delay | | ms |
| 4 | t _f | Reset fall time | C _{RST} = 50 pF | | μs |
| VSTBY Standby regulator de-glitch timer | | | | | |
| 5 | t _{lvcp} | De-glitch filter time | 5 | 20 | μs |
| PGDLY Power good discharge time | | | | | |
| | t _{dch} | Power good delay capacitor discharge time | CPGDLY = 0.01uF | | μs |
| VBATW low input voltage warning | | | | | |
| 6 | t _{prlvw} | Low voltage output indicator propagation delay | | 1 | μs |
| 7 | t _{pfovsd} | | | 1 | μs |
| 8 | t _{pflvw} | | | 1 | μs |
| 9 | t _f | Fall time | | 1 | μs |

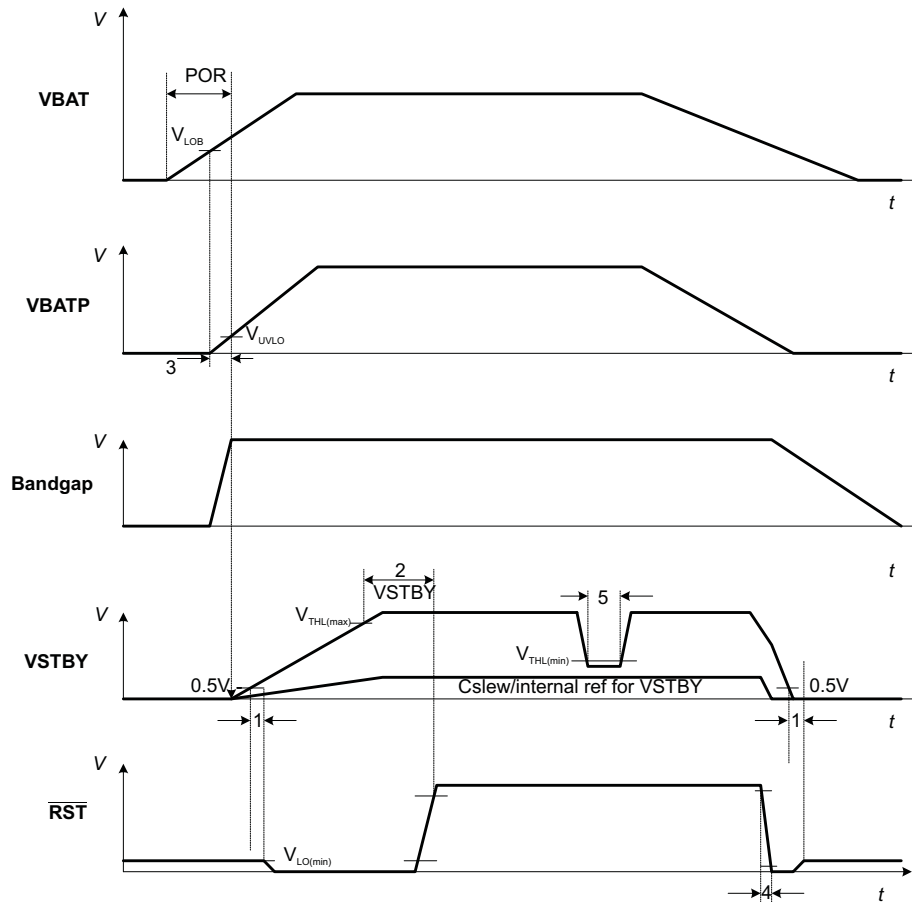


Figure 1. Input and Control Timing

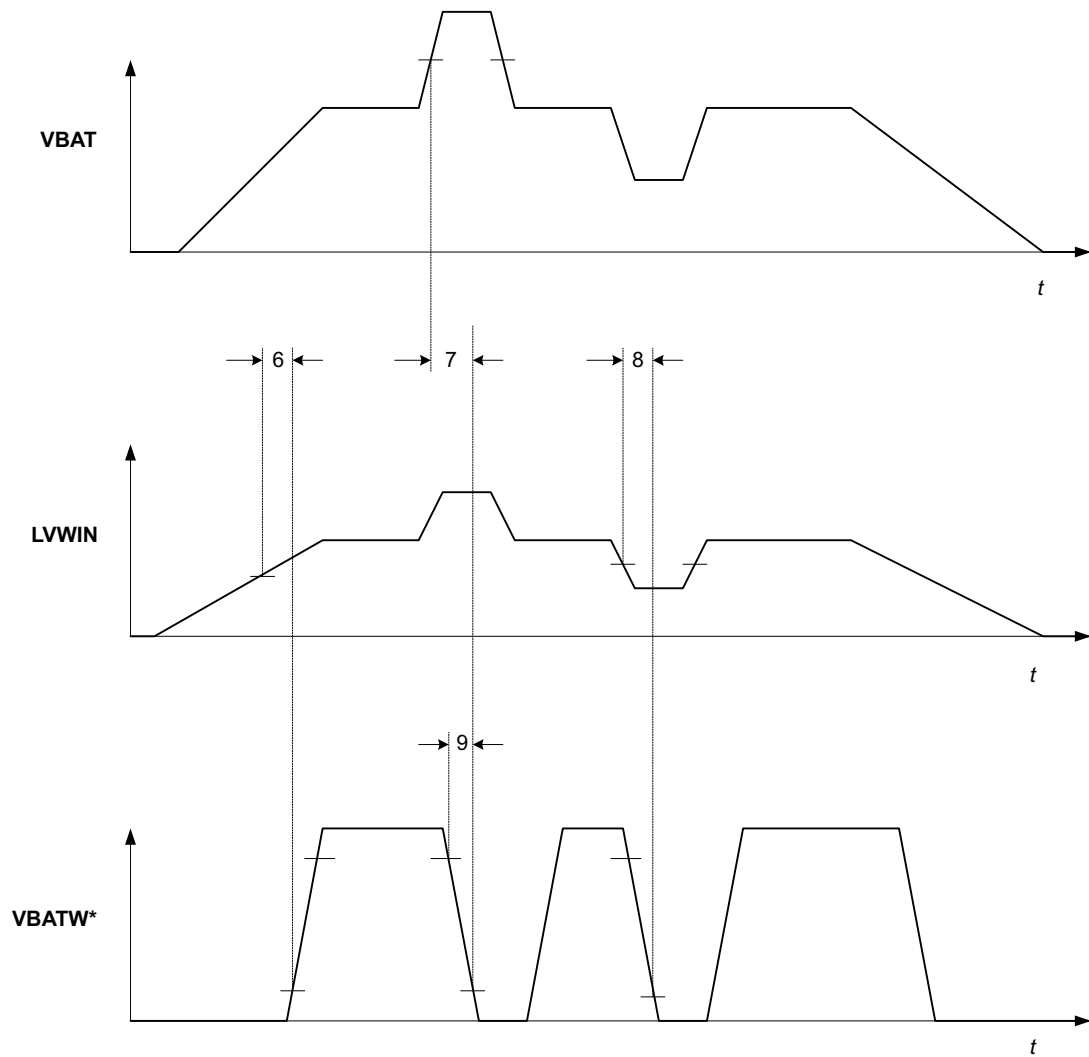


Figure 2. Input and Control Timing for $\overline{\text{VBATW}}$

I2C INTERFACE ELECTRICAL CHARACTERISTICS

VBAT = VBATP = 6 V to 18 V, T_j = -40°C to 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---------------------------|----------------------------------|-----|-----|------|
| I2CID Serial interface ID address input | | | | | |
| V _{IH} | Input high threshold | | 2 | | V |
| V _{IL} | Input low threshold | | | 0.8 | V |
| V _{HYS} | Hysteresis | | 0.3 | 0.8 | V |
| I _{LKG} | Input leakage current | I2CID = 3.3V | -1 | 1 | μA |
| SCL Serial clock input for synchronization | | | | | |
| V _{IH} | Input high threshold | | 2 | | V |
| V _{IL} | Input low threshold | | | 0.8 | V |
| V _{HYS} | Hysteresis | | 0.3 | 0.8 | V |
| I _{LKG} | Input leakage current | 0.3 V ≤ V _{SCL} ≤ 3.0 V | -1 | 1 | μA |
| C _{SCLIN} | Input line capacitance | | | 10 | pF |
| SDA Serial communications data line | | | | | |
| V _{IH} | Input high threshold | | 2 | | V |
| V _{IL} | input low threshold | | | 0.8 | V |
| V _{HYS} | Hysteresis | | 0.3 | 0.8 | V |
| I _{Leakage} | Leakage current | 0.3 V ≤ V _{SDA} ≤ 3.0 V | -1 | 1 | μA |
| V _{SAT} | Output saturation voltage | I _{OL} = 3 mA | | 0.4 | V |
| | | I _{OL} = 6 mA | | 0.6 | V |
| C _{SDAIN} | Input line capacitance | | | 10 | pF |

I2C INTERFACE SWITCHING CHARACTERISTICS^{(1) (2)}VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted) (see [Figure 3](#))

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|--|---|--------------------------------------|-------------------|-----|------|
| SCL Serial clock timing | | | | | |
| 1 | f _{SCL} Serial clock frequency | Standard mode | 0 | 100 | kHz |
| | | Fast mode | 0 | 400 | kHz |
| 2 | t _{HD, STA} Hold time for repeated start | Standard mode | 4 | | μs |
| | | Fast mode | 0.6 | | μs |
| 3 | t _{LOW} Clock low pulse width | Standard mode | 4.7 | | μs |
| | | Fast mode | 1.3 | | μs |
| 4 | t _{HIGH} Clock high pulse width | Standard mode | 4 | | μs |
| | | Fast mode | 0.6 | | μs |
| 5 | t _{SU, STA} Setup time for repeated start | Standard mode | 4.7 | | μs |
| | | Fast mode | 0.6 | | μs |
| 6 | t _{r, SCL} Clock rise time | Standard mode | | 1 | μs |
| | | Fast mode, C _{SCL} = 10 pF | 21 ⁽³⁾ | 300 | ns |
| | | Fast mode, C _{SCL} = 400 pF | 60 | 300 | ns |
| 7 | t _{f, SCL} Clock fall time | Standard mode | | 0.3 | μs |
| | | Fast mode, C _{SCL} = 10 pF | 21 | 300 | ns |
| | | Fast mode, C _{SCL} = 400 pF | 60 | 300 | ns |
| 8 | t _{SP, SCL} Clock input noise pulse | | | 50 | ns |
| SDA Serial communications data line | | | | | |
| 9 | t _{SU, DAT} Serial data setup time | Standard mode | 250 | | ns |
| | | Fast mode | 100 | | ns |
| 10 | t _{r, SDA} Data rise time | Standard mode | | 1 | μs |
| | | Fast mode, C _{SDA} = 10 pF | 21 | 300 | ns |
| | | Fast mode, C _{SDA} = 400 pF | 60 | 300 | ns |
| 11 | t _{f, SDA} Data fall time | Standard mode | | 300 | ns |
| | | Fast mode, C _{SDA} = 10 pF | 21 | 300 | ns |
| | | Fast mode, C _{SDA} = 400 pF | 60 | 300 | ns |
| 12 | t _{SP, SDA} SDA input noise pulse | | | 50 | ns |
| 13 | t _{fo, SDA} SDA output pulse time | Standard mode | | 250 | ns |
| | | Fast mode, C _{SDA} = 10 pF | 21 | 250 | ns |
| | | Fast mode, C _{SDA} = 400 pF | 60 | 250 | ns |
| 14 | t _{SU, STO} Stop bit setup time | Standard mode | 4.0 | | μs |
| | | Fast mode | 0.6 | | μs |
| 15 | t _{BU} Bus free between stop and start bit | Standard mode | 4.7 | | μs |
| | | Fast mode | 1.3 | | μs |

(1) Capacitance on serial interface pins SCL and SDA are 10 pF ≥ C_{SCL}, C_{SDA} ≥ 400 pF

(2) Parameters assured by worst case test program execution in fast mode.

(3) The total load capacitance range for SCL and SDA for I2C specification

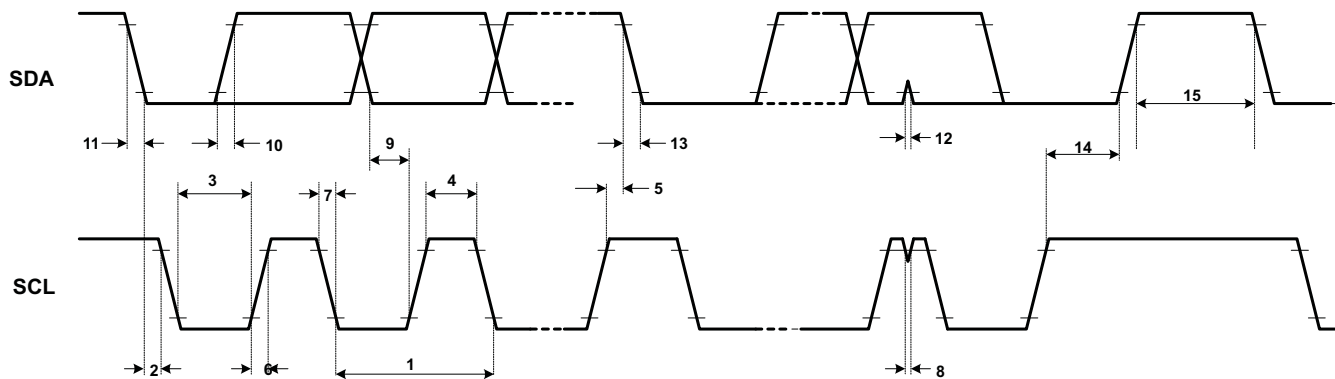


Figure 3. Serial Communication AC Timing (I2C Interface)

SWITCHING REGULATORS ELECTRICAL CHARACTERISTICS

VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|--------------------|------|------|
| Switch mode regulators (Channel 1) | | | | | |
| I _O | Output current | | 0.4 ⁽¹⁾ | 4.0 | A |
| V _O | Regulated output voltage range | | 1.2 | 10 | V |
| V _{FB1} | Feedback voltage input | | 980 | 1020 | mV |
| V _{OTOL} | Regulated output voltage tolerance | I _O = I _O (max) to I _O (min), Includes external feedback resistors | -5 | 5 | % |
| V _{ISCTH} | Short circuit current, voltage threshold ⁽²⁾ | | 60 | 120 | mV |
| V _{DO} | Dropout voltage ⁽³⁾ | I _O = I _O (max), VBAT = 9 V, Includes drop due to V _{ISCTH} | | 400 | mV |
| dV/dt | Output voltage soft-start slew rate ⁽⁴⁾ | Step response on regulator enable, I _O = I _O (max) | | 10 | V/ms |
| | | | | 5 | % |
| V _{P_SC} | Overshoot ⁽⁵⁾ | I _O = I _{SC} (max), Remove short | | 5 | % |
| V _{P_TR} | Load transient response ⁽⁵⁾ | I _O = I _O (min) to I _O (max) | -5 | | % |
| | | I _O = I _O (max) to I _O (min) | | 5 | % |
| I _{VGT1_SRC} | Gate drive source current (high side) | VGT1 = VGB1 = 6 V, measure time calculate current | 210 | 330 | mA |
| I _{VGT1_SINK} | Gate drive sink current (high side) | | 500 | 1020 | mA |
| I _{VGB1_SRC} | Gate drive source current (low side) | | 90 | 135 | mA |
| I _{VGB1_SINK} | Gate drive sink current (low side) | | 440 | 1300 | mA |
| Switch mode regulators (Channel 2), SW2EN = 1 (unless otherwise noted) | | | | | |
| I _O | Output current | | 0.4 ⁽¹⁾ | 4.0 | A |
| V _O | Regulated output voltage range | | 1.2 | 10 | V |
| V _{FB1} | Feedback voltage input | | 980 | 1020 | mV |
| V _{OTOL} | Regulated output voltage tolerance | I _O = I _O (max) to I _O (min), Includes external feedback resistors | -5 | 5 | % |
| V _{ISCTH} | Short circuit current, voltage threshold ⁽²⁾ | | 60 | 120 | mV |
| V _{DO} | Dropout voltage ⁽³⁾ | I _O = I _O (max), VBAT = 9 V, Includes drop due to V _{ISCTH} | | 400 | mV |
| dV/dt | Output voltage soft-start slew rate ⁽⁴⁾ | Step response on regulator enable, I _O = I _O (max) | | 10 | V/ms |
| V _{P_SC} | Overshoot ⁽⁵⁾ | I _O = I _{SC} (max), Remove short | | 5 | % |
| V _{P_TR} | Load transient response ⁽⁵⁾ | I _O = I _O (min) to I _O (max) | -5 | | % |
| | | I _O = I _O (max) to I _O (min) | | 5 | % |
| I _{VGT2_SRC} | Gate drive source current (High side) | VGT1 = VGB1 = 6V, measure time calculate current | 210 | 330 | mA |
| I _{VGT2_SINK} | Gate drive sink current (High side) | | 500 | 1020 | mA |
| I _{VGB2_SRC} | Gate drive source current (Low side) | | 90 | 135 | mA |
| I _{VGB2_SINK} | Gate drive sink current (Low side) | | 440 | 1300 | mA |

(1) MIN based on 10% of MAX current shown. For MAX lower currents I_O MIN will be 10% of the lower MAX current.

(2) The output remains stable using soft-start conditions when the output drops from regulation to 0 V. The IC is not damaged by a hard short to ground.

(3) Lower VBAT until the output drops to 0.1 V. Measure VBAT – V_O.

(4) Design information- Not tested. Specified by CSLEW current and bench characterization.

(5) Design information – Not tested

SWITCHING REGULATORS SWITCHING CHARACTERISTICS

VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|-----|---------------------|-------------------------------------|--------------------|---------------------|------|
| 1 | f _{SW} | Nominal operating frequency | 165 | | kHz |
| 1 | f _{SWTOL} | Operating frequency tolerance | -15 | 15 | % |
| 1 | f _{SYN CH} | Synch frequency range nominal | 225 | 400 | kHz |
| 1 | D _{SYN CH} | Synch input duty ratio | 40 | 60 | % |
| 2 | t _r | Gate drive transition time, rising | | 500 ⁽¹⁾ | ns |
| 3 | t _f | Gate drive transition time, falling | | 100 ⁽¹⁾ | ns |
| 4 | t _{DS} | Synchronous switch on delay | 20 | 100 ⁽²⁾ | ns |
| 5 | t _{dt} | Top switch on delay | 20 | 100 | ns |
| | t _{dc} | Minimum on time | 3.5 ⁽³⁾ | 98.2 ⁽⁴⁾ | % |

- (1) Switching times will vary for different external FET.
- (2) Delay time is intended to guard against shoot-through losses and will be dependent upon the switch transition times. Measurements are done at either threshold values or 50% as shown below.
- (3) D_{on(min)} = (1.2 V × (1 - t_{ol})) / V_{ov(max)} = (1.2 V × 0.95) / 33 V.
- (4) Min refresh time of 220 ns every five periods at 440 kHz.

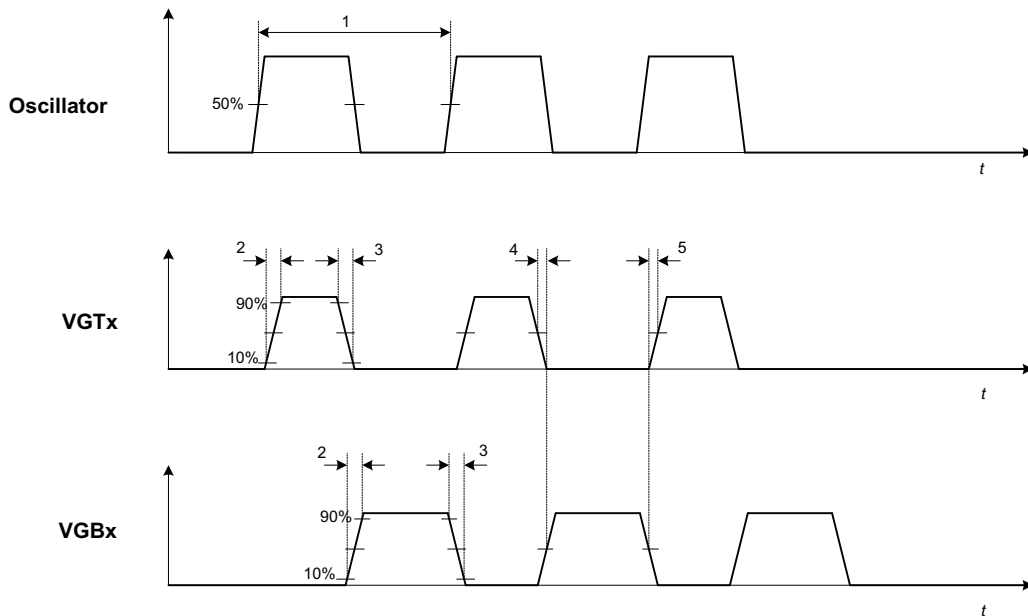


Figure 4. Switching Regulators Timing

STANDBY REGULATOR (VSTBY) ELECTRICAL CHARACTERISTICS

VINLR = 3 V to 18 V, VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|--|--|------|------|------|
| I _O | Output current | Active mode | 5 | 300 | mA |
| | | Standby mode | 0.05 | 300 | |
| V _O | Regulated output voltage range | V _{STBYS} = (V _O + V _{DO}) to 18 V, I _O = I _{O(max)} ⁽¹⁾ to I _{O(min)} , T _A = -40°C to 50°C, V _{STBYS} = 18 V to 26.5 V, I _O = I _{O(max)} ⁽²⁾ to I _{O(min)} | 1.2 | 3.6 | V |
| V _{STBYS} | Feedback input voltage for standby regulator | | 980 | 1020 | mV |
| V _{STBY} | Load regulation | I _O = I _{O(max)} to I _{O(min)} , V _O + V _{DO} < V _{STBYS} < 18 V, 1% nominal (3% worse case) tolerance resistors, I _O = I _{O(max)} to I _{O(min)} , V _{INSB} = 18 V to 26.5 V | -5 | 5 | % |
| | | I _O = I _{O(max)} , 18 V < V _{INSB} < 26.5 V | | 8 | |
| LR | Load regulation | I _O = I _{O(max)} to I _{O(min)} | -4 | 0 | % |
| SR | Line regulation | I _O = I _{O(max)} , V _O + V _{DO} < V _{STBYS} < 18 V | -4 | 4 | % |
| I _{SC} | Short circuit current limit | V _{STBY} = 0 V ⁽³⁾ | 310 | 1400 | mA |
| V _{DO} | Dropout voltage ⁽⁴⁾ | I _O = 300 mA | | 1200 | mV |
| V _{LVRTH} | Low-voltage reset threshold | Lower V _O until goes low | 900 | 950 | mV |
| T _{SD} | Thermal shutdown ⁽⁵⁾ | | 150 | 210 | C |
| T _{HYS} | Hysteresis | | 5 | 15 | C |
| ΔV/ΔT | Output voltage slew rate ⁽⁶⁾ | Step response on regulator, I _O = I _{O(min)} | | 10 | V/mS |
| V _{OP_SC} | Overshoot ⁽⁵⁾ | I _O = I _{SC(min)} , Remove short | | 5 | % |
| V _{P_TR} | Load transient response ⁽⁵⁾ | Active mode, V _{STBY} = 1.2 V, C _{VSTBY} = 1.0 μF, Δt = 10 μs, I _O = I _{O(min)} to I _{O(max)} , I _O = I _{O(max)} to I _{O(min)} | -6 | 6 | % |
| | | Active mode, V _{STBY} = 3.6 V, C _{VSTBY} = 1.0 μF, Δt = 10 μs, I _O = I _{O(min)} to I _{O(max)} , I _O = I _{O(max)} to I _{O(min)} | -6 | 6 | |
| | | Standby mode, V _{STBY} = 1.2 V, C _{VSTBY} = 1.0 μF, Δt = 10 μs, I _O = -100 mA to I _{O(max)} , I _O = I _{O(max)} to -100mA | -6 | 6 | |
| | | Standby mode, V _{STBY} = 3.6 V, C _{VSTBY} = 1.0 μF, Δt = 10 μs, I _O = -100 mA to I _{O(max)} , I _O = I _{O(max)} to -100 mA | -6 | 6 | |
| V _{PRSS} | Power supply rejection ratio ⁽⁵⁾ | I _O = 0.5×I _{O(max)} , f _o = 120 Hz to 10 kHz, V _{STBYS} = 14 Vdc and 1 Vac (p-p) | 50 | | dB |
| | | I _O = 0.5×I _{O(max)} , f _o = 20 to 20 kHz, V _{STBYS} = 14 Vdc and 1 Vac (p-p) | 45 | | |
| V _N | Output noise | 100-kHz low-pass filter, f _o = 20 Hz to 100 kHz, I _{VSTBY} = -5mA | | 400 | μV |
| | | 100-kHz low-pass filter, f _o = 20 Hz to 20 kHz, I _{VSTBY} = -5mA | | 200 | |
| t _{tr} | Output voltage transient response | I _O = I _{O(min)} to I _{O(max)} , C _{O(max)} | | 40 | μs |
| CO | Output capacitance | C _{O(nom)} = 1.0 μF, 16 V | 0.53 | 1.15 | μF |
| R _{ESR} | Output capacitance ESR | f = 1 kHz, T _A = 125°C | | 8.75 | Ω |
| DF | Output capacitor dissipation factor | f = 1 kHz, T _A = -40°C | | 1 | % |
| | | f = 1 kHz, T _A = 25°C | | 3.5 | |
| | | f = 1 kHz, T _A = 125°C | | 5.5 | |

- (1) This nomenclature is meant to agree with the convention that current flow into the pin is a positive. Therefore I_{O(max)} is a smaller magnitude current and I_{O(min)} is larger magnitude current throughout the parametric tables
- (2) Design information- Not tested, parameter assured by characterization.
- (3) The output remains stable using soft-start conditions when the output drops from regulation to 0 V. The IC is not damaged by a hard short to ground.
- (4) Lower VBAT until the output drops to 0.1 V. Measure VBAT – V_O.
- (5) Design information – Not tested
- (6) Design information- Not tested. Specified by CSLEW current and bench characterization.

LINEAR REGULATOR (VLR) ELECTRICAL CHARACTERISTICS

VINLR = 3 V to 18 V, VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------|--|---|------|------|------|
| I _O | Output current | | 5 | 650 | mA |
| V _O | Regulated output voltage range | VINLR = (V _O + V _{DO}) to 18 V, I _O = I _O (max) to I _O (min), T _A = -40°C to 50°C, VINLR = 18 V to 26.5 V, I _O = I _O (max) to I _O (min) | 1.2 | 8.5 | V |
| V _{LRS} | Feedback input voltage | | 980 | 1020 | mV |
| V _{LR} | Output voltage tolerance | I _O = I _O (max) to I _O (min), V _O + V _{DO} < VINLR < 18 V, 1% nominal (3% worse case) tolerance resistors | -5 | 5 | % |
| | | I _O = I _O (max) to I _O (min), VINLR = 18V to 26.5V | | 8 | |
| LR | Load regulation | I _O = I _O (max) to I _O (min) | -4 | 1 | % |
| SR | Line regulation | I _O = I _O (max), V _O + V _{DO} < VINLR < 18 V | -4 | 4 | % |
| | | I _O = I _O (max), 18 V < VINLR < 26.5 V | -4.0 | 4 | |
| I _{SC} | Short circuit current limit | V _{LR} = 0 V ⁽¹⁾ | 0.7 | 2.7 | A |
| V _{DO} | Dropout voltage ⁽²⁾ | I _O = -200mA | | 400 | mV |
| | | I _O = -600mA | | 1.7 | V |
| T _{SD} | Thermal shutdown ⁽³⁾ | | 150 | 210 | °C |
| T _{HYS} | Hysteresis | | 5 | 15 | °C |
| V _{OP_SC} | Overshoot | I _O = I _{SC} (min), Remove short | | 5 | % |
| V _{P_TR} | Load transient response ⁽³⁾ | VLR = 1.2V, CVLR = 1.0 μF, Δt = 10 μs, I _O = I _O (min) to I _O (max), I _O = I _O (max) to I _O (min) | -6 | 6 | % |
| | | VLR = 8.5 V, CVLR = 1.0 μF, Δt = 10 μs, I _O = I _O (min) to I _O (max), I _O = I _O (max) to I _O (min) | -6 | 6 | |
| V _{PRSS} | Power supply rejection ratio ⁽³⁾ | I _O = 0.5×I _O (max), f _o = 120 Hz to 10 kHz, VINLR = 14 Vdc and 1 Vac (p-p) | 50 | | dB |
| | | I _O = 0.5×I _O (max), f _o = 20 Hz to 20 kHz, VINLR = 14 Vdc and 1 Vac (p-p) | 45 | | |
| V _N | Output noise ⁽³⁾ | 100-kHz low-pass filter, f _o = 20 Hz to 100 kHz, I _{VLR} = -5mA | | 400 | μV |
| | | Weighted filter, f _o = 20 Hz to 20 kHz, I _{VLR} = -5 mA | | 200 | |
| t _{tr} | Output voltage transient response ⁽³⁾ | I _O = I _O (min) to I _O (max), C _O (max) | | 40 | μs |
| C _O | Output capacitance ⁽³⁾ | C _O (nom) = 1.0 μF, 16 V | 0.53 | 1.15 | μF |
| R _{ESR} | Output capacitance ESR ⁽³⁾ | f = 1 kHz, T _A = 125°C | | 8.75 | Ω |
| DF | Output capacitor dissipation factor ⁽³⁾ | f = 1 kHz, T _A = -40°C | | 1 | % |
| | | f = 1 kHz, T _A = 25°C | | 3.5 | |
| | | f = 1 kHz, T _A = 125°C | | 5.5 | |

(1) The output remains stable using soft-start conditions when the output drops from regulation to 0 V. The IC is not damaged by a hard short to ground.

(2) Lower VBAT until the output drops to 0.1 V. Measure VBAT – V_O.

(3) Design information – Not tested

LINEAR REGULATOR SWITCHING CHARACTERISTICS

VINLR = 3 V to 18 V, VBAT = VBATP = 6 V to 18 V, T_J = -40°C to 150°C (unless otherwise noted) (see [Figure 5](#))

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|-----|---|-----------------|-----|-----|------|
| 1 | t _{don} Turn-on delay | | | 15 | μs |
| 2 | t _{doff} Turn-off delay | | | 15 | μs |
| 3 | t _{dovsd} Delay timer over-voltage shutdown | | | 200 | μs |
| 4 | t _{drovsd} Delay timer return from over-voltage shutdown | | | 200 | μs |

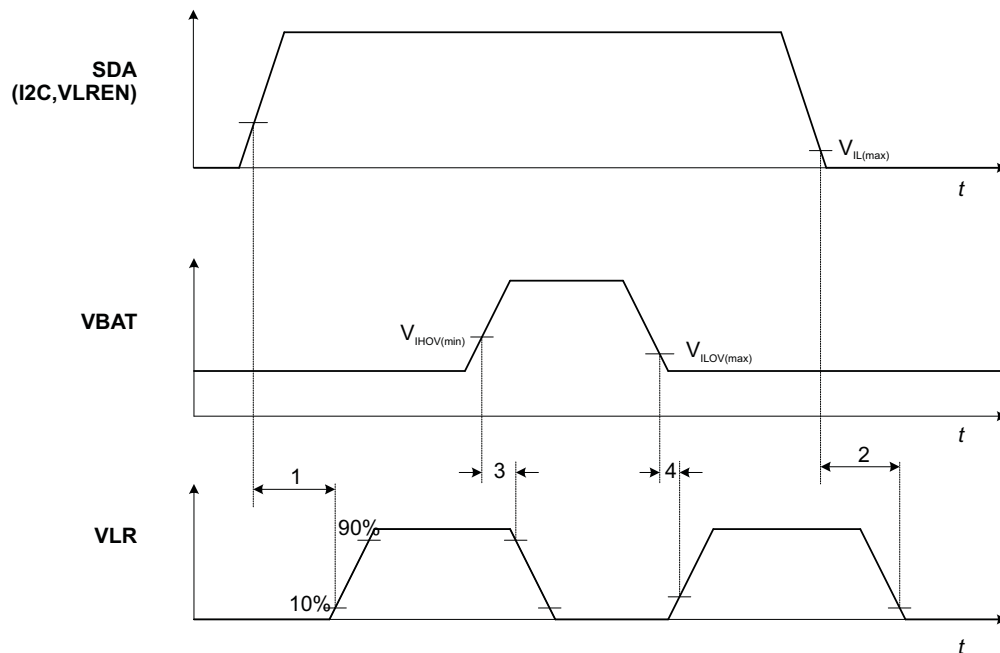


Figure 5. Linear Regulator Timing

HIGH-SIDE DRIVER (HSD) ELECTRICAL CHARACTERISTICS

VBAT = VBATP = 6 V to 18 V, HSD1EN = 1, T_J = -40°C to 150°C (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|-------|------------------|------|
| V _{SAT} HSD output saturation voltage | I _{HSD} = -300 mA | | 0.6 | V |
| | I _{HSD} = -450 mA, t = 0.5 s | | 1.2 | V |
| I _{LKG} Leakage current | HSD1EN = 0, HSD = 0 V | -5 | 5 | μA |
| | HSD1EN = 0, R _{HSD} = 20 Ω to -1 V | -100 | | μA |
| | HSD1EN = 0, VBAT = HSD | -100 | 100 | μA |
| | HSD1EN = 0, VBAT = HSD = 34 V | -100 | 100 | μA |
| | VBAT = open, C _{VBAT} = 1 mF, HSD = 18 V | 0 | 10 | mA |
| I _{STG} High-side short circuit current | GND = open, R _{HSD} = 20 Ω to -1 V | | (1)15 | mA |
| | HSD = 0 V | 0.310 | 1.4 | A |
| T _{SD} HSD thermal shutdown ⁽³⁾ | HSD = VBAT | -2 | 2 ⁽²⁾ | mA |
| | I _{HSD} = -100 μA | 150 | 190 | °C |
| T _{HYS} Hysteresis | | 5 | 15 | °C |

- (1) The condition does not damage the IC or any external components connected to the IC.
- (2) The limits are based on characterization. This condition does not damage the IC and or any external components connected to the IC.
- (3) Design information – Not tested

HIGH-SIDE DRIVER (HSD) SWITCHING CHARACTERISTICS

VBAT = VBATP = 6 V to 18 V, HSD1EN = 1, T_J = -40°C to 150°C (unless otherwise noted) (see FIGURE)

| NO. | PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|-----|--|--------------------------|-----|-----|------|
| 1 | t _{don} Turn-on delay ⁽¹⁾ | | 0 | 15 | μs |
| 2 | t _{doff} Turn-off delay | R _{HSD} = 180 Ω | 0 | 200 | μs |
| 3 | t _r Rise time, 10% to 90% | | 25 | 75 | μs |
| 4 | t _{dovsd} Delay timer over-voltage shutdown | | 0 | 200 | μs |
| 5 | t _{dprovsd} Delay timer return from over-voltage shutdown | | 0 | 200 | μs |

- (1) Design information – Not tested

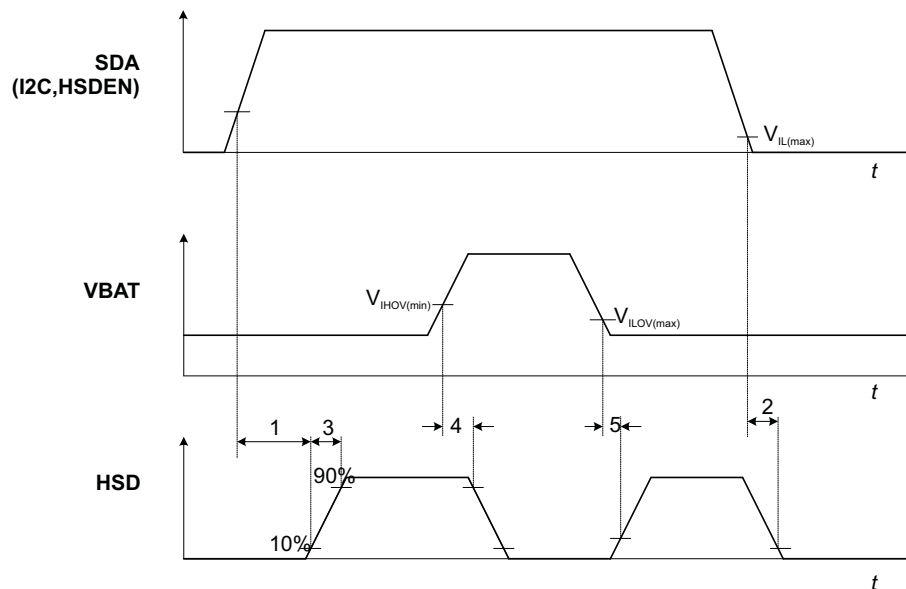
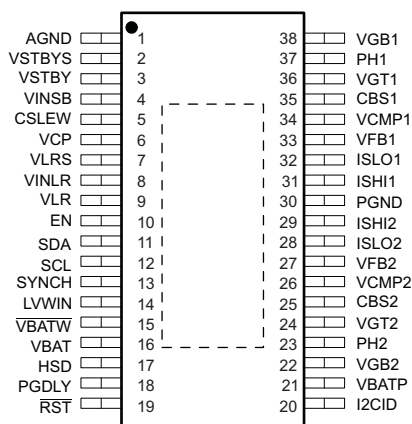


Figure 6. HSD Timing

DEVICE INFORMATION

DAP PACKAGE (TOP VIEW)



TERMINAL FUNCTIONS

| NAME | NO. | I/O | DEFAULT STATE | DESCRIPTION |
|--------|-----|--------|---------------|---|
| AGND | 1 | Ground | - | Analog ground reference |
| VSTBYS | 2 | I | - | Voltage feedback for standby regulator |
| VSTBY | 3 | O | - | Regulated output, for standby and normal mode |
| VINSB | 4 | Power | - | Power input for standby regulator |
| CSLEW | 5 | O | Low | Capacitor to control VSTBY slew rate |
| VCP | 6 | I | - | Storage capacitor for charge pump |
| VLRS | 7 | I | - | Voltage feedback for switched linear regulator |
| VINLR | 8 | Power | - | Input power for switched linear regulator |
| VLR | 9 | O | - | Linear regulator output, switched using serial interface |
| EN | 10 | I | Low | Input command for active mode |
| SDA | 11 | I/O | - | Serial bidirectional data line for I2C |
| SCL | 12 | I | - | Serial clock input for synchronization of data communications for I2C |
| SYNCH | 13 | I | Low | External clock input for synchronization of switching frequency for SMPS |
| LVWIN | 14 | I | - | Low-voltage warning input |
| VBATW | 15 | O | Open | Battery voltage warning output |
| VBAT | 16 | Power | - | Input power for high side driver switch |
| HSD | 17 | O | - | High side driver output |
| PGDLY | 18 | I | - | Power good delay capacitor input for VSTBY regulator |
| RST | 19 | O | Low | Low-voltage reset indicator for VSTBY (active low) |
| I2CID | 20 | I | Low | Chip Identifier for I2C |
| VBATP | 21 | Power | - | Battery voltage input for IC with external protection for reverse connections |
| VGB2 | 22 | O | Low | Low side gate drive output for channel 2 (synchronous switch) |
| PH2 | 23 | I | - | Phase reference for bootstrap drive channel 2 |
| VTG2 | 24 | O | Low | High side gate drive output for channel 2 (synchronous switch) |
| CBS2 | 25 | I | - | Bootstrap capacitor for high side gate drive channel 2 |
| VCMP2 | 26 | I | - | Compensation feedback for channel 2 |
| VFB2 | 27 | I | - | Regulated output voltage feedback for channel 2 |
| ISLO2 | 28 | I | - | Low side of output current sense, channel 2 |
| ISH2 | 29 | I | - | High side of output current sense, channel 2 |
| PGND | 30 | Ground | - | Power ground, switching regulator ground reference |

TERMINAL FUNCTIONS (continued)

| NAME | NO. | I/O | DEFAULT STATE | DESCRIPTION |
|-------|-----|-----|---------------|--|
| ISHI1 | 31 | I | - | High side of output current sense, channel 1 |
| ISLO1 | 32 | I | - | Low side of output current sense, channel 1 |
| VFB1 | 33 | I | - | Regulated output voltage feedback for channel 1 |
| VCMP1 | 34 | I | - | Compensation feedback for channel 1 |
| CBS1 | 35 | I | - | Bootstrap capacitor for high side gate drive channel 1 |
| VGT1 | 36 | O | Low | High side gate drive output for channel 1 (synchronous switch) |
| PH1 | 37 | I | - | Phase reference for bootstrap drive channel 1 |
| VGB1 | 38 | O | Low | Low side gate drive output for channel 1 (synchronous switch) |

Typical Application Schematic

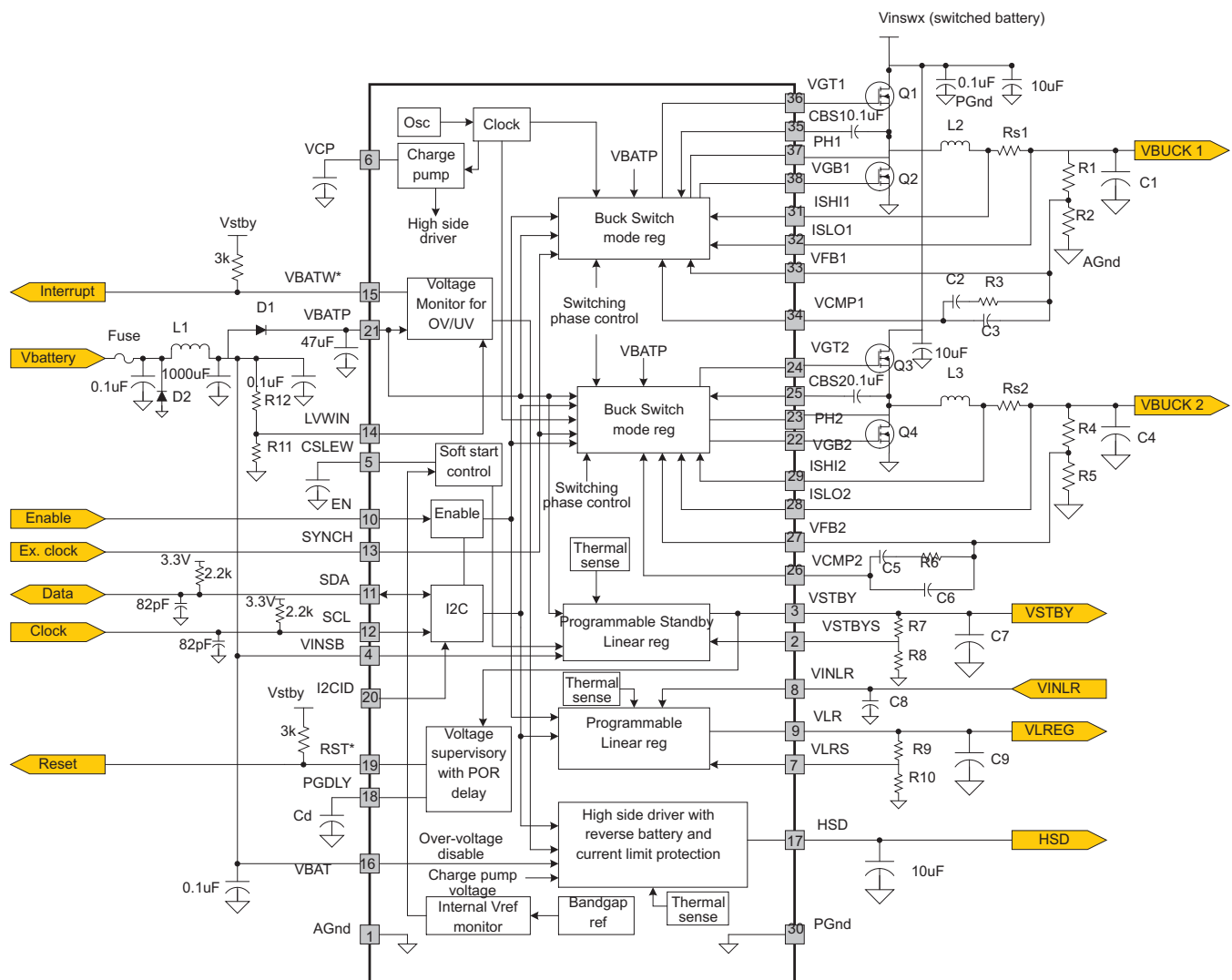


Figure 7. Typical Application Schematic

Operating Mode Definition

Figure 8 shows the operating modes of the TPS43331.

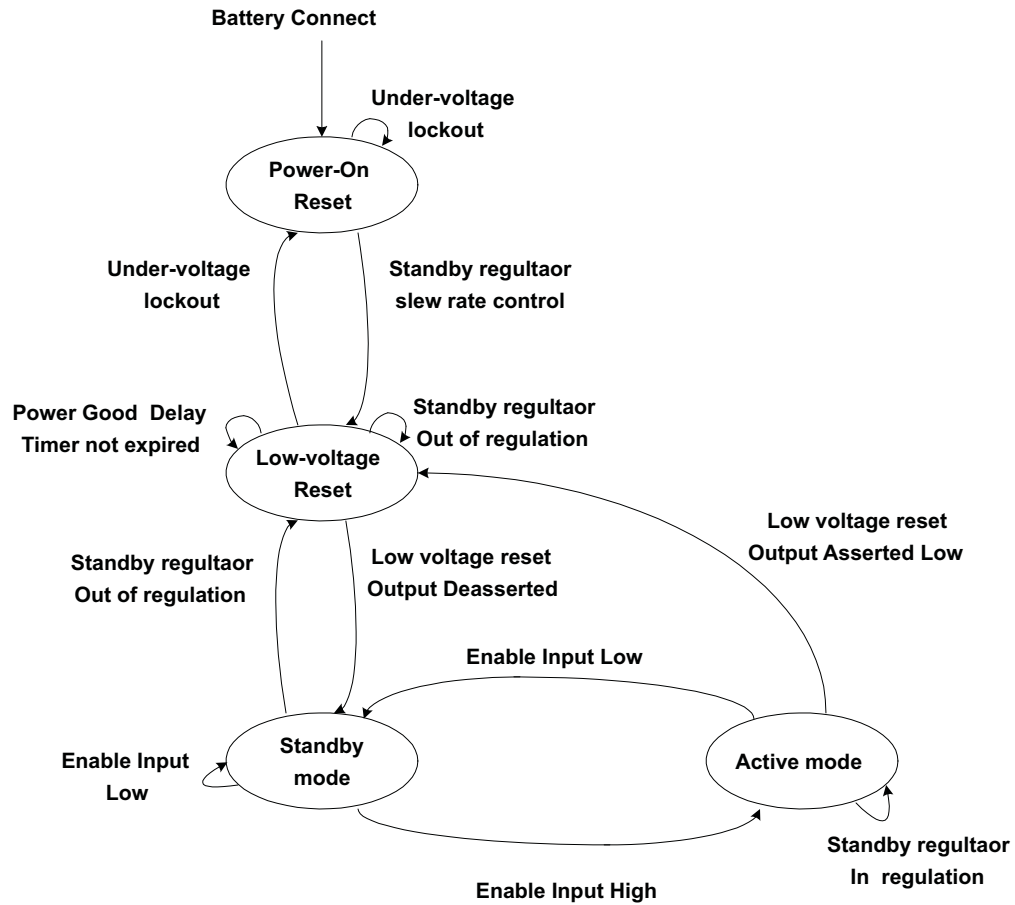


Figure 8. Operating Modes

TYPICAL CHARACTERISTICS

FEEDBACK REFERENCE
vs
AMBIENT TEMPERATURE

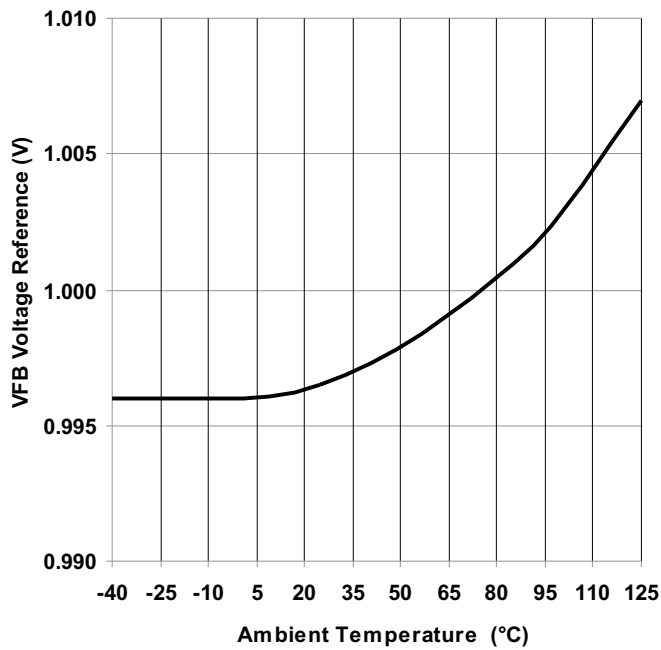


Figure 9.

INTERNAL FIXED SWITCHING FREQUENCY
vs
AMBIENT TEMPERATURE

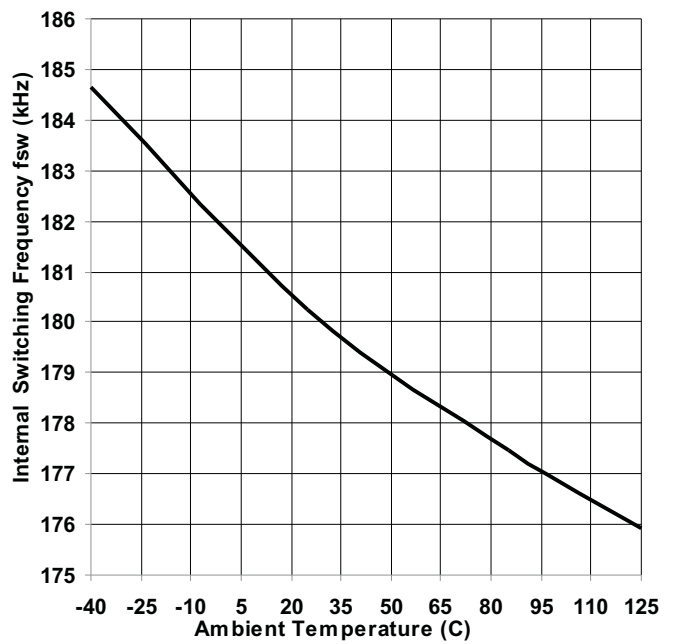


Figure 10.

EFFICIENCY
vs
LOAD CURRENT
(VBUCK 1, V_{OUT} = 5 V)

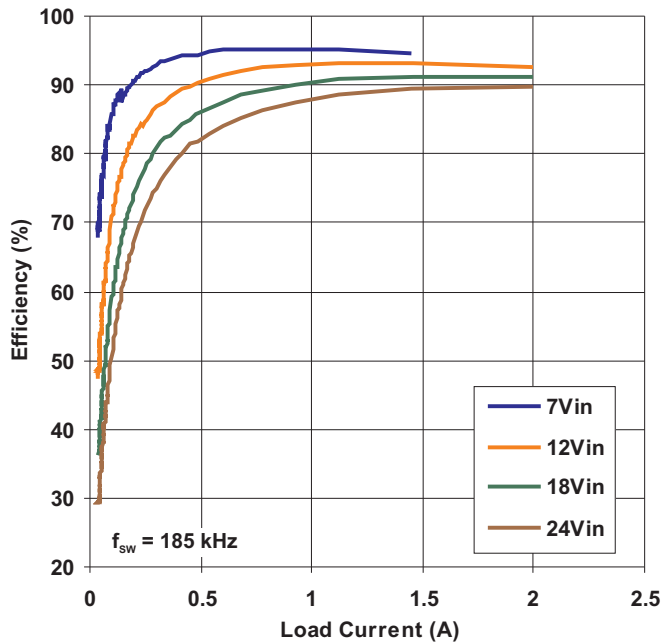


Figure 11.

EFFICIENCY
vs
LOAD CURRENT
(VBUCK 2, V_{OUT} = 3.3 V)

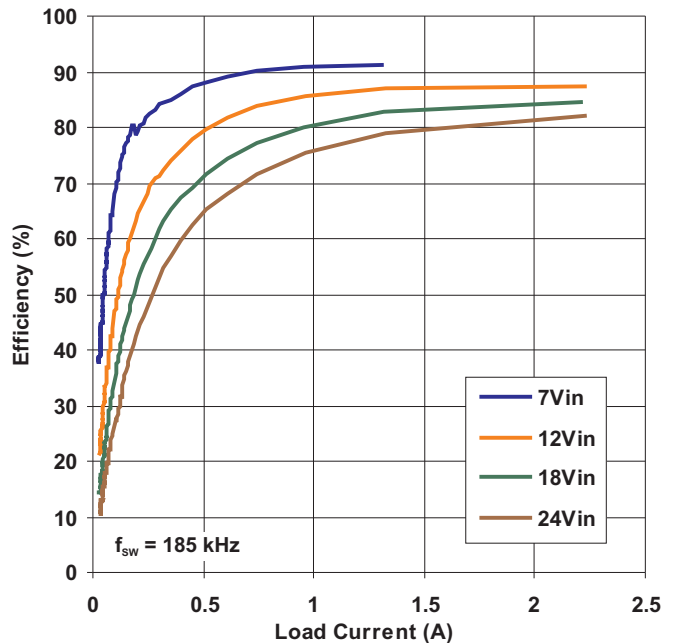


Figure 12.

TYPICAL CHARACTERISTICS (continued)

**HSD RDS ON RESISTANCE
VS
AMBIENT TEMPERATURE**

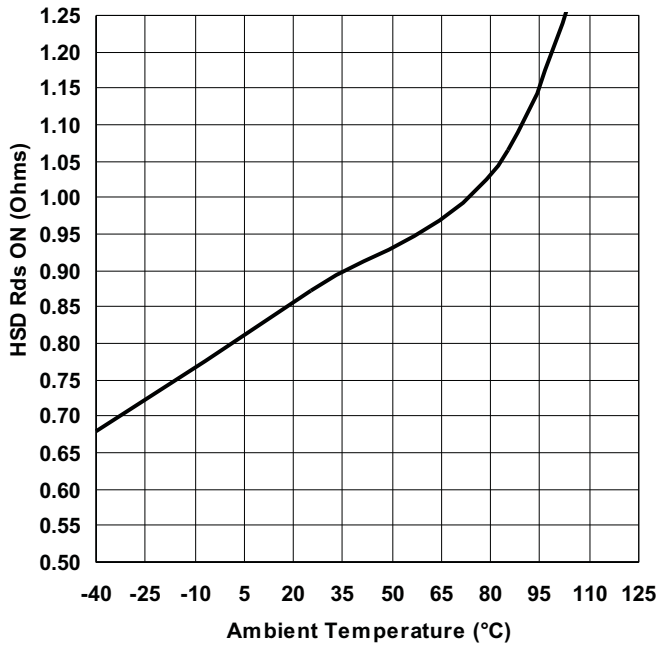


Figure 13.

**OVER-CURRENT VOLTAGE THRESHOLD
VS
AMBIENT TEMPERATURE**

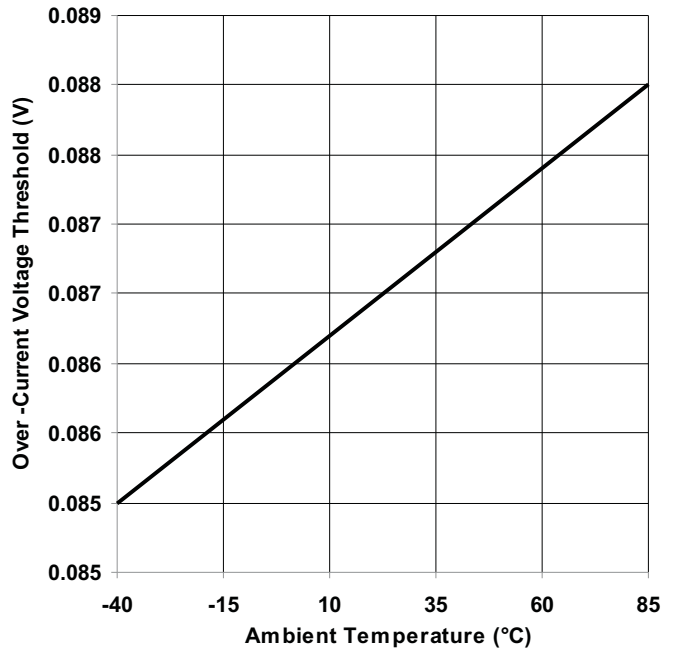


Figure 14.

**QUIESCENT CURRENT
VS
AMBIENT TEMPERATURE**

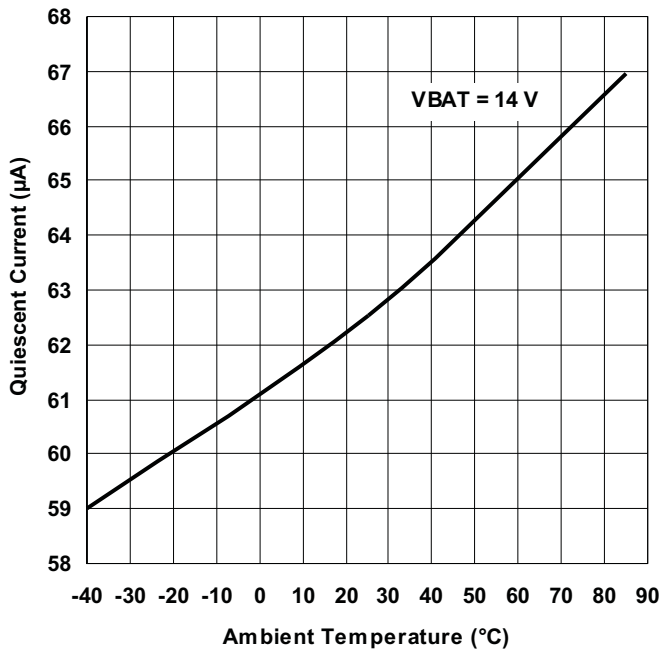


Figure 15.

**VLR DROPOUT VOLTAGE
VS
AMBIENT TEMPERATURE**

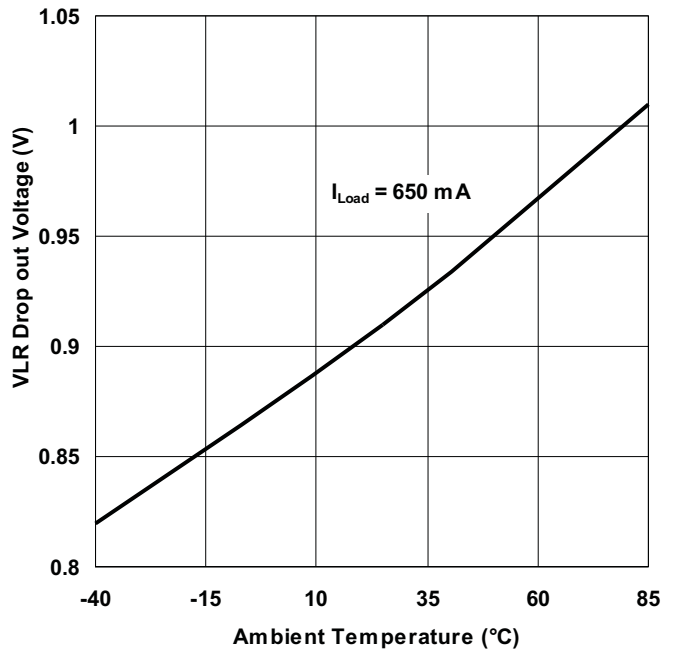


Figure 16.

TYPICAL CHARACTERISTICS (continued)

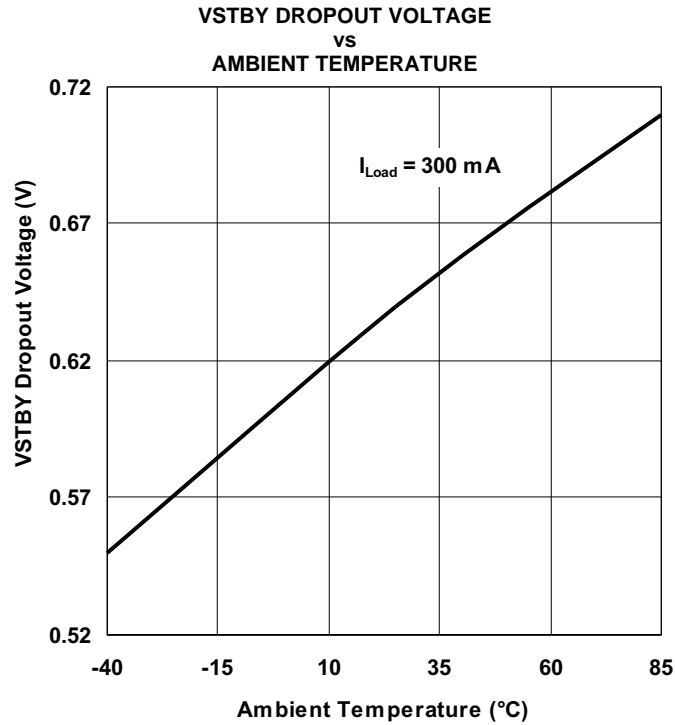


Figure 17.

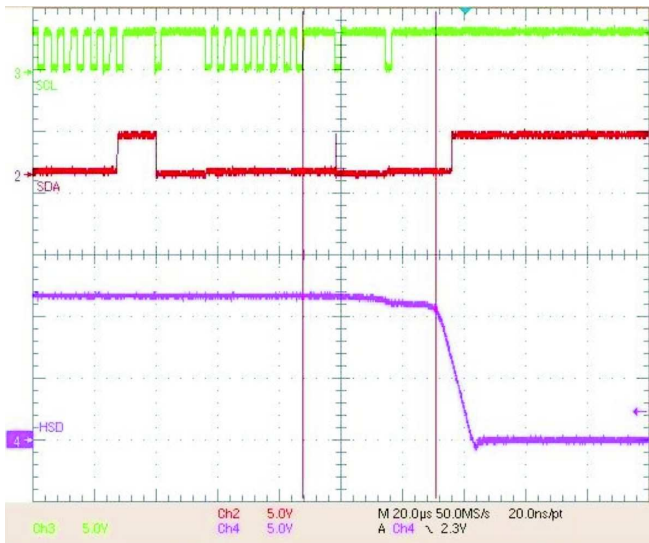


Figure 18. High-Side Driver (HSD) Output Power Down Delay From I2C Bit Disable, $\Delta t = 43 \mu\text{s}$

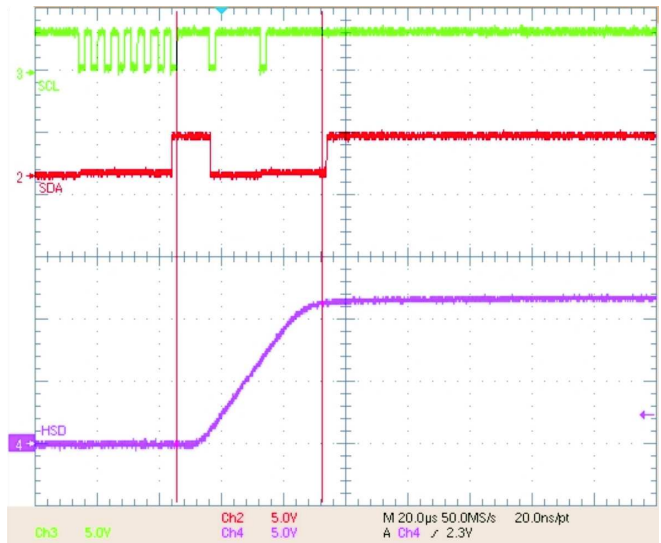


Figure 19. High-Side Driver (HSD) Output Power ON Delay From I2C Bit Enable, $\Delta t = 47 \mu\text{s}$

TYPICAL CHARACTERISTICS (continued)

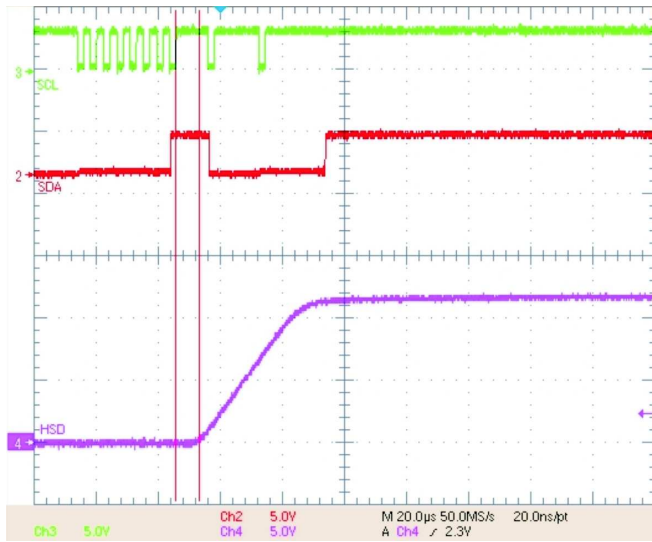


Figure 20. High-Side Driver (HSD) Output Turn ON Delay From I2C Bit Enable, $\Delta t = 7.6 \mu s$

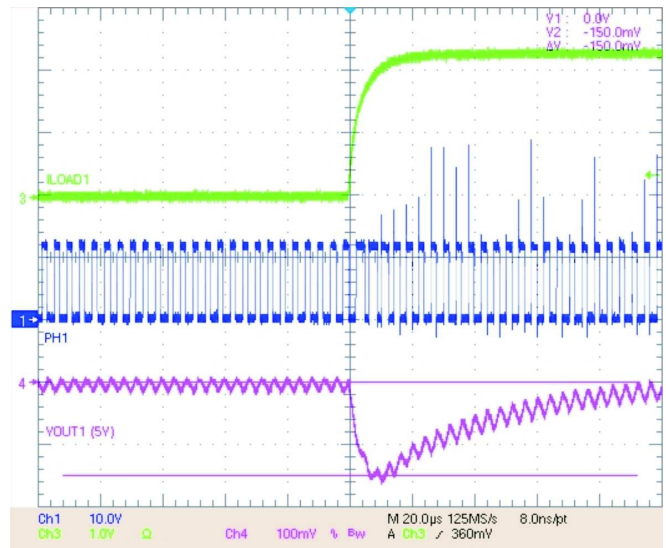


Figure 21. Load Step on VBUCK 1 From 0 A to 2 A, V_{OUT1} Droop = 150 mV

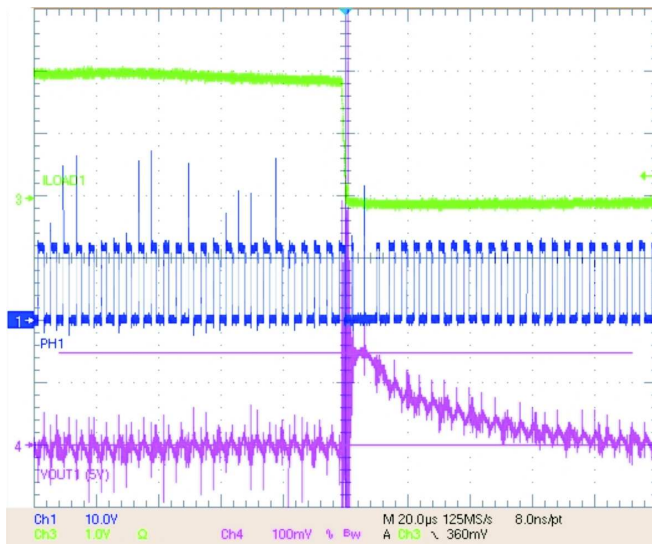


Figure 22. Load Step on VBUCK 1 From 2 A to 0 A, V_{OUT1} Overshoot = 148 mV

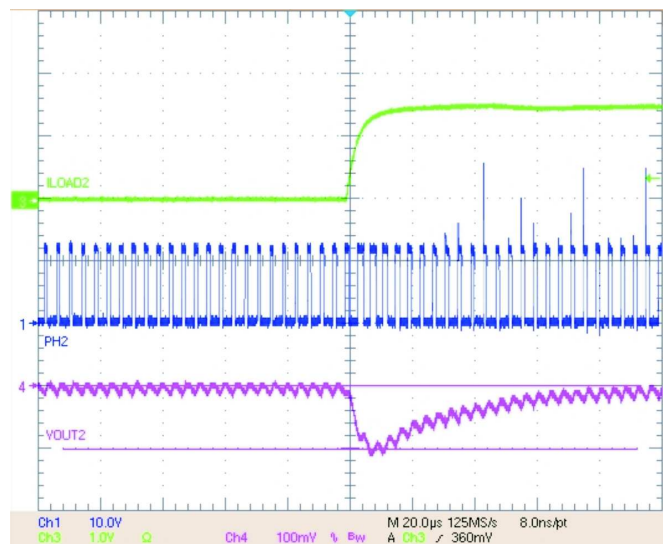


Figure 23. Load Step on VBUCK 2 From 0 A to 1.3 A, V_{OUT1} Droop = 102 mV

TYPICAL CHARACTERISTICS (continued)

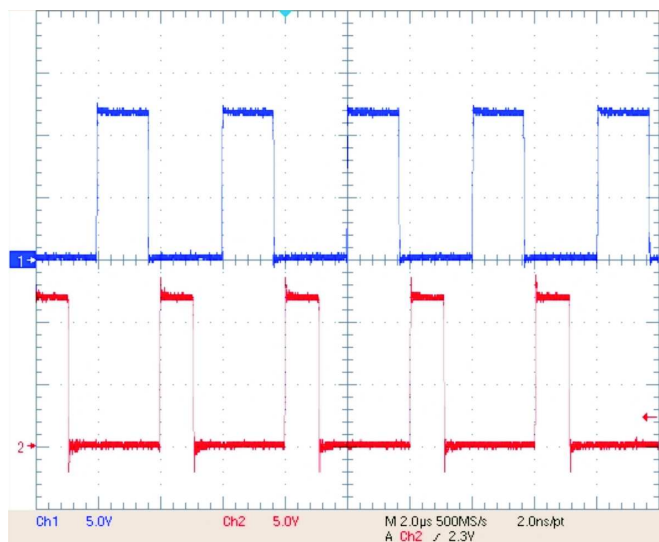


Figure 24. VBUCK 1 and VBUCK 2 Switching 180° Out of Phase

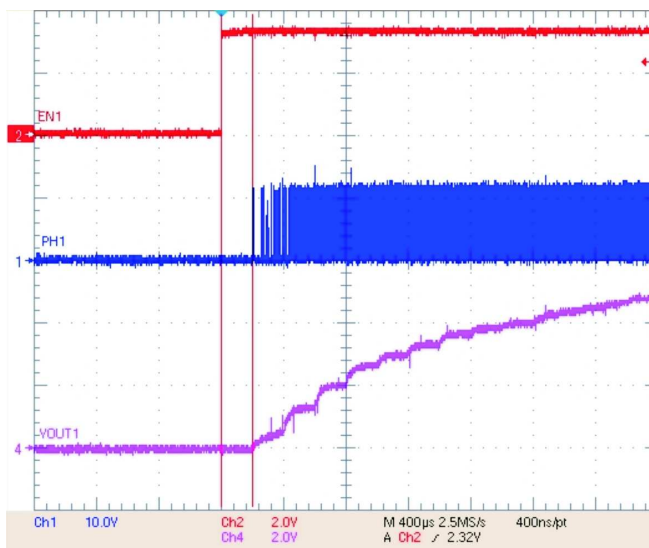


Figure 25. VBUCK 1 Turn ON Delay From Enable Going High, $\Delta t = 200 \mu s$

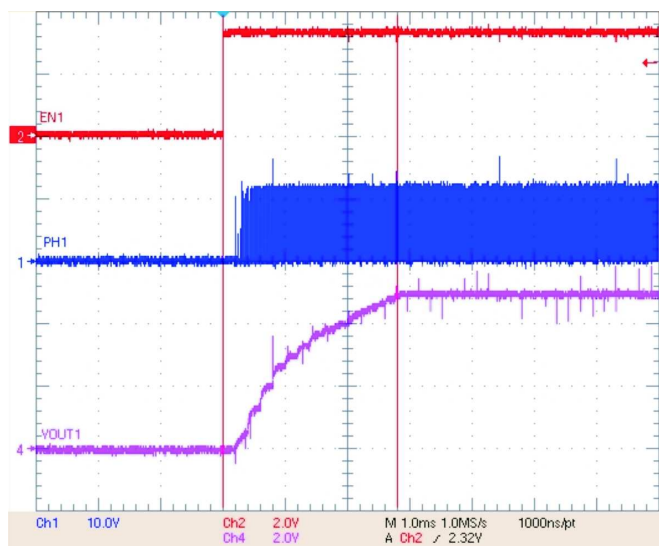


Figure 26. VBUCK 1 Power ON Delay From Enable Going High, $\Delta t = 2.8 \text{ ms}$ ($I_{Load} = 1.3 \text{ A}$)

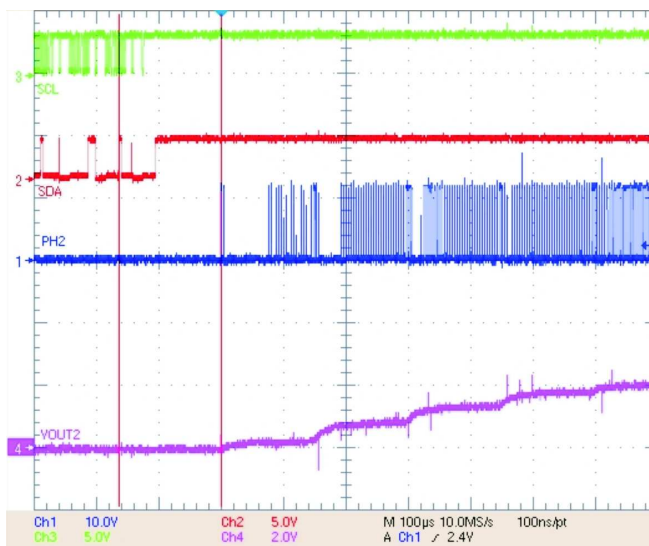


Figure 27. VBUCK 2 Turn ON Delay From I2C Enable Bit Going High, $\Delta t = 164 \mu s$

TYPICAL CHARACTERISTICS (continued)

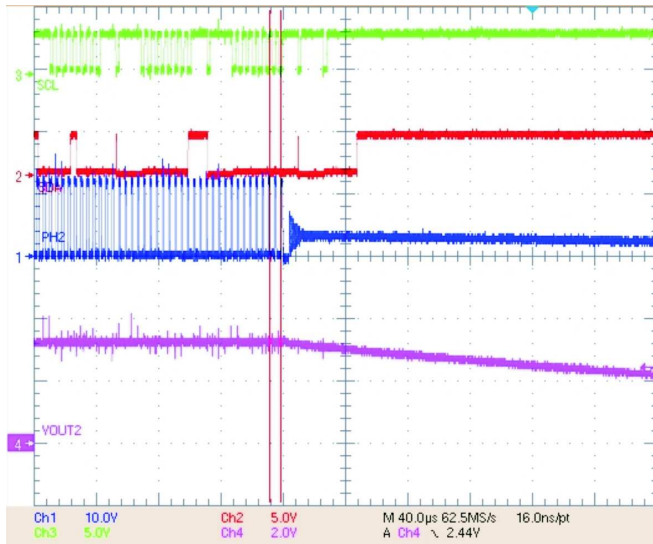


Figure 28. VBUCK 2 Turn OFF Delay From I2C Enable Bit Going Low, $\Delta t = 7.2 \mu s$

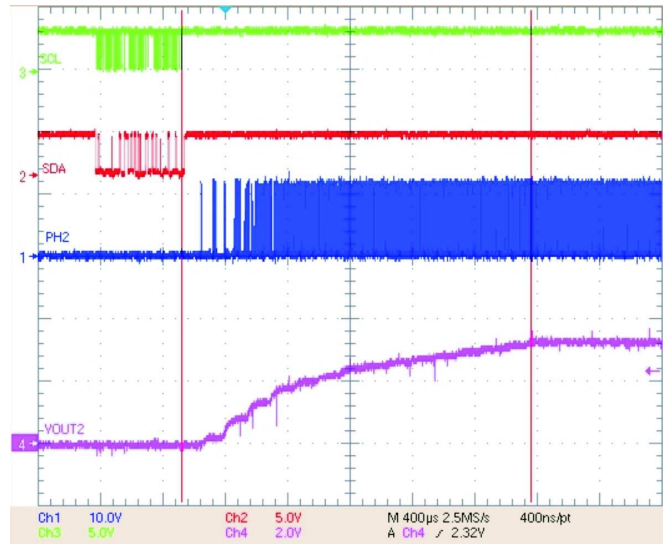


Figure 29. VBUCK 2 Power ON Delay From I2C Enable Bit Going High, $\Delta t = 2.24 ms$

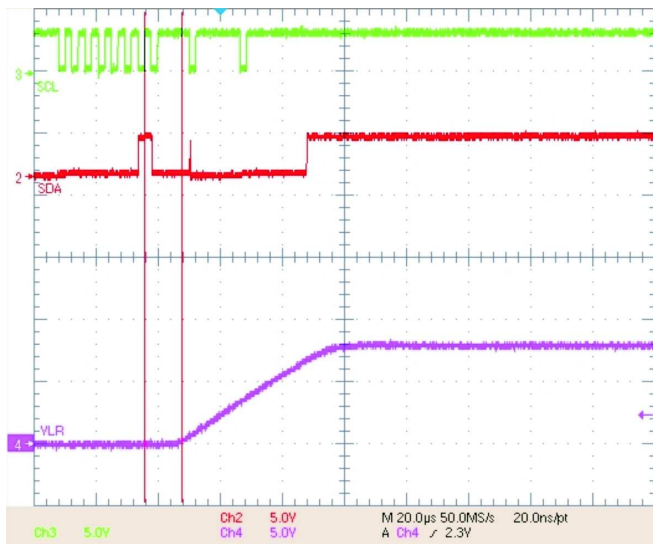


Figure 30. Linear Regulator (VLR) Turn ON Delay From I2C Enable Bit Going High, $\Delta t = 12 \mu s$

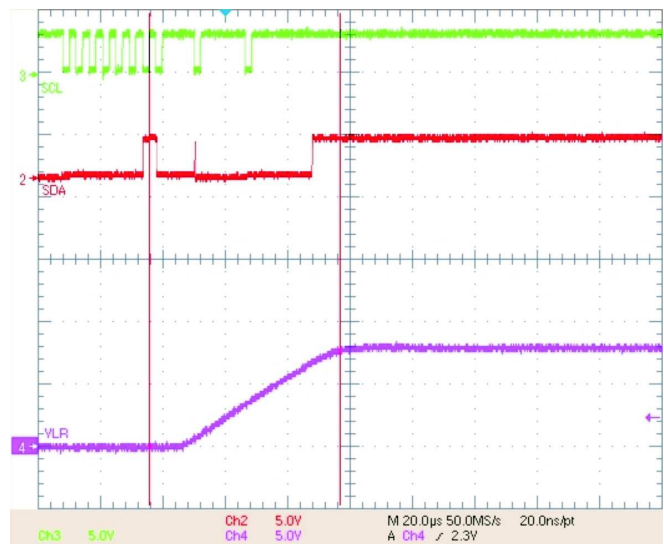


Figure 31. Linear Regulator (VLR) Power ON Delay From I2C Enable Bit Going High, $\Delta t = 61.2 \mu s$

TYPICAL CHARACTERISTICS (continued)

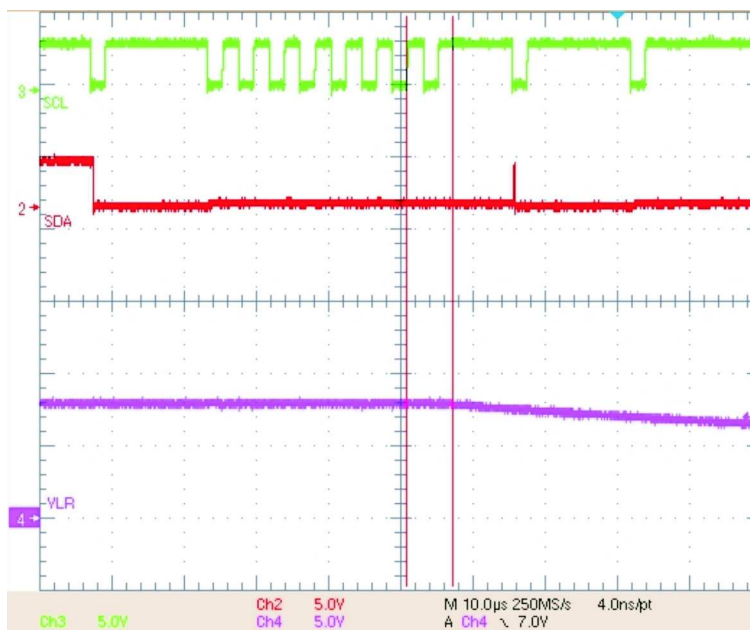


Figure 32. Linear Regulator (VLR) Turn OFF Delay From I2C Enable Bit Going Low, $\Delta t = 6.4 \mu s$

DEVICE INFORMATION

Overview

The TPS43331 is a combination of two switched mode synchronous step down controllers and two linearly regulated power supplies. There is also a protected high side output, controlled by a discrete input to switch auxiliary input power to other devices in the system. The standby regulator VSTBY is enabled once the input power from the protected terminal of the battery supply is available to the device. The standby regulator consumes less than 75 μA with less than 100 μA of load current on the regulated output terminal (VSTBY). In this condition the device is operating in the low power mode and current consumption from the input voltage source is minimized. The standby regulator on initial power up has a soft start function (CSLEW); the voltage ramp on the CSLEW is used to control the output voltage ramp rate of the standby regulator.

The second linearly regulated supply will be controlled through the serial communications. A digital bit assigned in a register controls if the VLR output is enabled (bit = 1) or disabled (bit = 0). This regulator is powered from either protected battery input or regulated voltage source. Both linearly regulated supplies can be programmed to a specified output voltage range based on feedback threshold setting on their respective sense terminals (VSTBYS and VLRS).

The two switch-mode synchronous step down controllers are configured to drive external NMOS power switches, and control the energy in the inductor by limiting the current using a resistor current sense feedback. The output voltage is regulated using external resistor feedback network. The regulated output voltage can be programmed to a specified range using different feedback thresholds at the VFB(x) terminal. The switch mode step down controller channel 1 is enabled when the active mode terminal EN is set high (logic 1). The second switch mode controller channel 2 is activated using the serial communications interface. Both switch mode configuration have dead time implementation to prevent simultaneous conduction during the switching phase. This is achieved by monitoring the voltage on the phase node to control gate drive sequencing. To minimize ripple current on the input line the two buck regulators are switched 180° out of phase. In addition, the SYNCH pin can be used to alter the switching frequency of both regulators and synchronize it to an external clock operating between 150 kHz and 400 kHz. Although the switching is now synchronous with the external clock, both regulators always operate 180° out of phase with respect to each other. During initial power up the switch mode regulator has a soft start function based on the internal oscillator and independent of the external clock signal on the synchronization input (SYNCH).

The high side switch output is powered from battery and has internal reverse blocking to prevent conduction when the power input line is bias negative with respect to high side driver output terminal. This output is current limited in the event of a short to ground condition. The output is controlled through serial communications, a single bit setting with the default being output OFF state.

The voltage supervisor circuitry monitors the standby voltage output and activates the reset line (pulls $\overline{\text{RST}}$ low) if the regulated output voltage is below low voltage threshold. There is a power good delay timer function (PGDLY) which allows the output voltage to stabilize before the $\overline{\text{RST}}$ line is de-asserted. This delay time can be programmed externally using a capacitor. The second voltage supervisor monitors the scaled value of the input voltage source sensed on the LVWIN terminal. If the voltage sensed at this node is below the internal threshold setting, the voltage warning output terminal ($\overline{\text{VBATW}}$) is pulled low. Alternatively if the VBAT input is above an over-voltage set point (27V to 31V), the outputs are disabled and voltage warning output terminal ($\overline{\text{VBATW}}$) is pulled low.

The serial communications is using the inter-IC communications (I2C) interface bus. The maximum frequency of operation is 400-kbaud, and a chip identifier terminal (I2CID) sets the address for communications.

Thermal sensing and protection is implemented for both the linear regulators and the high side driver outputs. Thermal shutdown on any one output will NOT directly disable any other output circuitry.

Detailed Description

Unregulated Battery Input Voltage (VBAT)

This input terminal will have an external input filter and voltage suppression above 40V for protection. The input is used to provide the operating voltage for the high side driver output, and used for sensing over voltage condition in the system. The over voltage detection circuitry has hysteresis for noise rejection.

Protected Unregulated Battery Input Voltage (VBATP)

This terminal provides the power source for internal circuitry to bias band-gap reference, oscillator and other circuitry in the device. The voltage on this terminal is used to sense for system under-voltage condition.

Low-Voltage Warning Input (LVWIN)

This input is used to detect low voltage condition. The input voltage source is scaled using external resistor network (programmable) to set the threshold for detection of low voltage condition. Once the input voltage is below the set threshold the low voltage warning output terminal is pulled low ($\overline{\text{VBATW}}$).

Voltage Warning Output ($\overline{\text{VBATW}}$)

This is an open drain output which is pulled up to supply with an external resistor. This output is asserted low when either of the following conditions is satisfied.

- Detection of low-voltage condition
- Detection of over-voltage condition

If the fault condition is removed the $\overline{\text{VBATW}}$ output is de-asserted (output goes high).

Low-Voltage Reset ($\overline{\text{RST}}$)

This output indicates if there is a low voltage on the standby regulator output (VSTBY). The output is de-asserted once the standby regulator achieves proper regulation and after the power delay timer has expired. This low voltage reset circuitry is functional for voltages above 0.5V on the standby regulator output terminal. Additionally the low voltage reset output will remain low if the standby regulator input voltage is in the under-voltage lock out mode.

Power-Good Delay Timer Input (PGDLY)

The capacitor on this terminal programs power good delay timer function. A current source on this pin charges an external capacitor once the standby regulator achieves proper regulation. Once the voltage on the capacitor exceeds the internal threshold the internal comparator will de-assert the reset output line. The external capacitor is discharged (reset) once the $\overline{\text{RST}}$ output is de-asserted, and so any subsequent power up sequence will start from zero time for the power good delay. The power good delay is not initiated as a result of external device asserting the reset output terminal.

Active Mode Enable Input (EN)

This input pin commands different modes of operation. When asserted low the device will enter low quiescent standby mode, with only the standby regulator ON. Once the input is asserted high the device is in active mode and regulator output control is achieved by discrete inputs and serial communications. The input is TTL-compatible with hysteresis for noise rejection. There is an internal pull down to guarantee a default state of standby mode.

Slew Rate Control Capacitor Input (CSLEW)

This pin provides the soft-start function for an internal reference used by the standby linear voltage regulator. An internal current source will charge an external capacitor to produce a linear voltage ramp at start up for the internal reference. This will be used to limit the slew rate of the output voltage of the standby regulator. An internal low side switch is used to discharge the capacitor in accordance with the operating mode requirements for slew rate control.

Soft start time must be greater than $dt_{ss} > 2\pi (LC)^{1/2}$

$C = dt \cdot I / dv$, where $dv = 1.2 \text{ V}$ and $I = 1.6 \mu\text{A}$ to $2.4 \mu\text{A}$ range, $dt > 2\pi (LC)^{1/2}$

Charge Pump Capacitor Input (VCP)

This pin has an external capacitor to provide storage for an internal charge pump.

Power Ground (PGND)

This pin is the power ground reference for the device. All switching nodes are referenced to this ground.

Analog Ground Reference (AGND)

This pin is reference ground for ALL non-power and non-switch-mode related ground termination inside the device.

Inter-IC Communications Interface (I2CID)

The serial communications interface is a 7-bit address for controlling the switch mode controller 2 (VBUCK 2), linear regulator (VLR) and high side driver output (HSD). There are two lines SCL and SDA to control the communications between the master and the slave. An I2CID terminal is used to address the IC in a system where multiple IC’s may be implemented. The SDA terminal has an internal FET switch to pull the SDA low as an acknowledgement signal back to the main controller. An active high allows access to the register.

Clock Input (SCL)

This is an input pin for a clock signal input from the master control. The clock signal is used to synchronize the data communications between the master device and the slave (TPS43331). The input signal will be TTL-compatible with hysteresis for noise rejection.

Data Line (SDA)

The pin is a data line communications between the master and slave device. The input signal is TTL-compatible with hysteresis for noise rejection. An internal pull down driver will provide an acknowledgement signal back to the master controller.

Interface Chip Identifier (I2CID)

The pin is used as a chip identification input for the I2C interface between the master and the slave device. The input signal is TTL-compatible with hysteresis for noise rejection. The state of the input signal is reflected in the I2C chip address byte 0. The value of the signal on this terminal is latched on a POR condition. A low leakage internal pull-down is implemented to ensure the default state is zero.

The IC requires a three-byte access from the microcontroller (Chip address, Register address and data)

Register Definition for I2C

Chip Address Byte

The IC supports two addresses by using bit 4 of the chip address byte and the I2CID input. The state of the I2CID input pin is read into bit 3 of the chip address byte (indicated by X in the frame above).

The valid chip addresses for writing to this IC is a \$0001000 (0x08) and \$0001100 (0x0C), since the LSB of the chip address byte is a read/write bit, these two addresses translate into hex values of 0x10 and 0x18 respectively.

Frame format requires two-byte access from the master controller.

- The first byte contains the address information
- The second byte contains the data information

Table 1. Frame Format

| | Chip address Byte 0 | | | | | | | | Register Address | | | | | | | | Data Byte 0 | | | | | | | | | | | | |
|---|---------------------|---|---|---|---|---|---|---|------------------|---|---|---|---|---|---|---|-------------|---|---|---|---|---|---|---|---|---|---|---|---|
| S | 0 | 0 | 0 | 1 | X | 0 | 0 | 0 | 0 | A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | A | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 | A | P |
| | MSB | | | | | | | | LSB | | | | | | | | | | | | | | | | | | | | |

The data format/transfer will be the following order:

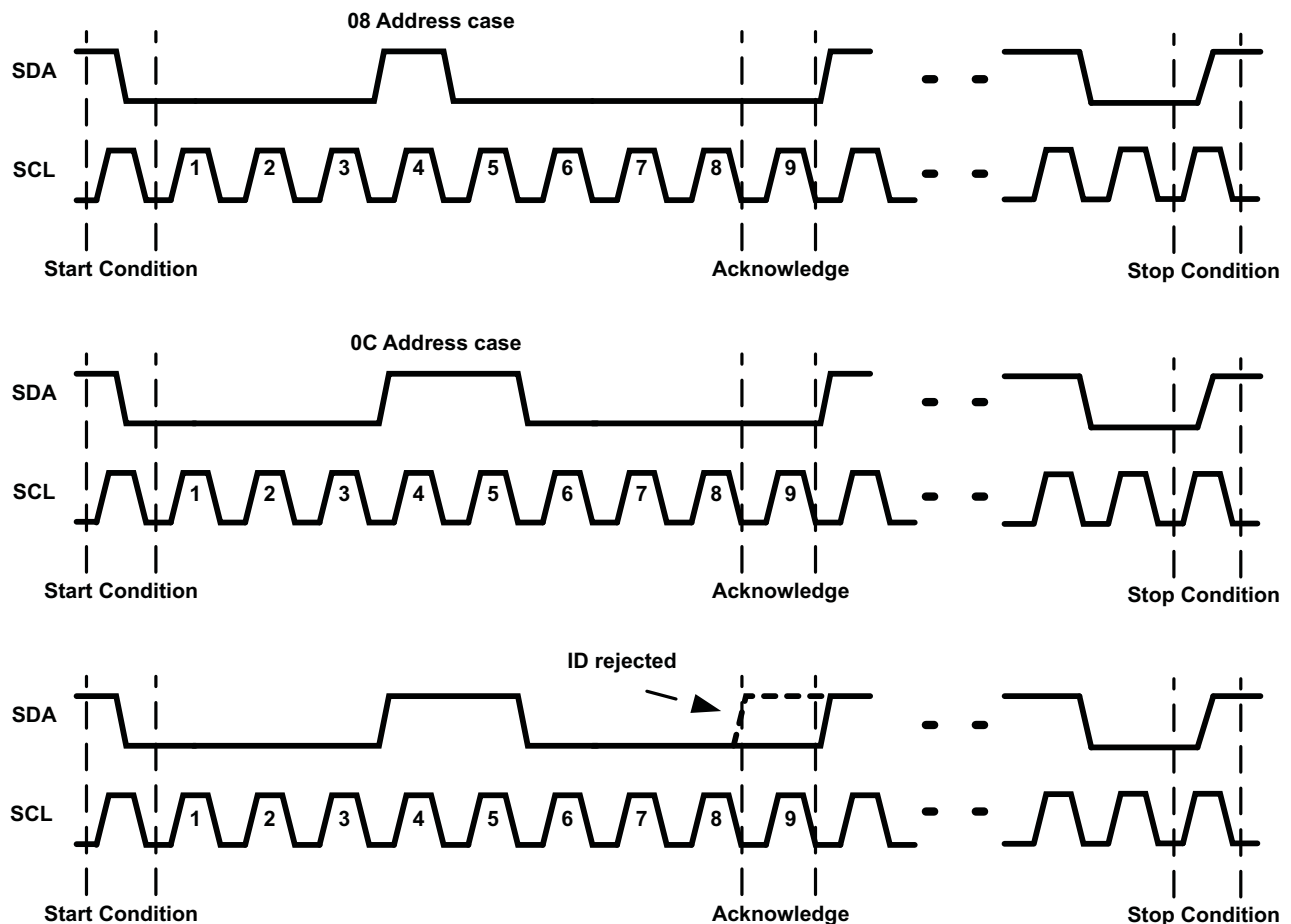
MSB first to LSB last; Bit 7 of each byte is the MSB. Bit 0 of each byte is the LSB.

Bit 0 (LSB) in the address byte defines the read/write bit; a value of 0 indicates a data write.

The bit marked "X" in the address byte indicates the state of the I2CID input.

Transmission format:

1. The data transfer begins with a start signal (S), where the SDA transitions from high to low while SCL is high (see Figure 33)
2. After 8 bits are transmitted and detected the IC (TPS43331) will send an acknowledge pulse (A) to the master.
3. After each successive writes of 8 bits, the IC sends an acknowledge pulse to the master
4. The message communications is completed (stop condition P) when SDA transitions from low to high while SCL is high.



Note: Bit #8 is used for read or write options, with
 Bit 8 = 1 is read
 Bit 8 = 0 is write

Figure 33. I2C Communications

If a transfer is interrupted by a stop condition, the partial byte transmission shall not be latched. Only the prior messages transmitted and acknowledged are latched.

Table 2. Data register bit field definition

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|-------|------|-------|
| Definition | X | X | X | X | X | SW2EN | LREN | HSDEN |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

SW2EN default state = 0, switcher 2 is OFF (disabled)

SW2EN = 1, switcher 2 ON (enabled)

LREN default state = 0, the switched linear regulator (VLR) is OFF

LREN = 1, the switched linear regulator (VLR) is ON

HSDEN default state = 0, the high side switch is OFF

HSDEN = 1, the high side switch is ON

Switch Mode Regulators

There are two switch-mode controllers when configured with external power switches form the buck (step-down) regulators. One switch-mode regulator is controlled by an enable input control (EN) and the second is controlled by a bit using the serial communications interface.

Short-circuit detection is achieved by current sensed through an external sense resistor in series with the inductor. The current limit is applied on a cycle-by cycle basis. Once over-current is detected the output is disabled for the remainder of the cycle, and is enabled on the next clock edge.

Upper FET Gate Drive Outputs (VGT1 and VGT2)

These outputs are the gate drive signals for the external high side FETs for each switch-mode controller.

The output voltage is clamped to prevent excessive gate drive voltage to the external MOS devices. These outputs are a push-pull configuration and are current limited for charging a capacitive load.

Lower FET gate driver outputs (VGB1 and VGB2)

These outputs are the gate drive signals for the external low side FETs for each switch-mode controller. The switching signal is 180 degrees out of phase with the upper gate drive signals for each controller. The lower gate drive controls the FET for synchronous switching. These output signals are clamped to prevent excessive gate voltage to the external MOS devices. These outputs are a push-pull configuration and are current limited for charging a capacitive load.

Bootstrap capacitor input (CBS1 and CBS2)

These terminals are the bootstrap capacitor inputs for switcher 1 and switcher 2 respectively. These capacitors act as the voltage supply for the upper gate drive circuitry. The capacitors are re-charged on every low side synchronous switching action. In the case of 100% duty cycle for the upper FET, the device will automatically reduce the duty cycle to approximately 95% on every fifth cycle to allow these capacitors to re-charge.

Phase Reference for High-Side Bootstrap Supply (PH1 and PH2)

These terminals provide a floating voltage reference for the high-side FET gate drive circuitry for switcher 1 and switcher 2 respectively. These nodes are used to monitor the status of the upper external FETs, and allow switching of the lower external FETs without shorting the supply.

Current Sense High-Side (ISH1 and ISH2)

These are the high-side current sense resistor node inputs for switcher 1 and switcher 2 respectively. The common mode range of the combined high-side and low-side current sense inputs supports the entire output voltage range.

Current Sense Low-Side (ISLO1 and ISLO2)

These are the low-side current sense resistor node inputs for switcher 1 and switcher 2 respectively. The common mode range of the combined high-side and low-side current sense inputs supports the entire output voltage range.

Regulated Output Sense Voltage Feedback (VFB1 and VFB2)

These are the input pins for the voltage output feedback signals for switcher 1 and switcher 2 respectively. The external resistor network setting on these pins programs the desired regulated output voltages for each switch-mode converter.

Feedback Compensation Input (VCMP1 and VCMP2)

These are the input pins for the converter compensation feedback for switcher 1 and switcher 2 respectively.

Synchronization Input (SYNCH)

This is an input pin for feeding an external clock to synchronize the switching frequency of both switch-mode regulators. The IC will detect a small number of edges (2 to 5) prior to recognizing a valid external clock input signal and synchronizing the internal operation with an external clock input. The regulator operates with an external input clock signal until a low voltage reset or a command to go into a sleep mode.

Standby Linear Regulator Input (VINSB)

This is the input pin for the operating voltage of the standby regulator. The voltage source for the standby regulator requires an external blocking diode in the module for reverse supply conditions. This input pin requires the necessary filtering and protection against positive and negative transients to prevent damage to the IC (see application schematic)

Standby Regulator Output (VSTBY)

This is the regulated output of the standby regulator, and derives the voltage source from the VINSB terminal. The regulator has an internal linear current limit for protection against shorts to ground. The output voltage will recover to the specified range once the fault condition is removed. This output remains within the tolerance of the specification during positive transient events on the input. An under-shoot condition during any load transient event will not assert a reset condition on the \overline{RST} output, proving the load transient is within the specified range.

Once the regulator drops-out due to low input voltage on VINSB, the output tracks the input voltage minus the saturation voltage of the pass device. The device will enter thermal shut down if the local die temperature exceeds the thermal shut-down threshold. The thermal shut-down has hysteresis such that the output enables once the local die temperature falls below the disable threshold. If the output falls below the specified low voltage reset, the IC will notify this condition by asserting the rest line \overline{RST} low.

Standby Regulator Sense Voltage (VSTBYS)

This pin is used to program the regulated output voltage to a range specified in the parametric table. An external resistor network is used to ratio the output voltage and fed back into the VSTBYS pin.

Switched Linear Regulator Input (VINLR)

This is the input pin for the operating voltage of the switched linear regulator. The voltage source for this regulator requires an external blocking diode in the module for reverse supply conditions. This input pin requires the necessary filtering and protection against positive and negative transients to prevent damage to the IC (see application schematic).

Switched Linear Regulator Output (VLR)

This is the regulated output of the switched linear regulator, and derives the voltage source from the VINLR terminal. The regulator has an internal linear current limit for protection against shorts to ground. The output voltage will recover to the specified range, once the fault condition is removed. This output remains within the tolerance of the specification during load transient event on the output line. The output is disabled in the event VBAT exceeding the over-voltage shut-down threshold VOVS. The output will be enabled once the VBAT input voltage falls below the internal set threshold (with hysteresis).

Once the regulator drops-out due to low input voltage on VINLR, the output tracks the input voltage minus the saturation voltage of the pass device. The device will enter thermal shut down if the local die temperature exceeds the thermal shut-down threshold. The thermal shut-down has hysteresis such that the output enables once the local die temperature falls below the disable threshold.

Switched Linear Regulator Sense Voltage (VLRS)

This pin is used to program the regulated output voltage to a range specified in the parametric table. An external resistor network is used to ratio the output voltage and fed back into the VLRS pin.

High-Side Driver Output (HSD)

This pin is the output of the high side driver (switched input voltage). The output is enabled through a bit in the I2C data register. If the voltage on the VBAT supply exceed the over-voltage shut-down threshold VOVS this output is disabled. Upon return from the fault condition the output recovers to the state set by the enable bit (HSDEN) in I2C data register without any intervention from the system. The output is stable during any soft-start conditions or specified load transients. This output is protected against:

- Short to module supply
- Short to module ground
- Short through the load to -1 V
- Unpowered short to module supply
- Reverse supply (-13 V)

The output has short circuit protection with a linear current limit and thermal shutdown with hysteresis.

If the local die temperature exceeds the thermal shutdown detection threshold this output is disabled. This output is enabled once the local die temperature falls below the detection threshold with hysteresis providing the HSDEN bit is set.

The invoking of thermal shut down on this output does not directly affect any other outputs or circuitry in the IC. The operation of the switch is not affected during the re-circulation of an inductive load providing the negative voltage applied to this pin is within the specified limits

Multiple Power Supply Configuration for Vehicle Audio Applications

[Figure 34](#) shows an example of configuration for car audio power supply application. Other combinations are possible dependent on the system requirements

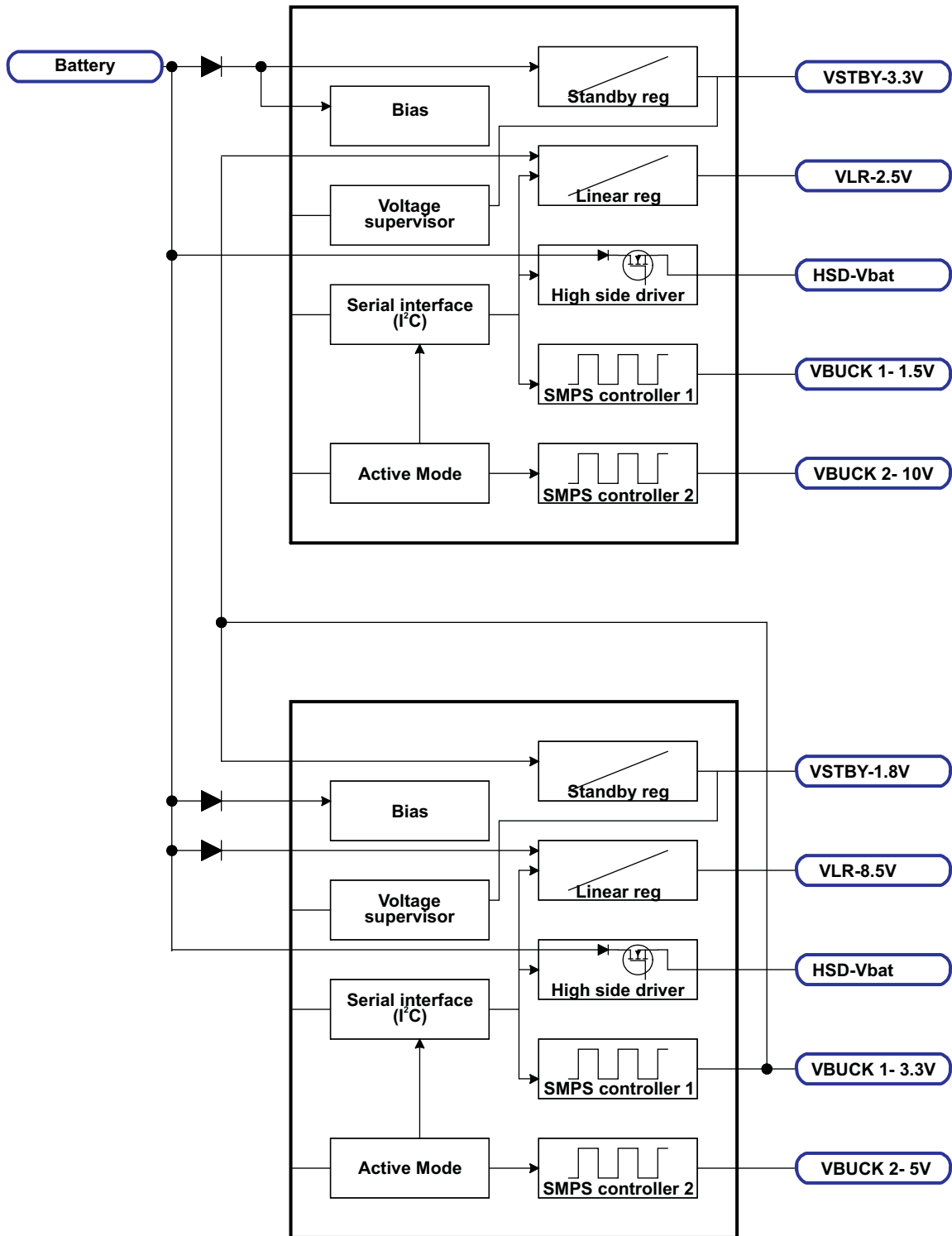


Figure 34. Multiple Power Supply for Vehicle Audio

APPLICATION INFORMATION

Type II Compensation

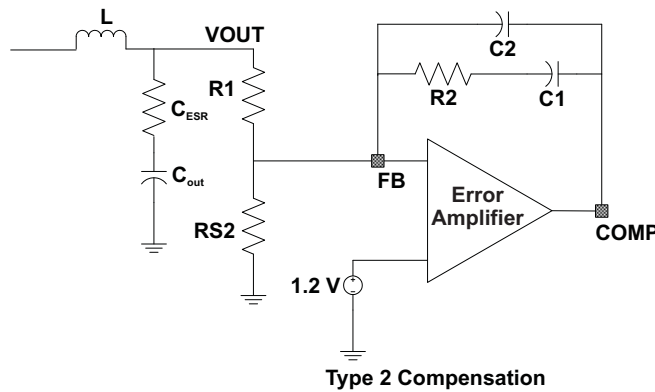


Figure 35. Type II Compensation

Double pole frequency response due to the LC output filter The LC output filter gives a "Double Pole" which has a -180 degree phase shift

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_o}} \text{ (Hz)} \tag{1}$$

The ESR of the output capacitor C gives a zero that has a 90 degree phase shift

$$f_{ESR} = \frac{1}{2\pi \times C_o \times ESR} \text{ (Hz)} \tag{2}$$

R1 and RS2 are chosen biased on Vout desired

$$V_{OUT} = V_{ref} \times \frac{R1 + RS2}{RS2} \text{ (Volts)} \tag{3}$$

Where

$$V_{ref} = 1 \text{ V}$$

Resistor values

Select RS2 = 10 kΩ

$$R1 = \frac{RS2(V_{OUT} - V_{ref})}{V_{ref}} \tag{4}$$

$$R1 = \frac{10000(V_{OUT} - 1.0)}{1.0} \tag{5}$$

$$R2 = \frac{f_c \times V_{ramp} \times R1}{V_{IN} \times f_{LC}} \text{ (Ohms)} \tag{6}$$

Where

$$V_{ramp} = 1.8 \text{ V}, V_{IN} = \text{typical input operating voltage}$$

$$f_c = f_{sw} \times 0.1 \text{ (the cut-off freq, when the gain is 1 is called the unity gain frequency).}$$

The f_c is typically 1/5 to 1/10 of the switching frequency

PWM modulator gain K

$$K = \frac{V_{in}}{V_{ramp}} \tag{7}$$

Gain of Amplifier

$$A_V = \frac{R_2}{R_1} \tag{8}$$

$$f_z = \frac{f_c}{K} \text{ (Hz)} \tag{9}$$

$$f_p = f_c \times K \text{ (Hz)} \tag{10}$$

$$C_1 = \frac{10}{2\pi \times R_2 \times f_{LC}} \tag{11}$$

$$C_2 = \frac{C_1}{(\pi \times R_2 \times C_1 \times f_{SW}) - 1} \tag{12}$$

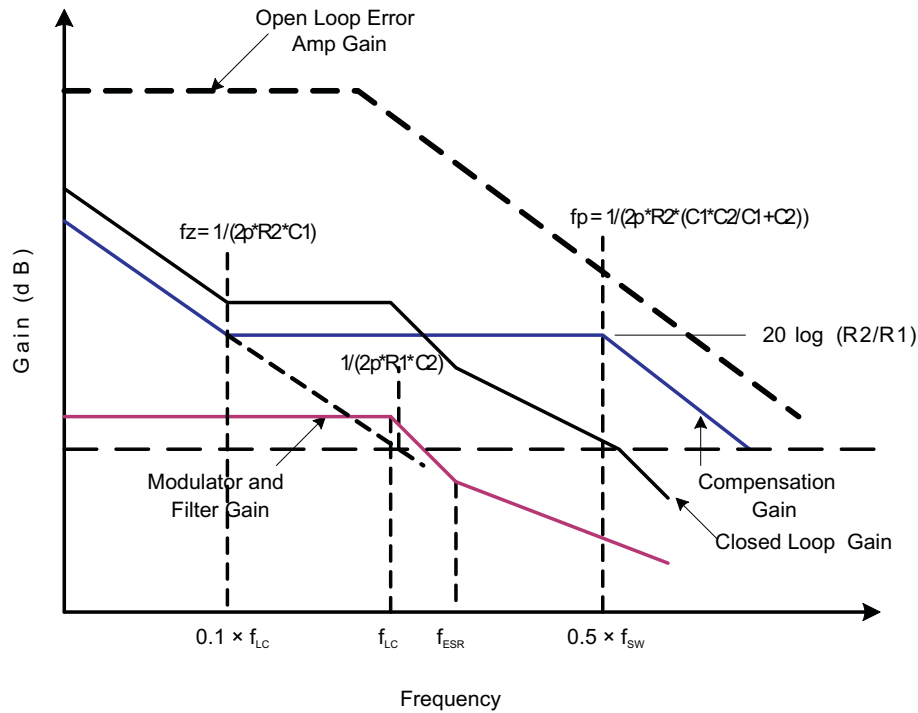
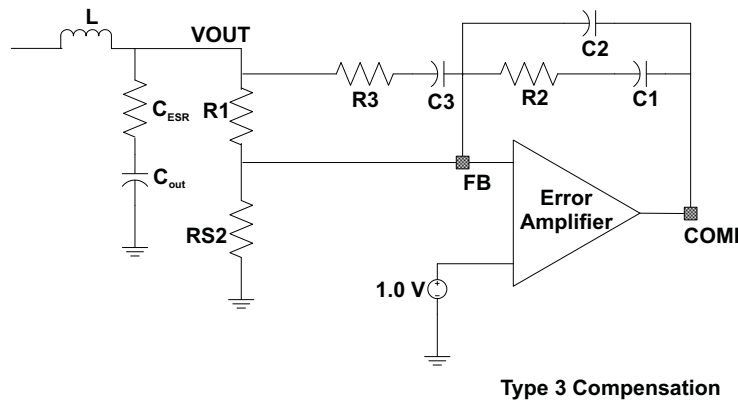


Figure 36. Type II Bode Plots

Type III Compensation



Type 3 Compensation

Figure 37. Type III Compensation

$f_c = f_{sw} \times 0.1$ (the cut-off frequency when the gain is 1 is called the unity gain frequency).

The f_c is typically 1/5 to 1/10 of the switching frequency double pole frequency response due to the LC output filter.

The LC output filter gives a "Double Pole" which has a -180° phase shift.

$$f_{LC} = \frac{1}{2\pi\sqrt{LC_{out}}} \text{ (Hz)} \quad (13)$$

The ESR of the output capacitor C gives a zero that has a 90 degree phase shift

$$f_{ESR} = \frac{1}{2\pi \times C_{out} \times ESR} \text{ (Hz)} \quad (14)$$

$$V_{out} = \frac{V_{ref} \times (R1 + RS2)}{RS2} \text{ (Volts)} \quad (15)$$

Where

$$V_{ref} = 1 \text{ V}$$

PWM modulator gain K

$$K = \frac{V_{in}}{V_{ramp}} \quad (16)$$

Where

$$V_{ramp} = 1.8 \text{ V}$$

V_{in} = typical input operating voltage

Gain of amplifier

$$A_v = \frac{R2 \times (R1 + R3)}{R1 \times R3} \quad (17)$$

$$f_{P1} = \frac{C1 + C2}{2\pi \times R2 \times (C1 \times C2)} \text{ (Hz)} \quad (18)$$

$$f_{P2} = \frac{1}{2\pi \times R3 \times C3} \text{ (Hz)} \quad (19)$$

$$f_{Z1} = \frac{1}{2\pi \times R2 \times C1} \text{ (Hz)} \quad (20)$$

$$f_{Z2} = \frac{1}{2\pi \times (R1 + R3) \times C3} \text{ (Hz)} \quad (21)$$

Guidelines for compensation components

Make the two zeroes close to the double pole (LC); e.g., $f_{Z1} \approx f_{Z2} \approx 1/2\pi(LC_{OUT})^{1/2}$

1. Make first zero below the filter double pole (approx 50% to 75% of f_{LC})
2. Make second zero at filter double pole (f_{LC})

Make the two poles above the cross-over frequency f_c .

1. Make first pole at the ESR frequency (f_{ESR})
2. Make the second pole at 0.5 the switching frequency ($0.5 \times f_{SW}$)

Resistor values

Select $RS2 = 10k$

$$R1 = \frac{RS2 \times (V_{out} - V_{ref})}{V_{ref}} \text{ (Ohms)} \quad (22)$$

$$R1 = \frac{10000 \times (V_{out} - 1.0)}{1.0} \text{ (Ohms)} \quad (23)$$

$$R2 = \frac{f_c \times V_{ramp} \times R1}{f_{LC} \times V_{in}} \text{ (Ohms)} \quad (24)$$

Calculate C1 based on placing a zero at 50% to 75% of the output filter double pole frequency.

$$C1 = \frac{1}{\pi \times R2 \times f_{LC}} \text{ (Farads)} \tag{25}$$

Calculate C2 by placing the first pole at the ESR zero frequency.

$$C2 = \frac{C1}{(2\pi \times R2 \times C1 \times f_{ESR}) - 1} \text{ (Farads)} \tag{26}$$

Set the second pole at 0.5 the switching frequency and also set the second zero at the output filter double pole frequency.

$$R3 = \frac{R1}{\left(\frac{f_{SW}}{2} \times \frac{1}{f_{LC}}\right) - 1} \text{ (Ohms)} \tag{27}$$

$$C3 = \frac{1}{\pi \times R3 \times f_{SW}} \text{ (Farads)} \tag{28}$$

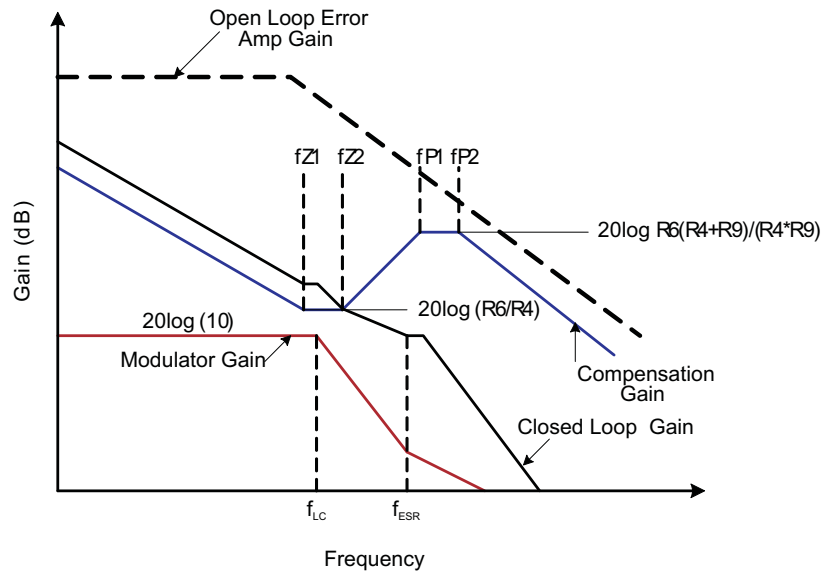


Figure 38. Type III Bode Plots

Component Calculations

Buck mode; (VBUCK 1, VBUCK 2)

Select inductor ripple current ΔI_L desired: for example $\Delta I_L = I_{Ripple} = 0.4 \times I_{OUT(max)}$

Where, $I_{OUT(max)}$ = Maximum output current

Typical inductor ripple current is between 20% to 40% of maximum output current

Calculate inductor L:

$$L = \frac{(V_{in(max)} - V_{out})V_{out}}{f_{SW} \times I_{ripple} \times V_{in(max)}} \text{ (Henries)} \tag{29}$$

Where

f_{SW} is the regulator's switching frequency

I_{Ripple} = Allowable ripple current in the inductor, 20% to 40% of maximum $I_{OUT(max)}$

The RMS and peak current flowing in Inductor is

$$I_{L(rms)} = \sqrt{I_{out}^2 + \frac{I_{ripple}^2}{12}} \text{ (Amps)} \quad (30)$$

Inductor peak current:

$$I_{L(peak)} = I_{out} + \frac{I_{ripple}}{2} \text{ (Amps)} \quad (31)$$

Output voltage ripple:

$$\Delta V_{out} = \Delta L \left(ESR + \frac{1}{8 \times f_{SW} \times C_{out}} \right) \text{ (Volts p-p)} \quad (32)$$

Usually the first term is dominant. The output ripple voltage is typically within the tolerance of the output specification.

Output capacitor

$$C_{out} = \frac{L(I_{out(max)}^2 - I_{out(min)}^2)}{V_{out(max)}^2 - V_{out(min)}^2} \text{ (Farads)} \quad (33)$$

Where

$I_{OUT(max)}$ is max output current

$I_{OUT(min)}$ is min output current

The difference between the output current max to min is the worst case load step in the system

$V_{OUT(max)}$ is max tolerance of regulated output voltage

$V_{OUT(min)}$ is the min tolerance of regulated output voltage

Power Dissipation

The power dissipation is largely dependent on the MOSFET driver current and input voltage. The drive current is proportional to the total gate charge of the external MOSFET.

$$P_{Gate} = Q_g \times V_{DR} \times f_{SW} \text{ (Watts)} \quad (34)$$

Assuming both high and low side MOSFETs are identical in a synchronous configuration, the total power dissipation is

$$P_{controller1} = 2 \times Q_g \times f_{SW} \times V_{IN} \text{ (Watts) per channel} \quad (35)$$

Dual Channel Controller the total power dissipation is

$$P_{controller 1 \& 2} = 4 \times Q_g \times f_{SW} \times V_{IN} \text{ (Watts)} \quad (36)$$

IC power consumption

$$P_{IC} = I_q \times V_{IN} \text{ (Watts)} \quad (37)$$

Standby Linear Regulator

$$P_{STBY_REG} = (V_{INSB} - V_{STBY}) \times I_{VSTBY} \text{ (Watts)} \quad (38)$$

Linear Regulator

$$P_{LIN_REG} = (V_{INLR} - V_{LR}) \times I_{VLR} \text{ (Watts)} \quad (39)$$

High side driver

$$P_{HSD} = I_{HSD} \times 0.6 \text{ (Watts) for up to 300 mA output current} \quad (40)$$

$$P_{Total} = P_{controller 1 \& 2} + P_{STBY_REG} + P_{LIN_REG} + P_{IC} + P_{HSD} \text{ (Watts)} \quad (41)$$

Design Guide – Step by Step Design Procedure

The following are details of a switching regulator design using the following requirements.

Table 3. Design Requirements

| | |
|--|------------------------------|
| Input voltage minimum $V_{in(min)}$ | 8 V |
| Input voltage maximum $V_{in(max)}$ | 26 V |
| Input voltage minimum $V_{in(typ)}$ | 14 V |
| Output voltage buck regulator 1 - VBUCK 1 | Min = 4.75 V, Mmax = 5.25 V |
| Output voltage buck regulator 2 - VBUCK 2 | Min = 3.135 V, Max = 3.465 V |
| Converter switching frequency, f_{sw} | 250 kHz |
| Maximum output current on buck regulator 1 - VBUCK 1 | 2.0 A |
| Maximum output current on buck regulator 2 - VBUCK 2 | 1.5 A |
| Maximum ripple current I_{ripple} | $0.2 \cdot I_{out}$ |

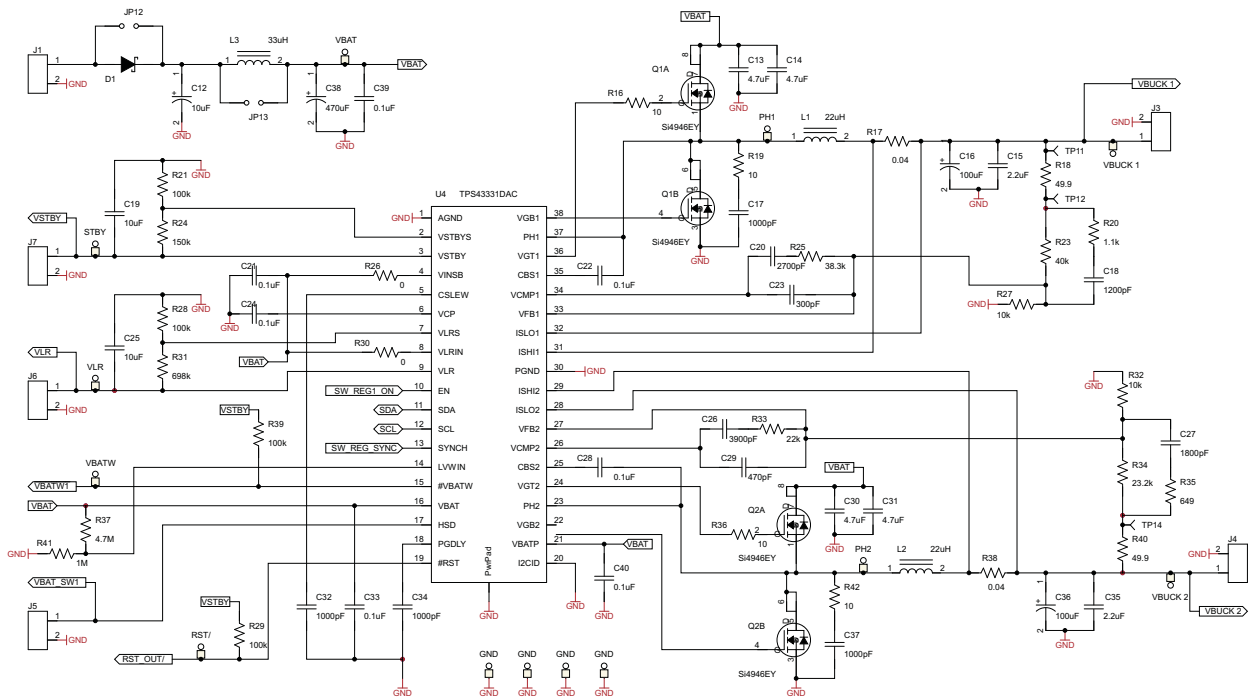


Figure 39. Design Circuit

Assume Type III Compensation network for each buck regulator.

Buck Regulator 1 (VBUCK 1)

STEP 1. Calculate the inductor value

Using Equation 29, to find the Inductor value, assume inductor ripple current of 0.8 A.

$$L = \frac{(V_{in(max)} - V_{out})V_{out}}{f_{sw} \times I_{ripple} \times V_{in(max)}} = \frac{(26 - 5)5}{250 \times 10^3 \times 0.8 \times 26} = 20.2 \times 10^{-6} \text{ (Henries)} \tag{42}$$

L = 20.2 µH, use a value of 22 µH

STEP 2. Inductor peak current

Using Equation 31, the peak inductor current.

$$I_{L(\text{peak})} = I_{\text{out}} + \frac{I_{\text{ripple}}}{2} = 2 + \frac{0.8}{2} = 2.4(\text{Amps}) \quad (43)$$

$$I_{L\text{-peak}} = 2.4 \text{ A}$$

STEP 3. Calculating the output capacitance (Co)

Using Equation 33, the output capacitance

$$C_{\text{out}} = \frac{L(I_{\text{out}(\text{max})}^2 - I_{\text{out}(\text{min})}^2)}{V_{\text{out}(\text{max})}^2 - V_{\text{out}(\text{min})}^2} = \frac{22 \times 10^{-6} (2^2 - (20 \times 10^{-3})^2)}{5.15^2 - 4.85^2} = 29.3 \times 10^{-6} (\text{Farads}) \quad (44)$$

Assume a tolerance of $\pm 3\%$ to allow for some margin, $I_{\text{out min}}$ current of 20ma. Using Equation 34, the output capacitor $C_{\text{out}(\text{min})} = 29.3 \mu\text{F}$, with temperature variations and manufacture tolerance choose a value of 68 μF or greater.

$C_{\text{OUT}} = 100 \mu\text{F}$ for this design

STEP 4. Calculating loop compensation values

Using Equation 13 to determine the "double pole"

$$f_{\text{LC}} = \frac{1}{2\pi\sqrt{LC_{\text{out}}}} = \frac{1}{2 \times 3.142 \sqrt{22 \times 10^{-6} \times 100 \times 10^{-6}}} = 3990(\text{Hz}) \quad (45)$$

$$f_{\text{LC}} = 3.39 \text{ kHz}$$

Using Equation 14 to determine the zero due to the ESR of the output capacitor C_o with $\text{ESR} = 0.1 \Omega$

$$f_{\text{ESR}} = \frac{1}{2\pi \times C_{\text{out}} \times \text{ESR}} = \frac{1}{2 \times 3.142 \times 100 \times 10^{-6} \times 0.1} = 15.9 \times 10^3 (\text{Hz}) \quad (46)$$

$$f_{\text{ESR}} = 15.9 \text{ kHz}$$

$$f_c = 0.1 \times f_{\text{sw}} = 25 \text{ kHz}$$

Using Equation 23 and assuming $R27 = 10 \text{ k}$

$$R23 = \frac{10000 \times (V_{\text{out}} - 1)}{1} = \frac{10000 \times (5 - 1)}{1} = 40 \times 10^3 (\text{Ohms}) \quad (47)$$

$$R23 = 40 \text{ k}\Omega$$

Using Equation 24

$$R25 = \frac{f_c \times V_{\text{ramp}} \times R1}{f_{\text{LC}} \times V_{\text{IN}}} = \frac{25 \times 10^3 \times 1.8 \times 40 \times 10^3}{3.39 \times 10^3 \times 14} = 37900 (\text{Ohms}) \quad (48)$$

$$R25 = 37.9 \text{ k}\Omega, \text{ Choose } R25 = 38.3 \text{ k}\Omega$$

Using Equation 25

$$C20 = \frac{1}{\pi \times R2 \times f_{\text{LC}}} = \frac{1}{3.142 \times 38.3 \times 10^3 \times 3.39 \times 10^3} = 2450 \times 10^{-12} (\text{Farads}) \quad (49)$$

$$C20 = 2450 \text{ pF}, \text{ Choose } C20 = 2700 \text{ pF}$$

Using Equation 26

$$C23 = \frac{C1}{(2\pi \times R2 \times C1 \times f_{\text{ESR}})^{-1}} = \frac{2.7 \times 10^{-9}}{(2 \times 3.142 \times 38.3 \times 10^3 \times 2.7 \times 10^{-9} \times 15.9 \times 10^3)^{-1}} = 289 \times 10^{-12} (\text{Farads}) \quad (50)$$

$$C23 = 289 \text{ pF}, \text{ Choose } C23 = 300 \text{ pF}$$

Using Equation 27

$$R20 = \frac{R23}{\left(\frac{f_{\text{sw}}}{2} \times \frac{1}{f_{\text{LC}}}\right)^{-1}} = \frac{40 \times 10^3}{\left(\frac{250 \times 10^3}{2} \times \frac{1}{3.39 \times 10^3}\right)^{-1}} = 1.1 \times 10^3 (\text{Ohms}) \quad (51)$$

$$R20 = 1.12 \text{ k}\Omega, \text{ Choose } R20 = 1.1 \text{ k}\Omega$$

Using [Equation 28](#)

$$C_{18} = \frac{1}{\pi \times R3 \times f_{SW}} = \frac{1}{3.142 \times 1.1 \times 10^3 \times 250 \times 10^3} = 1.142 \times 10^{-9} \text{ (Farads)} \quad (52)$$

$C_{18} = 1142 \text{ pF}$, Choose $C_{18} = 1200 \text{ pF}$

Buck Regulator 2 (VBUCK 2)

Using the same method for calculating the component values for Buck Regulator 2, with the set output conditions, the following values are selected.

STEP 5. Calculate the inductor value

Using [Equation 29](#) to find the inductor value, assume Inductor ripple current of 0.3 A

$L = 19.2 \text{ } \mu\text{H}$, use a value of $22 \text{ } \mu\text{H}$

STEP 6. Inductor peak current

From [Equation 31](#), the peak inductor current

$$I_{L,pk} = 1.65 \text{ A}$$

STEP 7. Calculating the output capacitance (Co)

Assume a tolerance of $\pm 3\%$ to allow for some margin, IOUT min current of 20 mA. Using [Equation 33](#), the output capacitor

$C_{OUT(min)} = 32.7 \text{ } \mu\text{F}$, with temperature variations and manufacture tolerance choose a value of $100 \text{ } \mu\text{F}$ for this design.

$$C_{OUT} = 100 \text{ } \mu\text{F}$$

STEP 8. Calculating loop compensation values

Using [Equation 13](#) to determine the "double pole"

$$f_{LC} = 3.39 \text{ kHz}$$

Using [Equation 14](#), to determine the zero due to the ESR of the output capacitor C_O with $ESR = 0.1 \text{ } \Omega$

$$f_{ESR} = 15.9 \text{ kHz}$$

$$f_C = 0.1 \times f_{sw} = 25 \text{ kHz}$$

Using [Equation 23](#) and assuming $R32 = 10 \text{ k}\Omega$

$$R34 = 23 \text{ k}\Omega$$

Using [Equation 24](#)

$$R33 = 21.8 \text{ k}\Omega$$
, Choose $R33 = 22 \text{ k}\Omega$

Using [Equation 25](#)

$$C26 = 4260 \text{ pF}$$
, Choose $C26 = 3900 \text{ pF}$

Using [Equation 26](#)

$$C29 = 515 \text{ pF}$$
, Choose $C29 = 470 \text{ pF}$

Using [Equation 27](#)

$$R35 = 642 \text{ } \Omega$$
, Choose $R35 = 649 \text{ } \Omega$

Using [Equation 28](#)

$$C27 = 1967 \text{ pF}$$
, Choose $C27 = 1800 \text{ pF}$

Power Dissipation Derating

The power dissipation curve (see [Figure 40](#)) is based on attachment of the exposed power pad to the printed circuit board with multi layer FR4. The data is based of JEDEC JESD 51-5 standard board with thermal via and high K profile. The user must review Texas Instruments TI Technical Brief (SLMA002) for recommended method of exposed pad attachment.

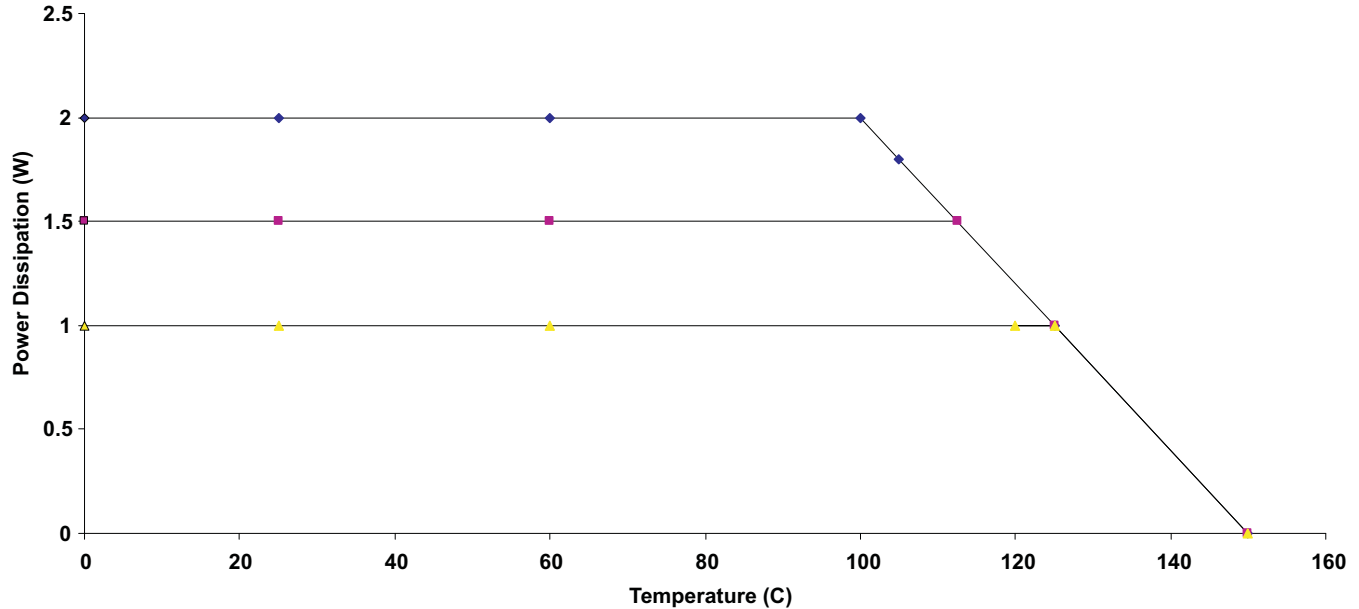


Figure 40. Power Dissipation Derating

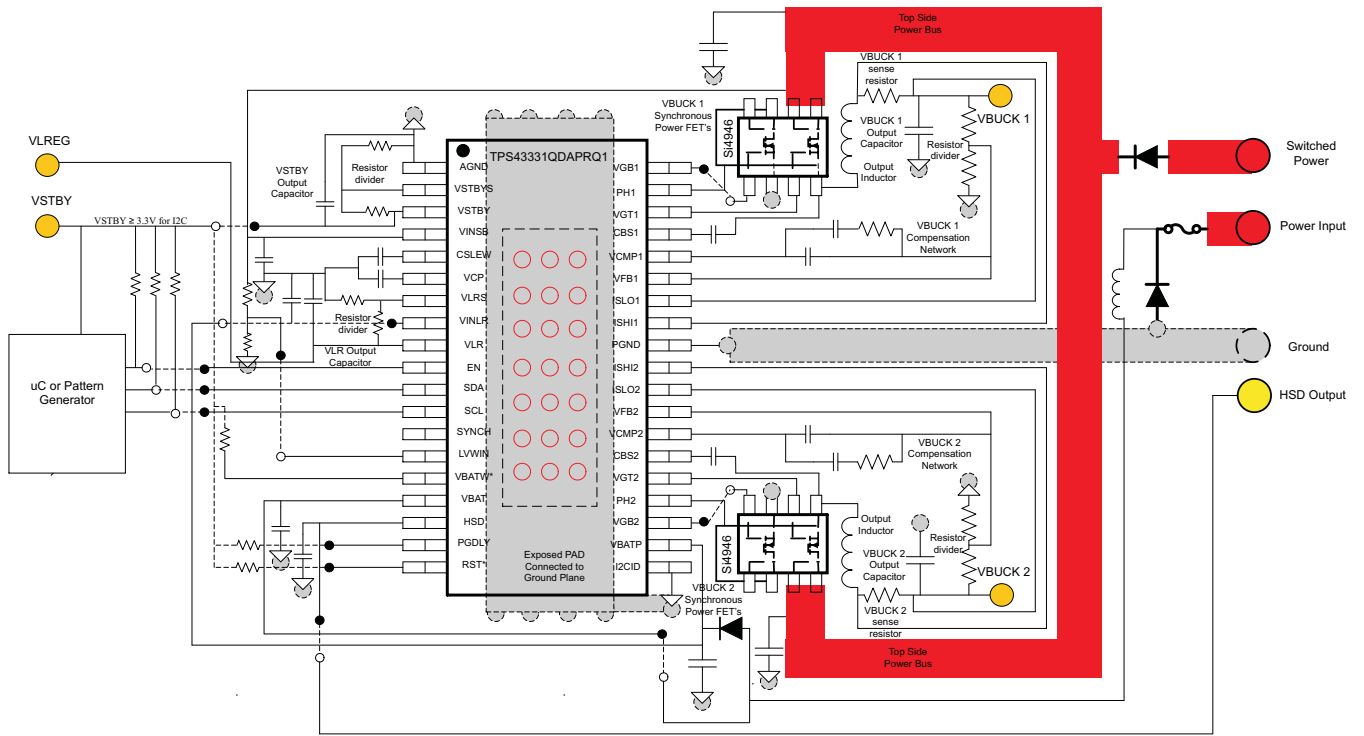
Grounding and Circuit Layout Considerations

The TPS43331 has two separate ground terminations (AGND and PGND) pins. The ground signal consists of a plane to minimize its impedance. Try to separate the low signal ground termination from the power ground signal. The high power noisy circuits like the output, synchronous rectifier, MOSFET driver decoupling capacitor and the input capacitor should be connected to the PGND plane. The AGND plane should only make a single point connection to the PGND plane.

The sensitive nodes like the feedback resistor divider, oscillator resistor (to set frequency), current sense, and compensation circuitry should be connected to the AGND plane.

Try and minimize the high current carrying loops to a minimum, by ensuring optimal component placement. Ensure the bypass capacitors are located as close as possible to their respective power and ground pins.

Sensitive circuits such as sense feedback, frequency setting resistor for the oscillator, current sense and compensation circuits should NOT be located near the dv/dt nodes, these include the gate drive outputs, phase pins and boost circuits (bootstrap).



- Connection to backside of PCB through vias
- Connection to topside of PCB through vias
- ⊙ Connection to ground plane of PCB through vias
- Power bus
- Voltage Output rails
- Thermal Vias

Figure 41. PCB Layout

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|----------------------------|----------------------|------------------------------|-----------------------------|
| TPS43331QDAPRQ1 | ACTIVE | HTSSOP | DAP | 38 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

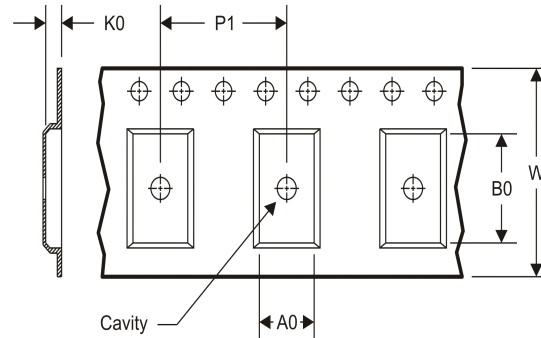
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL INFORMATION
REEL DIMENSIONS

TAPE DIMENSIONS


| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS43331QDAPRQ1 | HTSSOP | DAP | 38 | 2000 | 330.0 | 24.4 | 8.6 | 13.0 | 1.8 | 12.0 | 24.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS

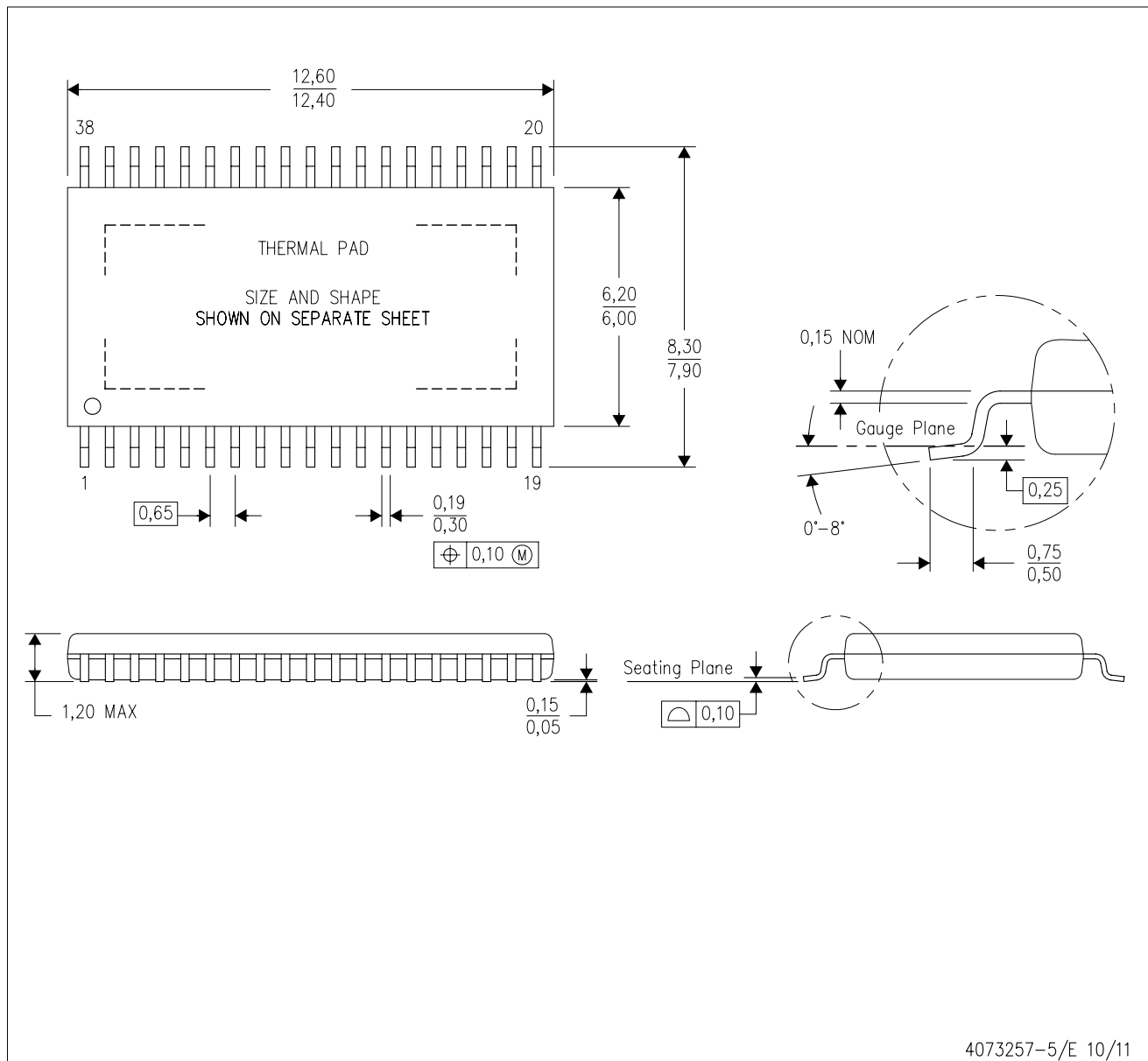


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS43331QDAPRQ1 | HTSSOP | DAP | 38 | 2000 | 367.0 | 367.0 | 45.0 |

MECHANICAL DATA

DAP (R-PDSO-G38) PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- ⚠ Falls within JEDEC MO-153 Variation DDT-1.

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

DAP (R-PDSO-G38)

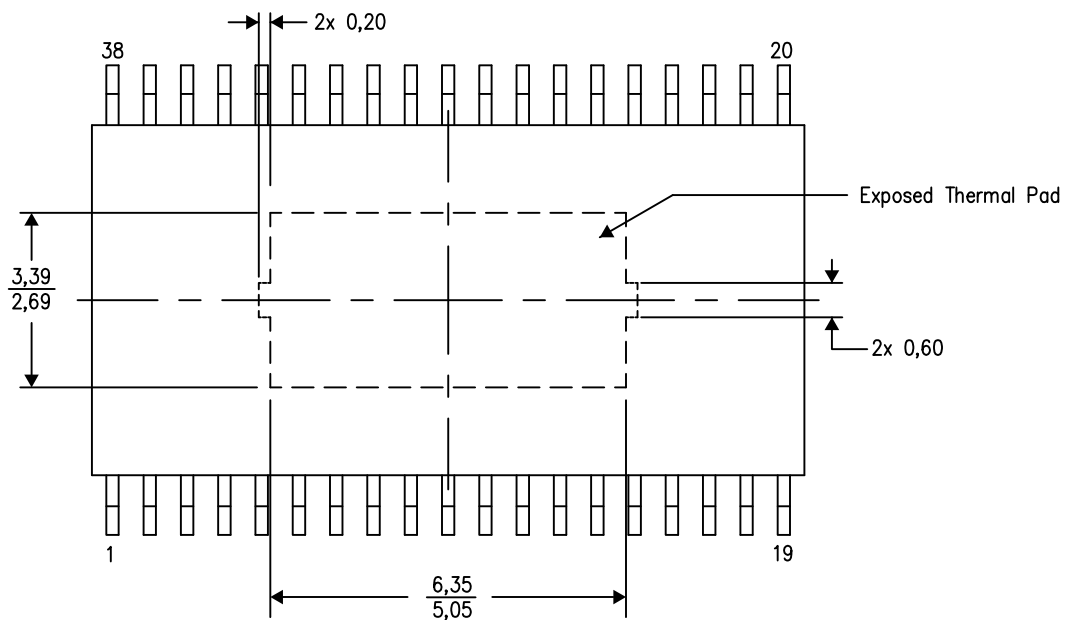
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

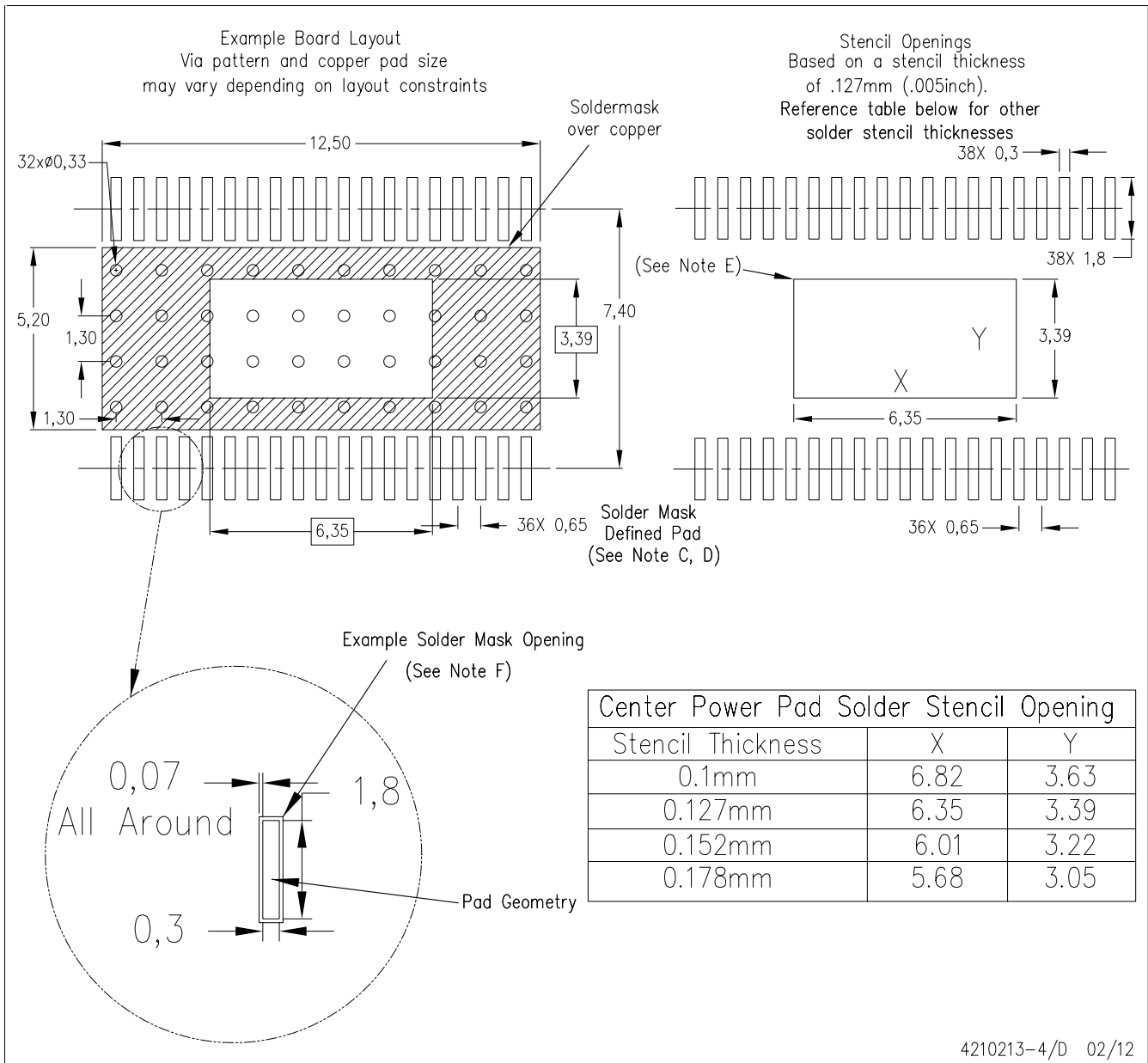
4206319-7/K 04/12

NOTE: All linear dimensions are in millimeters

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LAND PATTERN DATA

DAP (R-PDSO-G38) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - Contact the board fabrication site for recommended soldermask tolerances.

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