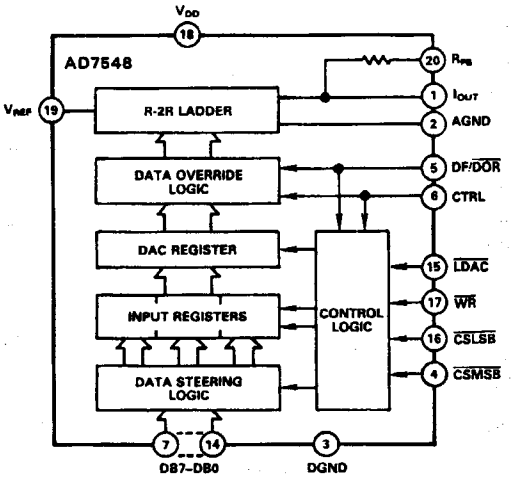
# LC²MOS
# 8-Bit µP-Compatible 12-Bit DAC
# AD7548

## FEATURES
**8-Bit Bus Compatible 12-Bit DAC**
**All Grades 12-Bit Monotonic Over Full Temperature Ranges**
**Operation Specified at +5V, +12V or +15V Power Supply**
**Low Gain Drift of 5ppm/°C Maximum**
**Full 4 Quadrant Multiplication**
**Skinny DIP and Surface Mount Packages**

## APPLICATIONS
**8-Bit Microprocessor Based Control Systems**
**Programmable Amplifiers**
**Function Generation**
**Servo Control**

## AD7548 FUNCTIONAL BLOCK DIAGRAM




## GENERAL DESCRIPTION
The AD7548 is a 12-bit monolithic CMOS D/A converter for use with 8-bit bus microprocessors. Data is loaded in two bytes to input holding registers as shown in the block diagram opposite. The AD7548 can be configured to accept either left- or right-justified data, least significant byte or most significant byte first, using standard TTL compatible control inputs.

A separate load DAC control input allows the user the choice of updating the analog output coincident with loading new data to the DAC input register or at any time after the data loading event. This feature is especially important in multi-DAC systems where simultaneous update of all DACs is required.

The new Linear Compatible CMOS (LC² MOS) process used in the manufacture of the AD7548 allows precision thin-film linear circuitry and high-speed low-power CMOS logic to be integrated on the same small chip. The high-speed logic allows direct interfacing to most of the popular 8-bit microprocessors.

## PRODUCT HIGHLIGHTS
1. Microprocessor Compatibility
   High speed input control (TTL/5V CMOS compatible) allow direct interfacing to most of the popular 8-bit microprocessors.
2. Guaranteed Monotonicity
   The AD7548 is guaranteed monotonic to 12-bits over the full temperature range for all grades and at all specified supply voltages.
3. Selectable Data Input Format
   Left- or right-justified data, least significant or most significant byte first. This allows the AD7548 to be interfaced with microprocessors using either Motorola or Intel-type data formatting.
4. Monolithic Construction
   For increased reliability and reduced package size – 0.3″ 20-pin DIP and 20-terminal surface mount packages.
5. Single Supply Operation – See Figure 8.
6. Low Gain Error and Gain Error T.C.

Rev. A
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# AD7548* PRODUCT PAGE QUICK LINKS

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## COMPARABLE PARTS

View a parametric search of comparable parts.

## DOCUMENTATION

**Application Notes**

- AN-225: 12-Bit Voltage-Output DACs for Single-Supply 5V and 12V Systems

**Data Sheet**

- AD7548: LC$^2$MOS 8-Bit µP Compatible 12-Bit DAC Scanned Data Sheet

## REFERENCE MATERIALS

**Solutions Bulletins & Brochures**

- Digital to Analog Converters ICs Solutions Bulletin

## DESIGN RESOURCES

- AD7548 Material Declaration
- PCN-PDN Information
- Quality And Reliability
- Symbols and Footprints

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# SPECIFICATIONS[1] ($V_{DD}$ = +5V, $V_{REF}$ = +10V; $I_{OUT}$ = AGND = 0V. All specifications $T_{min}$ to $T_{max}$ unless otherwise specified)

| Parameter | J, A Versions | K, B Versions | S Version | T Version | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ACCURACY | | | | | | |
| Resolution | 12 | 12 | 12 | 12 | Bits | |
| Relative Accuracy | ±1 | ±1/2 | ±1 | ±1/2 | LSB max | |
| Differential Nonlinearity | ±1 | ±1/2 | ±1 | ±1/2 | LSB max | All grades guaranteed monotonic to 12-bits over temperature. |
| Full Scale Error | ±6 | ±3 | ±6 | ±3 | LSB max | Measured using internal $R_{FB}$ and includes effects of leakage current and gain TC. Full Scale Error can be trimmed to zero. |
| Gain Temperature Coefficient[2]; ΔGain/ΔTemperature | ±5 | ±5 | ±5 | ±5 | ppm/°C max | Typical value is 2ppm/°C |
| Output Leakage Current $I_{OUT}$ (Pin 1) | | | | | | |
| +25°C | ±5 | ±5 | ±5 | ±5 | nA max | All digital inputs = 0V |
| $T_{min}$ to $T_{max}$ | ±25 | ±25 | ±150 | ±150 | nA max | |
| REFERENCE INPUT | | | | | | |
| Input Resistance, Pin 19 | 7 | 7 | 7 | 7 | kΩ min | Typical Input Resistance = 11kΩ |
| | 20 | 20 | 20 | 20 | kΩ max | |
| DIGITAL INPUTS | | | | | | |
| $V_{IH}$ (Input High Voltage) | 2.4 | 2.4 | 2.4 | 2.4 | V min | |
| $V_{IL}$ (Input Low Voltage) | 0.8 | 0.8 | 0.8 | 0.8 | V max | |
| $I_{IN}$ (Input Current) | | | | | | |
| +25°C | ±1 | ±1 | ±1 | ±1 | μA max | $V_{IN}$ = 0V or $V_{DD}$ |
| $T_{min}$ to $T_{max}$ | ±10 | ±10 | ±10 | ±10 | μA max | |
| $C_{IN}$ (Input Capacitance)[2] | 7 | 7 | 7 | 7 | pF max | |
| POWER SUPPLY | | | | | | |
| $V_{DD}$ Range | 4.75/5.25 | 4.75/5.25 | 4.75/5.25 | 4.75/5.25 | V min/V max | Specifications guaranteed over this range |
| $I_{DD}$ | 2 | 2 | 2 | 2 | mA max | All digital inputs $V_{IL}$ or $V_{IH}$ |
| | 300 | 300 | 300 | 300 | μA max | All digital inputs 0V or $V_{DD}$ |

# SPECIFICATIONS[1] ($V_{DD}$ = +12V to +15V, $V_{REF}$ = +10V; $I_{OUT}$ = AGND = 0V. All specifications $T_{min}$ to $T_{max}$ unless otherwise specified)

| Parameter | J, A Versions | K, B Versions | S Version | T Version | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|
| ACCURACY | | | | | | |
| Resolution | 12 | 12 | 12 | 12 | Bits | |
| Relative Accuracy | ±1 | ±1/2 | ±1 | ±1/2 | LSB max | |
| Differential Nonlinearity | ±1 | ±1/2 | ±1 | ±1/2 | LSB max | All grades guaranteed monotonic to 12-bits over temperature. |
| Full Scale Error | ±6 | ±3 | ±6 | ±3 | LSB max | Measured using internal $R_{FB}$ and includes effects of leakage current and gain TC. Full Scale Error can be trimmed to zero. |
| Gain Temperature Coefficient[2]; ΔGain/ΔTemperature | ±5 | ±5 | ±5 | ±5 | ppm/°C max | Typical value is 2ppm/°C |
| Output Leakage Current $I_{OUT}$ (Pin 1) | | | | | | |
| +25°C | ±5 | ±5 | ±5 | ±5 | nA max | All digital inputs = 0V |
| $T_{min}$ to $T_{max}$ | ±25 | ±25 | ±150 | ±150 | nA max | |
| REFERENCE INPUT | | | | | | |
| Input Resistance, Pin 19 | 7 | 7 | 7 | 7 | kΩ min | Typical Input Resistance = 11kΩ |
| | 20 | 20 | 20 | 20 | kΩ max | |
| DIGITAL INPUTS | | | | | | |
| $V_{IH}$ (Input High Voltage) | 2.4 | 2.4 | 2.4 | 2.4 | V min | |
| $V_{IL}$ (Input Low Voltage) | 0.8 | 0.8 | 0.8 | 0.8 | V max | |
| $I_{IN}$ (Input Current) | | | | | | |
| +25°C | ±1 | ±1 | ±1 | ±1 | μA max | $V_{IN}$ = 0V or $V_{DD}$ |
| $T_{min}$ to $T_{max}$ | ±10 | ±10 | ±10 | ±10 | μA max | |
| $C_{IN}$ (Input Capacitance)[2] | 7 | 7 | 7 | 7 | pF max | |
| POWER SUPPLY | | | | | | |
| $V_{DD}$ Range | 11.4/15.75 | 11.4/15.75 | 11.4/15.75 | 11.4/15.75 | V min/V max | Specifications guaranteed over this range |
| $I_{DD}$ | 3 | 3 | 3 | 3 | mA max | All digital inputs $V_{IL}$ or $V_{IH}$ |
| | 1 | 1 | 1 | 1 | mA max | All digital inputs 0V or $V_{DD}$ |

NOTES
[1]Temperature range as follows: J, K Versions; 0 to +70°C
A, B Versions; −40°C to +85°C
S, T Versions; −55°C to +125°C
[2]Guaranteed by design but not production tested.
Specifications subject to change without notice.

## TIMING CHARACTERISTICS[1] ($V_{DD}$ = +5V, $V_{REF}$ = +10V, $I_{OUT}$ = AGND = 0V unless otherwise stated)

| Parameter | Limit at $T_A$ = 25°C | Limit[2] at $T_A$ = 0 to +70°C −40°C to +85°C | Limit[2] at $T_A$ = −55°C to +125°C | Units | Test Conditions/Comments |
|---|---|---|---|---|---|
| $t_{DS}$ | 240 | 240 | 290 | ns min | Data Valid Setup Time |
| $t_{DH}$ | 50 | 50 | 70 | ns min | Data Valid Hold Time |
| $t_{CWS}$ | 30 | 40 | 50 | ns min | $\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time |
| $t_{CWH}$ | 15 | 20 | 25 | ns min | $\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time |
| $t_{LWS}$ | 30 | 40 | 50 | ns min | $\overline{LDAC}$ to $\overline{WR}$ Setup Time |
| $t_{LWH}$ | 15 | 20 | 25 | ns min | $\overline{LDAC}$ to $\overline{WR}$ Hold Time |
| $t_{WR}$ | 250 | 280 | 320 | ns min | Write Pulse Width |

## TIMING CHARACTERISTICS[1] ($V_{DD}$ = +12V to +15V, $V_{REF}$ = +10V, $I_{OUT}$ = AGND = 0V unless otherwise stated)

| Parameter | Limit at $T_A$ = 25°C | Limit[2] at $T_A$ = 0 to +70°C −40°C to +85°C | Limit[2] at $T_A$ = −55°C to +125°C | Units | Test Conditions/Comments |
|---|---|---|---|---|---|
| $t_{DS}$ | 160 | 190 | 230 | ns min | Data Valid Setup Time |
| $t_{DH}$ | 30 | 30 | 50 | ns min | Data Valid Hold Time |
| $t_{CWS}$ | 30 | 40 | 50 | ns min | $\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Setup Time |
| $t_{CWH}$ | 15 | 20 | 25 | ns min | $\overline{CSMSB}$ or $\overline{CSLSB}$ to $\overline{WR}$ Hold Time |
| $t_{LWS}$ | 30 | 40 | 50 | ns min | $\overline{LDAC}$ to $\overline{WR}$ Setup Time |
| $t_{LWH}$ | 15 | 20 | 25 | ns min | $\overline{LDAC}$ to $\overline{WR}$ Hold Time |
| $t_{WR}$ | 170 | 200 | 240 | ns min | Write Pulse Width |

## AC PERFORMANCE CHARACTERISTICS

These characteristics are included for Design Guidance only and are not subject to test. ($V_{REF}$ = +10V; $I_{OUT}$ = AGND = 0V, Output Amplifier is AD544 except where stated)

| Parameter | Version | $V_{DD}$ = +5V $T_A$ = +25°C | $V_{DD}$ = +5V $T_A$ = $T_{MIN}$, $T_{MAX}$ | $V_{DD}$ = +12V to +15V $T_A$ = +25°C | $V_{DD}$ = +12V to +15V $T_A$ = $T_{MIN}$, $T_{MAX}$ | Units | Test Conditions/Comments |
|---|---|---|---|---|---|---|---|
| Output Current Settling Time | | 1.5 | – | 1 | – | µs typ | To 0.01% of full scale range. $I_{OUT}$ load = 100Ω, $C_{EXT}$ = 13pF. DAC register alternately loaded with all 1s and all 0s |
| Digital to Analog Glitch Impulse | | 400 | – | 330 | – | nV-sec typ | Measured with $V_{REF}$ = 0V, $I_{OUT}$ load = 100Ω, $C_{EXT}$ = 13pF. DAC register alternately loaded with all 1s and all 0s |
| Multiplying Feedthrough Error[3] | | 3 | 5 | 3 | 5 | mV p-p typ | $V_{REF}$ = ±5V, 10kHz sine wave DAC register loaded with all 0s. |
| Total Harmonic Distortion | | −85 | – | −85 | – | dB typ | $V_{REF}$ = 6V rms @ 1kHz. DAC register loaded with all 1s. |
| Power Supply Rejection Δ GAIN/Δ $V_{DD}$ | | ±0.015 | ±0.03 | ±0.01 | ±0.02 | % per % max | $\Delta V_{DD}$ = ±5% |
| Output Capacitance $I_{OUT}$ (Pin 1) | | 200<br>100 | 200<br>100 | 200<br>100 | 200<br>100 | pF max<br>pF max | DAC register loaded with all 1s.<br>DAC register loaded with all 0s. |
| Output Noise Voltage Density (10Hz–100kHz) | | 15 | – | 15 | – | nV/√Hz typ | Measured between $R_{FB}$ and $I_{OUT}$ |

NOTES
[1]Guaranteed by design but not production tested.
[2]Temperature range as follows: J, K Versions; 0 to +70°C
A, B Versions; −40°C to +85°C
S, T Versions; −55°C to +125°C
[3]Feedthrough can be further reduced by connecting the metal lid on the ceramic package (Suffix D) to DGND.
Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS*

($T_A$ = +25°C unless otherwise noted)

| | |
|---|---|
| $V_{DD}$ (Pin 18) to DGND | +17V |
| $V_{REF}$ (Pin 19) to AGND | ±25V |
| $V_{RFB}$ (Pin 20) to AGND | ±25V |
| Digital Input Voltage (Pins 4–17) to DGND | −0.3V, $V_{DD}$ |
| $V_{PIN\ 1}$ to DGND | −0.3V, $V_{DD}$ |
| AGND to DGND | −0.3V, $V_{DD}$ |
| Power Dissipation (Any Package) | |
| To +75°C | 450mW |
| Derates above +75°C | 6mW/°C |
| Operating Temperature Range | |
| Commercial (J, K Versions) | 0 to +70°C |
| Industrial (A, B Versions) | −40°C to +85°C |
| Extended (S, T Versions) | −55°C to +125°C |
| Storage Temperature | −65°C to +150°C |
| Lead Temperature (Soldering, 10secs) | +300°C |

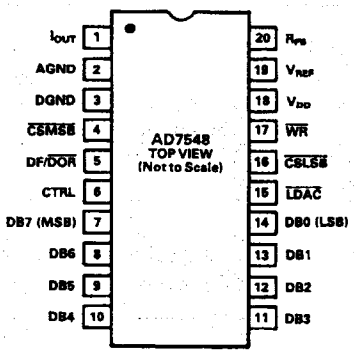
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION:**

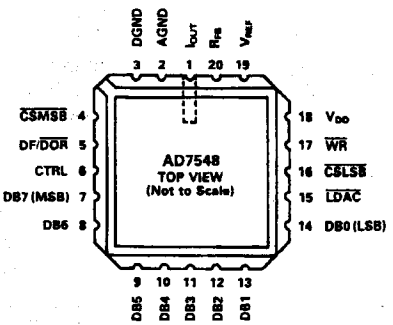
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.

## PIN CONFIGURATIONS

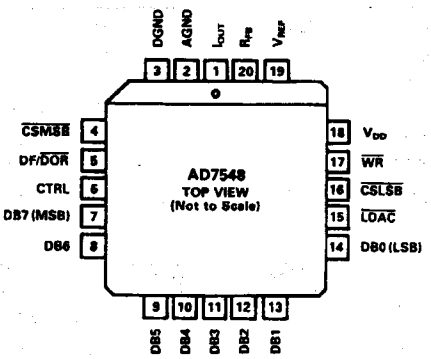
DIP




LCCC




PLCC




## ORDERING INFORMATION[1,2]

| Relative Accuracy $T_{min}$–$T_{max}$ | Full-Scale Error $T_{min}$–$T_{max}$ | Temperature Range and Package Options[3] 0 to +70°C | −25°C to +85°C | −55°C to +125°C |
|---|---|---|---|---|
| | | Plastic DIP (N-20) | Hermetic (Q-20) | Hermetic (Q-20) |
| ±1LSB | ±6LSB | AD7548JN | AD7548AQ | AD7548SQ |
| ±1/2LSB | ±3LSB | AD7548KN | AD7548BQ | AD7548TQ |
| | | PLCC[4] (P-20A) | | LCCC[5] (E-20A) |
| ±1LSB | ±6LSB | AD7548JP | | AD7548SE |
| ±1/2LSB | ±3LSB | AD7548KP | | AD7548TE |

NOTES

[1]To order MIL-STD-883, Class B processed parts, add/883B to part number. Contact your local sales office for military data sheet.

[2]Analog Devices reserves the right to ship ceramic (package outline D-20) packages in lieu of cerdip (package outline Q-20) packages.

[3]See Section 13 for package outline information.

[4]PLCC: Plastic Leaded Chip Carrier.

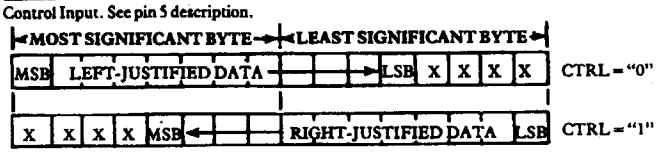
[5]LCCC: Leadless Ceramic Chip Carrier.

## PIN FUNCTION DESCRIPTION

| PIN | MNEMONIC | DESCRIPTION |
|---|---|---|
| 1 | $I_{OUT}$ | DAC current OUT bus. Normally terminated at virtual ground of output amplifier. |
| 2 | AGND | Analog Ground. |
| 3 | DGND | Digital Ground. |
| 4 | $\overline{CSMSB}$ | Chip Select Most Significant (MS) Byte. Active Low Input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers. |
| 5 | DF/$\overline{DOR}$ | Data Format/Data Override. When this input is LOW, data in the DAC register is forced to one of two override codes selected by CTRL. When the override signal is removed, the DAC output returns to reflect the value in the DAC register. With DF/$\overline{DOR}$ HIGH, CTRL selects either a left or right justified input data format. For normal operation, DF/$\overline{DOR}$ is held HIGH. |

| DF/$\overline{DOR}$ | CTRL | FUNCTION |
|---|---|---|
| 0 | 0 | DAC register contents overridden by all 0's |
| 0 | 1 | DAC register contents overriden by all 1's |
| 1 | 0 | Left-justified input data selected |
| 1 | 1 | Right-justified input data selected |

| PIN | MNEMONIC | DESCRIPTION |
|---|---|---|
| 6 | CTRL | Control Input. See pin 5 description. |




X = Don't care states.

| PIN | MNEMONIC | DESCRIPTION |
|---|---|---|
| 7 | DB7 | Data Bit 7. Most Significant Bit (MSB). |
| 8 | DB6 | Data Bit 6. |
| 9 | DB5 | Data Bit 5. |
| 10 | DB4 | Data Bit 4. |
| 11 | DB3 | Data Bit 3. |
| 12 | DB2 | Data Bit 2. |
| 13 | DB1 | Data Bit 1. |
| 14 | DB0 | Data Bit 0. Least Significant Bit (LSB). |
| 15 | $\overline{LDAC}$ | Load DAC Input, active LOW. This signal, in combination with others, is used to load the DAC register from either the input register or the external data bus. |
| 16 | $\overline{CSLSB}$ | Chip Select Least Significant (LS) Byte. Active LOW input. Used in combination with $\overline{WR}$ to load external data into the input register or in combination with $\overline{WR}$ and $\overline{LDAC}$ to load external data into both input and DAC registers. |
| 17 | $\overline{WR}$ | WRITE Input. This active low signal, in combination with others is used in loading external data into the AD7548 input register and in transferring data from the input register to the DAC register. |

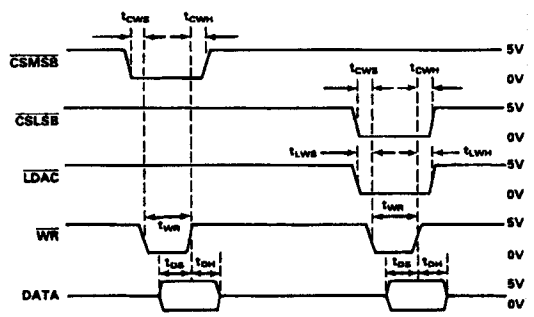
| $\overline{WR}$ | $\overline{CSMSB}$ | $\overline{CSLSB}$ | $\overline{LDAC}$ | FUNCTION |
|---|---|---|---|---|
| 0 | 1 | 0 | 1 | Load LS Byte to Input Register. |
| 0 | 1 | 0 | 0 | Load LS Byte to Input Register and DAC Register. |
| 0 | 0 | 1 | 1 | Load MS Byte to Input Register. |
| 0 | 0 | 1 | 0 | Load MS Byte to Input Register and DAC Register. |
| 0 | 1 | 1 | 0 | Load Input Register to DAC Register. |
| 1 | X | X | X | No Data Transfer |

| PIN | MNEMONIC | DESCRIPTION |
|---|---|---|
| 18 | $V_{DD}$ | +5V to +15V Supply Input. |
| 19 | $V_{REF}$ | Reference Voltage Input. |
| 20 | $R_{FB}$ | Feedback Resistor. Used for normal D/A conversion. |

## CONTROL INPUT INFORMATION

Figure 1a shows the data load timing diagram for the AD7548.

Figure 1b shows the simplified input control structure of the AD7548.




NOTES
1. ALL INPUT SIGNAL RISE AND FALL TIMES MEASURED FROM 10% TO 90% OF +5V. $t_r = t_f = 20ns$.
2. TIMING MEASUREMENT REFERENCE LEVEL IS $\frac{V_H + V_L}{2}$.
3. $\overline{CSMSB}$ (PIN 4) AND $\overline{CSLSB}$ (PIN 16) MAY BE INTERCHANGED.
4. FOR LEFT-JUSTIFIED DATA CTRL = +0V WITH DF/$\overline{DOR}$ = +5V. FOR RIGHT-JUSTIFIED DATA CTRL = +5V WITH DF/$\overline{DOR}$ = +5V.

*Figure 1a. AD7548 Timing Diagram*

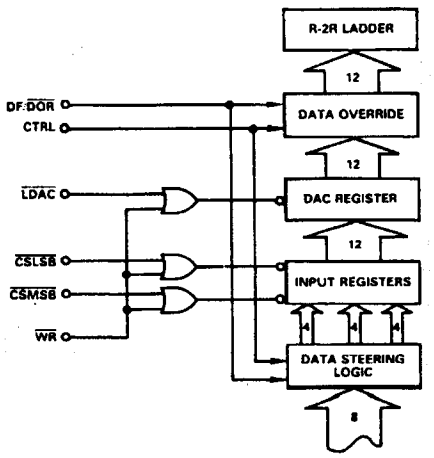



*Figure 1b. Simplified AD7548 Input Control Structure*

## GENERAL CIRCUIT INFORMATION

The simplified D/A circuit is shown in Figure 2. An inverted R-2R ladder structure is used, which steers binarily weighted currents between $I_{OUT}$ and AGND, thus maintaining a constant current in each ladder leg independent of the switch state.

The input resistance at $V_{REF}$ is constant and equal to the value "R" in Figure 2. Since the input resistance is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low temperature coefficient external $R_{FB}$ is recommended to define scale factor).

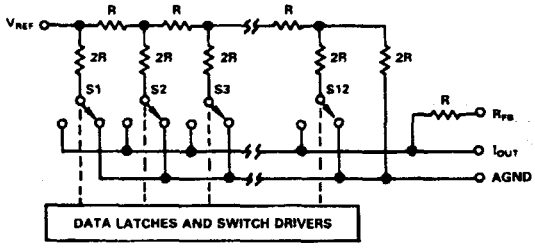



*Figure 2. AD7548 Simplified Functional Diagram*

## EQUIVALENT CIRCUIT ANALYSIS

Figure 3 shows an equivalent circuit for the analog section of the AD7548 D/A converter. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages. The resistor $R_O$, denotes the equivalent output resistance of the DAC which varies with input code (excluding all 0's code) from 0.8R to 2R, where R is typically 11kΩ. $C_{OUT}$ is the capacitance due to the current steering switches and varies from about 50pF to 120pF (typical values) depending upon the digital input. $g(V_{REF}, N)$ is the Thevenin equivalent voltage generator due to the reference input voltage, $V_{REF}$, and the transfer function of R-2R ladder, N.

For further information on CMOS multiplying D/A converters refer to "Application Guide to CMOS Multiplying D/A Converters" available from Analog Devices, Publication Number G479–15–8/78.

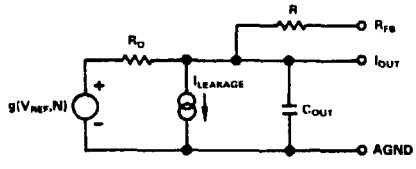



*Figure 3. AD7548 Equivalent Analog Output Circuit*

## DATA LOADING

The AD7548 accepts incoming data in either left-justified format or right-justified format depending on the control inputs DF/$\overline{DOR}$ and CTRL.

(See pin description of DF/$\overline{DOR}$ and CTRL on preceding page).

Two operating modes are possible for controlling the transfer of data from the input register to the DAC register, the automatic transfer mode and the strobed transfer mode.

## AUTOMATIC TRANSFER MODE

This is the simplest and fastest method of transferring data to the DAC register. It is facilitated by connecting $\overline{LDAC}$ to either $\overline{CSMSB}$, as shown in Figure 10, or $\overline{CSLSB}$.

Figure 4 shows the timing diagram for automatic transfer of 8 +4-bit data to the DAC register. The first write cycle loads the first byte of data to the input register. The second write cycle loads the second byte of data to the input register and automatically transfers both bytes to the DAC register.

Updating a single byte (High or Low) in the DAC register can be achieved in one write cycle using the automatic transfer mode.

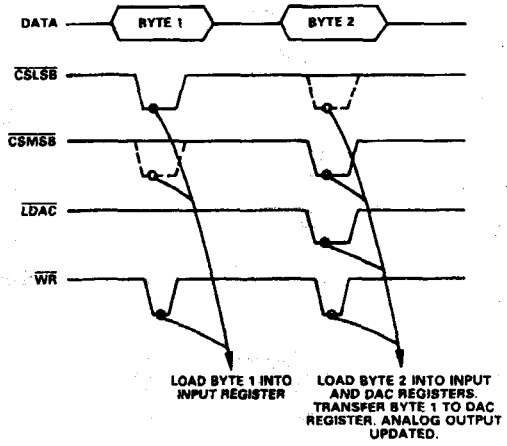



*Figure 4. Automatic Transfer Mode*

## STROBED TRANSFER MODE

Figure 5 shows the timing diagram for the strobed transfer of 8 +4-bit data to the DAC register. Three write cycles are required for this transfer mode. The first two write cycles sequentially load bytes 1 and 2 into the input register. The third write cycle transfers data from the input register to the DAC register.

The strobed transfer mode allows the DAC registers of several AD7548's to be updated simultaneously, as shown in Figure 13, by means of a master strobe signal connected to the $\overline{LDAC}$ of each device.

A single byte of data (High or Low) can be transferred to the DAC register in two write cycles using the strobed transfer mode.

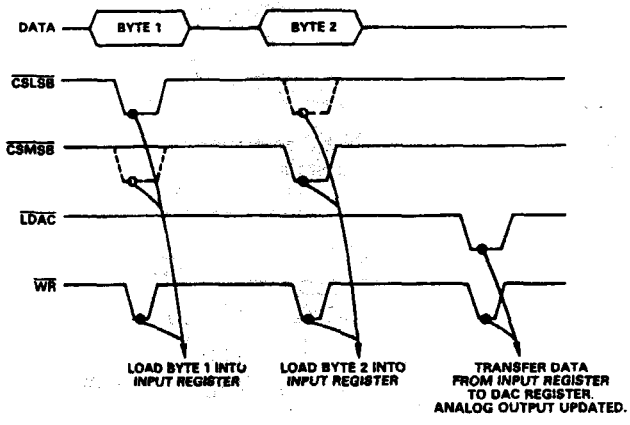



*Figure 5. Strobed Transfer Mode*

## DATA OVERRIDE

The contents of the DAC register can be overridden by pulling DF/$\overline{DOR}$ (pin 5) LOW. The CTRL (pin 6) input then determines whether the DAC register data is overidden by all 0s (CTRL LOW) or all 1s (CTRL HIGH). This feature allows the user to calibrate the AD7548 in circuits such as Figure 6 without calling on the microprocessor to load calibration data.

## UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

Figure 6 shows the analog circuit connections required for unipolar binary operation. With a dc input voltage or current (positive or negative polarity) applied at pin 19, the circuit is a unipolar D/A converter. With an ac input voltage the circuit provides 2-quadrant multiplication (digitally controlled attenuation).

Table I shows the code relationship for the circuit of Figure 6.

For full scale trimming the DAC register is loaded with 1111 1111 1111. This is most easily accomplished by using the data override function. R1 is then adjusted for $V_{OUT} = -V_{IN}$ (4095/4096). Alternatively full scale can be adjusted by omitting R1 and R2 and trimming the reference voltage magnitude.

Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps.

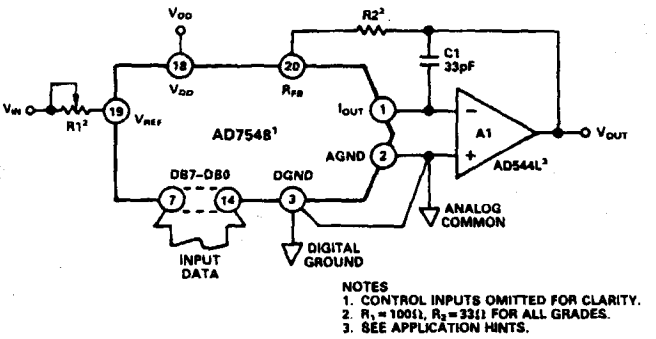



*Figure 6. Unipolar Binary Operation*

| Binary Number in DAC Register MSB LSB | Analog Output, $V_{OUT}$ |
|---|---|
| 1111 1111 1111 | $-V_{IN}\left(\frac{4095}{4096}\right)$ |
| 1000 0000 0000 | $-V_{IN}\left(\frac{2048}{4096}\right) = -1/2V_{IN}$ |
| 0000 0000 0001 | $-V_{IN}\left(\frac{1}{4096}\right)$ |
| 0000 0000 0000 | 0V |

*Table I. Unipolar Binary Code Table for Circuit of Figure 6*

## BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

Figure 7 and Table II illustrate the recommended circuit and code relationship for bipolar operation. The circuit uses offset binary input coding. However, 2's complement coding can be accommodated if the MSB is inverted (done in software) before data is loaded into the DAC.

With the DAC register loaded to 1000 0000 0000, adjust R1 for $V_{OUT} = 0V$ (alternatively one can omit R1 and R2 and adjust the ratio of R3 and R4 for $V_{OUT} = 0V$). Full scale trimming can be accomplished by adjusting the amplitude of $V_{IN}$ or by varying the value of R5.

R3, R4 and R5 must be selected to match within 0.01% and they should be the same type of resistor (preferably metal film) so that their temperature coefficients match. Mismatch of R3 to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

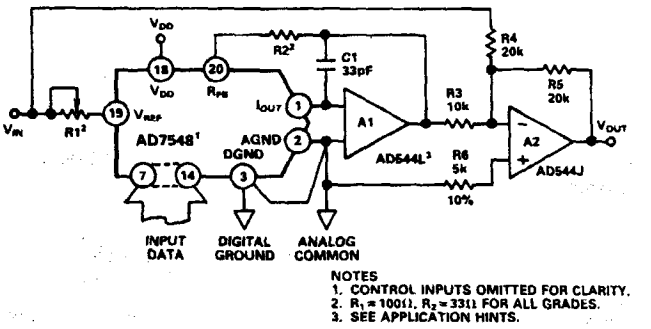



*Figure 7. Bipolar Operation (Offset Binary Coding)*

| Binary Number in DAC Register MSB LSB | Analog Output, $V_{OUT}$ |
|---|---|
| 1111 1111 1111 | $+V_{IN}\left(\frac{2047}{2048}\right)$ |
| 1000 0000 0001 | $+V_{IN}\left(\frac{1}{2048}\right)$ |
| 1000 0000 0000 | 0V |
| 0111 1111 1111 | $-V_{IN}\left(\frac{1}{2048}\right)$ |
| 0000 0000 0000 | $-V_{IN}\left(\frac{2048}{2048}\right)$ |

*Table II. Bipolar Code Table for Offset Binary Circuit of Figure 7*

## SINGLE SUPPLY OPERATION

Figure 8 shows the AD7548 connected in a voltage switching mode. The input voltage is connected to $I_{OUT}$. The D/A converter output voltage is taken from the $V_{REF}$ pin and has a constant impedance equal to R. $R_{FB}$ is not used in this circuit. The input voltage $V_{IN}$ must always be positive with respect to AGND in order to prevent an internal diode from turning on. To maintain linearity the input voltage should remain within 2.5V of AGND with $V_{DD}$ from +12V to +15V.

The output voltage $V_{OUT}$ of Figure 8 is expressed as

$$V_{OUT} = (V_{IN})\,(D)\left(\frac{R_1 + R_2}{R_1}\right)$$

Where D is a fractional representation of the digital input word ($0 \leq D \leq 4095/4096$).

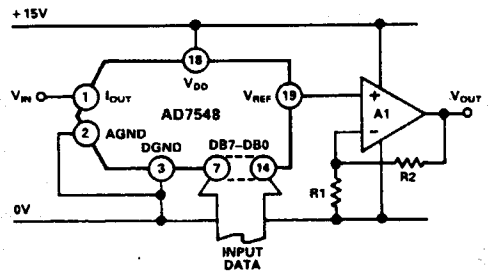



*Figure 8. Single Supply Operation Using Voltage Switching Mode*

## APPLICATION HINTS

**Output Offset:** CMOS D/A converters in circuits such as Figures 6 and 7 exhibit a code dependent output resistance which in turn cause a code dependent amplifier noise gain. The effect is a code dependent differential nonlinearity term at the amplifier output which, depends on $V_{OS}$ where $V_{OS}$ is the amplifier input offset voltage. To maintain monotonic operation it is recommended that $V_{OS}$ be no greater than $(25 \times 10^{-6})(V_{REF})$ over the temperature range of operation. Suitable op amps are AD517L and AD544L. The AD517L is best suited for fixed reference applications with low bandwidth requirements: it has extremely low offset (50μV) and in most applications will not require an offset trim. The AD544L has a much wider bandwidth and higher slew rate and is recommended for multiplying and other applications requiring fast settling. An offset trim on the AD544L may be necessary in some circuits.

**General Ground Management:** AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the AD7548. In more complex systems where the AGND and DGND intertie is on the backplane, it is recommended that two diodes be connected in inverse parallel between the AD7548 AGND and DGND pins (1N914 or equivalent).

**Temperature Coefficients:** The gain temperature coefficient of the AD7548 has a maximum value of 5ppm/°C and typical value of 2ppm/°C. This corresponds to worst case gain shifts of 2LSBs and 0.8LSBs respectively over a 100°C temperature range. When trim resistors R1 and R2 are used to adjust full scale range, the temperature coefficient of R1 and R2 should also be taken into account. The reader is referred to Analog Devices Application Note "Gain Error and Gain Temperature Coefficient of CMOS Multiplying DACs", Publication Number E630–10–6/81.

**High Frequency Considerations:** AD7548 output capacitance works in conjunction with the amplifier feedback resistance to add a pole to the open loop response. This can cause ringing or oscillation. Stability can be restored by adding a phase compensation capacitor in parallel with the feedback resistor.

**Feedthrough:** The dynamic performance of the AD7548 will depend upon the gain and phase stability of the output amplifier, together with the optimum choice of PC board layout and decoupling components. A suggested printed circuit layout for Figure 6 is shown in Figure 9 which minimizes feedthrough from $V_{REF}$ to the output in multiplying applications.

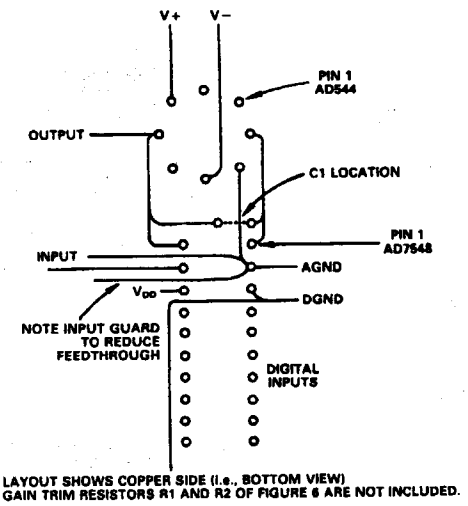



*Figure 9. Suggested Layout for AD7548 and Op Amp*

For additional information on multiplying DACs refer to "Application Guide to CMOS Multiplying D/A Converters", Publication Number G479–15–8/78, available from Analog Devices.

## MICROPROCESSOR INTERFACING

### AD7548 – MC6800 INTERFACE

A typical 6800 configuration using the automatic transfer mode of the AD7548 is shown in Figure 10. Table III gives a sample loading routine written in re-entrant form. Data load and store instructions use extended addressing. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY + 1. The data is considered right-justified with the four most significant bits occupying the lower half of XXYY + 1. The AD7548 is assigned a base address of PPQQ. This address selects the low byte register of the AD7548. Address PPQQ + 1 selects both the high byte register and the $\overline{LDAC}$ control input.

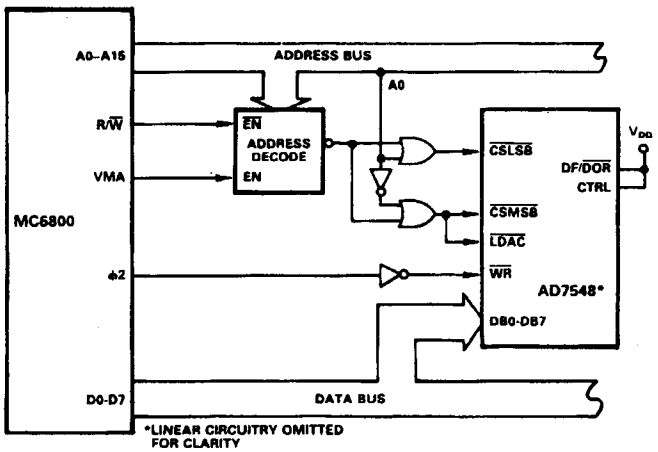



*Figure 10. AD7548 – MC6800 Interface (Automatic Transfer Mode)*

| | | | |
|---|---|---|---|
| | JSR | WWZZ | Jump to AD7548 subroutine |
| WWZZ | PSH A | | Push A onto stack |
| | TPA | | |
| | PSH A | | Push CCR onto stack |
| | LDA A | $XXYY | |
| | STA A | $PPQQ | Load low byte to AD7548 |
| | LDA A | $XXYY + 1 | |
| | STA A | $PPQQ + 1 | Load high byte to AD7548 and update analog output |
| | PUL A | | |
| | TAP | | Pull CCR from stack |
| | PUL A | | Pull A from stack |
| | RTS | | Return to main program |

*Table III. Sample Routine for AD7548 – MC6800 Interface*

### AD7548 – 8085A INTERFACE

Figure 11 shows a typical AD7548 to 8085A microprocessor interface configured for automatic transfer of 8 + 4-bit right-justified data. Table IV gives a sample loading routine written in re-entrant form. The 12-bit data to be passed to the subroutine is stored in locations XXYY and XXYY + 1. The four most significant data bits occupy the lower half of XXYY + 1. As before, addresses PPQQ and PPQQ + 1 select the $\overline{CSLSB}$ and $\overline{CSMSB}/\overline{LDAC}$ control inputs respectively. Since only two instructions (LHLD, SHLD) are required to both fetch and load the 12-bit data word to the AD7548, it may be more efficient to insert these instructions as required in the main program rather than use a subroutine such as illustrated here.

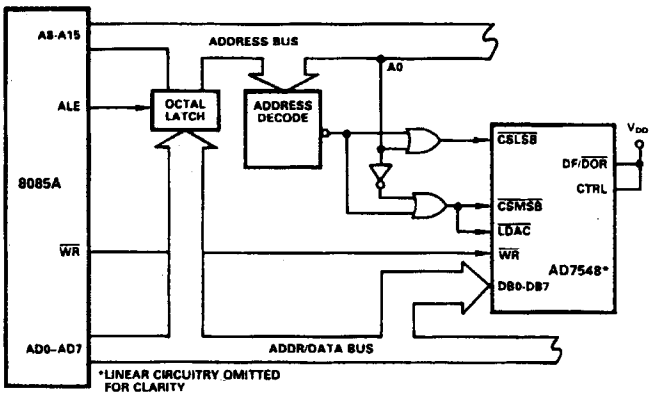



*Figure 11. AD7548 – 8085A Interface (Automatic Transfer Mode)*

| | | | |
|---|---|---|---|
| | CALL | 7548 | |
| 7548 | PUSH | PSW | Push register contents onto stack |
| | PUSH | H | |
| | LHLD | XXYY | Fetch 12-bit data |
| | SHLD | PPQQ | Load 12-bit data |
| | POP | H | Pop register contents from stack |
| | POP | PSW | |
| | RET | | Return to main program |

*Table IV. Sample Routine for AD7548–8085A Interface*

## AD7548 – MC6809 INTERFACE

The AD7548 can be interfaced to the MC6809 microprocessor as shown in Figure 12 for automatic transfer of 8 + 4-bit data. Similar to the 8085A instructions LHLD and SHLD, the 6809 has two instructions to fetch and store 12-bit (16-bit) data to the AD7548, LDD and STD. However, in the 6809, the high byte of data is moved first, then the low byte (this is the opposite of the 8085A). This means that if the 12-bit data is assumed to reside at addresses XXYY and XXYY + 1 then XXYY must contain the high byte. It also means that the address decoding logic of Figure 11 must be slightly changed so that the even-order AD7548 address, PPQQ from before, selects the $\overline{CSMSB}$ input to load the high byte first. In this automatic transfer configuration $\overline{LDAC}$ is tied to the $\overline{CSLSB}$ input. The AD7548 analog output can thus be updated using only two instructions as follows:

```
LDD    $XXYY
STD    $PPQQ
```

The strobed transfer configuration is shown in Figure 13 with a dedicated decoder output assigned to each chip select input. The common $\overline{LDAC}$ signal allows simultaneous update of both AD7548 DAC registers.

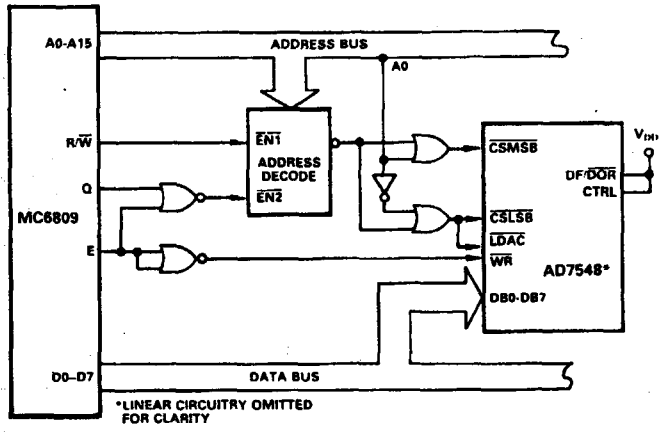



*Figure 12. AD7548 – MC6809 Interface (Automatic Transfer Mode)*

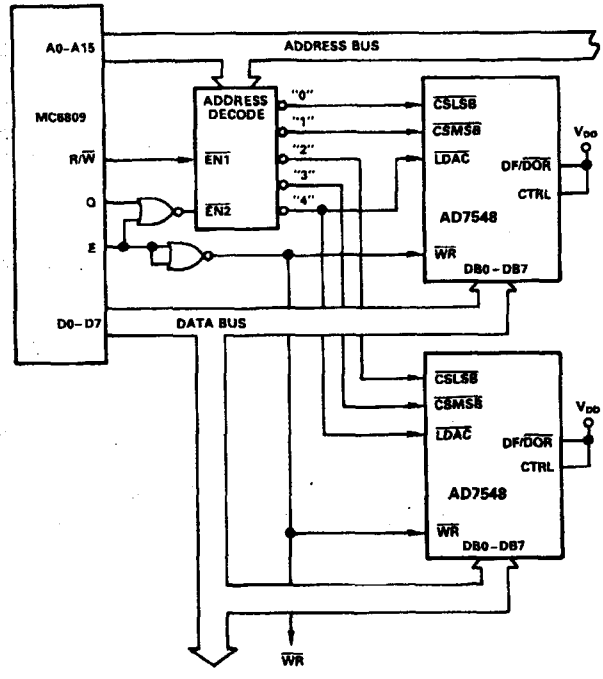



*Figure 13. AD7548 – MC6809 Interface (Strobed Transfer Mode)*

## AD7548 – 6502 INTERFACE

Figure 14 shows a typical AD7548 to 6502 microprocessor interface configured for automatic transfer of right-justified data. As a programming example, Figure 15 shows a flow chart for producing a 12-bit (4095-step-max) voltage ramp under 6502 control. Index registers X and Y of the 6502 form a 12-bit counter with the X-register holding the low byte of data and the Y-register the high byte. Table V shows the program listing. The X-register is compared with $FF_H$ and the Y-register with $10_H$ to determine when the ramp voltage has reached its maximum value ($FFF_H$). By changing the comparison data in the program the maximum ramp output voltage can be varied from levels corresponding to $FFF_H$ down to $000_H$. In the program listing of Table V the AD7548 has been assigned contiguous addresses 0400 (low byte) and 0401 (high byte and DAC register).

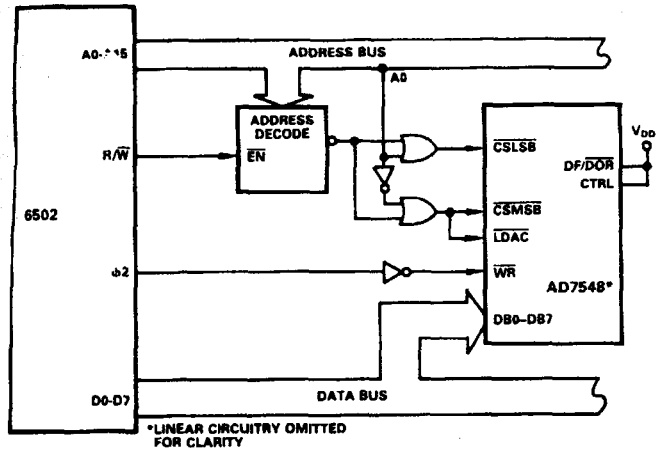



*Figure 14. AD7548 – 6502 Interface (Automatic Transfer Mode)*

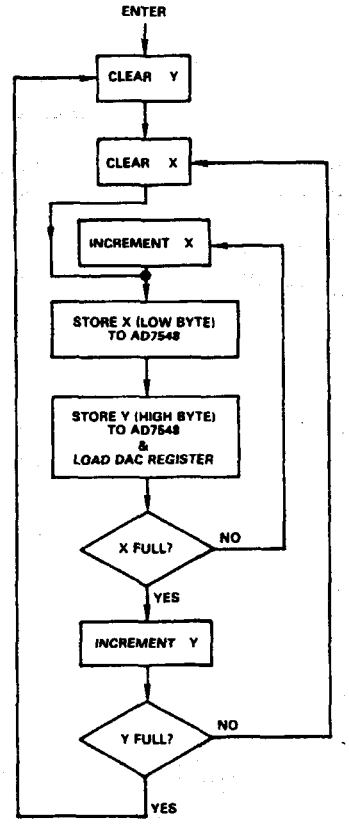



*Figure 15. Flow Chart for Voltage Ramp Generation*

| ADDRESS | OP-CODE | MNEMONIC | OPERAND |
|---|---|---|---|
| 0000 | A0 | LDY | # 00 |
| 01 | 00 | | |
| 02 | A2 | LDX | # 00 |
| 03 | 00 | | |
| 04 | 4C | JMP | 0008 |
| 05 | 08 | | |
| 06 | 00 | | |
| 07 | E8 | INX | |
| 08 | 8E | STX | 0400 |
| 09 | 00 | | |
| 0A | 04 | | |
| 0B | 8C | STY | 0401 |
| 0C | 01 | | |
| 0D | 04 | | |
| 0E | E0 | CPX | # FF |
| 0F | FF | | |
| 10 | D0 | BNE | 0007 |
| 11 | F5 | | |
| 12 | C8 | INY | |
| 13 | C0 | CPY | # 10 |
| 14 | 10 | | |
| 15 | D0 | BNE | 0002 |
| 16 | EB | | |
| 17 | FO | BEQ | 0000 |
| 0018 | E7 | | |

*Table V. Program Listing for Figure 15*

## AD7548 – Z80 INTERFACE

Figure 16 shows a typical AD7548 to Z80 microprocessor interface configured for automatic transfer of right-justified data. Similar to the 8085A and 6809 cases, 16-bit load instructions are available in the Z80 which can fetch and load 12-bit data to the AD7548. Since the low byte of data is moved first and assuming the 12-bit data resides at addresses XXYY and XXYY + 1, address XXYY must contain the low byte. As before, addresses PPQQ and PPQQ + 1 select the AD7548 $\overline{CSLSB}$ and $\overline{CSMSB}$/$\overline{LDAC}$ control inputs respectively. Choosing the Z80 register pair BC to hold the 12-bit data, the two instructions required to update the AD7548 analog output are as follows:

LD BC, (XXYY)
LD (PPQQ), BC

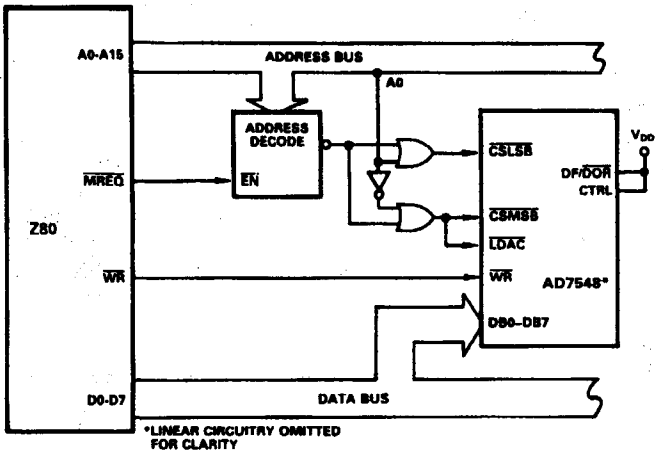
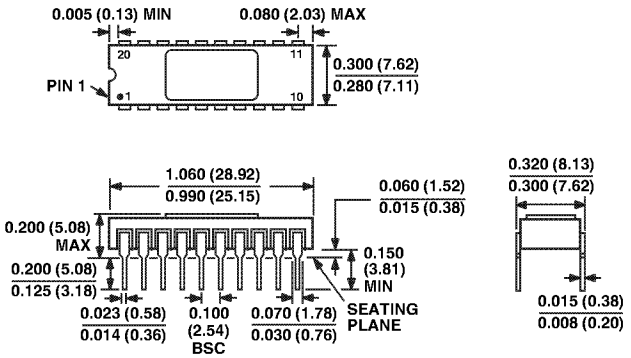
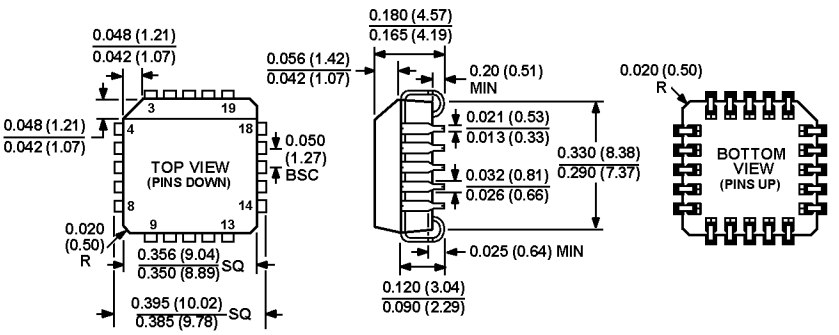



*Figure 16. AD7548 – Z80 Interface (Automatic Transfer Mode)*



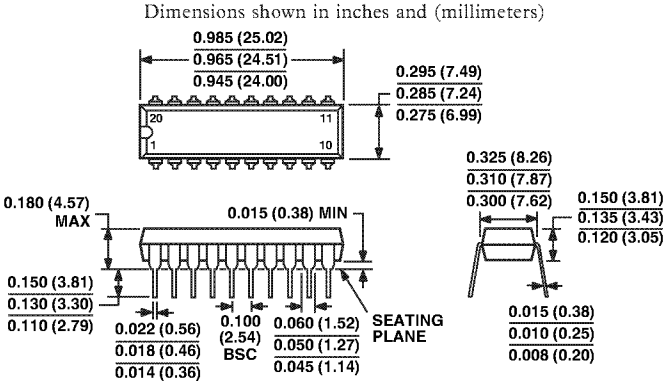

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

20-Lead Plastic Dual In-Line Package [PDIP]
(N-20)
Dimensions shown in inches and (millimeters)

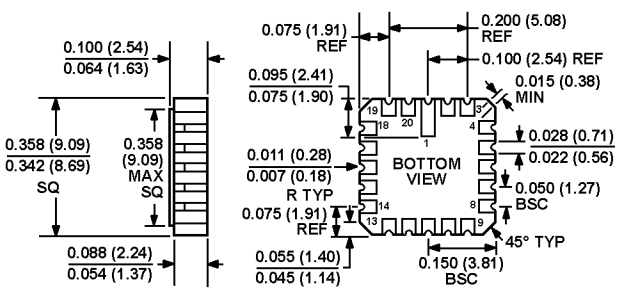



COMPLIANT TO JEDEC STANDARDS MO-047AA
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

*Figure 40. 20-Lead Plastic Leaded Chip Carrier [PLCC]*
*(P-20A)*
*Dimensions shown in inches and (mm)*



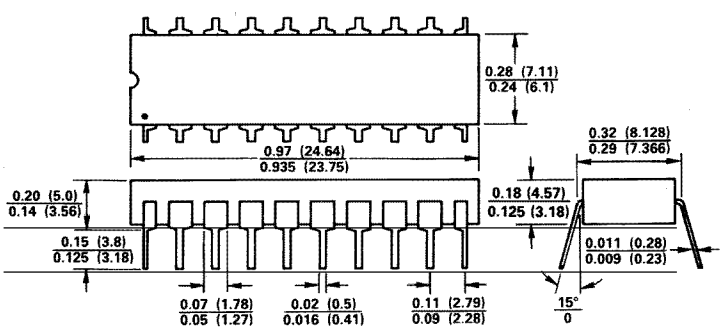

COMPLIANT TO JEDEC STANDARDS MO-095-AE
CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN




CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

022106-A

*Figure 24. 20-Terminal Ceramic Leadless Chip Carrier [LCC]*
*(E-20)*
*Dimensions shown in inches and (millimeters)*




20-Lead Cerdip
(Q-20)