WCSS0418V1P

256K x 18 Synchronous-Pipelined Cache RAM

Features

- **Supports 100-MHz bus for Pentium® and PowerPC™ operations with zero wait states**
- **Fully registered inputs and outputs for pipelined operation**
- **256K by 18 common I/O architecture**
- **3.3V core power supply**
- **2.5V / 3.3V I/O operation**
- **Fast clock-to-output times**
  - **— 3.5 ns (for 166-MHz device)**
  - **— 4.0 ns (for 133-MHz device)**
  - **— 5.5 ns (for 100-MHz device)**
- **User-selectable burst counter supporting Intel® Pentium interleaved or linear burst sequences**
- **Separate processor and controller address strobes**
- **Synchronous self-timed writes**
- **Asynchronous Output Enable**
- **JEDEC-standard 100 TQFP pinout**
- **"ZZ" Sleep Mode option and Stop Clock option**

Functional Description

The WCSS0418V1P is a 3.3V, 256K by 18 synchronous-pipelined cache SRAM designed to support zero wait state secondary cache with minimal glue logic.

The WCSS0418V1P I/O pins can operate at either the 2.5V or the 3.3V level. The I/O pins are 3.3V tolerant when V_{D-DQ}=2.5V.

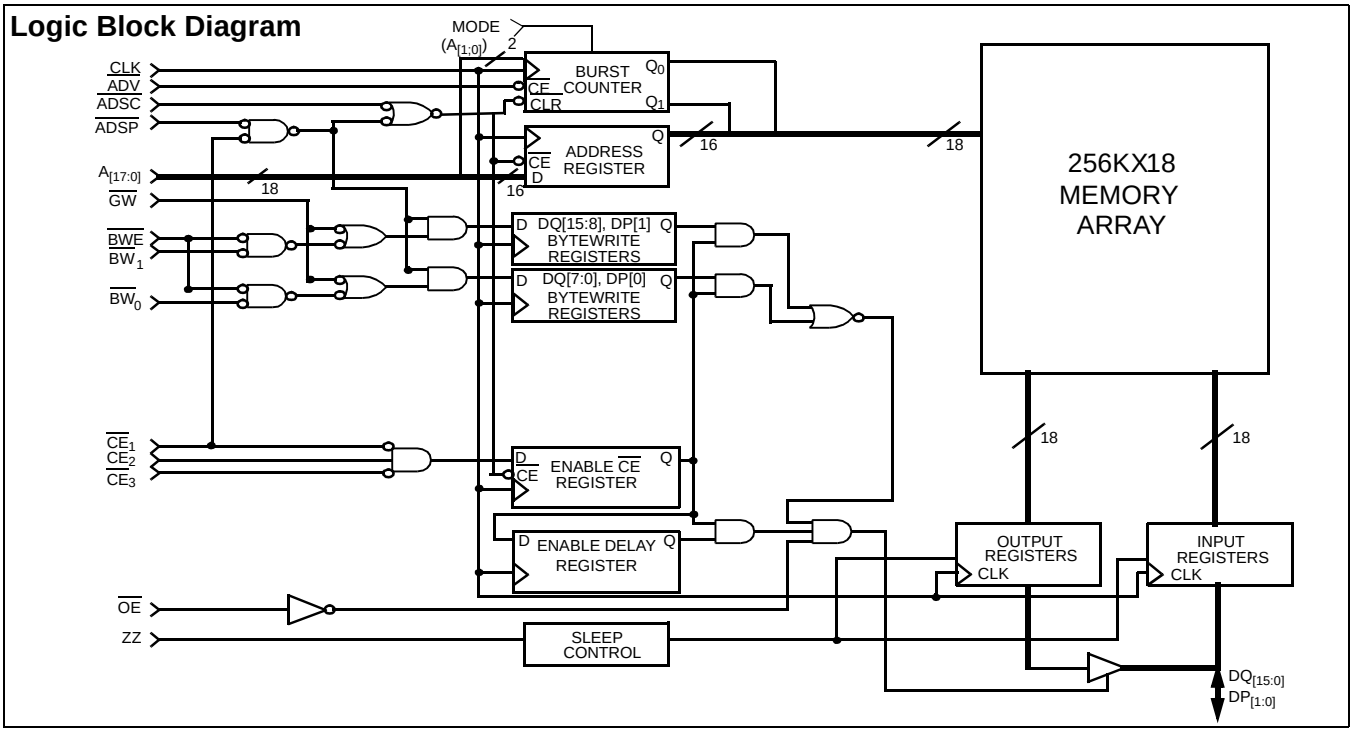
All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise is 3.5 ns (166-MHz device).

The WCSS0418V1P supports either the interleaved burst sequence used by the Intel Pentium processor or a linear burst sequence used by processors such as the PowerPC. The burst sequence is selected through the MODE pin. Accesses can be initiated by asserting either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$) at clock rise. Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A 2-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the four Byte Write Select ($\overline{BW}_{[1:0]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are conducted with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. In order to provide proper data during depth expansion, $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.

Logic Block Diagram

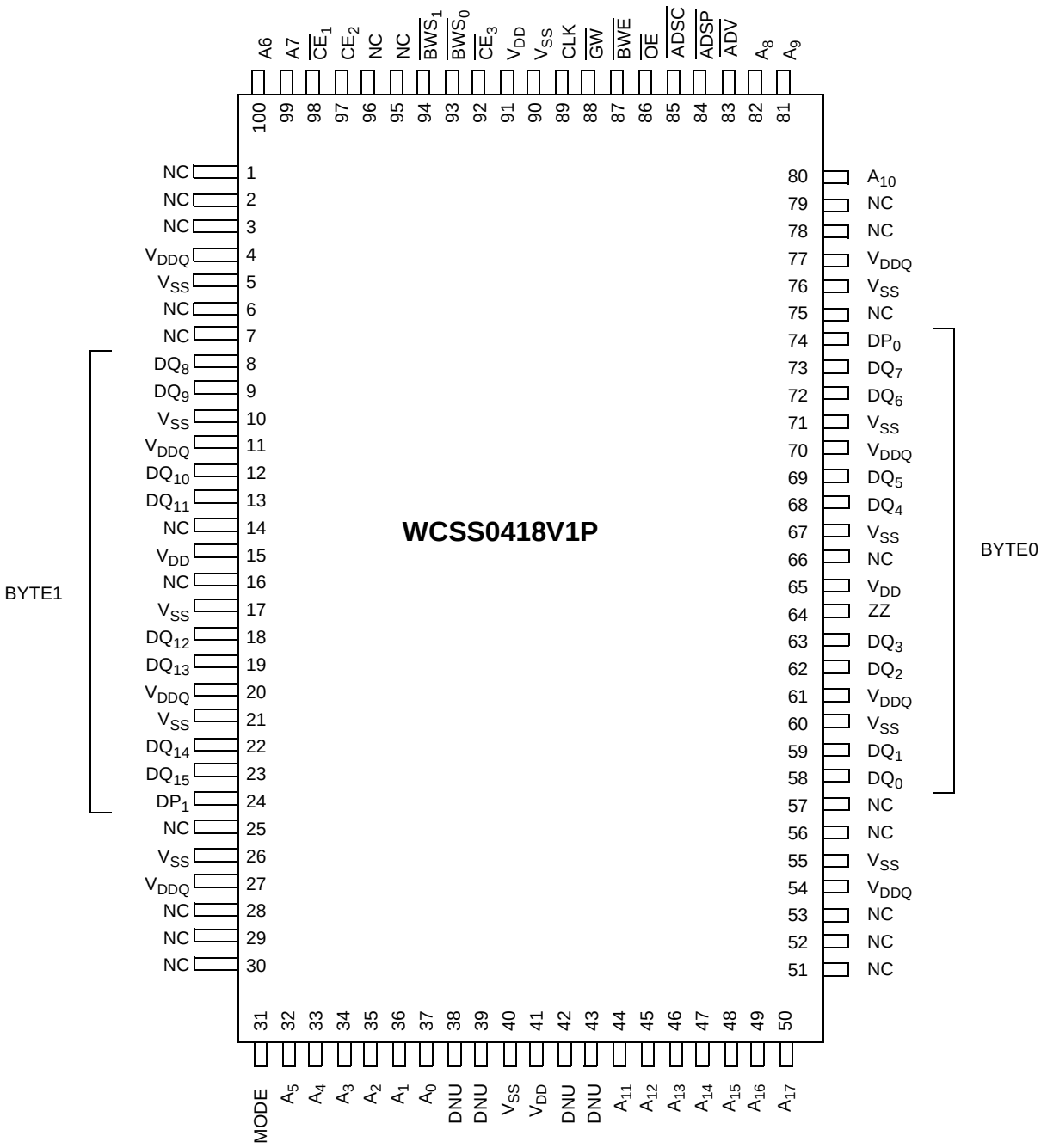


Selection Guide

		-166	-133	-100
Maximum Access Time (ns)		3.5	4.0	5.5
Maximum Operating Current (mA)	Commercial	420	375	325
Maximum CMOS Standby Current (mA)	Commercial	10	10	10

Pin Configurations

100-Lead TQFP



Pin Configurations (continued)

119-Ball BGA

	1	2	3	4	5	6	7
A	V_{DDQ}	A	A	$\overline{ADSP}$	A	A	V_{DDQ}
B	NC	CE_2	A	$\overline{ADSC}$	A	$\overline{CE_3}$	NC
C	NC	A	A	V_{DD}	A	A	NC
D	DQ_b	NC	V_{SS}	NC	V_{SS}	DQP_a	NC
E	NC	DQ_b	V_{SS}	$\overline{CE_1}$	V_{SS}	NC	DQ_a
F	V_{DDQ}	NC	V_{SS}	$\overline{OE}$	V_{SS}	DQ_a	V_{DDQ}
G	NC	DQ_b	$\overline{BW_b}$	$\overline{ADV}$	V_{ss}	NC	DQ_a
H	DQ_b	NC	V_{SS}	$\overline{GW}$	V_{SS}	DQ_a	NC
J	V_{DDQ}	V_{DD}	NC	V_{DD}	NC	V_{DD}	V_{DDQ}
K	NC	DQ_b	V_{SS}	CLK	V_{SS}	NC	DQ_a
L	DQ_b	NC	V_{ss}	NC	$\overline{BW_a}$	DQ_a	NC
M	V_{DDQ}	DQ_b	V_{SS}	$\overline{BWE}$	V_{SS}	NC	V_{DDQ}
N	DQ_b	NC	V_{SS}	A1	V_{SS}	DQ_a	NC
P	NC	DQP_b	V_{SS}	A0	V_{SS}	NC	DQ_a
R	NC	A	MODE	V_{DD}	V_{SS}	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V_{DDQ}	NC	NC	NC	NC	NC	V_{DDQ}

Pin Definitions

Name	I/O	Description
$A_{[17:0]}$	Input-Synchronous	Address Inputs used to select one of the 64K address locations. Sampled at the rising edge of the CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is active LOW, and $\overline{CE_1}$, CE_2, and $\overline{CE_3}$ are sampled active. $A_{[1:0]}$ feed the 2-bit counter.
$\overline{BW_{[1:0]}}$	Input-Synchronous	Byte Write Select Inputs, active LOW. Qualified with $\overline{BWE}$ to conduct byte writes to the SRAM. Sampled on the rising edge of CLK.
$\overline{GW}$	Input-Synchronous	Global Write Enable Input, active LOW. When asserted LOW on the rising edge of CLK, a global write is conducted (ALL bytes are written, regardless of the values on $\overline{BW_{[1:0]}}$ and $\overline{BWE}$).
$\overline{BWE}$	Input-Synchronous	Byte Write Enable Input, active LOW. Sampled on the rising edge of CLK. This signal must be asserted LOW to conduct a byte write.
CLK	Input-Clock	Clock Input. Used to capture all synchronous inputs to the device. Also used to increment the burst counter when $\overline{ADV}$ is asserted LOW, during a burst operation.
$\overline{CE_1}$	Input-Synchronous	Chip Enable 1 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with CE_2 and $\overline{CE_3}$ to select/deselect the device. $\overline{ADSP}$ is ignored if $\overline{CE_1}$ is HIGH.
CE_2	Input-Synchronous	Chip Enable 2 Input, active HIGH. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and $\overline{CE_3}$ to select/deselect the device.
$\overline{CE_3}$	Input-Synchronous	Chip Enable 3 Input, active LOW. Sampled on the rising edge of CLK. Used in conjunction with $\overline{CE_1}$ and CE_2 to select/deselect the device.
$\overline{OE}$	Input-Asynchronous	Output Enable, asynchronous input, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are three-stated, and act as input data pins. $\overline{OE}$ is masked during the first clock of a read cycle when emerging from a deselected state.
$\overline{ADV}$	Input-Synchronous	Advance Input Signal, sampled on the rising edge of CLK. When asserted, it automatically increments the address in a burst cycle.
$\overline{ADSP}$	Input-Synchronous	Address Strobe from Processor, sampled on the rising edge of CLK. When asserted LOW, $A_{[17:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized. $\overline{ASDP}$ is ignored when $\overline{CE_1}$ is deasserted HIGH.

Pin Definitions (continued)

Name	I/O	Description
$\overline{ADSC}$	Input-Synchronous	Address Strobe from Controller, sampled on the rising edge of CLK. When asserted LOW, $A_{[17:0]}$ is captured in the address registers. $A_{[1:0]}$ are also loaded into the burst counter. When $\overline{ADSP}$ and $\overline{ADSC}$ are both asserted, only $\overline{ADSP}$ is recognized.
ZZ	Input-Asynchronous	ZZ "sleep" Input. This active HIGH input places the device in a non-time critical "sleep" condition with data integrity preserved. Leaving ZZ floating or NC will default the device into an active state. ZZ pin has an internal pull-down.
$DQ_{[15:0]}$ $DP_{[1:0]}$	I/O-Synchronous	Bidirectional Data I/O lines. As inputs, they feed into an on-chip data register that is triggered by the rising edge of CLK. As outputs, they deliver the data contained in the memory location specified by $A_{[17:0]}$ during the previous clock rise of the read cycle. The direction of the pins is controlled by $\overline{OE}$. When $\overline{OE}$ is asserted LOW, the pins behave as outputs. When HIGH, $DQ_{[15:0]}$ and $DP_{[1:0]}$ are placed in a three-state condition.
V_{DD}	Power Supply	Power Supply inputs to the core of the device. Should be connected to 3.3V power supply.
V_{SS}	Ground	Ground for the core of the device. Should be connected to ground of the system.
V_{DDQ}	I/O Power Supply	Power Supply for the I/O circuitry. Should be connected to a 3.3V or 2.5V power supply.
V_{SSQ}	I/O Ground	Ground for the I/O circuitry. Should be connected to ground of the system.
MODE	Input-Static	Selects Burst Order. When tied to GND selects linear burst sequence. When tied to V_{DDQ} or left floating selects interleaved burst sequence. This is a strap pin and should remain static during device operation. When left floating or NC, defaults to interleaved burst order. Mode pin has an internal pull-up.
NC		No Connects.

Introduction

Functional Overview

All synchronous inputs pass through input registers controlled by the rising edge of the clock. All data outputs pass through output registers controlled by the rising edge of the clock. Maximum access delay from the clock rise (t_{CO}) is 3.5 ns (166-MHz device).

The WCSS0418V1P supports secondary cache in systems utilizing either a linear or interleaved burst sequence. The interleaved burst order supports Pentium and i486 processors. The linear burst sequence is suited for processors that utilize a linear burst sequence. The burst order is user selectable, and is determined by sampling the MODE input. Accesses can be initiated with either the Processor Address Strobe ($\overline{ADSP}$) or the Controller Address Strobe ($\overline{ADSC}$). Address advancement through the burst sequence is controlled by the $\overline{ADV}$ input. A two-bit on-chip wraparound burst counter captures the first address in a burst sequence and automatically increments the address for the rest of the burst access.

Byte write operations are qualified with the Byte Write Enable ($\overline{BWE}$) and Byte Write Select ($\overline{BW}_{[1:0]}$) inputs. A Global Write Enable ($\overline{GW}$) overrides all byte write inputs and writes data to all four bytes. All writes are simplified with on-chip synchronous self-timed write circuitry.

Three synchronous Chip Selects ($\overline{CE}_1$, CE_2, $\overline{CE}_3$) and an asynchronous Output Enable ($\overline{OE}$) provide for easy bank selection and output three-state control. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH.

Single Read Accesses

This access is initiated when the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ or $\overline{ADSC}$ is asserted LOW, (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active, and (3) the write signals ($\overline{GW}$, $\overline{BWE}$) are all deasserted HIGH. $\overline{ADSP}$ is ignored if $\overline{CE}_1$ is HIGH. The address presented to the address inputs ($A_{[17:0]}$) is stored into the address advancement logic and the Address Register while being presented to the memory core. The corresponding data is allowed to propagate to the input of the Output Registers. At the rising edge of the next clock the data is allowed to propagate through the output register and onto the data bus within 3.5 ns (166-MHz device) if $\overline{OE}$ is active LOW. The only exception occurs when the SRAM is emerging from a deselected state to a selected state, its outputs are always three-stated during the first cycle of the access. After the first cycle of the access, the outputs are controlled by the $\overline{OE}$ signal. Consecutive single read cycles are supported. Once the SRAM is deselected at clock rise by the chip select and either $\overline{ADSP}$ or $\overline{ADSC}$ signals, its output will three-state immediately.

Single Write Accesses Initiated by $\overline{ADSP}$

This access is initiated when both of the following conditions are satisfied at clock rise: (1) $\overline{ADSP}$ is asserted LOW, and (2) $\overline{CE}_1$, CE_2, $\overline{CE}_3$ are all asserted active. The address presented to $A_{[17:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The write signals ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW}_{[1:0]}$) and $\overline{ADV}$ inputs are ignored during this first cycle.

$\overline{ADSP}$-triggered write accesses require two clock cycles to complete. If $\overline{GW}$ is asserted LOW on the second clock rise, the data presented to the $DQ_{[15:0]}$ and $DP_{[1:0]}$ inputs is written into the corresponding address location in the RAM core. If $\overline{GW}$ is HIGH, then the write operation is controlled by $\overline{BWE}$ and $\overline{BW}_{[1:0]}$ signals. The WCSS0418V1P provides byte write capability that is described in the Write Cycle Description table. Asserting the Byte Write Enable input ($\overline{BWE}$) with the selected Byte Write ($\overline{BW}_{[1:0]}$) input will selectively write to only the desired bytes. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the WCSS0418V1P is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the $DQ_{[15:0]}$ and $DP_{[1:0]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, $DQ_{[15:0]}$ and $DP_{[1:0]}$ are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Single Write Accesses Initiated by $\overline{ADSC}$

$\overline{ADSC}$ write accesses are initiated when the following conditions are satisfied: (1) $\overline{ADSC}$ is asserted LOW, (2) ADSP is deasserted HIGH, (3) $\overline{CE_1}$, CE_2, $\overline{CE_3}$ are all asserted active, and (4) the appropriate combination of the write inputs ($\overline{GW}$, $\overline{BWE}$, and $\overline{BW_{[1:0]}}$) are asserted active to conduct a write to the desired byte(s). $\overline{ADSC}$-triggered write accesses require a single clock cycle to complete. The address presented to $A_{[17:0]}$ is loaded into the address register and the address advancement logic while being delivered to the RAM core. The $\overline{ADV}$ input is ignored during this cycle. If a global write is conducted, the data presented to the $DQ_{[15:0]}$ and $DP_{[1:0]}$ is written into the corresponding address location in the RAM core. If a byte write is conducted, only the selected bytes are written. Bytes not selected during a byte write operation will remain unaltered. A synchronous self-timed write mechanism has been provided to simplify the write operations.

Because the WCSS0418V1P is a common I/O device, the Output Enable ($\overline{OE}$) must be deasserted HIGH before presenting data to the $DQ_{[15:0]}$ and $DP_{[1:0]}$ inputs. Doing so will three-state the output drivers. As a safety precaution, $DQ_{[15:0]}$ and $DP_{[1:0]}$ are automatically three-stated whenever a write cycle is detected, regardless of the state of $\overline{OE}$.

Burst Sequences

The WCSS0418V1P provides a two-bit wraparound counter, fed by $A_{[1:0]}$, that implements either an interleaved or linear burst sequence. The interleaved burst sequence is designed specifically to support Intel Pentium applications. The linear burst sequence is designed to support processors that follow a linear burst sequence. The burst sequence is user selectable through the MODE input.

Asserting $\overline{ADV}$ LOW at clock rise will automatically increment the burst counter to the next address in the burst sequence. Both read and write burst operations are supported.

Interleaved Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	00	11	10
10	11	00	01
11	10	01	00

Linear Burst Sequence

First Address	Second Address	Third Address	Fourth Address
$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$	$A_{[1:0]}$
00	01	10	11
01	10	11	00
10	11	00	01
11	00	01	10

Sleep Mode

The ZZ input pin is an asynchronous input. Asserting ZZ places the SRAM in a power conservation “sleep” mode. Two clock cycles are required to enter into or exit from this “sleep” mode. While in this mode, data integrity is guaranteed. Accesses pending when entering the “sleep” mode are not considered valid nor is the completion of the operation guaranteed. The device must be deselected prior to entering the “sleep” mode. $\overline{CE_1}$, CE_2, $\overline{CE_3}$, $\overline{ADSP}$, and $\overline{ADSC}$ must remain inactive for the duration of t_{ZZREC} after the ZZ input returns LOW.

ZZ Mode Electrical Characteristics

Parameter	Description	Test Conditions	Min.	Max.	Unit
I_{DDZZ}	Snooze mode standby current	$ZZ \geq V_{DD} - 0.2V$		3	mA
t_{ZZS}	Device operation to ZZ	$ZZ \geq V_{DD} - 0.2V$		$2t_{CYC}$	ns
t_{ZZREC}	ZZ recovery time	$ZZ \leq 0.2V$	$2t_{CYC}$		ns

Cycle Descriptions[1, 2, 3]

Next Cycle	Add. Used	ZZ	$\overline{CE_3}$	CE_2	$\overline{CE_1}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{OE}$	DQ	Write
Unselected	None	L	X	X	1	X	0	X	X	Hi-Z	X
Unselected	None	L	1	X	0	0	X	X	X	Hi-Z	X
Unselected	None	L	X	0	0	0	X	X	X	Hi-Z	X
Unselected	None	L	1	X	0	1	0	X	X	Hi-Z	X
Unselected	None	L	X	0	0	1	0	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	0	X	X	X	Hi-Z	X
Begin Read	External	L	0	1	0	1	0	X	X	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	X	1	1	0	0	DQ	Read
Continue Read	Next	L	X	X	1	X	1	0	1	Hi-Z	Read
Continue Read	Next	L	X	X	1	X	1	0	0	DQ	Read
Suspend Read	Current	L	X	X	X	1	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	X	1	1	1	0	DQ	Read
Suspend Read	Current	L	X	X	1	X	1	1	1	Hi-Z	Read
Suspend Read	Current	L	X	X	1	X	1	1	0	DQ	Read
Begin Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Begin Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
Begin Write	External	L	0	1	0	1	0	X	X	Hi-Z	Write
Continue Write	Next	L	X	X	X	1	1	0	X	Hi-Z	Write
Continue Write	Next	L	X	X	1	X	1	0	X	Hi-Z	Write
Suspend Write	Current	L	X	X	X	1	1	1	X	Hi-Z	Write
Suspend Write	Current	L	X	X	1	X	1	1	X	Hi-Z	Write
ZZ “Sleep”	None	H	X	X	X	X	X	X	X	Hi-Z	X

Notes:

1. X = “Don't Care,” 1 = HIGH, 0 = LOW.
2. Write is defined by $\overline{BWE}$, $\overline{BW_{[1:0]}}$, and $\overline{GW}$. See Write Cycle Description table.
3. The DQ pins are controlled by the current cycle and the $\overline{OE}$ signal. $\overline{OE}$ is asynchronous and is not sampled with the clock.

Write Cycle Description[4, 5, 6]

Function	$\overline{GW}$	$\overline{BWE}$	$\overline{BW_3}$	$\overline{BW_2}$	$\overline{BW_1}$	$\overline{BW_0}$
Read	1	1	X	X	X	X
Read	1	0	1	1	1	1
Write Byte 0 - $DQ_{[7:0]}$	1	0	1	1	1	0
Write Byte 1 - $DQ_{[15:8]}$	1	0	1	1	0	1
Write Bytes 1, 0	1	0	1	1	0	0
Write Byte 2 - $DQ_{[23:16]}$	1	0	1	0	1	1
Write Bytes 2, 0	1	0	1	0	1	0
Write Bytes 2, 1	1	0	1	0	0	1
Write Bytes 2, 1, 0	1	0	1	0	0	0
Write Byte 3 - $DQ_{[31:24]}$	1	0	0	1	1	1
Write Bytes 3, 0	1	0	0	1	1	0
Write Bytes 3, 1	1	0	0	1	0	1
Write Bytes 3, 1, 0	1	0	0	1	0	0
Write Bytes 3, 2	1	0	0	0	1	1
Write Bytes 3, 2, 0	1	0	0	0	1	0
Write Bytes 3, 2, 1	1	0	0	0	0	1
Write All Bytes	1	0	0	0	0	0
Write All Bytes	0	X	X	X	X	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied..... –55°C to +125°C

Supply Voltage on V_{DD} Relative to GND.....–0.5V to +4.6V

DC Voltage Applied to Outputs in High Z State[7] ..... –0.5V to V_{DD} + 0.5V

DC Input Voltage[7]..... –0.5V to V_{DD} + 0.5V

Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current..... >200 mA

Operating Range

Range	Ambient Temperature[8]	V_{DD}	V_{DDQ}
Com'l	0°C to +70°C	3.3V –5%/+10%	2.5V –5% 3.3V +10%
Industrial	–40°C to +85°C		

Notes:

4. X = "Don't Care," 1 = Logic HIGH, 0 = Logic LOW.
5. The SRAM always initiates a read cycle when ADSP asserted, regardless of the state of $\overline{GW}$, $\overline{BWE}$, or $\overline{BW}_{[1:0]}$. Writes may occur only on subsequent clocks after the ADSP or with the assertion of ADSC. As a result, $\overline{OE}$ must be driven HIGH prior to the start of the write cycle to allow the outputs to three-state. $\overline{OE}$ is a don't care for the remainder of the write cycle.
6. $\overline{OE}$ is asynchronous and is not sampled with the clock rise. It is masked internally during write cycles. During a read cycle $DQ_{[15:0]}$;$DP_{[1:0]}$ = High-Z when $\overline{OE}$ is inactive or when the device is deselected, and $DQ_{[15:0]}$;$DP_{[1:0]}$ = data when $\overline{OE}$ is active.
7. Minimum voltage equals –2.0V for pulse durations of less than 20 ns.
8. T_A is the case temperature.

Electrical Characteristics Over the Operating Range

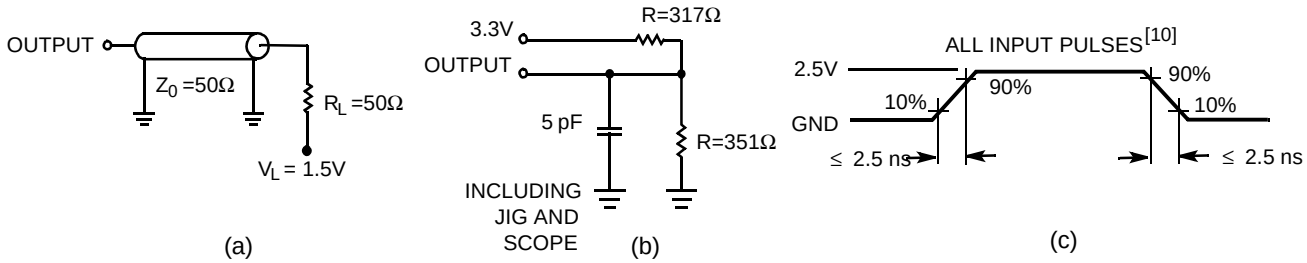
Parameter	Description	Test Conditions		Min.	Max.	Unit
V_{DD}	Power Supply Voltage	3.3V –5%/+10%		3.135	3.6	V
V_{DDQ}	I/O Supply Voltage	2.5V –5% to 3.3V +10%		2.375	3.6	V
V_{OH}	Output HIGH Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OH} = –4.0 mA		2.4		V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OH} = –2.0 mA		2.0		V
V_{OL}	Output LOW Voltage	V_{DDQ} = 3.3V, V_{DD} = Min., I_{OL} = 8.0 mA			0.4	V
		V_{DDQ} = 2.5V, V_{DD} = Min., I_{OL} = 2.0 mA			0.7	V
V_{IH}	Input HIGH Voltage	V_{DDQ} = 3.3V		2.0	V_{DD} + 0.3V	V
V_{IH}	Input HIGH Voltage	V_{DDQ} = 2.5V		1.7	V_{DD} + 0.3V	V
V_{IL}	Input LOW Voltage[7]	V_{DDQ} = 3.3V		–0.3	0.8	V
V_{IL}	Input LOW Voltage[7]	V_{DDQ} = 2.5V		–0.3	0.7	V
I_X	Input Load Current except ZZ and MODE	GND ≤ V_I ≤ V_{DDQ}		–5	5	µA
	Input Current of MODE	Input = V_{SS}		–30		µA
		Input = V_{DDQ}			5	µA
	Input Current of ZZ	Input = V_{SS}		–5		µA
		Input = V_{DDQ}			30	µA
I_{OZ}	Output Leakage Current	GND ≤ V_I ≤ V_{DDQ}, Output Disabled		–5	5	µA
I_{DD}	V_{DD} Operating Supply Current	V_{DD} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		420	mA
			7.5-ns cycle, 133 MHz		375	mA
			10-ns cycle, 100 MHz		325	mA
I_{SB1}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL} f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		150	mA
			7.5-ns cycle, 133 MHz		125	mA
			10-ns cycle, 100 MHz		115	mA
I_{SB2}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V, f = 0			10	mA
I_{SB3}	Automatic CS Power-Down Current—CMOS Inputs	Max. V_{DD}, Device Deselected, or V_{IN} ≤ 0.3V or V_{IN} ≥ V_{DDQ} – 0.3V f = f_{MAX} = $1/t_{CYC}$	6-ns cycle, 166 MHz		120	mA
			7.5-ns cycle, 133 MHz		95	mA
			10-ns cycle, 100 MHz		85	mA
I_{SB4}	Automatic CS Power-Down Current—TTL Inputs	Max. V_{DD}, Device Deselected, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = 0			18	mA

Capacitance[9]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V, V_{DDQ} = 3.3V	4	pF
C_{CLK}	Clock Input Capacitance		4	pF
$C_{I/O}$	Input/Output Capacitance		4	pF

Note:
9. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[11, 12, 13]

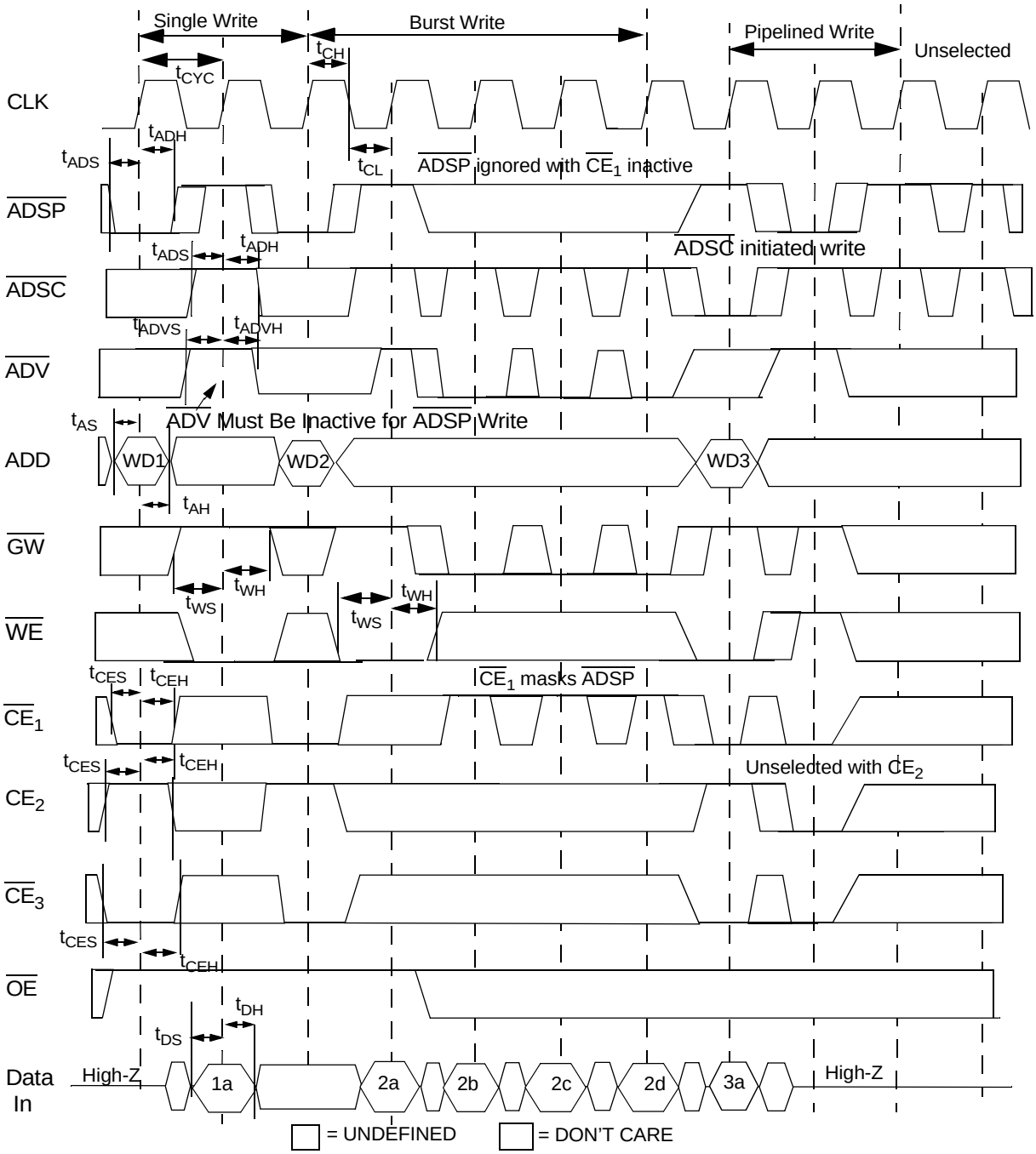
Parameter	Description	-166		-133		-100		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{CYC}	Clock Cycle Time	6.0		7.5		10		ns
t_{CH}	Clock HIGH	1.7		1.9		3.5		ns
t_{CL}	Clock LOW	1.7		1.9		3.5		ns
t_{AS}	Address Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{AH}	Address Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CO}	Data Output Valid After CLK Rise		3.5		4.0		5.5	ns
t_{DOH}	Data Output Hold After CLK Rise	1.5		2.0		2.0		ns
t_{ADS}	$\overline{ADSP}$, $\overline{ADSC}$ Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{ADH}	$\overline{ADSP}$, $\overline{ADSC}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{WES}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}_{[1:0]}$ Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{WEH}	$\overline{BWE}$, $\overline{GW}$, $\overline{BW}_{[1:0]}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{ADVS}	$\overline{ADV}$ Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{ADVH}	$\overline{ADV}$ Hold After CLK Rise	0.5		0.5		0.5		ns
t_{DS}	Data Input Set-Up Before CLK Rise	2.0		2.5		2.5		ns
t_{DH}	Data Input Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CES}	Chip Select Set-Up	2.0		2.5		2.5		ns
t_{CEH}	Chip Select Hold After CLK Rise	0.5		0.5		0.5		ns
t_{CHZ}	Clock to High-Z[12]		3.5		3.5		3.5	ns
t_{CLZ}	Clock to Low-Z[12]	0		0		0		ns
t_{EOHZ}	$\overline{OE}$ HIGH to Output High-Z[12, 13]		3.5		3.5		5.5	ns
t_{EOLZ}	$\overline{OE}$ LOW to Output Low-Z[12, 13]	0		0		0		ns
t_{EOV}	$\overline{OE}$ LOW to Output Valid[12]		3.5		4.0		5.5	ns

Notes:

10. Input waveform should have a slew rate of 1 V/ns.
11. Unless otherwise noted, test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and load capacitance. Shown in (a) and (b) of AC Test Loads.
12. t_{CHZ}, t_{CLZ}, t_{EOV}, t_{EOLZ}, and t_{EOHZ} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
13. At any given voltage and temperature, t_{EOHZ} is less than t_{EOLZ} and t_{CHZ} is less than t_{CLZ}.

Switching Waveforms

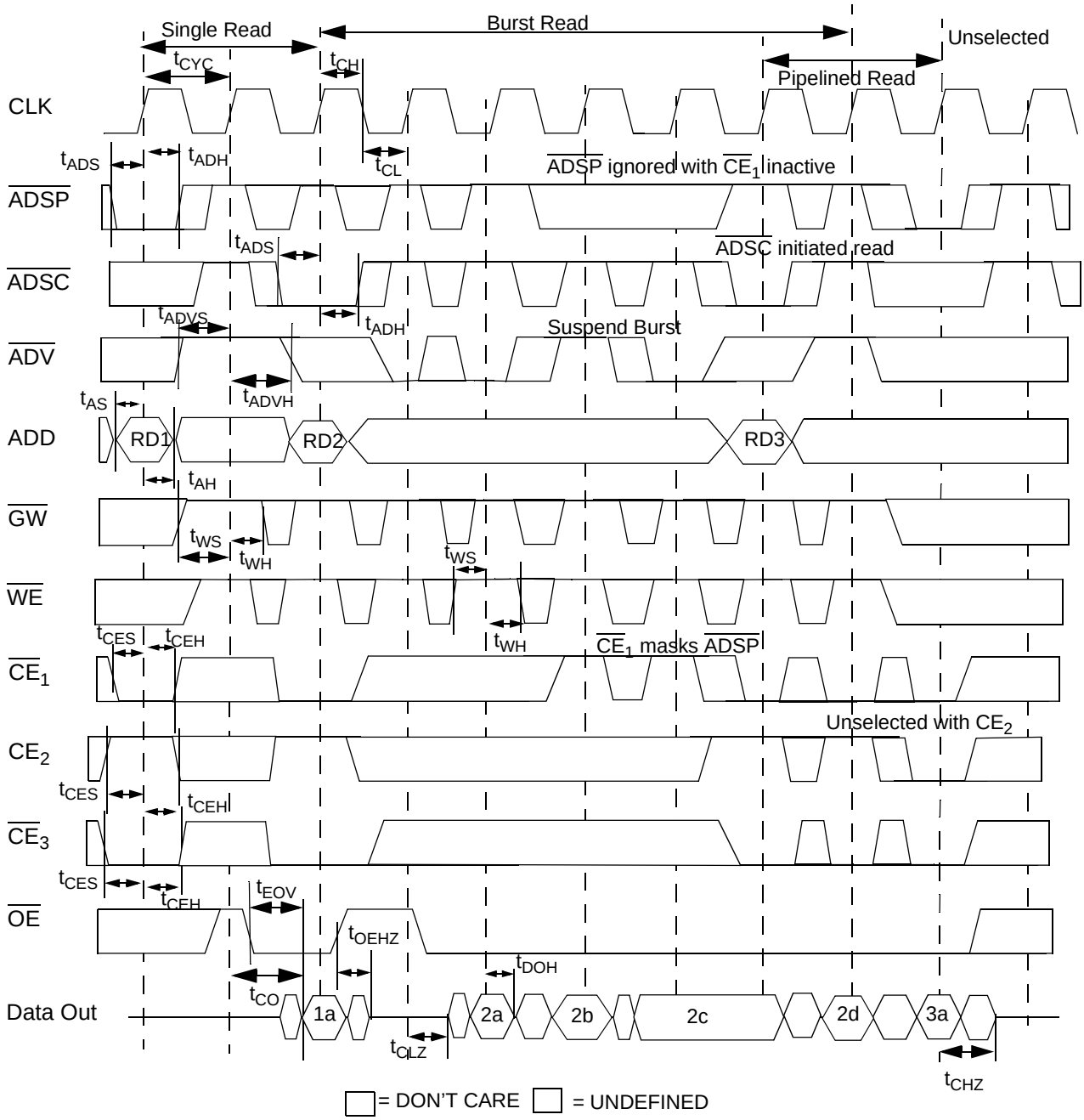
Write Cycle Timing[14, 15]



Notes:
14. $\overline{WE}$ is the combination of $\overline{BWE}$, $\overline{BW}_{[1:0]}$, and $\overline{GW}$ to define a write cycle (see Write Cycle Description table).
15. WDx stands for Write Data to Address X.

Switching Waveforms (continued)

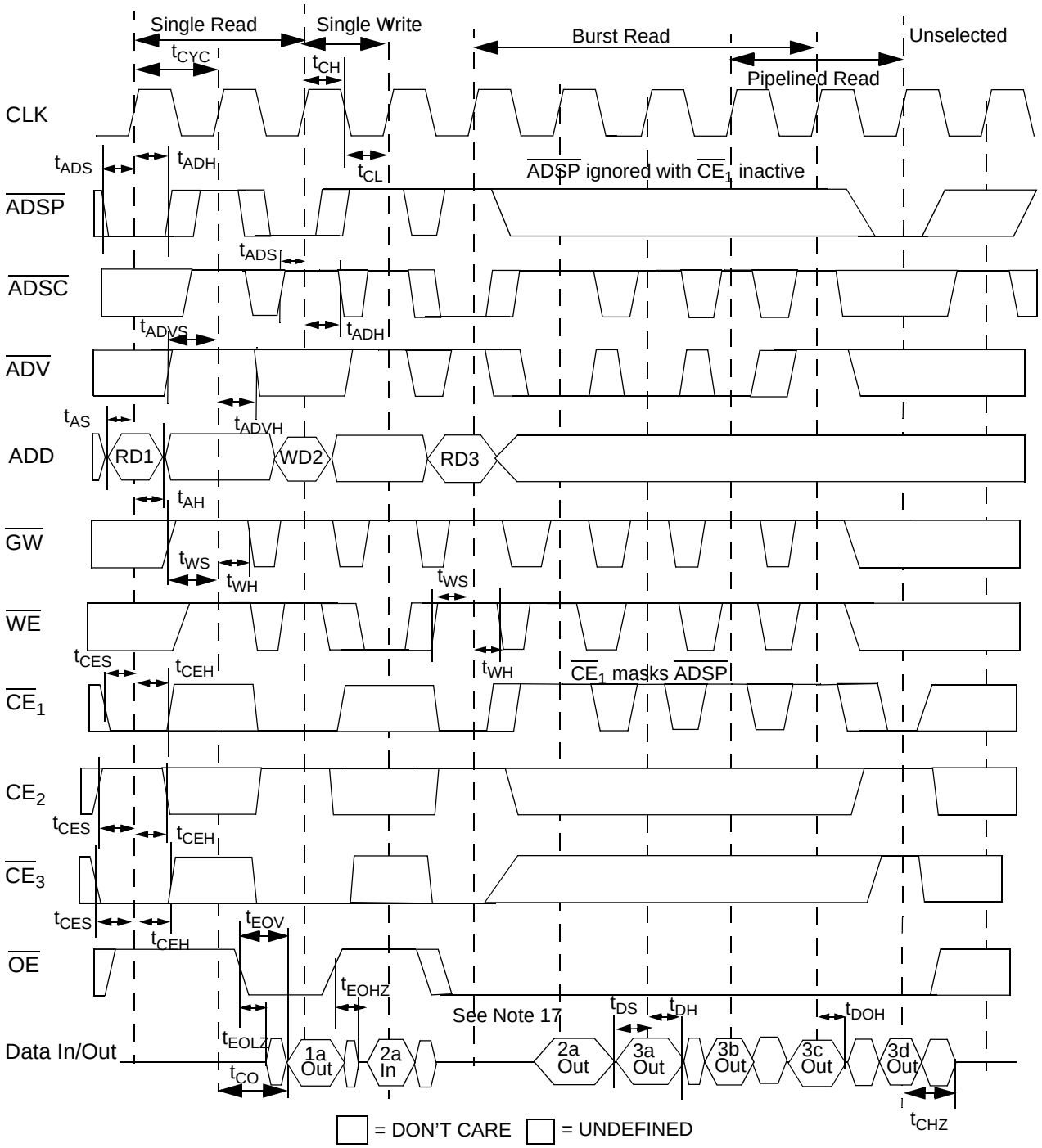
Read Cycle Timing[14, 16]



Note:
16. RDx stands for Read Data from Address X.

Switching Waveforms (continued)

Read/Write Cycle Timing[14, 15, 16, 17]

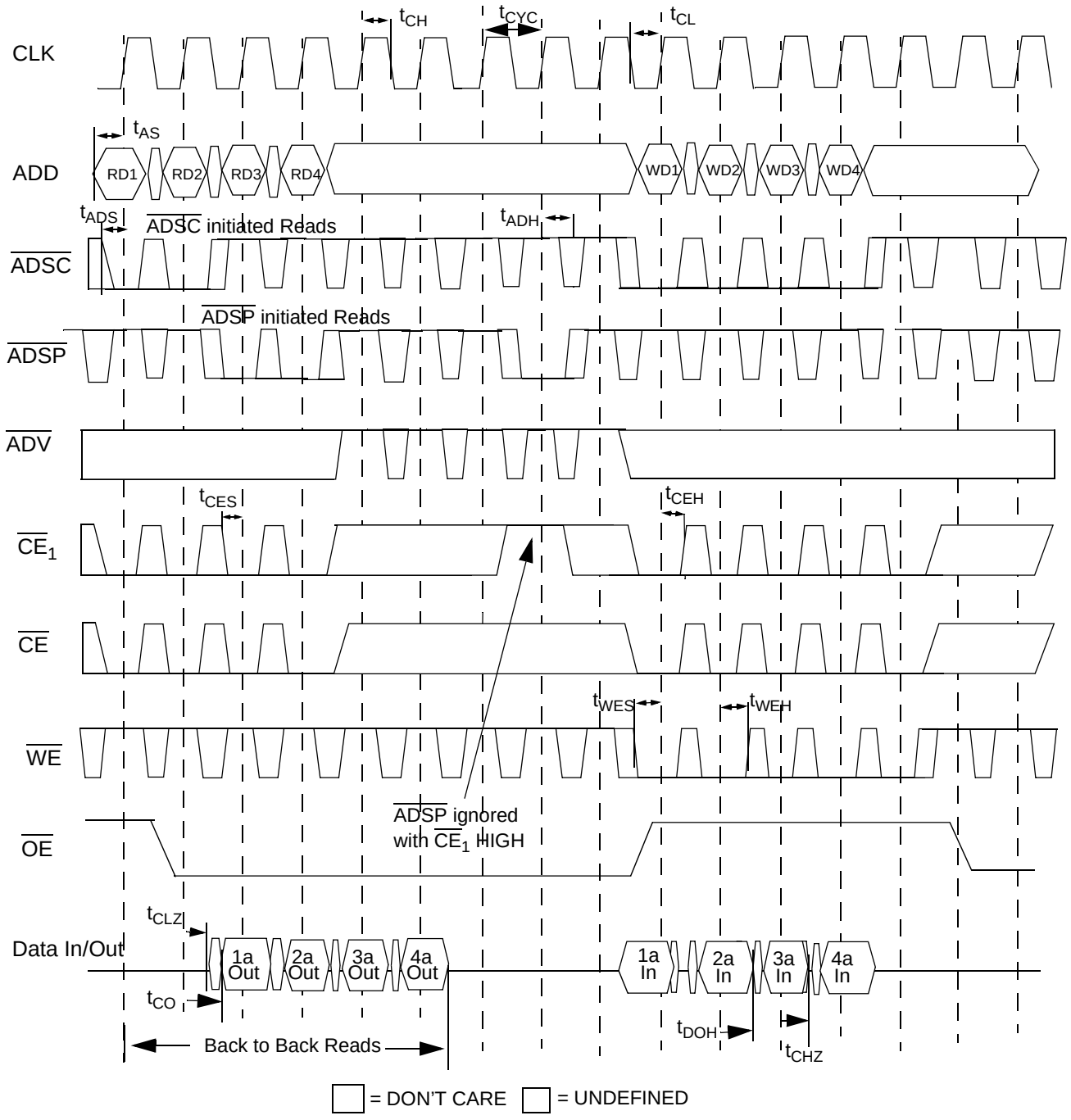


Note:

17. Data bus is driven by SRAM, but data is not guaranteed.

Switching Waveforms (continued)

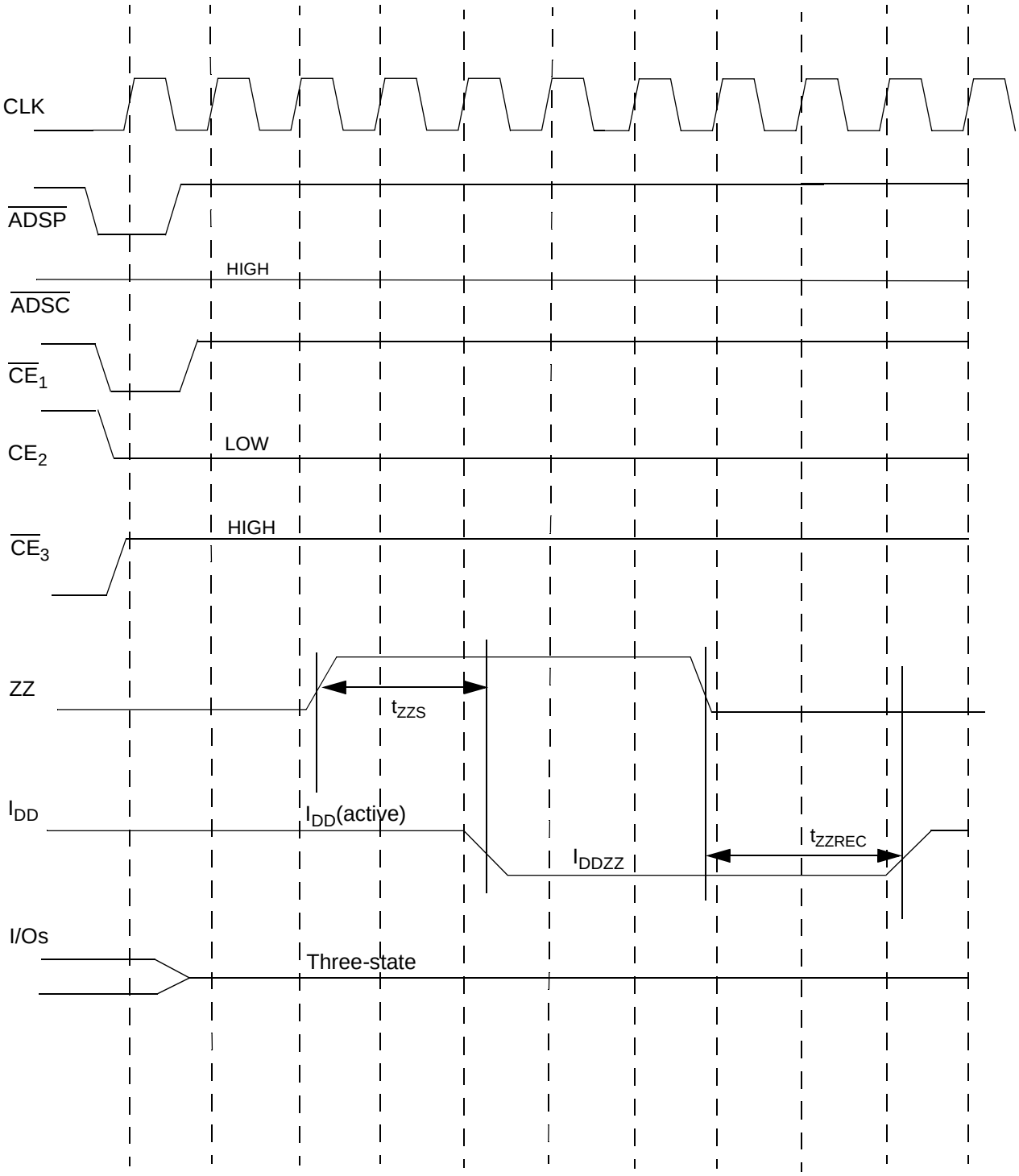
Pipeline Timing[18, 19]



Notes:
18. Device originally deselected.
19. CE is the combination of CE_2 and $\overline{CE_3}$. All chip selects need to be active in order to select the device.

Switching Waveforms (continued)

ZZ Mode Timing[20, 21]



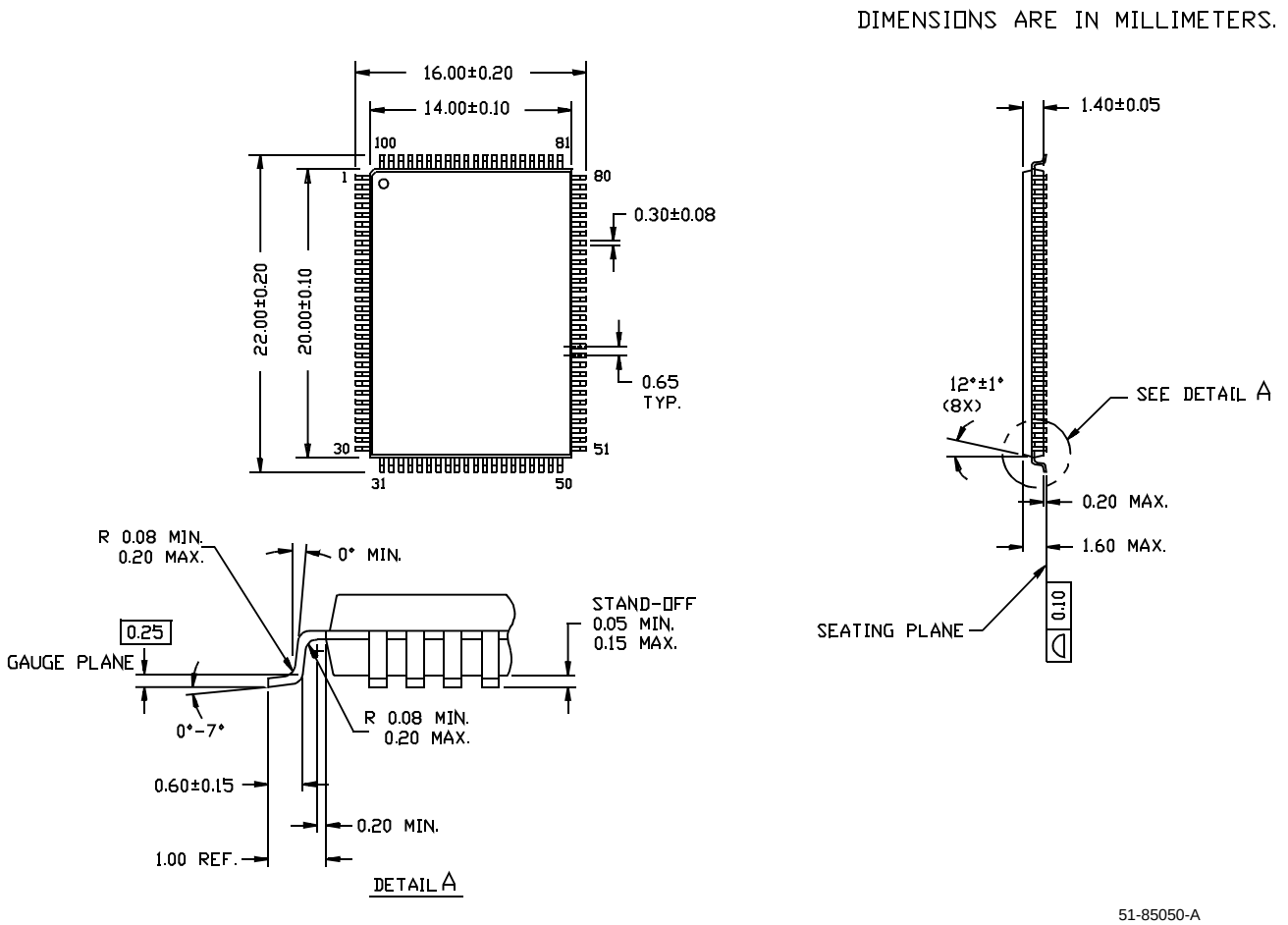
Notes:
20. Device must be deselected when entering “ZZ” mode. See Cycle Description table for all possible signal conditions to deselect the device.
21. I/Os are in three-state when exiting “ZZ” sleep mode.

Ordering Information

Speed (MHz)	Ordering Code	Package Name	Package Type	Operating Range
166	WCSS0418V1P-166AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	WCSS0418V1P-166BGC	BG119	119-Ball BGA	
133	WCSS0418V1P-133AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	WCSS0418V1P-133BGC	BG119	119-Ball BGA	
	WCSS0418V1P-133AI	A101	100-Lead Thin Quad Flat Pack	Industrial
	WCSS0418V1P-133BGI	BG119	119-Ball BGA	
100	WCSS0418V1P-100AC	A101	100-Lead Thin Quad Flat Pack	Commercial
	WCSS0418V1P-100BGC	BG119	119-Ball BGA	
	WCSS0418V1P-100AI	A101	100-Lead Thin Quad Flat Pack	Industrial
	WCSS0418V1P-100BGI	BG119	119-Ball BGA	

Package Diagrams

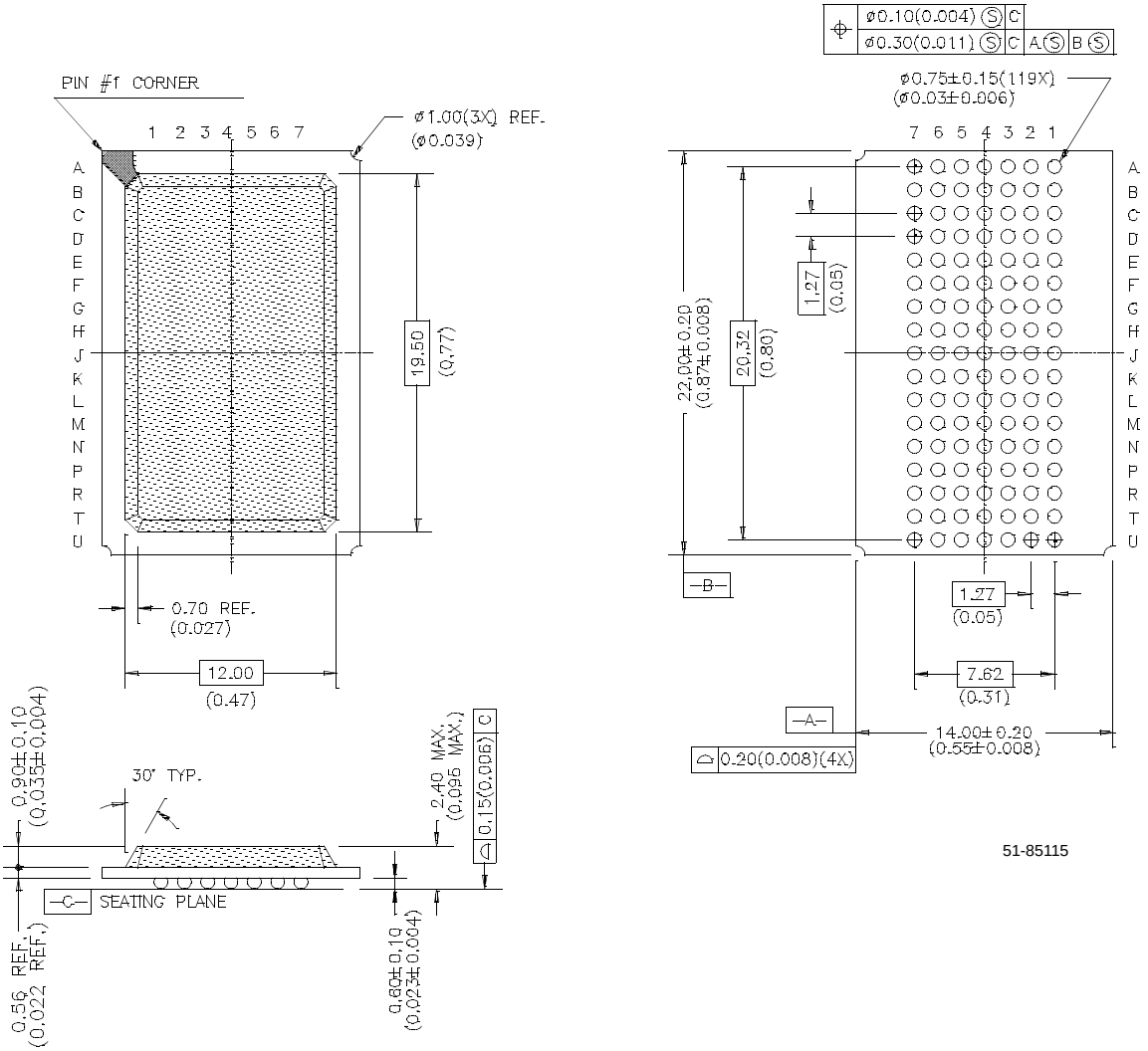
100-Pin Thin Plastic Quad Flatpack (14 x 20 x 1.4 mm) A101



Package Diagrams (continued)

119-Lead FBGA (14 x 22 x 2.4 mm) BG119

DIMENSION IN MILLIMETERS (INCHES)



Document Title: CY7C1327B 256K x 18 Synchronous-Pipelined Cache RAM Document Number: 38-05140				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	109884	09/10/01	SZV	Change from Spec number: 38-00935 to 38-05140
New	113310	02/04/02	GLC	Change from Spec number: 38-05140 to 38-05247