# plerow™ ALN1220AT

## Internally Matched LNA Module

## Features

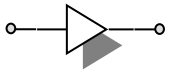
- $S_{21}$ = 19.0 dB @ 940 MHz
  = 16.0 dB @ 1500 MHz
- NF of 0.65 dB over Frequency
- Unconditionally Stable
- Single 5V Supply
- High OIP3 @ Low Current

## Description

The plerow™ ALN-series is the compactly designed surface-mount module for the use of the LNA with or without the following gain blocks in the infrastructure equipment of the mobile wireless (CDMA, GSM, PCS, PHS, WCDMA, DMB, WLAN, WiBro, WiMAX), GPS, satellite communication terminals, CATV and so on. It has an exceptional performance of low noise figure, high gain, high OIP3, and low bias current. The stability factor is always kept more than unity over the application band in order to ensure its unconditionally stable implementation to the application system environment. The surface-mount module package including the completed matching circuit and other components necessary just in case allows very simple and convenient implementation onto the system board in mass production level.

RoHS-compliant



1-stage Single Type

## Specifications (in Production)

Typ. @ T = 25°C, $V_s$ = 5 V, Freq. =1220 MHz, $Z_{o.sys}$ = 50 ohm

| Parameter | Unit | Specifications | | |
|---|---|---|---|---|
| | | Min | Typ | Max |
| Frequency Range | MHz | 940 | | 1500 |
| Gain | dB | 16.5 | 17.5 | |
| Gain Flatness | dB | | ± 1.5 | ± 1.6 |
| Noise Figure | dB | | 0.65 | 0.70 |
| Output IP3 (1) | dBm | 27 | 28 | |
| S11 / S22 (2) | dB | | | -13 / -8 |
| Output P1dB | dBm | 14 | 15 | |
| Switching Time (3) | μsec | | | |
| Supply Current | mA | | 40 | 60 |
| Supply Voltage | V | | 5 | |
| Impedance | Ω | | 50 | |
| Max. RF Input Power | dBm | C.W 29 ~ 31 (before fail) | | |
| Package Type & Size | mm | Surface Mount Type, 10Wx10Lx3.8H | | |

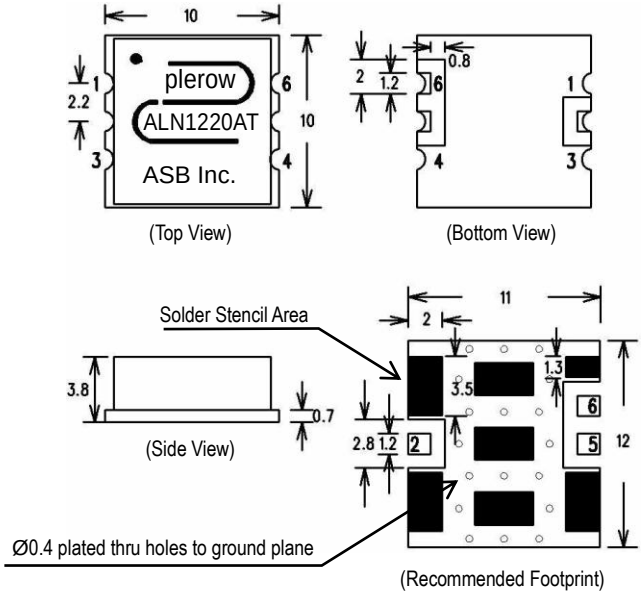
Operating temperature is -40°C to +85°C.
1) OIP3 is measured with two tones at an output power of +0 dBm / tone separated by 1 MHz.
2) S11/S22 (max) is the worst value within the frequency band.
3) Switching time means the time that takes for output power to get stabilized to its final level after switching DC voltage from 0 V to $V_S$.

## More Information


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## Outline Drawing (Unit: mm)




| Pin Number | Function |
|---|---|
| 2 | RF In |
| 5 | RF Out |
| 6 | Vs |
| Others | Ground |

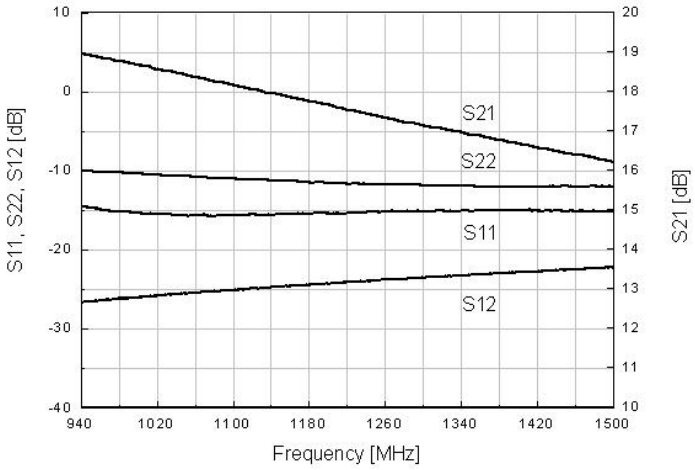
Note: 1. The number and size of ground via holes in a circuit board is critical for thermal RF grounding considerations.
2. We recommend that the ground via holes be placed on the bottom of all ground pins for better RF and thermal performance, as shown in the drawing at the left side.

## Typical Performance (Measured)

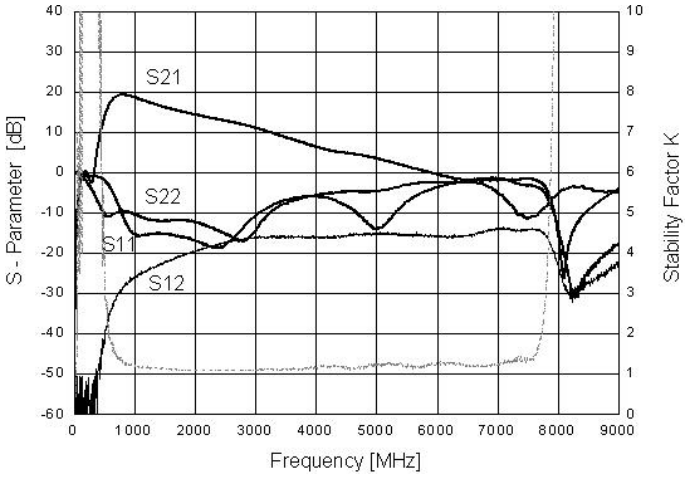
940~1500 MHz

+5 V

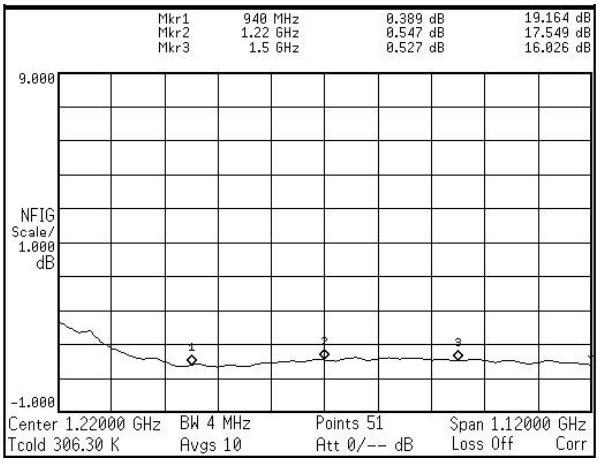
## S-parameters



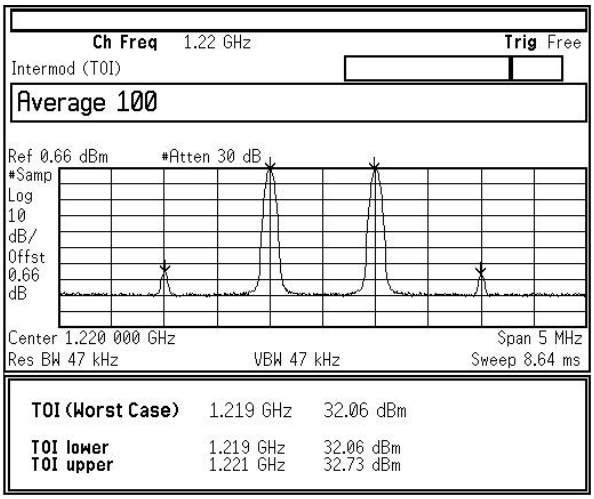

## S-parameters & K Factor



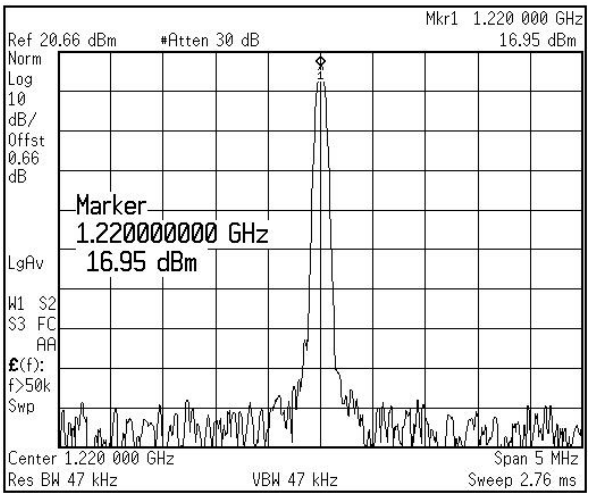

## Noise Figure




## OIP3




## P1dB



## RF Performance with Voltage Change

**1. S-parameter**

| | 940 MHz | | | 1220 MHz | | | | 1500 MHz | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | S21 (dB) | S11 (dB) | S22 (dB) | S21 (dB) | G/F (dB) | S11 (dB) | S22 (dB) | S21 (dB) | S11 (dB) | S22 (dB) |
| **4.50 V** | 18.86 | -13.77 | -9.652 | 17.42 | 2.76 | -14.66 | -11.46 | 16.10 | -14.62 | -12.03 |
| **4.75 V** | 18.91 | -14.16 | -9.841 | 17.47 | 2.75 | -15.04 | -11.58 | 16.16 | -14.95 | -12.02 |
| **5.00 V** | 18.94 | -14.47 | -9.995 | 17.51 | 2.75 | -15.40 | -11.67 | 16.19 | -15.26 | -12.01 |
| **5.25 V** | 18.97 | -14.79 | -10.12 | 17.53 | 2.75 | -15.73 | -11.76 | 16.22 | -15.50 | -11.95 |
| **5.50 V** | 18.99 | -15.06 | -10.26 | 17.55 | 2.75 | -16.00 | -11.86 | 16.24 | -15.75 | -11.88 |

**2. OIP3, P1dB & NF**

| | 940 MHz | | | 1220 MHz | | | 1500 MHz | | |
|---|---|---|---|---|---|---|---|---|---|
| | OIP3 (dBm) | P1dB (dBm) | NF (dB) | OIP3 (dBm) | P1dB (dBm) | NF (dB) | OIP3 (dBm) | P1dB (dBm) | NF (dB) |
| **4.50 V** | 27.62 | 14.70 | 0.380 | 30.47 | 15.83 | 0.577 | 31.26 | 16.51 | 0.527 |
| **4.75 V** | 28.75 | 15.45 | 0.390 | 31.50 | 16.25 | 0.570 | 32.07 | 17.11 | 0.537 |
| **5.00 V** | 29.10 | 16.06 | 0.398 | 32.06 | 16.95 | 0.547 | 32.74 | 17.60 | 0.527 |
| **5.25 V** | 29.44 | 16.52 | 0.417 | 32.47 | 17.20 | 0.570 | 33.15 | 18.05 | 0.531 |
| **5.50 V** | 29.87 | 17.00 | 0.422 | 32.96 | 17.85 | 0.565 | 33.51 | 18.45 | 0.545 |

**Note: tested at room temperature.**

## RF Performance with Operating Temperature

**1. S-parameter**

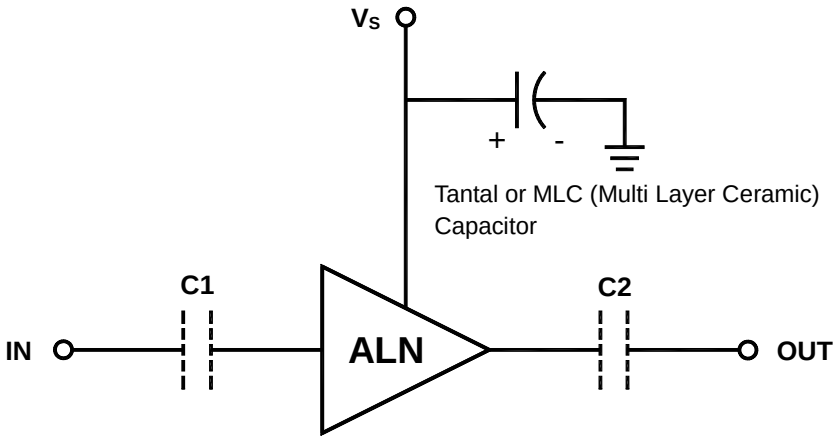
| | 940 MHz | | | 1220 MHz | | | | 1500 MHz | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | S21 (dB) | S11 (dB) | S22 (dB) | S21 (dB) | G/F (dB) | S11 (dB) | S22 (dB) | S21 (dB) | S11 (dB) | S22 (dB) |
| **-45 °C** | 19.16 | -13.02 | -10.62 | 17.75 | 2.70 | -15.85 | -11.37 | 16.46 | -17.38 | -11.29 |
| **-10 °C** | 19.04 | -13.95 | -10.20 | 17.65 | 2.71 | -15.62 | -11.40 | 16.33 | -16.29 | -11.97 |
| **25 °C** | 18.94 | -14.33 | -9.947 | 17.53 | 2.70 | -14.92 | -11.30 | 16.24 | -15.05 | -12.10 |
| **60 °C** | 18.82 | -14.56 | -9.752 | 17.40 | 2.71 | -14.57 | -11.12 | 16.11 | -14.66 | -11.95 |
| **85 °C** | 18.67 | -14.72 | -9.664 | 17.24 | 2.71 | -14.25 | -11.05 | 15.96 | -14.24 | -11.83 |

**2. OIP3, P1dB & NF**

| | 940 MHz | | | 1220 MHz | | | 1500 MHz | | |
|---|---|---|---|---|---|---|---|---|---|
| | OIP3 (dBm) | P1dB (dBm) | NF (dB) | OIP3 (dBm) | P1dB (dBm) | NF (dB) | OIP3 (dBm) | P1dB (dBm) | NF (dB) |
| **-45 °C** | 29.48 | 16.17 | 0.297 | 31.70 | 16.93 | 0.384 | 32.85 | 17.46 | 0.378 |
| **-10 °C** | 29.45 | 16.20 | 0.404 | 31.55 | 16.94 | 0.556 | 32.78 | 17.40 | 0.542 |
| **25 °C** | 29.35 | 16.26 | 0.450 | 31.45 | 16.96 | 0.579 | 32.75 | 17.38 | 0.603 |
| **60 °C** | 28.84 | 16.05 | 0.650 | 31.20 | 16.72 | 0.684 | 32.70 | 17.12 | 0.725 |
| **85 °C** | 28.35 | 15.87 | 0.772 | 30.76 | 16.51 | 0.784 | 32.15 | 16.67 | 0.805 |

**Note: tested at $V_s$= 5V.**

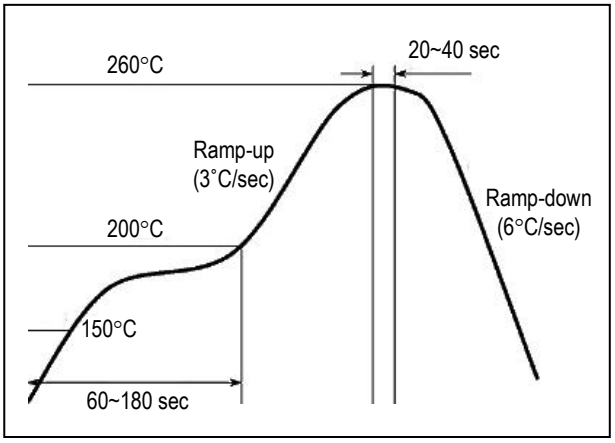
## Application Circuit



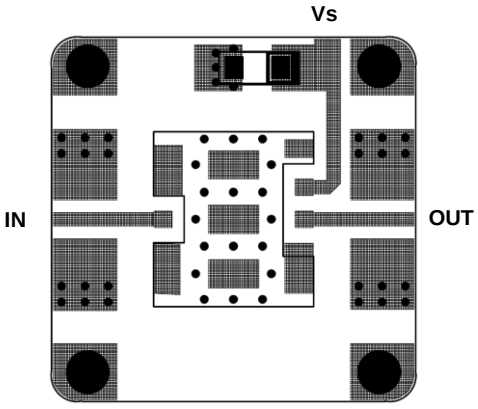

1) The tantal or MLC (Multi Layer Ceramic) capacitor is optional and for bypassing the AC noise introduced from the DC supply. The capacitance value may be determined by customer's DC supply status. The capacitor should be placed as close as possible to $V_s$ pin and be connected directly to the ground plane for the best electrical performance.

2) DC blocking capacitors are always necessarily placed at the input and output port for allowing only the RF signal to pass and blocking the DC component in the signal. The DC blocking capacitors are included inside the ALN module. Therefore, C1 & C2 capacitors may not be necessary, but can be added just in case that the customer wants. The value of C1 & C2 is determined by considering the application frequency.

## Recommended Soldering Reflow Process




## Evaluation Board Layout




Size 25x25mm
(for ALN-AT, BT, T Series – 10x10mm)