CY28346

Clock Synthesizer with Differential CPU Outputs

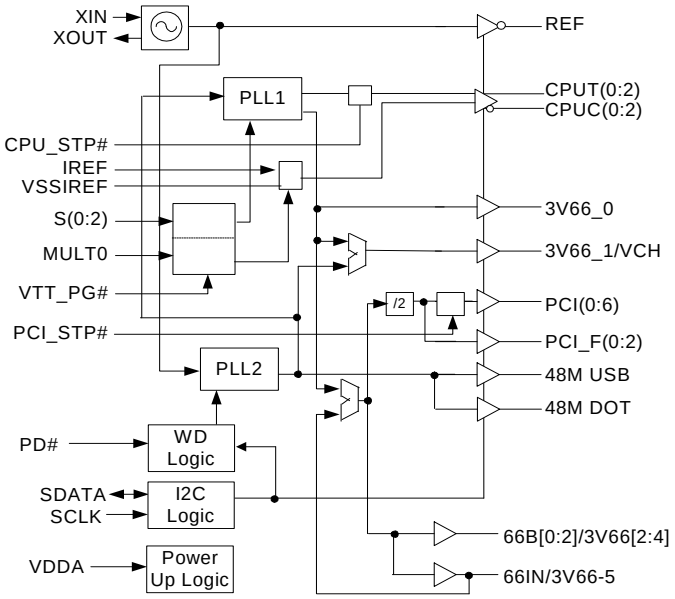
Features

- **Compliant with Intel® CK 408 Mobile Clock Synthesizer specifications**
- **3.3V power supply**
- **Three differential CPU clocks**
- **Ten copies of PCI clocks**
- **5/6 copies of 3V66 clocks**
- **SMBus support with read-back capabilities**
- **Spread Spectrum electromagnetic interference (EMI) reduction**
- **Dial-a-Frequency™ features**
- **Dial-a-dB™ features**
- **56-pin TSSOP and SSOP packages**

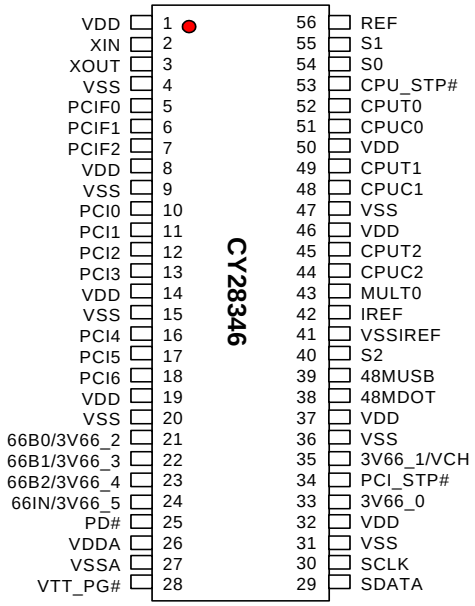
Table 1. Frequency Table[1]

S2	S1	S0	CPU (0:2)	3V66	66BUFF(0:2)/ 3V66(0:4)	66IN/3V66–5	PCI_FPCI	REF	USB/ DOT
1	0	0	66M	66M	66IN	66-MHz clock input	66IN/2	14.318M	48M
1	0	1	100M	66M	66IN	66-MHz clock input	66IN/2	14.318M	48M
1	1	0	200M	66M	66IN	66-MHz clock input	66IN/2	14.318M	48M
1	1	1	133M	66M	66IN	66-MHZ clock input	66IN/2	14.318M	48M
0	0	0	66M	66M	66M	66M	33 M	14.318M	48M
0	0	1	100M	66M	66M	66M	33 M	14.318M	48M
0	1	0	200M	66M	66M	66M	33 M	14.318M	48M
0	1	1	133M	66M	66M	66M	33 M	14.318M	48M
M	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
M	0	1	TCLK/2	TCLK/4	TCLK/4	TCLK/4	TCLK/8	TCLK	TCLK/2

Block Diagram



Pin Configuration



Note:
1. TCLK is a test clock driven on the XTAL_IN input during test mode. M = driven to a level between 1.0V and 1.8V. If the S2 pin is at a M level during power-up, a 0 state will be latched into the device's internal state register.

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Pin Description

Pin	Name	PWR	I/O	Description
2	XIN		I	**Oscillator Buffer Input**. Connect to a crystal or to an external clock.
3	XOUT	V_{DD}	O	**Oscillator Buffer Output**. Connect to a crystal. Do not connect when an external clock is applied at X_{IN}.
52, 51, 49, 48, 45, 44	CPUT(0:2), CPUC(0:2)	V_{DD}	O	**Differential Host Output Clock Pairs**. See *Table 1* for frequency/functionality.
10, 11, 12, 13, 16, 17, 18	PCI(0:6)	V_{DDP}	O	**PCI Clock Outputs**. Are synchronous to 66IN or 3V66 clock. See *Table 1*.
5, 6, 7	PCIF (0:2)	V_{DD}	O	**33MHz PCI Clocks**. ÷2 copies of 66IN or 3V66 clocks that may be free running (not stopped when PCI_STP# is asserted LOW) or may be stoppable depending on the programming of SMBus register Byte3,Bits (3:5).
56	REF	V_{DD}	O	**Buffered Output Copy of the Device's X_{IN} Clock**.
42	IREF	V_{DD}	I	**Current Reference Programming Input for CPU Buffers**. A resistor is connected between this pin and VSSIREF.
28	VTT_PG#	V_{DD}	I	**Qualifying Input that Latches S(0:2) and MULT0**. When this input is at a logic LOW, the S(0:2) and MULT0 are latched.
39	48MUSB	V_{DD48}	O	**Fixed 48 MHz USB Clock Outputs**.
38	48MDOT	V_{DD48}	O	**Fixed 48 MHZ DOT Clock Outputs**.
33	3V66_0	V_{DD}	O	**3.3V 66 MHz Fixed-frequency Clock**.
35	3V66_1/VCH	V_{DD}	O	**3.3V Clock Selectable with SMBus Byte0,Bit5, When Byte5,Bit5**. When Byte 0,Bit 5 is at a logic 1, then this pin is a 48M output clock. When Byte0,Bit5 is a logic 0, this is a 66M output clock (default).
25	PD#	V_{DD}	I PU	**Power-down Mode Pin**. A logic LOW level causes the device to enter a power-down state. All internal logic is turned off except for the SMBus logic. All output buffers are stopped.
43	MULT0		I PU	**Programming Input Selection for CPU Clock Current Multiplier**.
55, 54	S(0,1)	I	I	**Frequency Select Inputs**. See *Table 1*.
29	SDATA	I	I	**Serial Data Input**. Conforms to the SMBus specification of a Slave Receive/Transmit device. It is an input when receiving data. It is an open drain output when acknowledging or transmitting data.
30	SCLK	I	I	**Serial Clock Input**. Conforms to the SMBus specification.
40	S2	V_{DD}	I T	**Frequency Select Input**. See *Table 1*. This is a Tri-level input which is driven HIGH, LOW or driven to a intermediate level.
34	PCI_STP#	V_{DD}	I PU	**PCI Clock Disable Input**. When asserted LOW, PCI (0:6) clocks are synchronously disabled in a LOW state. This pin does not effect PCIF (0:2) clocks' outputs if they are programmed to be PCIF clocks via the device's SMBus interface.
53	CPU_STP#	V_{DD}	I PU	**CPU Clock Disable Input**. When asserted LOW, CPUT (0:2) clocks are synchronously disabled in a HIGH state and CPUC(0:2) clocks are synchronously disabled in a LOW state.
24	66IN/3V66_5	V_{DD}	I/O	**Input Connection for 66CLK(0:2) Output Clock Buffers** if S2 = 1, or output clock for fixed 66-MHz clock if S2 = 0. See *Table 1*.
21, 22, 23	66B(0:2)/ 3V66(2:4)	V_{DD}	O	**3.3V Clock Outputs**. These clocks are buffered copies of the 66IN clock or fixed at 66 MHz. See *Table 1*.
1, 8, 14, 19, 32, 37, 46, 50	V_{DD}		PWR	**3.3V Power Supply**.
4, 9, 15, 20, 27, 31, 36, 47	V_{SS}		PWR	**Common Ground**.
41	V_{SS}IREF		PWR	**Current Reference Programming Input for CPU Buffers**. A resistor is connected between this pin and IREF. This pin should also be returned to device V_{SS}.
26	V_{DDA}	–	PWR	**Analog Power Input**. Used for phase-locked loops (PLLs) and internal analog circuits. It is also specifically used to detect and determine when power is at an acceptable level to enable the device to operate.

Two-Wire SMBus Control Interface

The two-wire control interface implements a Read/Write slave only interface according to SMBus specification.

The device will accept data written to the D2 address and data may read back from address D3. It will not respond to any other addresses, and previously set control registers are retained as long as power in maintained on the device.

Serial Control Registers

Following the acknowledge of the Address Byte, two additional bytes must be sent:

1. “Command code” byte
2. “Byte count” byte.

Although the data (bits) in the command is considered “don’t care,” it must be sent and will be acknowledged. After the Command Code and the Byte Count have been acknowledged, the sequence (Byte 0, Byte 1, and Byte 2) described below will be valid and acknowledged.

Byte 0: CPU Clock Register[2,3]

Bit	@Pup	Pin#	Description
7	0		Spread Spectrum Enable. 0 = Spread Off, 1 = Spread On This is a Read and Write control bit.
6	0		CPU Clock Power-down Mode Select. 0 = Drive CPUT(0:2) to 4 or 6 IREF and drive CPUC(0:2) LOW when PD# is asserted LOW. 1 = Tri-state all CPU outputs. This is only applicable when PD# is LOW. It is not applicable to CPU_STP#.
5	0	35	3V66_1/VCH Frequency Select, 0 = 66M selected, 1 = 48M selected This is a Read and Write control bit.
4	Pin 53	44,45,48,49,51,52	CPU_STP#. Reflects the current value of the external CPU_STP# (pin 53) This bit is Read-only.
3	Pin 34	10,11,12,13,16,17,18	Reflects the current value of the internal PCI_STP# function when read. Internally PCI_STP# is a logical AND function of the internal SMBus register bit and the external PCI_STP# pin.
2	Pin 40		Frequency Select Bit 2. Reflects the value of SEL2 (pin 40). This bit is Read-only.
1	Pin 55		Frequency Select Bit 1. Reflects the value of SEL1 (pin 55). This bit is Read-only.
0	Pin 54		Frequency Select Bit 0. Reflects the value of SEL0 (pin 54). This bit is Read-only.

Byte 1: CPU Clock Register

Bit	@Pup	Pin#	Description
7	Pin 43	43	MULT0 (Pin 43) Value. This bit is Read-only.
6	0	53	CPUT/C(0:2) Output Functionality Control When CPU_STP# is Asserted. 0 = Drive CPUT(0:2) to 4 or 6 IREF and drive CPUC(0:2) LOW when CPU_STP# asserted LOW. 1 = three-state all CPU outputs. This bit will override Byte0,Bit6 such that even if it is 0, when PD# goes LOW the CPU outputs will be three-stated.
5	0	44,45	CPU2 Functionality Control When CPU_STP# is Asserted LOW. 1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW. This is a Read and Write control bit.
4	0	48,49	CPU1 Functionality Control When CPU_STP# is Asserted LOW. 1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW. This is a Read and Write control bit.
3	0	51,52	CPUT0 Functionality Control When CPU_STP# is Asserted LOW. 1 = Free Running, 0 = Stopped LOW with CPU_STP# asserted LOW. This is a Read and Write control bit.
2	1	44,45	CPUT/C2 Output Control. 1 = enabled, 0 = disable HIGH and CPUC2 disables LOW. This is a Read and Write control bit.
1	1	48,49	CPUT/C1 Output Control. 1 = enabled, 0 = disable HIGH and CPUC1 disables LOW. This is a Read and Write control bit.
0	1	51,52	CPUT/C0 Output Control. 1 = enabled, 0 = disable HIGH and CPUC0 disables LOW. This is a Read and Write control bit.

Notes:
2. PU = internal pull-up. PD = internal pull-down. T = tri-level logic input with valid logic voltages of LOW = < 0.8V, T = 1.0 – 1.8V and HIGH = > 2.0V.
3. The “Pin#” column lists the relevant pin number where applicable. The “@Pup” column gives the default state at power-up.

Byte 2: PCI Clock Control Register (all bits are Read and Write functional)

Bit	@Pup	Pin#	Description
7	0	53	REF Output Control. 0 = high strength, 1 = low strength.
6	1	18	PCI6 Output Control. 1 = enabled, 0 = forced LOW.
5	1	17	PCI5 Output Control. 1 = enabled, 0 = forced LOW.
4	1	16	PCI4 Output Control. 1 = enabled, 0 = forced LOW.
3	1	13	PCI3 Output Control. 1 = enabled, 0 = forced LOW.
2	1	12	PCI2 Output Control. 1 = enabled, 0 = forced LOW.
1	1	11	PCI1 Output Control. 1 = enabled, 0 = forced LOW.
0	1	10	PCI0 Output Control. 1 = enabled, 0 = forced LOW.

Byte 3: PCI_F Clock and 48M Control Register (all bits are Read and Write functional)

Bit	@Pup	Pin#	Description
7	1	38	48MDOT Output Control. 1 = enabled, 0 = forced LOW.
6	1	39	48MUSB Output Control. 1 = enabled, 0 = forced LOW.
5	0	7	PCI_STP#, Control of PCI_F2. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW.
4	0	6	PCI_STP#, Control of PCI_F1. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW.
3	0	5	PCI_STP#, Control of PCI_F0. 0 = Free Running, 1 = Stopped when PCI_STP# is LOW.
2	1	7	PCI_F2 Output Control. 1 = running, 0 = forced LOW.
1	1	6	PCI_F1 Output Control. 1 = running, 0 = forced LOW.
0	1	5	PCI_F0 Output Control. 1 = running, 0 = forced LOW.

Byte 4: DRCG Control Register (all bits are Read and Write functional)

Bit	@Pup	Pin#	Description
7	0		SS2 Spread Spectrum Control Bit (0 = down spread, 1 = center spread).
6	0		Reserved. Set = 0.
5	1	33	3V66_0 Output Enabled. 1 = enabled, 0 = disable.
4	1	35	3V66_1/VCH Output Enable. 1 = enabled, 0 = disabled.
3	1	24	3V66_5 Output Enable. 1 = enabled, 0 = disabled.
2	1	23	66B2/3V66_4 Output Enabled. 1 = enabled, 0 = disabled.
1	1	22	66B1/3V66_3 Output Enabled. 1 = enabled, 0 = disabled.
0	1	21	66B0/3V66_2 Output Enabled. 1 = enabled, 0 = disabled.

Byte 5: Clock Control Register (all bits are Read and Write functional)

Bit	@Pup	Pin#	Description
7	0		SS1 Spread Spectrum Control Bit.
6	1		SS0 Spread Spectrum Control Bit.
5	0		66IN to 66M delay Control MSB.
4	0		66IN to 66M delay Control LSB.
3	0		Reserved. Set = 0.
2	0		48MDOT Edge Rate Control. When set to 1, the edge is slowed by 15%.
1	0		Reserved. Set = 0.
0	0		USB edge rate control. When set to 1, the edge is slowed by 15%.

Byte 6: Silicon Signature Register[4] (all bits are Read-only)

Bit	@Pup	Pin#	Description
7	0		Revision = 0001
6	0		
5	0		
4	1		
3	0		Vendor Code = 0011
2	0		
1	1		
0	1		

Byte 7: Reserved Register

Bit	@Pup	Pin#	Description
7	0		Reserved. Set = 0.
6	0		Reserved. Set = 0.
5	0		Reserved. Set = 0.
4	0		Reserved. Set = 0.
3	0		Reserved. Set = 0.
2	0		Reserved. Set = 0.
1	0		Reserved. Set = 0.
0	0		Reserved. Set = 0.

Byte 8: Dial-a-Frequency Control Register N

Bit	@Pup	Name	Description
7	0		Reserved. Set = 0.
6	0	N6, MSB	These bits are for programming the PLL's internal N register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock.
5	0	N5	
4	0	N4	
3	0	N3	
2	0	N2	
1	0	N3	
0	0	N0, LSB	

Byte 9: Dial-a-Frequency Control Register R

Bit	@Pup	Name	Description
7	0		Reserved. Set = 0.
6	0	R5, MSB	These bits are for programming the PLL's internal R register. This access allows the user to modify the CPU frequency at very high resolution (accuracy). All other synchronous clocks (clocks that are generated from the same PLL, such as PCI) remain at their existing ratios relative to the CPU clock.
5	0	R4	
4	0	R3	
3	0	R2	
2	0	R1	
1	0	R0	
0	0	DAF_ENB	R and N register mux selection. 0 = R and N values come from the ROM. 1 = data is loaded from DAF (SMBus) registers.

Note:
4. When writing to this register, the device will acknowledge the Write operation, but the data itself will be ignored.

Dial-a-Frequency Features

SMBus Dial-a-Frequency feature is available in this device via Byte8 and Byte9.

P is a large-value PLL constant that depends on the frequency selection achieved through the hardware selectors (S1, S0). P value may be determined from *Table 2*.

Table 2. P Value

S(1:0)	P
0 0	32005333
0 1	48008000
1 0	96016000
1 1	64010667

Dial-a-dB Features

SMBus Dial-a-dB feature is available in this device via Byte8 and Byte9.

Spread Spectrum Clock Generation (SSCG)

Spread Spectrum is a modulation technique used to minimizing EMI radiation generated by repetitive digital signals. A clock presents the greatest EMI energy at the center frequency it is generating. Spread Spectrum distributes this energy over a specific and controlled frequency bandwidth therefore causing the average energy at any one point in this band to decrease in value. This technique is achieved by modulating the clock away from its resting frequency by a certain percentage (which also determines the amount of EMI reduction). In this device, Spread Spectrum is enabled by setting specific register bits in the SMBus control bytes. *Table 3* is a listing of the modes and percentages of Spread Spectrum modulation that this device incorporates.

Table 3. Spread Spectrum

SS2	SS1	SS0	Spread Mode	Spread%
0	0	0	Down	+0.00, –0.25
0	0	1	Down	+0.00, –0.50
0	1	0	Down	+0.00, –0.75
0	1	1	Down	+0.00, –1.00
1	0	0	Center	+0.13, –0.13
1	0	1	Center	+0.25, –0.25
1	1	0	Center	+0.37, –0.37
1	1	1	Center	+0.50, –1.50

Test and Measurement Set-up

For Differential CPU Output Signals

The following diagram shows lumped test load configurations for the differential Host Clock Outputs.

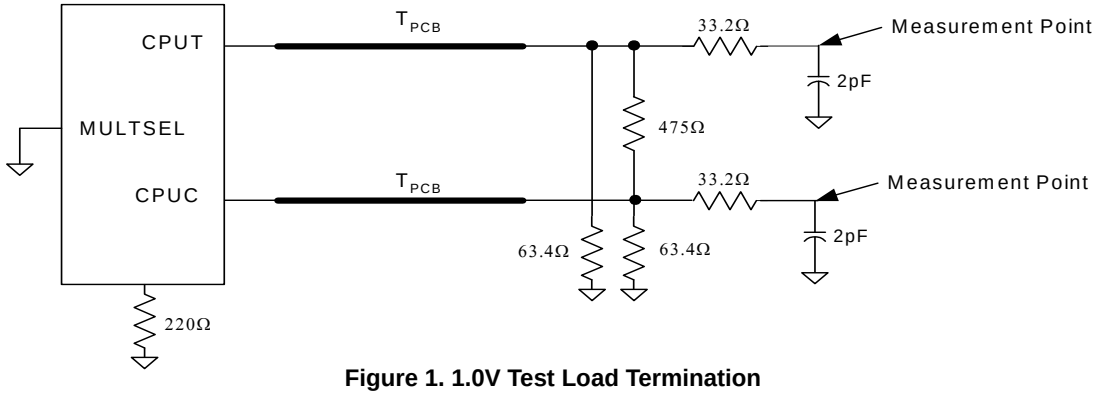


Figure 1. 1.0V Test Load Termination

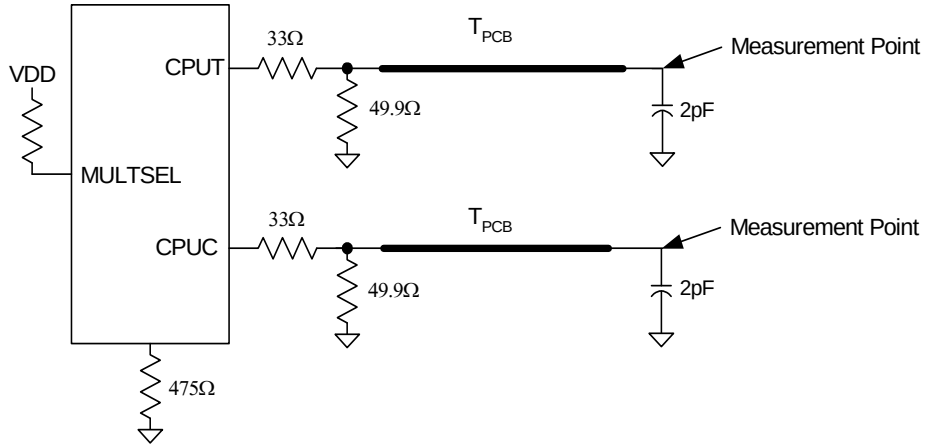


Figure 2. 0.7V Test Load Termination

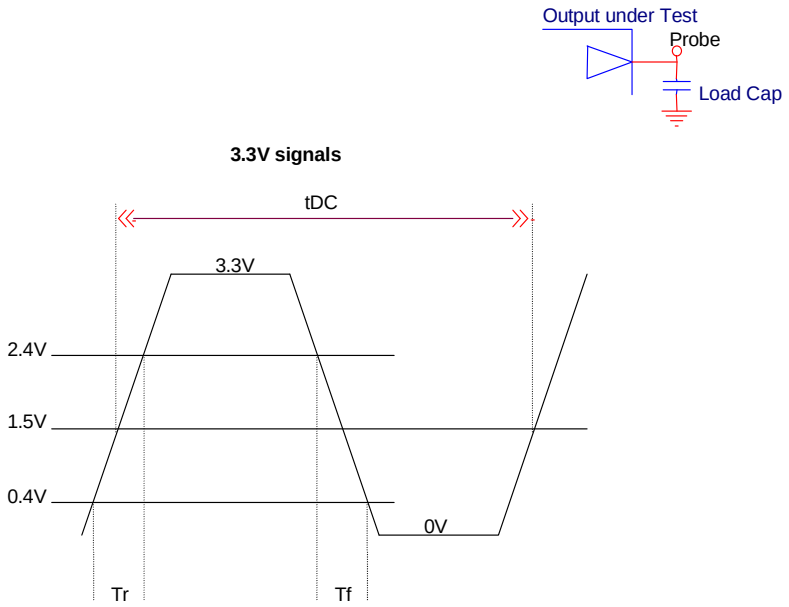


Figure 3. For Single-ended Output Signals

Buffer Characteristics

Current Mode CPU Clock Buffer Characteristics

The current mode output buffer detail and current reference circuit details are contained in the previous table of this data sheet. The following parameters are used to specify output buffer characteristics:

1. Output impedance of the current mode buffer circuit—Ro (see *Figure 4*).
2. Minimum and maximum required voltage operation range of the circuit—Vop (see *Figure 4*).
3. Series resistance in the buffer circuit—Ros (see *Figure 4*).
4. Current accuracy at given configuration into nominal test load for given configuration.

Iout is selectable depending on implementation. The parameters above apply to all configurations. Vout is the voltage at the pin of the device.

The various output current configurations are shown in the host swing select functions table. For all configurations, the deviation from the expected output current is ±7% as shown in the current accuracy table.

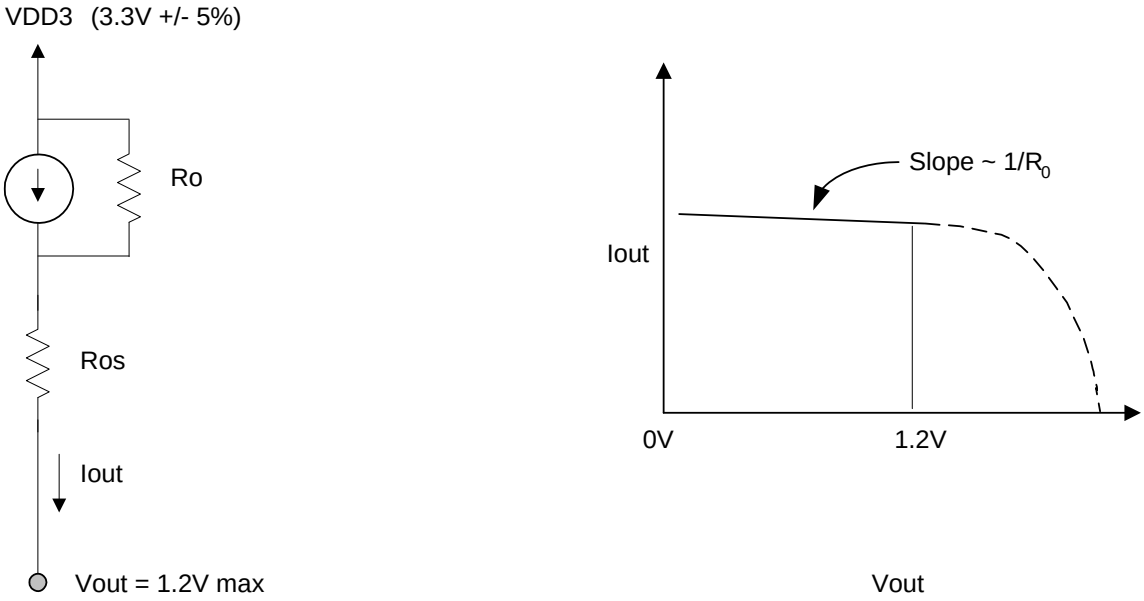


Figure 4. Buffer Characteristics

Table 4. Host Clock (HCSL) Buffer Characteristics

Characteristic	Min.	Max.
Ro	3000Ω (recommended)	N/A
Ros		
Vout	N/A	1.2V

Table 5. CPU Clock Current Select Function

Mult0	Board Target Trace/Term Z	Reference R, Iref – Vdd (3*Rr)	Output Current	Voh @ Z
0	50Ω	Rr = 221 1%, Iref = 5.00mA	Ioh = 4*Iref	1.0V @ 50
1	50Ω	Rr = 475 1%, Iref = 2.32mA	Ioh = 6*Iref	0.7V @ 50

Table 6. Group Timing Relationship and Tolerances

Description	Offset	Tolerance	Conditions
3V66 to PCI	2.5 ns	±1.0 ns	3V66 Leads PCI (unbuffered mode)
48MUSB to 48MDOT Skew	0.0 ns	±1.0 ns	0 degrees phase shift
66B(0:2) to PCI offset	2.5 ns	±1.0 ns	66B Leads PCI (buffered mode)

USB and DOT 48M Phase Relationship

The 48MUSB and 48MDOT clocks are in phase. It is understood that the difference in edge rate will introduce some inherent offset. When 3V66_1/VCH clock is configured for VCH (48-MHz) operation it is also in phase with the USB and DOT outputs. See *Figure 5*.

66IN to 66B(0:2) Buffered Prop Delay

The 66IN to 66B(0:2) output delay is shown in *Figure 6*.

The Tpd is the prop delay from the input pin (66IN) to the output pins (66B[0:2]). The outputs' variation of Tpd is described in the AC parameters section of this data sheet. The measurement taken at 1.5V.

66B(0:2) to PCI Buffered Clock Skew

Figure 7 shows the difference (skew) between the 3V33(0:5) outputs when the 66M clocks are connected to 66IN. This offset is described in the Group Timing Relationship and Tolerances section of this data sheet. The measurements were taken at 1.5V.

3V66 to PCI Un-Buffered Clock Skew

Figure 8 shows the timing relationship between 3V66(0:5) and PCI(0:6) and PCI_F(0:2) when configured to run in the unbuffered mode.

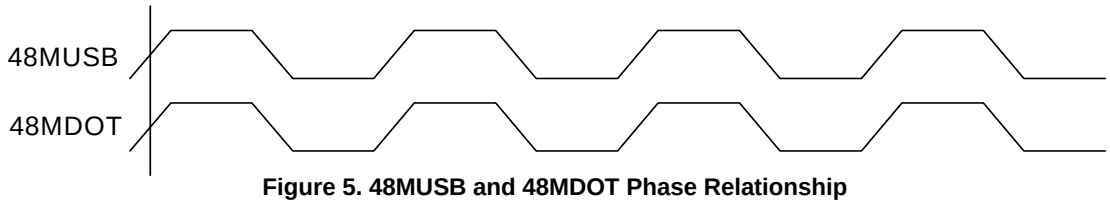


Figure 5. 48MUSB and 48MDOT Phase Relationship

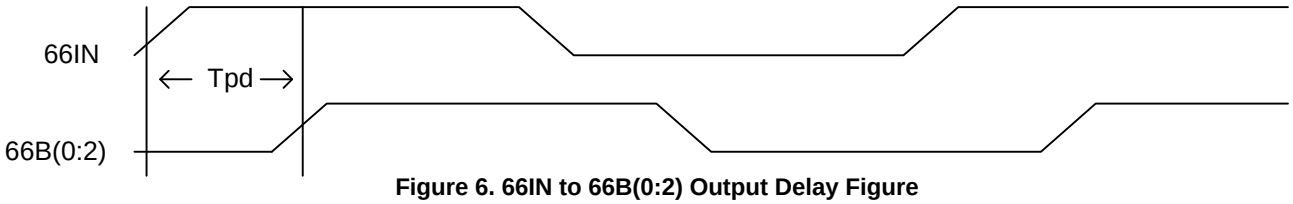


Figure 6. 66IN to 66B(0:2) Output Delay Figure

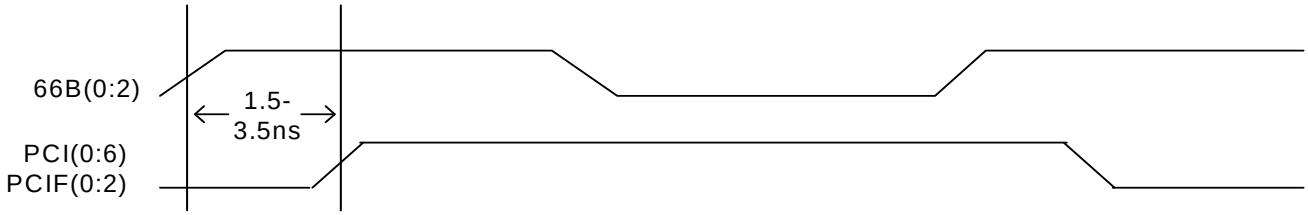


Figure 7. Buffer Mode – 33V66(0:1); 66BUF(0:2) Phase Relationship

Special Functions

PCI_F and IOAPIC Clock Outputs

The PCIF clock outputs are intended to be used, if required, for systems IOAPIC clock functionality. Any two of the PCI_F clock outputs can be used as IOAPIC 33 Mhz clock outputs. They are 3.3V outputs will be divided down via a simple resistive voltage divider to meet specific system IOAPIC clock voltage requirements. In the event that these clocks are not required, they can be used as general PCI clocks or disabled via the assertion of the PCI_STP# pin.

3V66_1/VCH Clock Output

The 3V66_1/VCH pin has a dual functionality that is selectable via SMBus.

Configured as DRCG (66M), SMBus Byte0, Bit 5 = “0”

The default condition for this pin is to power-up in a 66M operation. In 66M operation this output is SSCG-capable and when spreading is turned on, this clock will be modulated.

Configured as VCH (48M), SMBus Byte0, Bit 5 = “1”

In this mode, output is configured as a 48-Mhz non-spread spectrum output that is phase-aligned with other 48M outputs (USB and DOT) to within 1 ns pin-to-pin skew. The switching of 3V66_1/VCH into VCH mode occurs at system power-on. When the SMBus Bit 5 of Byte 0 is programmed from a “0” to a “1,” the 3V66_1/VCH output may glitch while transitioning to 48M output mode.

CPU_STP# Clarification

The CPU_STP# signal is an active LOW input used to synchronously stop and start the CPU output clocks while the rest of the clock generator continues to function.

CPU_STP# – Assertion

When CPU_STP# pin is asserted, all CPUT/C outputs that are set with the SMBus configuration to be stoppable via assertion of CPU_STP# will be stopped after being sampled by two falling CPUT/C clock edges. The final state of the stopped CPU signals is CPUT = HIGH and CPU0C = LOW. There is no change to the output drive current values during the stopped state. The CPUT is driven HIGH with a current value equal to (Mult 0 “select”) × (Iref), and the CPUC signal will not be driven. Due to external pull-down circuitry CPUC will be LOW during this stopped state.

CPU_STP# Deassertion

The deassertion of the CPU_STP# signal will cause all CPUT/C outputs that were stopped to resume normal operation in a synchronous manner (meaning that no short or stretched clock pulses will be produces when the clock resumes). The maximum latency from the deassertion to active outputs is no more than two CPUC clock cycles.

Three-state Control of CPU Clocks Clarification

During CPU_STP# and PD# modes, CPU clock outputs may be set to driven or undriven (tri-state) by setting the corresponding SMBus entry in Bit6 of Byte0 and Bit6 of Byte1.

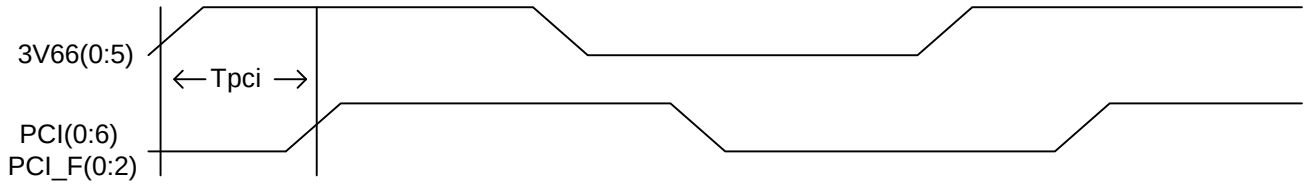


Figure 8. Unbuffered Mode – 3V66(0:5) to PCI (0:6) and PCI_F(0:2) Phase Relationship

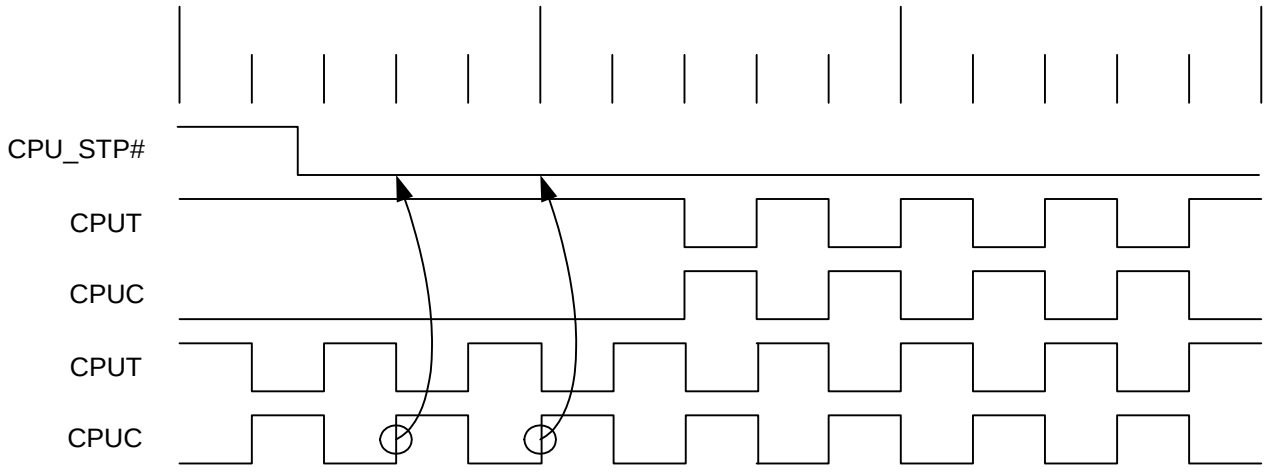


Figure 9. CPU_STP# Assertion Waveform

PCI_STP# Assertion

The PCI_STP# signal is an active LOW input used for synchronous stopping and starting the PCI outputs while the rest of the clock generator continues to function. The set-up time for capturing PCI_STP# going LOW is 10 ns (t_{setup}) (see *Figure 14*.) The PCI_F (0:2) clocks will not be affected by this pin if their control bits in the SMBus register are set to allow them to be free running.

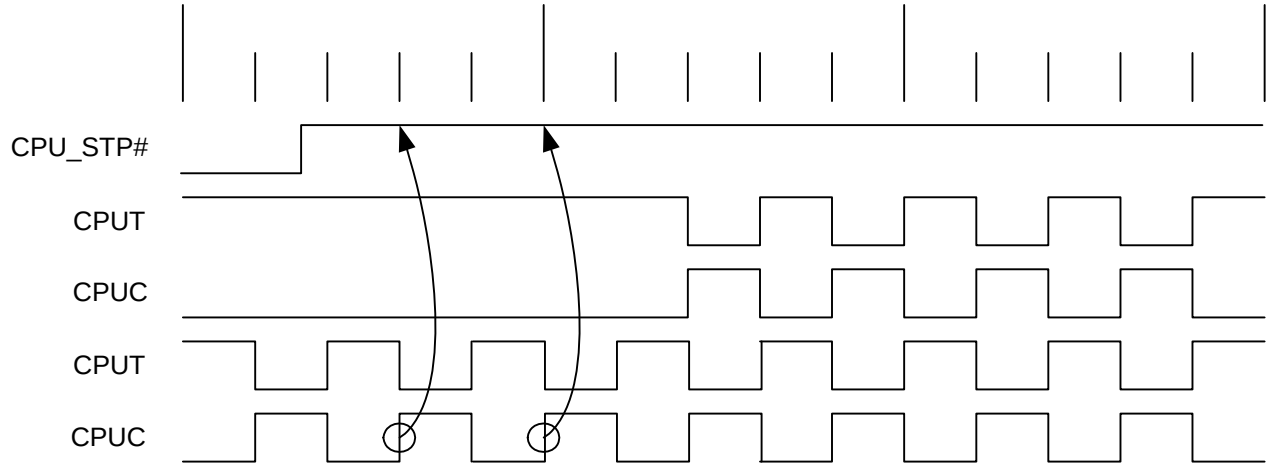


Figure 10. CPU_STP# Deassertion Waveform

Table 7. Cypress Clock Power Management Truth Table

B0b6	B1b6	PD#	CPU_STP#	Stoppable CPUT	Stoppable CPUC	Non-Stop CPUT	Non-Stop CPUC
0	0	1	1	Running	Running	Running	Running
0	0	1	0	Iref x6	Iref x6	Running	Running
0	0	0	1	Iref x2	LOW	Iref x2	LOW
0	0	0	0	Iref x2	LOW	Iref x2	LOW
0	1	1	1	Running	Running	Running	Running
0	1	1	0	Hi-Z	Hi-Z	Running	Running
0	1	0	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
0	1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	1	1	Running	Running	Running	Running
1	0	1	0	Iref x6	Iref x6	Running	Running
1	0	0	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	0	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	1	1	1	Running	Running	Running	Running
1	1	1	0	Hi-Z	Hi-Z	Running	Running
1	1	0	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z
1	1	0	0	Hi-Z	Hi-Z	Hi-Z	Hi-Z

PCI_STP# – Deassertion (transition from logic “0” to logic “1”)

The deassertion of the PCI_STP# signal will cause all PCI(0:6) and stoppable PCI_F(0:2) clocks to resume running in a synchronous manner within two PCI clock periods after PCI_STP# transitions to a HIGH level.

Note. The PCI STOP function is controlled by two inputs. One is the device PCI_STP# pin number 34 and the other is SMBus Byte 0,Bit 3. These two inputs to the function are logically AND’ed. If either the external pin or the internal SMBus register bit is set LOW, the stoppable PCI clocks will be stopped in a logic LOW state. Reading SMBus Byte 0,Bit 3 will return a 0 value if either of these control bits are set LOW (which indicates that the devices stoppable PCI clocks are not running).

PD# (Power-down) Clarification

The PD# (power-down) pin is used to shut off all clocks prior to shutting off power to the device. PD# is an asynchronous active LOW input. This signal is synchronized internally to the device powering down the clock synthesizer. PD# is an asynchronous function for powering up the system. When PD# is LOW, all clocks are driven to a LOW value and held there and the VCO and PLLs are also powered down. All clocks are shut down in a synchronous manner so has not to cause glitches while transitioning to the LOW “stopped” state.

PD# – Assertion

When PD# is sampled LOW by two consecutive rising edges of the CPUC clock, then on the next HIGH-to-LOW transition of PCIF, the PCIF clock is stopped LOW. On the next HIGH-to-LOW transition of 66Buff, the 66Buff clock is stopped LOW. From this time, each clock will stop LOW on its next HIGH-to-LOW transition, except the CPUT clock. The CPU clocks are held with the CPUT clock pin driven HIGH with a value of 2 × Iref, and CPUC undriven. After the last clock has stopped, the rest of the generator will be shut down.

PD# – Deassertion

The power-up latency between PD# rising to a valid logic ‘1’ level and the starting of all clocks is less than 3.0 ms.

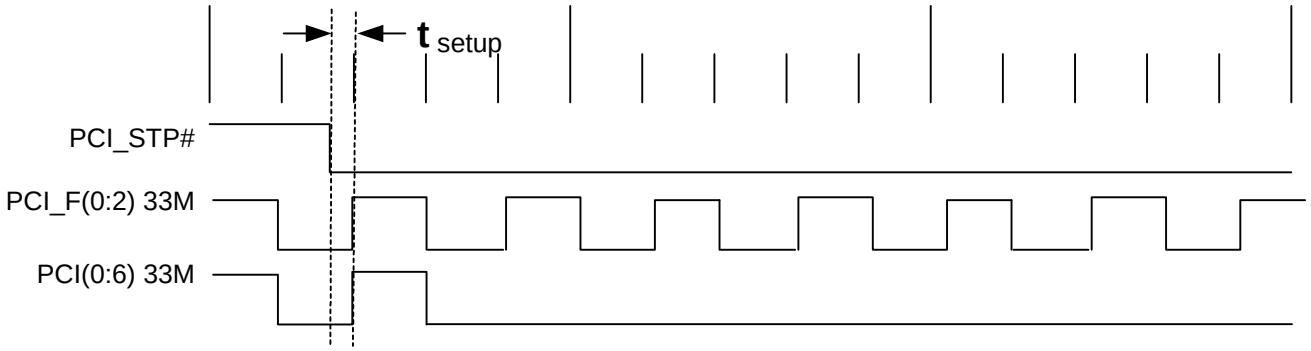


Figure 11. PCI_STP# Assertion Waveform

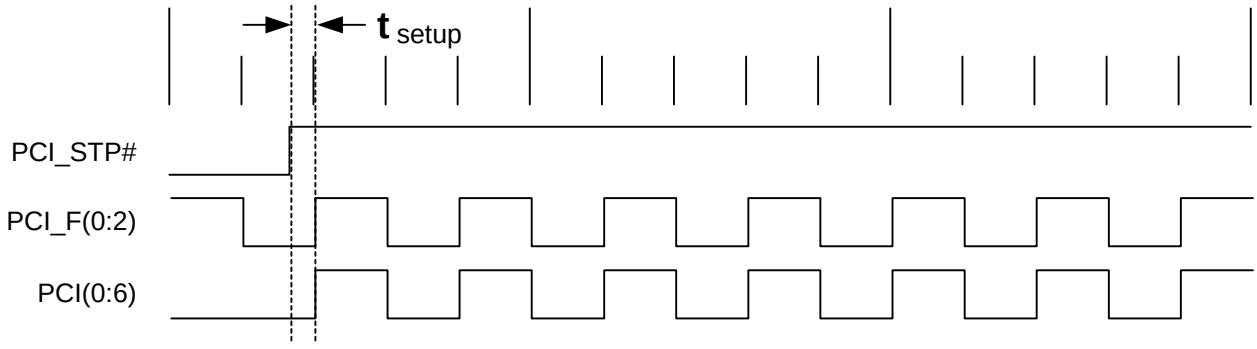


Figure 12. PCI_STP# Deassertion Waveform

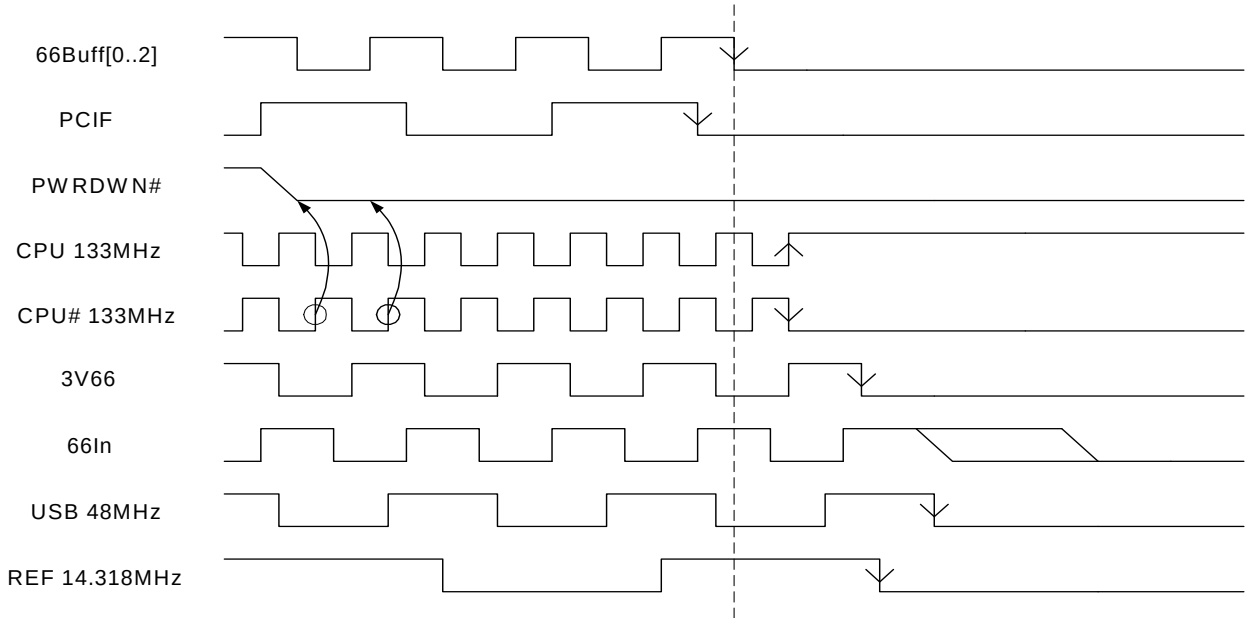


Figure 13. Power-down Assertion Timing Waveforms Figure—Buffered Mode

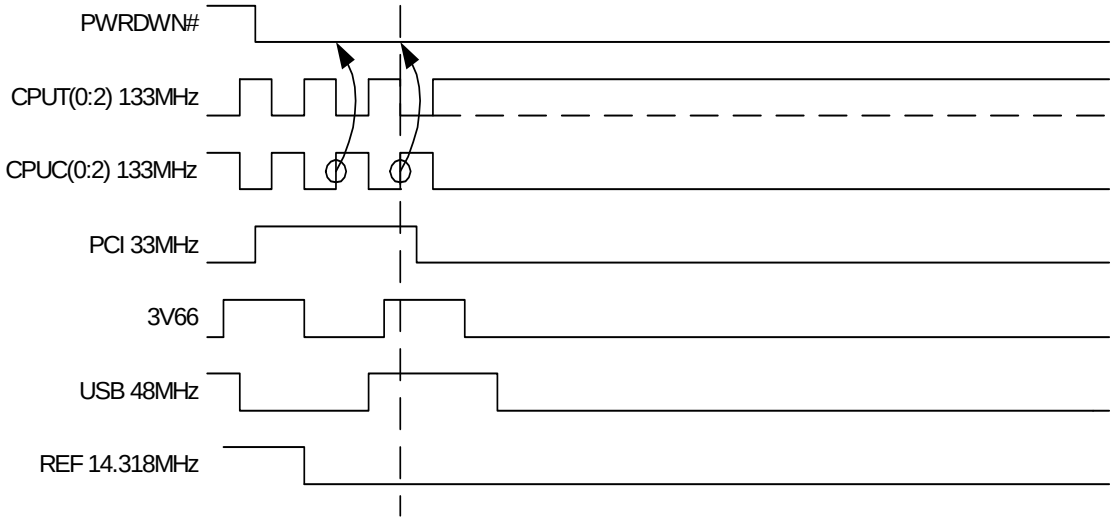


Figure 14. Power-down Assertion Timing Waveforms—Unbuffered Mode

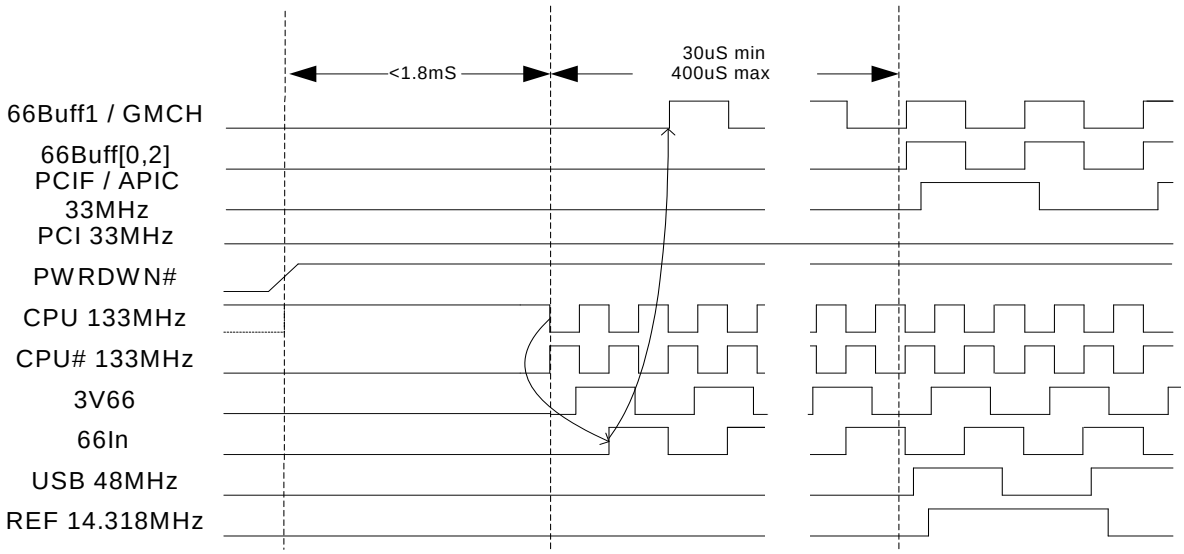


Figure 15. Power-down Deassertion Timing Waveforms—Buffered Mode

Table 8. PD# Functionality

PD#	DRCG	66CLK (0:2)	PCI_F/PCI	PCI	USB/DOT
1	66M	66Input	66Input/2	66Input/2	48M
0	LOW	LOW	LOW	LOW	LOW

Absolute Maximum Ratings[5]

Input Voltage Relative to V_{SS}: ..... V_{SS} – 0.3V
Input Voltage Relative to V_{DDQ} or AV_{DD}: ..... V_{DD} + 0.3V
Storage Temperature: ..... –65°C to + 150°C
Operating Temperature: ..... 0°C to +85°C
Maximum Power Supply: 3.5V

Current Accuracy[6]

Parameter	Conditions	Configuration	Load	Min.	Max.
Iout	V_{DD} = nominal (3.30V)	M0 = 0 or 1 and Rr (see *Table 1*)	Nominal test load for given configuration	–7% Inom	+ 7% Inom
Iout	V_{DD} = 3.30 ± 5%	All combinations of M0 or 1 and Rr (see *Table 1*)	Nominal test load for given configuration	–12% Inom	+ 12% Inom

DC Parameters (V_{DD} = V_{DDA} = 3.3V ±5%, TA = 0°C to +70°C)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{DD}3.3V	Dynamic Supply Current	All frequencies at maximum values[7]			280	mA
I_{PD}3.3V	Power-down Supply Current	PD# asserted			Note 8	mA
C_{IN}	Input Pin Capacitance				5	pF
C_{OUT}	Output Pin Capacitance				6	pF
L_{PIN}	Pin Inductance				7	nH
C_{XTAL}	Crystal Pin Capacitance	Measured from the X_{IN} or X_{OUT} pin to ground	30	36	42	pF

AC Parameters (V_{DD} = V_{DDA} = 3.3V ±5%, T_A = 0°C to +70°C)

Parameter	Description	66 MHz		100 MHz		133 MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
Crystal											
T_{DC}	X_{IN} Duty Cycle	47.5	52.5	47.5	52.5	47.5	52.5	47.5	52.5	%	9, 10, 11
T_{PERIOD}	X_{IN} period	69.84	71.0	69.84	71.0	69.84	71.0	69.84	71.0	ns	9, 12, 13, 10
V_{HIGH}	X_{IN} HIGH Voltage	$0.7V_{DD}$	V_{DD}	$0.7V_{DD}$	V_{DD}	$0.7V_{DD}$	V_{DD}	$0.7V_{DD}$	V_{DD}	V	
V_{LOW}	X_{IN} LOW Voltage	0	$0.3V_{DD}$	0	$0.3V_{DD}$	0	$0.3V_{DD}$	0	$0.3V_{DD}$	V	
T_R / T_F	X_{IN} Rise and Fall Times		10.0		10.0		10.0		10.0	ns	14
T_{CCJ}	X_{IN} Cycle to Cycle Jitter		500		500		500		500	ps	12, 15, 10
CPU at 0.7V Timing											
T_{DC}	CPUT and CPUC Duty Cycle	45	55	45	55	45	55	45	55	%	15, 16, 19
T_{PERIOD}	CPUT and CPUC Period	14.85	15.3	9.85	10.2	7.35	7.65	4.85	5.1	ns	15, 16, 19
T_{SKEW}	Any CPU to CPU Clock Skew		100		100		100		100	ps	12, 15, 16

Notes:
5. **Multiple Supplies:** The Voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.
6. Inom refers to the expected current based on the configuration of the device.
7. All outputs loaded as per maximum capacitive load table.
8. Absolute value = ((Programmed CPU Iref) × (2)) + 10 mA.
9. This parameter is measured as an average over 1 μs duration, with a crystal center frequency of 14.31818 MHz.
10. When Xin is driven from an external clock source.
11. This is required for the duty cycle on the REF clock out to be as specified. The device will operate reliably with input duty cycles up to 30/70 but the REF clock duty cycle will not be within data sheet specifications.
12. All outputs loaded as per*Table 9* below.
13. Probes are placed on the pins and measurements are acquired at 1.5V for 3.3V signals (see test and measurement set-up section of this data sheet).
14. Measured between $0.2V_{DD}$ and $0.7V_{DD}$.
15. This measurement is applicable with Spread ON or Spread OFF.
16. Measured at crossing point (Vx) or where subtraction of CLK–CLK# crosses 0V Measured from V_{OL} = 0.175V to V_{OH} = 0.525V.
17. Measured from V_{OL} = 0.175V to V_{OH} = 0.525V.
18. Determined as a fraction of 2*(Trise–Tfall)/ (Trise+Tfall).
19. Test load is Rta = 33.2Ω, Rd = 49.9Ω.

AC Parameters (V_{DD} = V_{DDA} = 3.3V ±5%, T_A = 0°C to +70°C) (continued)

Parameter	Description	66 MHz		100 MHz		133 MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
T_{CCJ}	CPU Cycle to Cycle Jitter		150		150		150		150	ps	15, 16, 19
T_R/T_F	CPUT and CPUC Rise and Fall Times	175	700	175	700	175	700	175	700	ps	15, 17, 20
	Rise/Fall Matching		20%		20%		20%		20%		17, 18, 19
DeltaT_R	Rise Time Variation		125		125		125		125	ps	17, 19
DeltaT_F	Fall Time Variation		125		125		125		125	ps	17, 19
V_{CROSS}	Crossing Point Voltage at 0.7V Swing	280	430	280	430	280	430	280	430	mV	15, 19
CPU at 1.0V Timing											
T_{DC}	CPUT and CPUC Duty Cycle	45	55	45	55	45	55	45	55	%	15, 16
T_{PERIOD}	CPUT and CPUC Period	14.85	15.3	9.85	10.2	7.35	7.65	4.85	5.1	nS	15, 16
T_{SKEW}	Any CPU to Any CPU Clock Skew		100		100		100		100	pS	12, 15, 16
T_{CCJ}	CPU Cycle to Cycle Jitter		150		150		150		150	pS	12, 16
Differential T_R/T_F	CPUT and CPUC Rise and Fall Times	175	467	175	467	175	467	175	467	ps	15, 20
SE–DeltaSlew	Absolute Single- ended Rise/Fall Waveform Symmetry		325		325		325		325	ps	21, 22
V_{CROSS}	Cross Point at 1.0V swing	510	760	510	760	510	760	510	760	mV	22
3V66											
T_{DC}	3V66 Duty Cycle	45	55	45	55	45	55	45	55	%	12, 13
T_{PERIOD}	3V66 Period	15.0	15.3	15.0	15.3	15.0	15.3	15.0	15.3	ns	9, 12, 13
T_{HIGH}	3V66 HIGH Time	4.95		4.95		4.95		4.95		ns	23
T_{LOW}	3V66 LOW Time	4.55		4.55		4.55		4.55		ns	24
T_R/T_F	3V66 Rise and Fall Times	0.5	2.0	0.5	2.0	0.5	2.0	0.5	2.0	ns	25
T_{SKEW} Unbuffered	3V66 to 3V66 Clock Skew		500		500		500		500	ps	12, 13
T_{SKEW} Buffered	3V66 to 3V66 Clock Skew		250		250		250		250	ps	12, 13
T_{CCJ}	DRCG Cycle to Cycle Jitter		250		250		250		250	ps	12, 13

Notes:

20. Measurement taken from differential waveform, from –0.35V to +0.35V.
21. Measurements taken from common mode waveforms, measure rise/fall time from 0.41 to 0.86V. Rise/fall time matching is defined as “the instantaneous difference between maximum CLK rise (fall) and minimum CLK# fall (rise) time or minimum CLK rise (fall) and maximum CLK# fall (rise) time.” This parameter is designed form waveform symmetry.
22. Measured in absolute voltage, i.e., single-ended measurement.
23. THIGH is measured at 2.4V for non-host outputs.
24. TLOW is measured at 0.4V for all outputs.
25. Probes are placed on the pins, and measurements are acquired between 0.4V and 2.4V for 3.3V signals (see test and measurement set-up section of this data sheet).

AC Parameters (V_{DD} = V_{DDA} = 3.3V ±5%, T_A = 0°C to +70°C) (continued)

Parameter	Description	66 MHz		100 MHz		133 MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
66B											
T_{DC}	66B(0:2) Duty Cycle	45	55	45	55	45	55	45	55	%	12, 13
T_R/T_F	66B(0:2) Rise and Fall Times	0.5	2.0	0.5	2.0	0.5	2.0	0.5	2.0	ns	12, 25
T_{SKEW}	Any 66B to Any 66B Skew		175		175		175		175	ps	12, 13
T_{PD}	66IN to 66B(0:2) Propagation Delay	2.5	4.5	2.5	4.5	2.5	4.5	2.5	4.5	ns	12, 13
T_{CCJ}	66B(0:2) Cycle to Cycle Jitter		100		100		100		100	ps	12, 13, 26
PCI											
T_{DC}	PCI_F(0:2) PCI (0:6) Duty Cycle	45	55	45	55	45	55	45	55	%	12, 13
T_{PERIOD}	PCI_F(0:2) PCI (0:6) Period	30.0		30.0		30.0		30		nS	9, 12, 13
T_{HIGH}	PCI_F(0:2) PCI (0:6) HIGH Time	12.0		12.0		12.0		12.0		nS	23
T_{LOW}	PCI_F(0:2) PCI (0:6) LOW Time	12.0		12.0		12.0		12.0		nS	24
T_R/T_F	PCI_F(0:2) PCI (0:6) Rise and Fall Times	0.5	2.0	0.5	2.0	0.5	2.0	0.5	2.0	nS	25
T_{SKEW}	Any PCI Clock to Any PCI Clock Skew		500		500		500		500	pS	12, 13
T_{CCJ}	PCI_F(0:2) PCI (0:6) Cycle to Cycle Jitter		250		250		250		250	ps	12, 13
48MUSB											
T_{DC}	48MUSB Duty Cycle	45	55	45	55	45	55	45	55	%	12, 13
T_{PERIOD}	48MUSB Period	20.8299	20.8333	20.8299	20.8333	20.8299	20.8333	20.8299	20.8333	ns	12, 13
T_R/T_F	48MUSB Rise and Fall Times	1.0	2.0	1.0	2.0	1.0	2.0	1.0	2.10	ns	12, 25
T_{CCJ}	48MUSB Cycle to Cycle Jitter		350		350		350		350	ps	9, 12, 13
48MDOT											
T_{DC}	48MDOT Duty Cycle	45	55	45	55	45	55	45	55	%	12, 13
T_{PERIOD}	48MDOT Period	20.837		20.837		20.837		20.837		ns	12, 13
T_R/T_F	48MDOT Rise and Fall Times	0.5	1.0	0.5	1.0	0.5	1.0	0.5	1.0	ns	12, 13
T_{CCJ}	48MDOT Cycle to Cycle Jitter		350		350		350		350	ps	12, 13
REF											
T_{DC}	REF Duty Cycle	45	55	45	55	45	55	45	55	%	12, 13
T_{PERIOD}	REF Period	69.84	71.0	69.84	71.0	69.84	71.0	69.84	71.0	ns	12, 13
T_R/T_F	REF Rise and Fall Times	1.0	4.0	1.0	4.0	1.0	4.0	1.0	4.0	ns	12, 25
T_{CCJ}	REF Cycle to Cycle Jitter		1000		1000		1000		1000	ps	12, 13

Note:
26. This figure is in addition to any jitter already present when the 66IN pin is being used as an input. Otherwise a 500-ps jitter figure is specified.

AC Parameters (V_{DD} = V_{DDA} = 3.3V ±5%, T_A = 0°C to +70°C) (continued)

Parameter	Description	66 MHz		100 MHz		133 MHz		200 MHz		Unit	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
T_{PZL}/T_{PZH}	Output Enable Delay (All Outputs)	1.0	10.0	1.0	10.0	1.0	10.0	1.0	10.0	ns	10
T_{PZL}/T_{PZH}	Output disable delay (all outputs)	1.0	10.0	1.0	10.0	1.0	10.0	1.0	10.0	ns	10
T_{STABLE}	All Clock Stabilization from Power-up		3		3		3		3	ms	10
T_{SS}	Stopclock Set-up Time	10.0		10.0		10.0		10.0		ns	27
T_{SH}	Stopclock Hold Time	0		0		0		0		ns	27
T_{SU}	Oscillator Start-up Time		X		X		X		X	ms	28

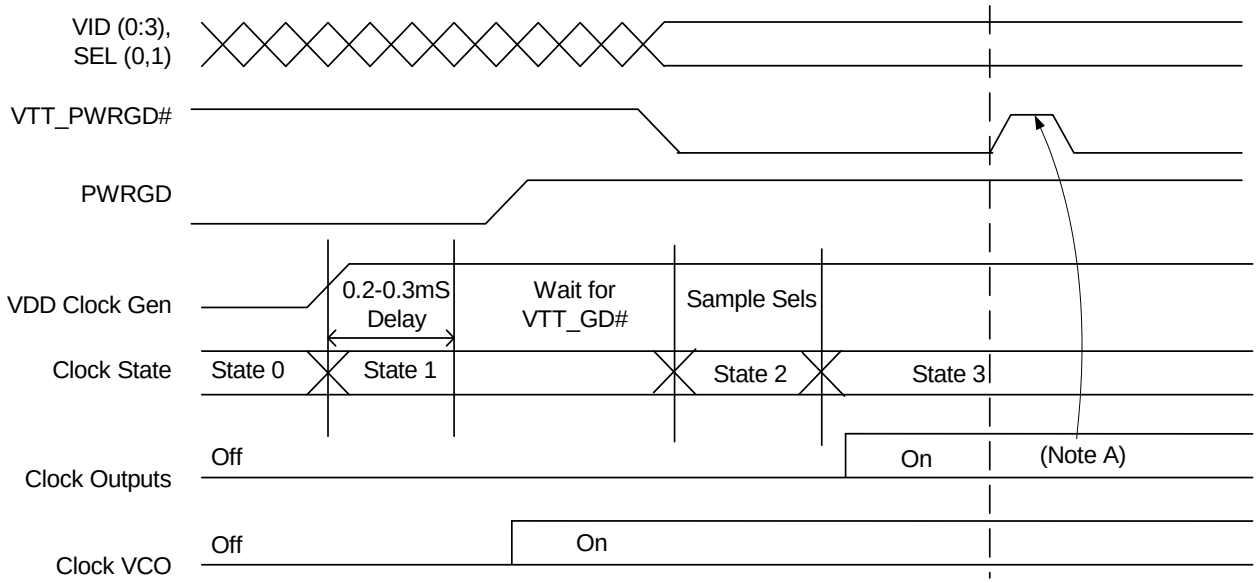


Figure 16. VTT_PWRGD# Timing Diagram29[29]

Table 9. Maximum Lumped Capacitive Output Loads

Clock	Max. Load	Units
PCI Clocks	30	pF
3V66 (0,1)	30	pF
66B(0:2)	30	pF
48MUSB Clock	20	pF
48MDOT	10	pF
REF Clock	50	pF

Notes:
27. CPU_STP# and PCI _STP# set-up time with respect to any PCI_F clock to guarantee that the effected clock will stop or start at the next PCI_F clock's rising edge
28. When crystal meets minimum 40Ω device series resistance specification.
29. Device is not affected, VTT_PWRGD# is ignored.

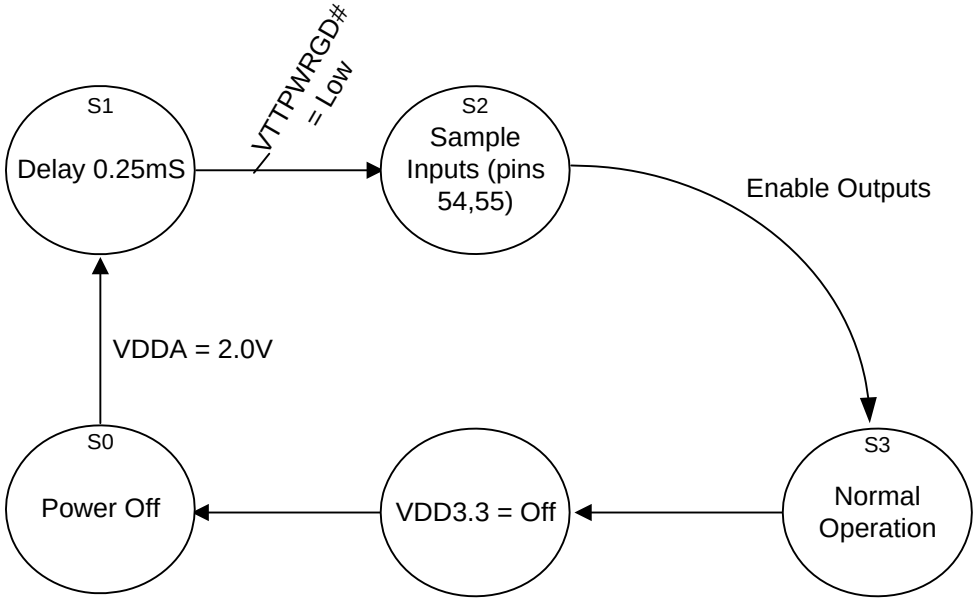


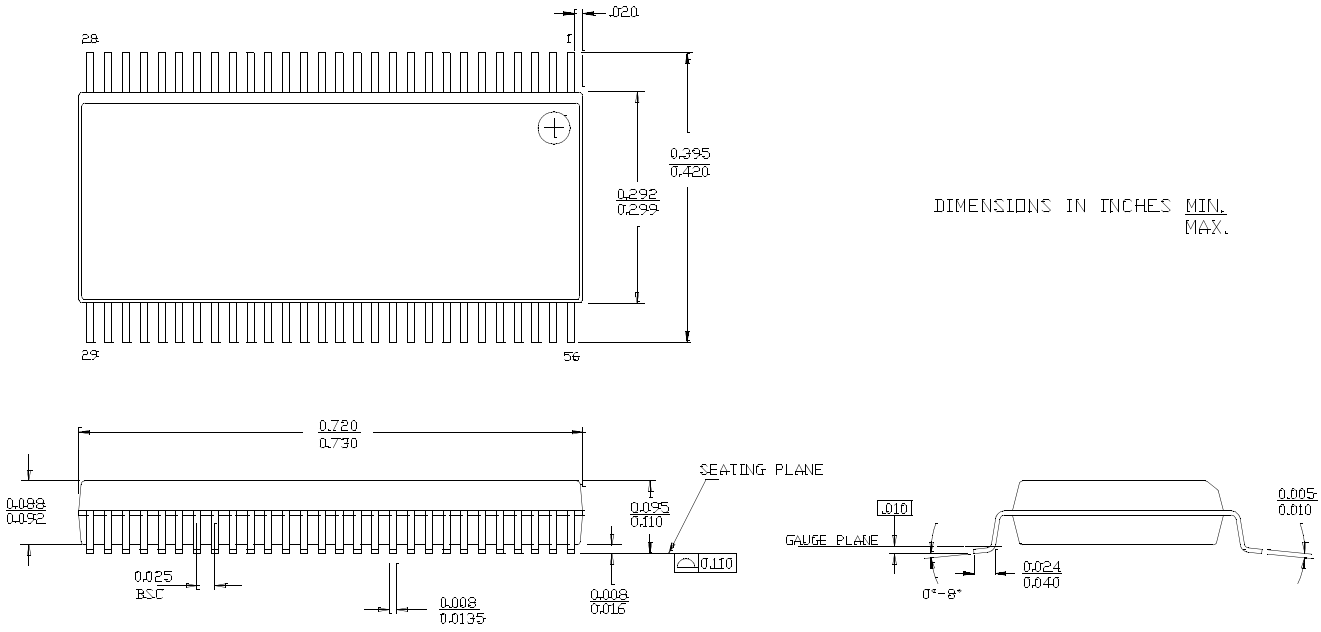
Figure 17. Clock Generator Power-up/Run State Diagram

Ordering Information

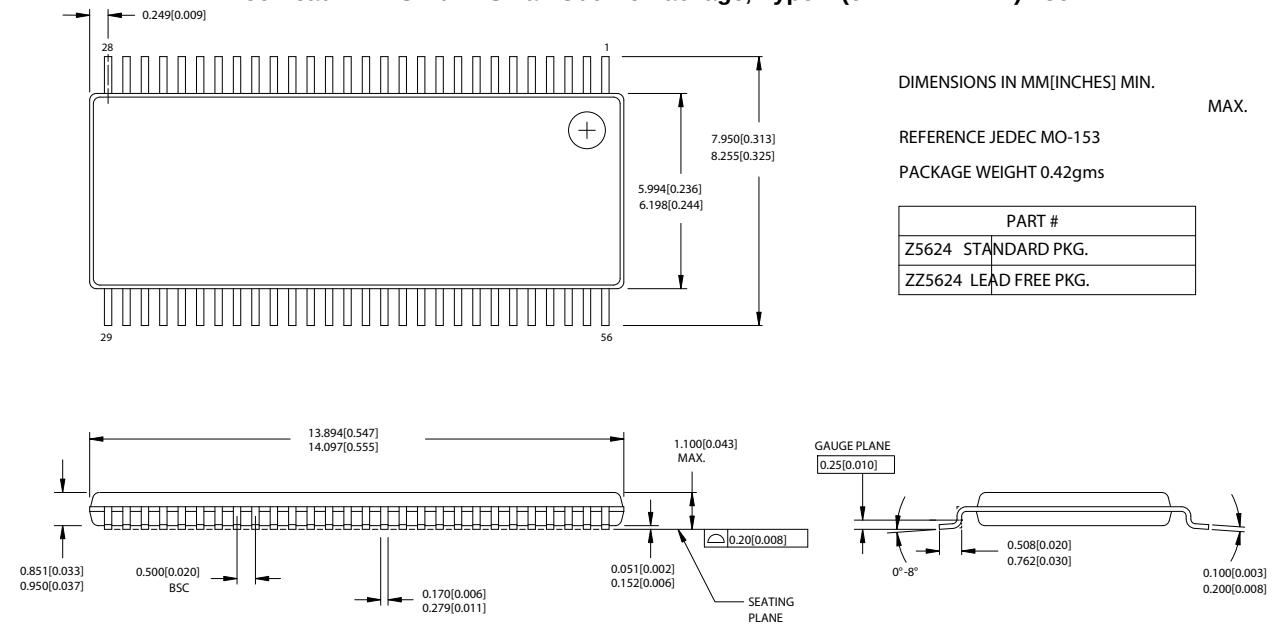
Part Number	Package Type	Product Flow
CY28346OC	56-pin SSOP – Tube	Commercial, 0° to 70°C
CY28346OCT	56-pin SSOP – Tape and Reel	Commercial, 0° to 70°C
CY28346ZC	56-pin TSSOP – Tube	Commercial, 0° to 70°C
CY28346ZCT	56-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C
Lead-free		
CY28346OXC	56-pin SSOP – Tube	Commercial, 0° to 70°C
CY28346OXCT	56-pin SSOP – Tape and Reel	Commercial, 0° to 70°C
CY28346ZXC	56-pin TSSOP – Tube	Commercial, 0° to 70°C
CY28346ZXCT	56-pin TSSOP – Tape and Reel	Commercial, 0° to 70°C

Package Drawing and Dimensions

56-lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package, Type II (6 mm x 12 mm) Z56



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