BQ24392-Q1 Dual SPST USB 2.0 High Speed Switch With USB Battery Charging Specification Revision 1.2 Detection

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- USB 2.0 High Speed Switch
- Detects USB Battery Charging Specification Version 1.2 (BCv1.2) Compliant Chargers
- Compatible Accessories
  - Dedicated Charging Port
  - Standard Downstream Port
  - Charging Downstream Port
- Non-Standard Chargers
  - Apple™ Charger
  - TomTom™ Charger
  - USB Chargers Not Compliant With Battery Charging Specification Version 1.2 (BCv1.2)
- –2-V to 28-V VBUS Voltage Range
- ESD Performance Tested per JESD 22
  - 4000-V Human-Body Model
  - 1500-V Charged-Device Model (C101)
- ESD Performance DP_CON/DM_CON to GND
  - ±8-kV Contact Discharge (IEC 61000-4-2)

2 Applications

- Rear Seat Entertainment
- GPS Systems

3 Description

The BQ24932-Q1 is a dual single-pole single-throw (SPST) USB 2.0 high-speed isolation switch with charger detection capabilities for use with micro and mini-USB ports. This USB switch allows mobile phones, tablets, and other battery operated electronics to be charged from different adapters with minimal system software. The device's charger detection circuitry can support USB Battery Charging Specification version 1.2 (BCv1.2) compliant, Apple™, TomTom™, and other non-standard chargers.

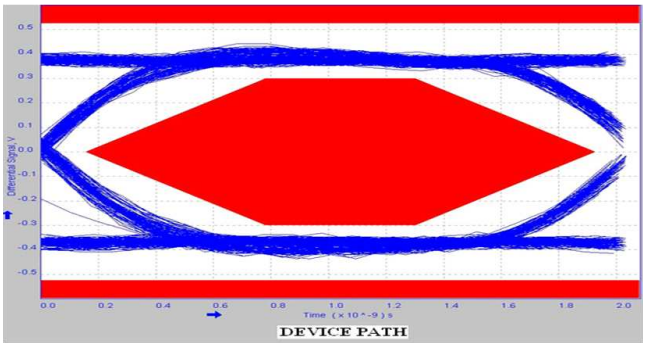
The BQ24932-Q1 device is powered through VBUS when a charger is attached to the micro or mini-USB port and has a 28 V tolerance to avoid the need for external protection.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ24392-Q1	UQFN (10)	2.05 mm × 1.55 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

480-Mbps USB 2.0 Eye Diagram With USB Switch



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- Changed diode direction from left facing to right facing in *Application Schematic*. ... 11

Changes from Revision A (September 2014) to Revision B — **Page**

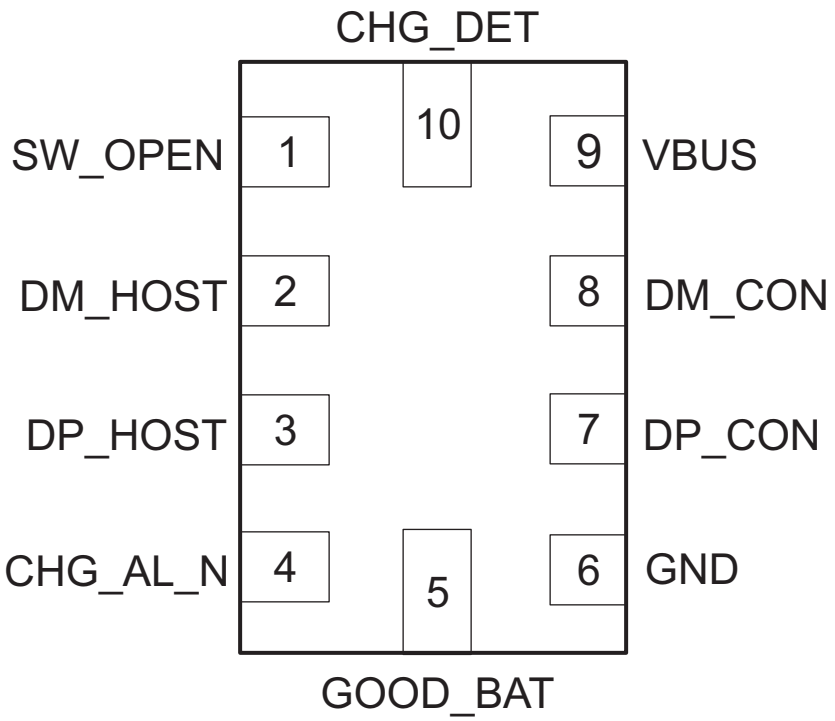
- Updated Features. ... 1

Changes from Original (August 2014) to Revision A — **Page**

- Initial full version release of document. ... 1

5 Terminal Configuration and Functions

RESR
(TOP VIEW)



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	SW_OPEN	O	USB switch status indicator Open-drain output. 10 kΩ external pull-up resistor required SW_OPEN = LOW indicates when switch is connected SW_OPEN = HIGH-Z indicates when switch is not connected
2	DM_HOST	I/O	D– signal to transceiver
3	DP_HOST	I/O	D+ signal to transceiver
4	CHG_AL_N	O	Charging status indicator Open-drain output. 10 kΩ external pull-up resistor required. CHG_AL_N = LOW indicates when charging allowed CHG_AL_N = HIGH-Z indicates when charging is not allowed
5	GOOD_BAT	I	Battery status indication from system This pin indicates the status of the battery GOOD_BAT = LOW indicates a dead battery GOOD_BAT = HIGH indicates a good battery
6	GND	–	Not internally connected
7	DP_CON	I/O	D+ signal from USB connector
8	DM_CON	I/O	D– signal from USB connector
9	VBUS	I	Supply pin from USB connector
10	CHG_DET	O	Charger detection indicator Push-pull output to the system CHG_DET = LOW indicates when a charger is not detected CHG_DET = HIGH indicates when a charger detected

6 Specifications

6.1 Absolute Maximum Ratings

over –40℃ to 125℃ temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Input Voltage	VBUS	–2	28	V
	CHG_AL_N	–2	28	
	DM_HOST	–0.3	7	
	DP_HOST	–0.3	7	
	GOOD_BAT	–0.3	7	
	DP_CON	–0.3	7	
	DM_CON	–0.3	7	
	CHG_DET	–0.3	7	

6.2 Handling Ratings

				MIN	MAX	UNIT
T_{stg}	Storage temperature range			–65	150	°C
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)			4000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (DP_CON and DM_CON to GND)	–8000	8000	
			Other pins		1500	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

	MIN	MAX	UNIT
VBUS	4.75	5.25	V
GOOD_BAT	0	VBUS	
DM_HOST	0	3.6	
DP_HOST	0	3.6	
DM_CON	0	3.6	
DP_CON	0	3.6	

6.4 Thermal Information

THERMAL METRIC (1)		BQ24392-Q1 RSE 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	167.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	95.8	
ψ_{JT}	Junction-to-top characterization parameter	4.7	
ψ_{JB}	Junction-to-board characterization parameter	95.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

V_{BUS} = 4.5 V to 5.5 V, T_A = –40°C to 125°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BUS_VALID}	VBUS Valid threshold		Rising VBUS threshold		3.5		V
V_{OH}	CHG_DET	CHG_DET	I_{OH} = –2 mA	3.5		VBUS(1)	V
V_{OL}	CHG_DET, SW_OPEN, CHG_AL_N	CHG_DET, SW_OPEN, CHG_AL_N	I_{OL} = 2 mA			0.4	V
V_{IH}	High-level input voltage	GOOD_BAT		1.1			V
V_{IL}	Low-level input voltage					0.5	V
R_{PD}	Internal pull-down resistance				950		kΩ
t_{DBP}	Dead battery provision timer				32	45	Mins
V_{USBIO}	Analog signal range	DM_CON, DP_CON, DM_HOST, DP_HOST		0		3.6	V
R_{ON}	ON-state resistance		V_{DM_HOST} and V_{DP_HOST} = 0 to 3.6 V, I_{DP_CON} and I_{DM_CON} = –2 mA		6	8	Ω
R_{ON}(flat)	ON-state resistance flatness				1.1	2.4	Ω
ΔR_{ON}	ON- state resistance match between channels		V_{DM_HOST} and V_{DP_HOST}T = 0.4 V, I_{DP_CON} and I_{DM_CON} = –2 mA		0.5		Ω
$I_{CC\text{-}SW(ON)}$	Current consumption		V_{VBUS} = 5 V, USB Switch ON; $V_{IH(GOOD\_BAT)}$= 1.1 V		250	350	µA
			V_{VBUS} = 5 V, USB Switch ON; $V_{IH(GOOD\_BAT)}$ = 2.5 V		80	115	µA
$I_{CC\text{-}SW(OFF)}$	Current consumption with USB switch off		V_{VBUS} = 5 V; USB Switch OFF		45	75	µA
$I_{USBI/O(ON)}$	Output port leakage current with USB switch on		V_I = OPEN, V_O = 0.3 V or 2.7 V, Switch ON		50	90	nA
$I_{USBI/O(OFF)}$	Leakage current with USB switch off		V_I = 0.3 V, V_O = 2.7 V or V_I = 2.7 V, V_O = 0.3 V, Switch OFF		45	75	nA
$C_{I(OFF)}$	Capacitance with USB switch off	DP_HOST, DM_HOST	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch OFF		2		pF
$C_{O(OFF)}$	Capacitance with USB switch off	DP_CON, DM_CON			10		pF
$C_{I(ON)}$	Capacitance with USB switch on	DP_HOST, DM_HOST	DC bias = 0 V or 3.6 V, f = 10 MHz, Switch ON		11		pF
$C_{O(ON)}$	Capacitance with USB switch on	DP_CON, DM_CON			11		pF
BW	Bandwidth		R_L = 50 Ω, Switch ON		1		GHz
O_{ISO}	Isolation with USB switch off		f = 240 MHz, R_L = 50 Ω, Switch OFF		–26		dB
X_{TALK}	Crosstalk		f = 240 MHz, R_L = 50 Ω		–30.5		dB

(1) CHG_DET max value will be clamped at 7 V when V_{VBUS} > 7 V

6.6 Typical Characteristics

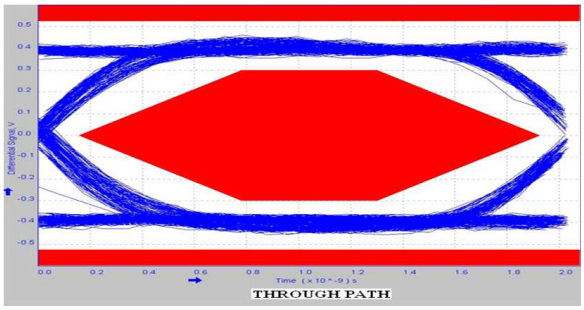


Figure 1. 480-Mbps USB 2.0 Eye Diagram with No Device

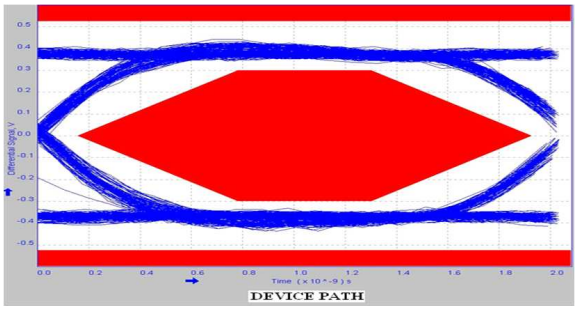


Figure 2. 480-Mbps USB 2.0 Eye Diagram with USB Switch

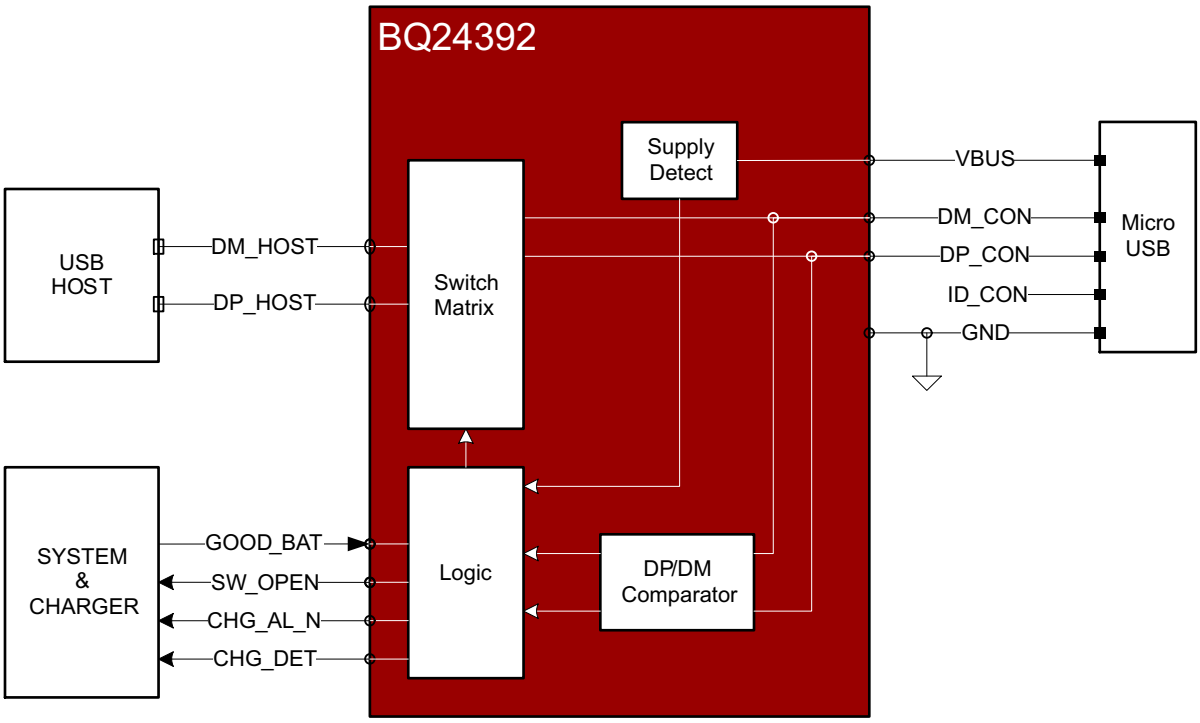
7 Detailed Description

7.1 Overview

The BQ24932-Q1 is a USB 2.0 high-speed isolation switch with charger detection capabilities for use with micro and mini-USB ports. Upon plugin of a Battery Charging Specification 1.2 (BCv1.2) compliant, Apple™, TomTom™, or other USB charger into a micro or mini-USB connector, the device will automatically detect the charger and operate the USB 2.0 high-speed isolation switch.

The BQ24932-Q1 device is powered through VBUS when a charger is attached to the micro or mini-USB port and has a 28-V tolerance to avoid the need for external protection.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Charger Detection

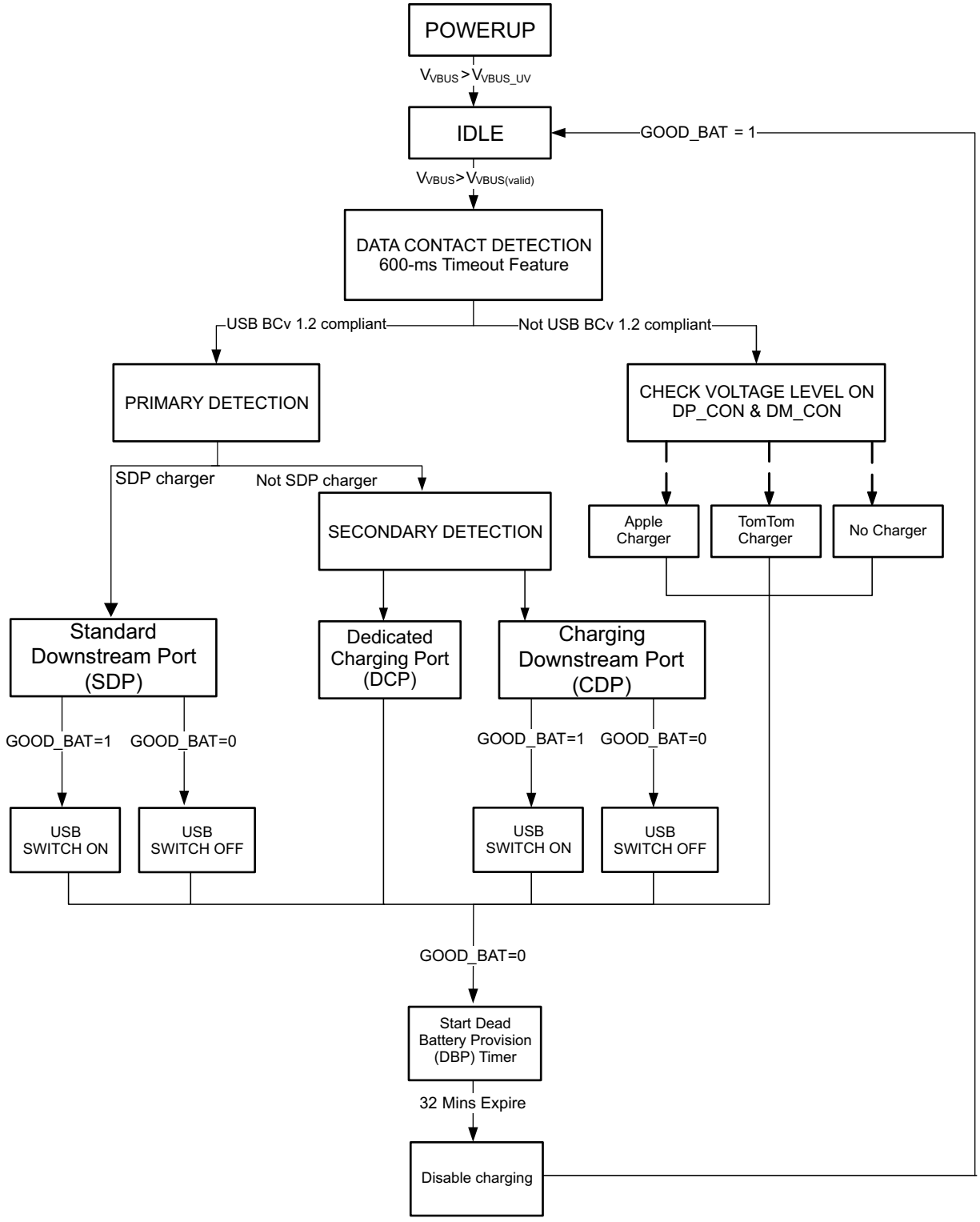


Figure 3. Logic Tree

Feature Description (continued)

When a micro or mini-USB accessory is inserted into the connector and once VVBUS is greater than V_{VBUS_VALID} threshold, the BQ24392-Q1 will enter into the Data Contact Detection (DCD) state which includes a 600-ms timeout feature that is prescribed in the USB Battery Charging Specification version 1.2 (BCv1.2). If the micro or mini-USB accessory is determined to be USB BCv1.2 compliant, a 130-ms debounce period will initiate and the BQ24392-Q1 will proceed to its primary detection and then secondary detection states to determine if a Dedicated Charging Port (DCP), Standard Downstream Port (SDP), or Charging Downstream Port (CDP) is attached to the USB-port. The minimum detection time for a DCP, SDP, and CDP is 130 ms, but can be as long as 600 ms due to the slow plug in effect.

If the GOOD_BAT pin is high, the USB 2.0 switches are automatically closed to enable data transfer after the device detects a Standard Downstream Port (SDP) or Charging Downstream Port (CDP) was connected.

If Data Contact Detection (DCD) fails, the BQ24392-Q1 proceeds to detect whether an Apple or TomTom charger was inserted by checking the voltage level on DP_CON and DM_CON. Thus, for Apple and TomTom chargers, detection time typically takes ~600 ms.

The 3 output pins CHG_AL_N, CHG_DET, and SW_OPEN change their status at the end of detection. Table 1 is the detection table with the GPIO status for each type of supported charger. More information on how to use the GPIOs is available in *Using the BQ24932 GPIOs* .

Table 1. Detection Table

Device Type	VBUS	DP_CON (D+)	DM_CON (D–)	GOOD_BAT (Input)	CHG_AL_N (Output)	CHG_DET (Output)	SW_OPEN (Output)	Switch Status	Charge Current
Standard Downstream Port	> 3.5 V	Pull-down R to GND	Pull-down R to GND	HIGH	LOW	LOW	LOW	Connected	Charge with 100mA/ Change the input current based on enumeration
				LOW	LOW	LOW	High-Z	Not Connected	Charge with 100 mA
Charging Downstream Port	> 3.5 V	Pull-down R to GND	V_{DM_SRC}	HIGH	LOW	HIGH	LOW	Connected	Charge with full current
				LOW	LOW	HIGH	High-Z	Not Connected	Charge with 100 mA
Dedicated Charging Port	> 3.5 V	Short to D–	Short to D+	X	LOW	HIGH	High-Z	Not Connected	Charge with full current
Apple Charger	> 3.5 V	2.0 V < V_{DP_CON} < 2.8 V	2.0 V < V_{DM_CON} < 2.8 V	X	LOW	HIGH	High-Z	Not Connected	Charge with full current
TomTom Charger	> 3.5 V	2.0 V < V_{DP_CON} < 3.1 V	2.0 V < V_{DM_CON} < 3.1 V	X	LOW	HIGH	High-Z	Not Connected	Charge with full current
PS/2 Charger	> 3.5 V	Pull-up R to V_{VBUS}	Pull-up R to V_{VBUS}	X	LOW	LOW	High-Z	Not Connected	Charge with 100 mA
Non-compliant USB Charger	> 3.5 V	Open	Open	X	LOW	LOW	High-Z	Not Connected	Charge with 100 mA
Any Device	< 3.5 V	Open	Open	X	High-Z	LOW	High-Z	Not Connected	No Charge
Any Device DBP Timer Expired	> 3.5 V	X	X	LOW	High-Z	LOW	High-Z	Not Connected	No Charge

If a charger has been detected and the GOOD_BAT pin is low, a Dead Battery Provision (DBP) timer is initiated. If the GOOD_BAT continues to be low for 30 minutes (maximum of 45 minutes), charging is disabled and CHG_AL_N goes into the High-Z state to indicate this. Toggling GOOD_BAT high after the DBP timer expires re-starts detection and the DBP timer.

7.4 Device Functional Modes

The BQ24392-Q1 has three functional modes:

1. Nothing inserted
2. Accessory inserted and detection running
3. Accessory inserted and detected

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Using the BQ24932 GPIOs

8.1.1.1 CHG_AL and CHG_DET

The BQ24392-Q1 has 2 charger indicators, CHG_AL_N and CHG_DET, that the host can use to determine whether it can charge and if it can charge at a low or high current. Table 2 demonstrates how these outputs should be interpreted. CHG_AL_N is an open drain output and is active when the output of the pin is low. CHG_DET is a push-pull output and is high in the active state.

Table 2. BQ24392-Q1 Outputs

CHG_AL_N	CHG_DET	
High-Z	X	Charging is not allowed
Low	Low	Low-current charging is allowed
Low	High	High-current charging is allowed

The system must define what is meant by low-current and high-current charging. If CHG_DET is high, a system could try to draw 2 A, 1.5 A, or 1.0 A. If the system is trying to support greater than 1.5-A chargers, then the system has to use a charger IC that is capable of monitoring the VBUS voltage as it tries to pull the higher current values. If the voltage on VBUS starts to drop because that high of a current is supported then the system has to reduce the amount of current it is trying to draw until it finds a stable state with VBUS not dropping.

8.1.1.2 SW_OPEN

SW_OPEN is an open drain output that indicates whether the USB switches are opened or closed. In the High-Z state the switches are open and in the active, or low state, the switches are closed. The host should monitor this pin to know when the switches are closed or open.

8.1.1.3 GOOD_BAT

GOOD_BAT is used by the host controller to indicate the status of the battery to the BQ24392-Q1. This pin affects the switch status for a SDP or CDP, and it also affects the Dead Battery Provision (DBP) timer as discussed in the *Charger Detection* section.

8.1.1.4 Slow Plug-in Event

As you insert a charger into the USB receptacle, the pins are configured so that the VBUS and GND pins make contact first. This presents a problem as the BQ24392-Q1 (or any other charger detection IC) requires access to the D+ and D– lines to run detection. This is why the BQ24392-Q1 has a standard 130-ms debounce time after VBUS valid to run the detection algorithm. This delay helps minimize the effects of the D+ and D– lines making contact after VBUS and GND.

Figure 4 is from the datasheet of a standard male micro-USB connector and shows how the data connections (red line) are slightly recessed from the power connections (blue line).

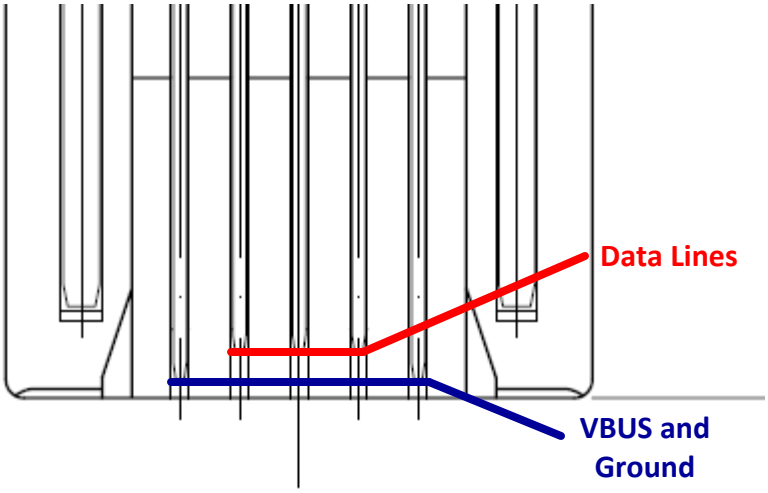


Figure 4. Data Connections Recessed from Power Connections

However, in some cases the charger is inserted very slowly, causing the VBUS and GND to make contact long before D+ and D–. Due to this effect, there is no guaranteed detection time as the detection time can vary based on how long it takes the user to insert the charger. If insertion takes longer than 600 ms, the detection algorithm of the BQ24392-Q1 will timeout and detect the charger as a non-standard charger.

8.2 Typical Application

The BQ24392-Q1 device is used between the micro or mini-USB connector port and USB host to enable and disable the USB data path and detect chargers that are inserted into the micro or mini-USB connector.

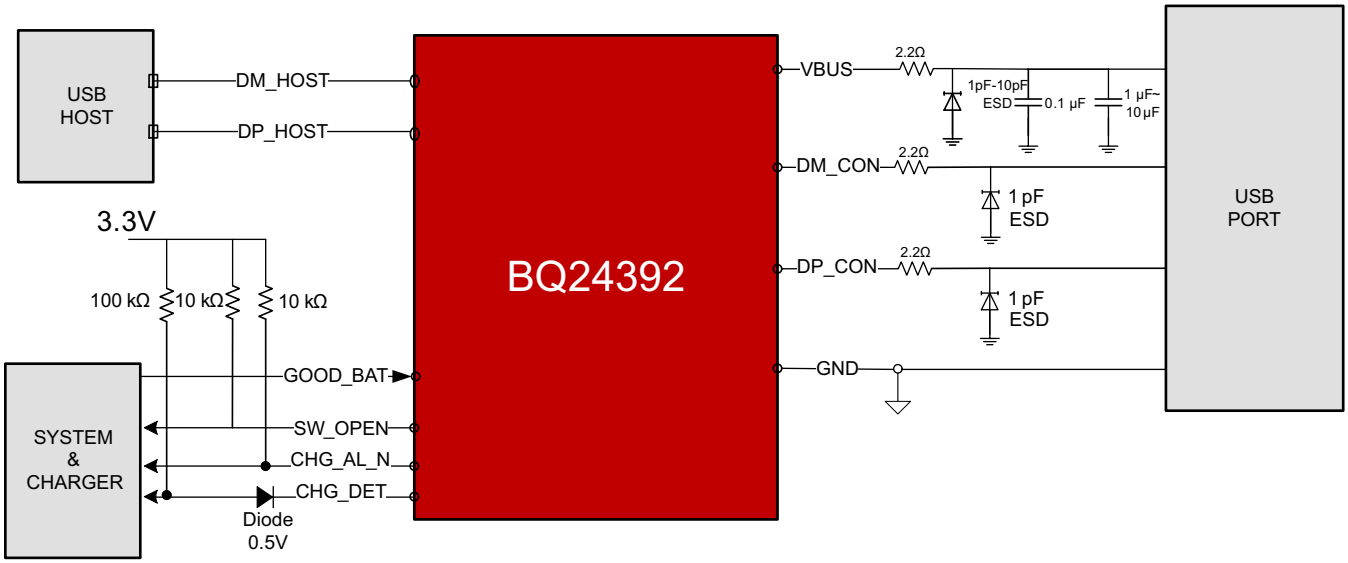


Figure 5. Application Schematic

Typical Application (continued)

8.2.1 Design Requirements

VBUS requires 1-µF – 10-µF and 0.1-µF bypass capacitors to reduce noise from circuit elements by providing a low impedance path to ground for the unwanted high frequency content. The 0.1-µF capacitor filters out higher frequencies and has a lower series inductance while the 1 µF ~ 10 µF capacitor filters out the lower frequencies and has a much higher series inductance. Using both capacitors will provide better load regulation across the frequency spectrum.

SW_OPEN and CHG_AL_N are open-drain outputs that require a 10-kΩ pull-up resistor to VDDIO and VBUS.

VBUS, DM_CON, and DP_CON are recommended to have an external resistor of 2.2 Ω to provide extra ballasting to protect the chip and internal circuitry.

DM_CON and DP_CON are recommended to have a 1-pF external ESD protection diode rated for 8-kV IEC protection to prevent failure in case of an 8-kV IEC contact discharge.

VBUS is recommended to have a 1-pF ~ 10-pF external ESD Protection Diode rated for 8-kV IEC protection to prevent failure in case of an 8-kV IEC contact discharge

CHG_DET is a push-pull output pin. An external pull-up and diode are shown to depict a typical 3.3-V system. The pull-up resistor and diode are optional. The pull-up range on the CHG_DET pin is from 3.5 V to V_{VBUS}. When V_{VBUS} > 7 V, CHG_DET will be clamped to 7 V.

8.2.2 Detailed Design Procedure

The minimum pull-up resistance for the open-drain data lines is a function of the pull-up voltage V_{PU}, output logic LOW voltage $V_{OL(max)}$, and Output logic LOW current I_{OL}.

$$R_{PU(MIN)} = (V_{PU} – V_{OL/MAX}) / I_{OL} \quad (1)$$

The maximum pull-up resistance for the open-drain data lines is a function of the maximum rise time of the desired signal, t_r, and the bus capacitance, C_b.

$$R_{PU(MAX)} = t_r / (0.8473 \times C_b) \quad (2)$$

8.2.3 Application Curves

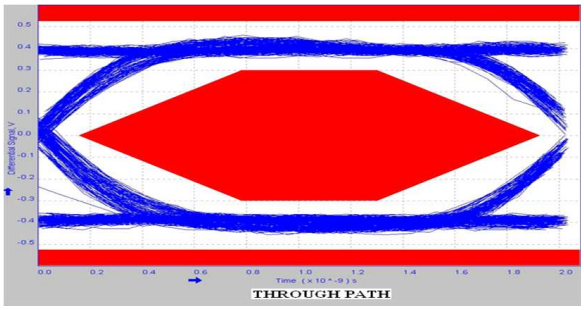


Figure 6. 480-Mbps USB 2.0 Eye Diagram with No Device

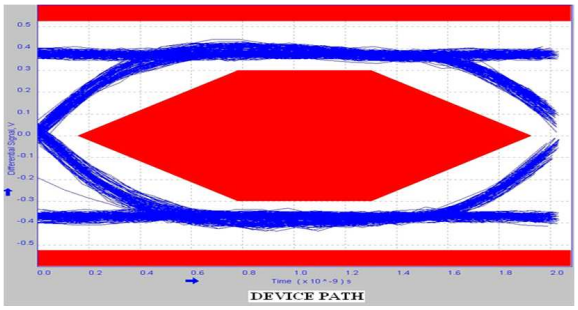


Figure 7. 480-Mbps USB 2.0 Eye Diagram with USB Switch

9 Power Supply Recommendations

Power to the device is supplied through the VBUS pin from the device that is inserted into the mini or micro-USB port. The power from the inserted devices should follow BCv1.2 specification.

10 Layout

10.1 Layout Guidelines

Place VBUS bypass capacitors as close to VBUS pin as possible and avoid placing the bypass caps near the DP/DM traces.

The high speed DP/DM traces should always be matched lengths and must be no more than 4 inches; otherwise, the eye diagram performance may be degraded. A high-speed USB connection is made through a shielded, twisted pair cable with a differential characteristic impedance of 90 Ω ±15%. In layout, the impedance of DP and DM traces should match the cable characteristic differential 90-Ω impedance.

Route the high-speed USB signals using a minimum of vias and corners. This reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. This reduces reflections on the signal traces by minimizing impedance discontinuities.

Do not route USB traces under or near crystals, oscillators, clock signal generators, switching regulators, mounting holes, magnetic devices or IC's that use or duplicate clock signals.

Avoid stubs on the high-speed USB signals because they cause signal reflections. If a stub is unavoidable, then the stub should be less than 200 mm.

Route all high-speed USB signal traces over continuous planes (VCC or GND), with no interruptions.

Avoid crossing over anti-etch, commonly found with plane splits.

Due to high frequencies associated with the USB, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in Figure 8.

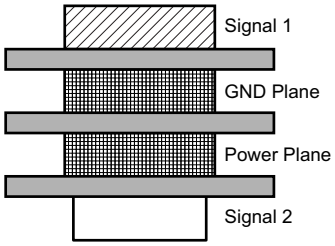


Figure 8. Four-Layer Board Stack-Up

The majority of signal traces should run on a single layer, preferably Signal 1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

10.2 Layout Example

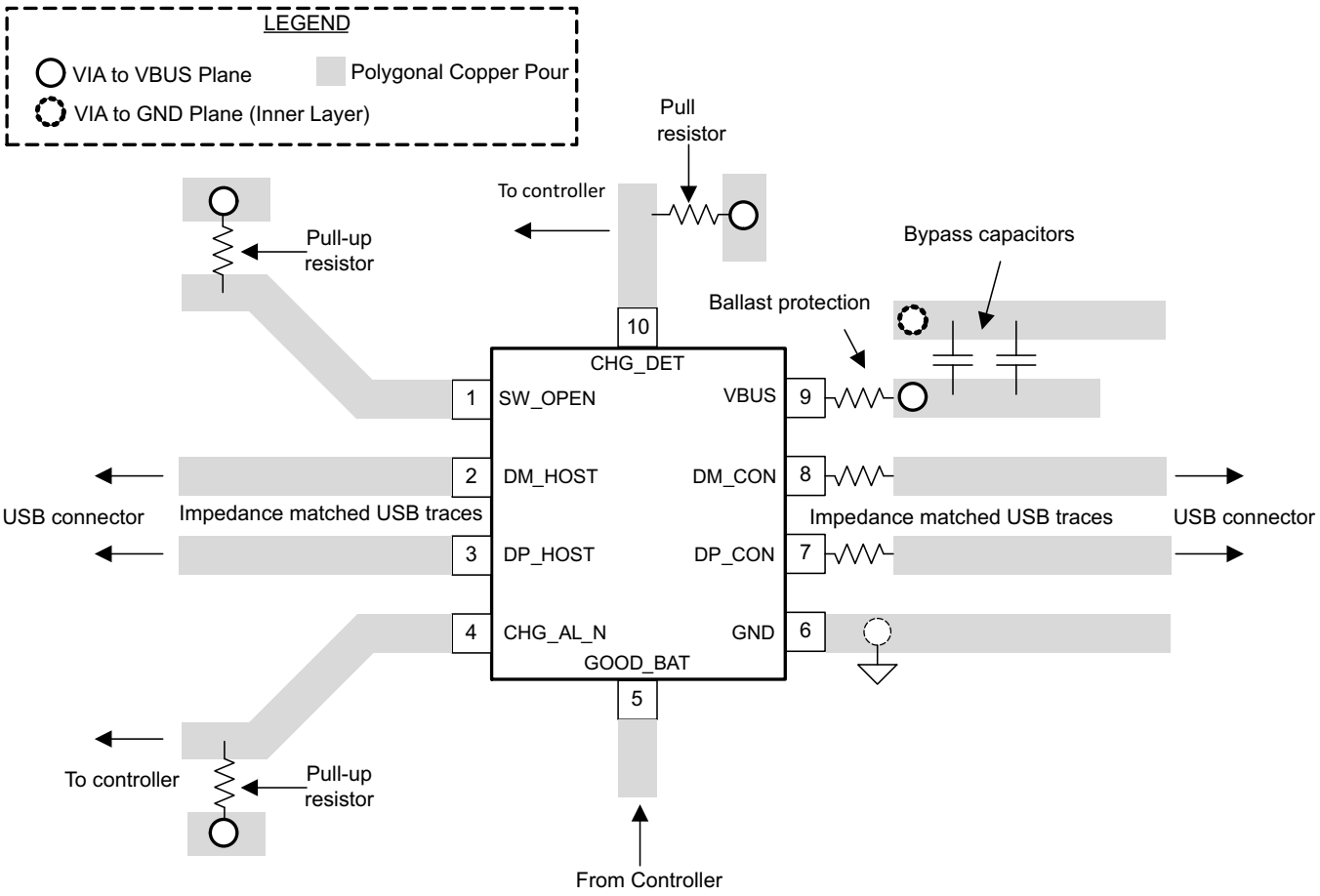


Figure 9. Package Layout

11 Device and Documentation Support

11.1 Trademarks

Apple is a trademark of Apple.
TomTom is a trademark of TomTom International.
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ24392QRSERQ1	ACTIVE	UQFN	RSE	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-3-260C-168 HR	-40 to 125	EXH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF BQ24392-Q1 :

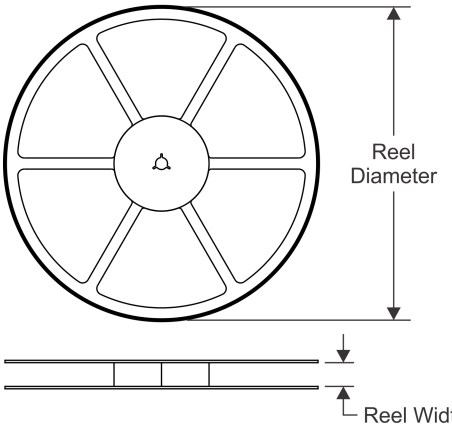
- Catalog: BQ24392

NOTE: Qualified Version Definitions:

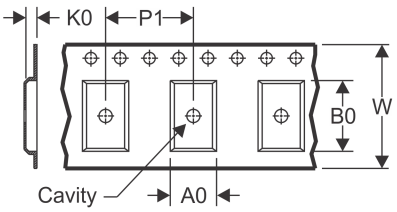
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

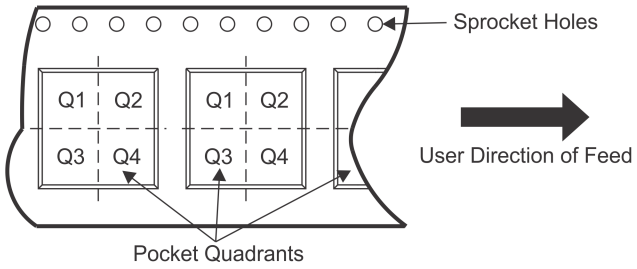


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

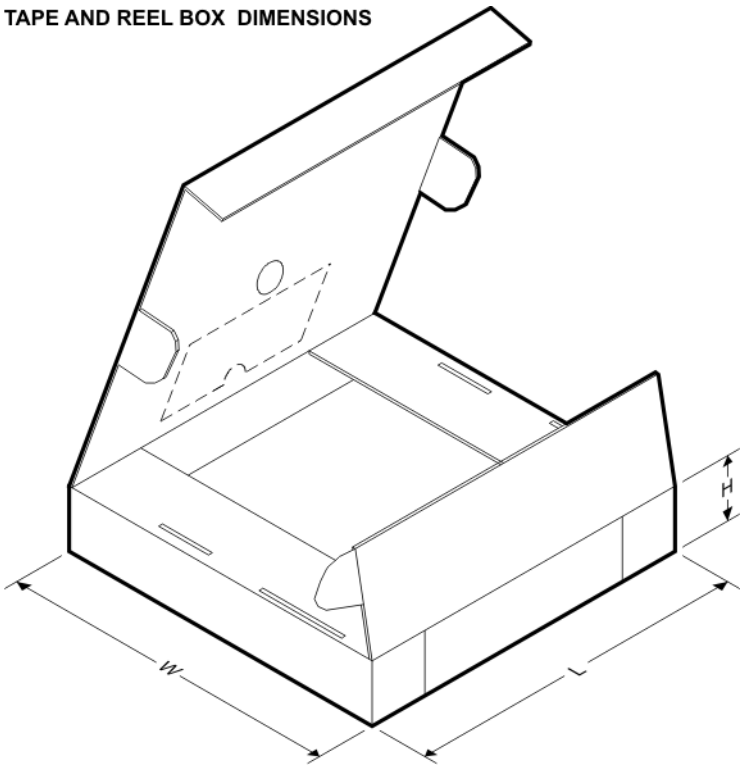
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24392QRSERQ1	UQFN	RSE	10	3000	180.0	8.4	1.68	2.13	0.76	4.0	8.0	Q1

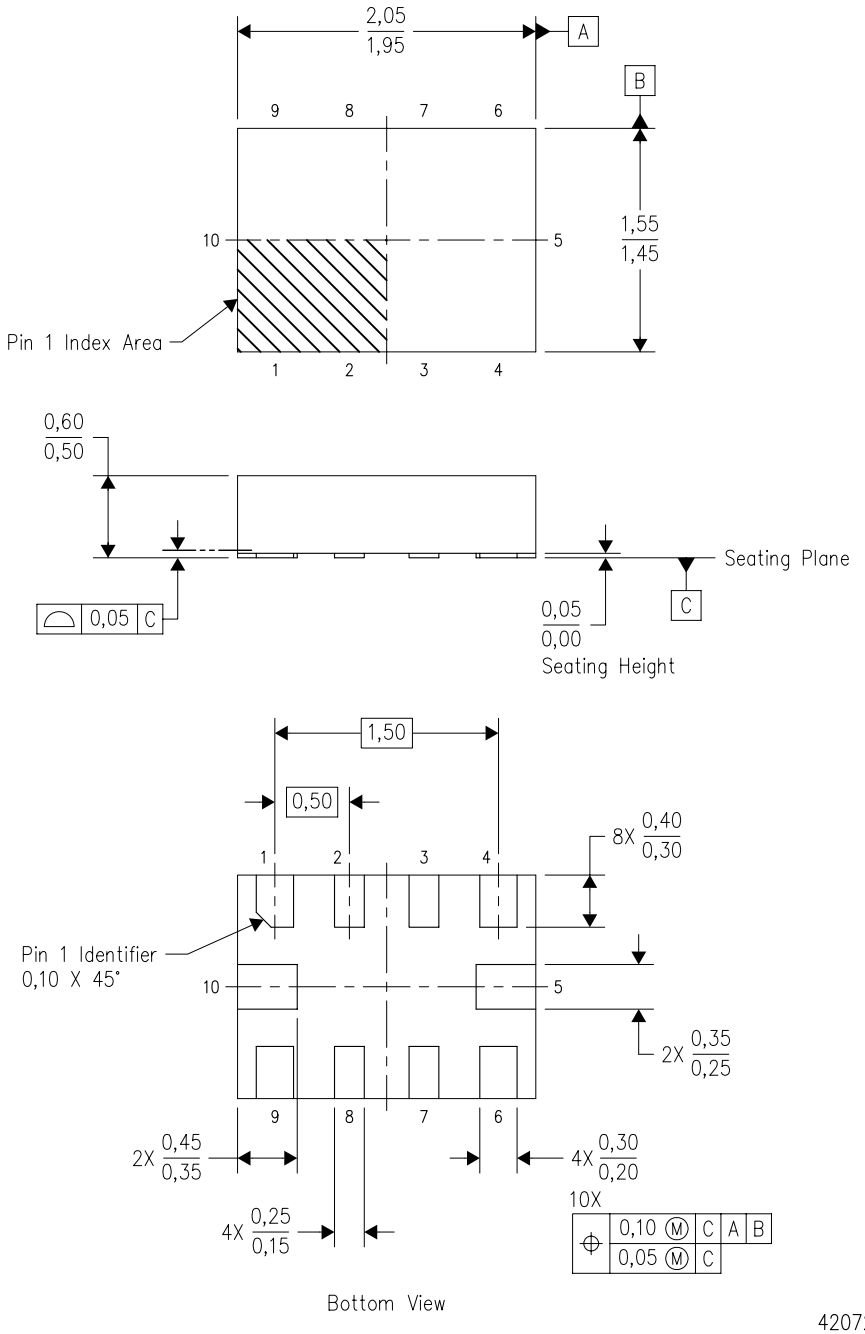
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24392QRSERQ1	UQFN	RSE	10	3000	223.0	270.0	35.0

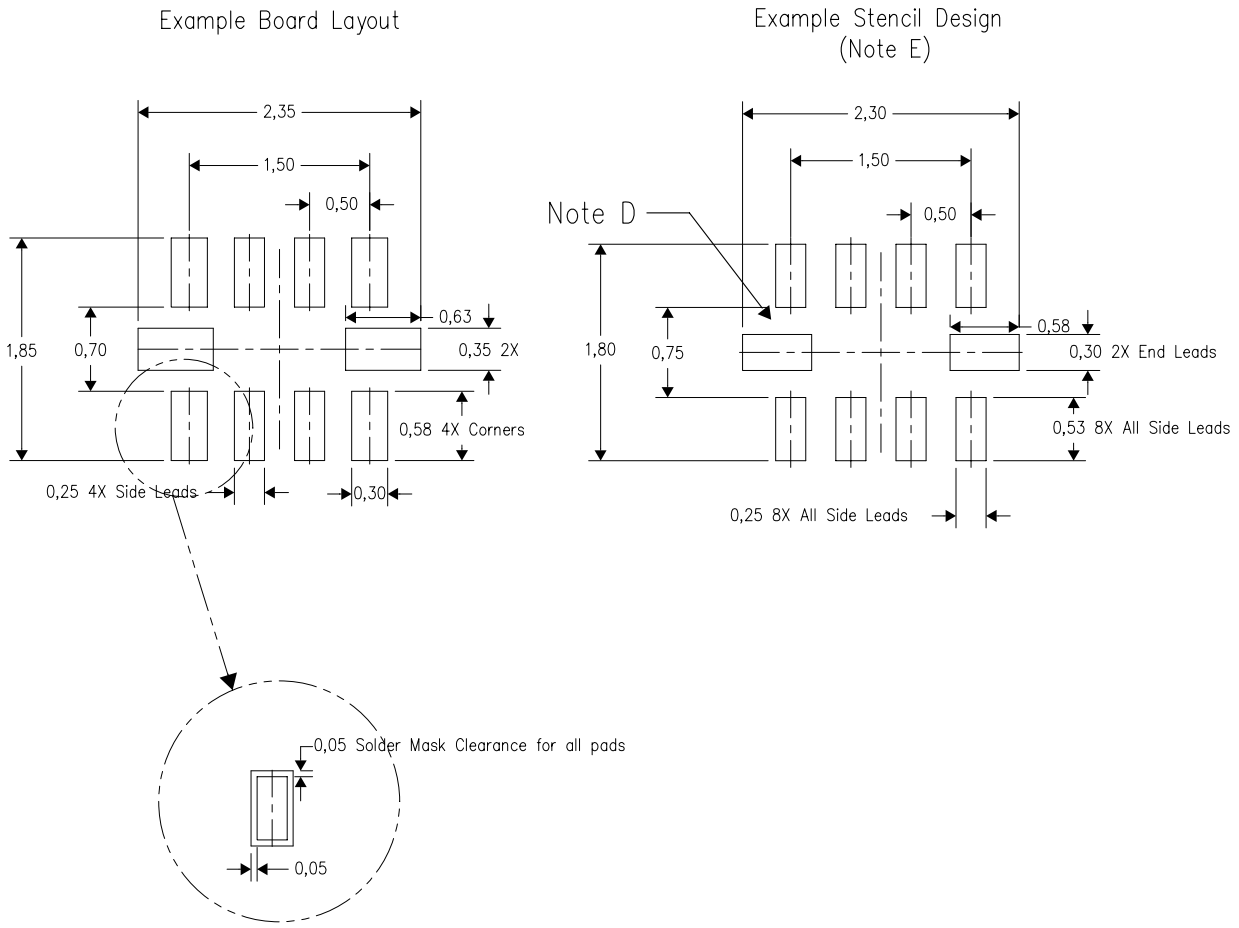
RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4207268–3/D 01/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation UEFD.

RSE (R–PUQFN–N10) PLASTIC QUAD FLATPACK NO–LEAD



4208106–3/E 01/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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