NEC

NEC Electronics Inc.

μPD6308
LCD COLUMN DRIVER

PRELIMINARY INFORMATION

Description

The μPD6308 can directly drive any multiplexed dot-matrix LCD organized with up to 40 columns. It is easily cascaded to fit the user's system.

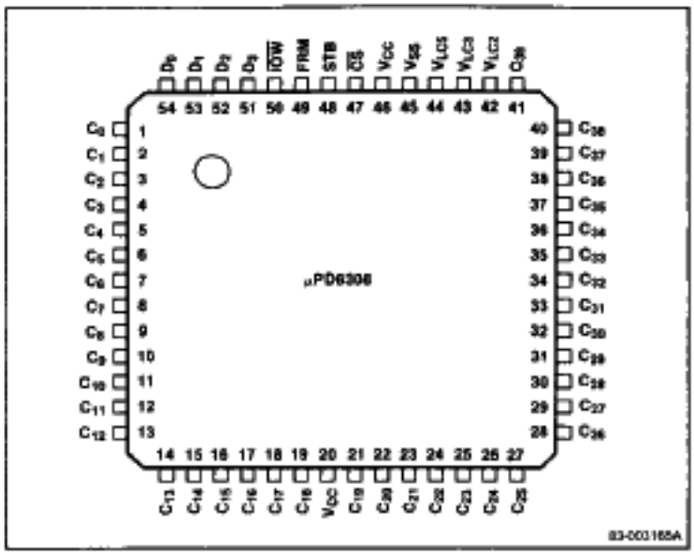
Features

- ☐ High voltage output 21 V maximum
- ☐ Directly controllable by the μPD72030
- ☐ CMOS technology
- ☐ Single 5 V ±10% power supply

Ordering Information

Part Number	Package Type
μPD6308G-F	54-pin plastic miniflat
μPD6308G-R	54-pin plastic miniflat (inverted leads)

Pin Configuration



Pin Identification

No.	Symbol	Function
1-19, 21-41	C_0-C_{39}	Column drive output
20	V_{CC}	Positive power supply
42-44	V_{LC2}, V_{LC3}, V_{LC5}	LCD drive supply
45	V_{SS}	Ground
46	V_{CC} (= V_{LC0}	Positive power supply and LCD drive supply
47	$\overline{CS}$	Chip select output
48	STB	Strobe input
49	FRM	Frame input
50	$\overline{IOW}$	I/O write input
51-54	D_3-D_0	Data input

6

Pin Functions

C_0-C_{39} (Column Drive Output)

LCD column drive output.

V_{LC2}, V_{LC3}, V_{LC5} (LCD Drive Supply)

Reference voltages used to drive C_0-C_{39}.

D_0-D_3 (Data Input)

This is the display data bus. Data in the 40-bit input latch is written via this bus four bits at a time, a total of 10 times.

FRM (Frame)

A high level input to this pin displays the positive frame and a low level input displays the negative frame.

STB (Strobe)

This is the column driver strobe input. At the leading edge of the STB input, the 40-bit display data in the input latch is transferred to the output latch to appear in the column drive output.

$\overline{IOW}$ (I/O Write)

This is the data write input. If $\overline{CS}$ is active and $\overline{IOW}$ goes low, data on D_0-D_3 is written to the input latch.

$\overline{CS}$ (Chip Select)

This input pin is connected to the chip select output of the row driver as the $\overline{IOW}$ enable. $\overline{CS}$ is active low.

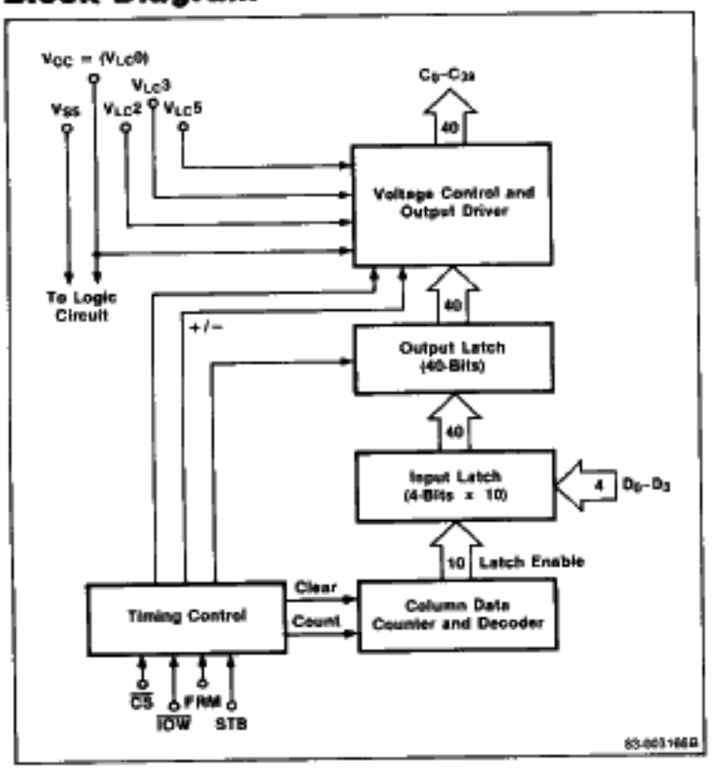
V_{CC} (= V_{LC0}) (Power Supply and LCD Drive Supply)

Connect the 5 V power supply between V_{CC} and V_{SS}. V_{CC} is also used for the column drive voltage.

V_{SS} (Ground)

Ground.

Block Diagram



Functional Description

Timing Control Circuit

This circuit controls the timing that operates each μPD6308 internal block.

Voltage Control Driver Circuit

This circuit generates the column signals for AC drive of the LCD panel. Table 1 lists C_0-C_{39} output levels. FRM' is obtained by internally synchronizing the FRM signal with the leading edge of the STB signal.

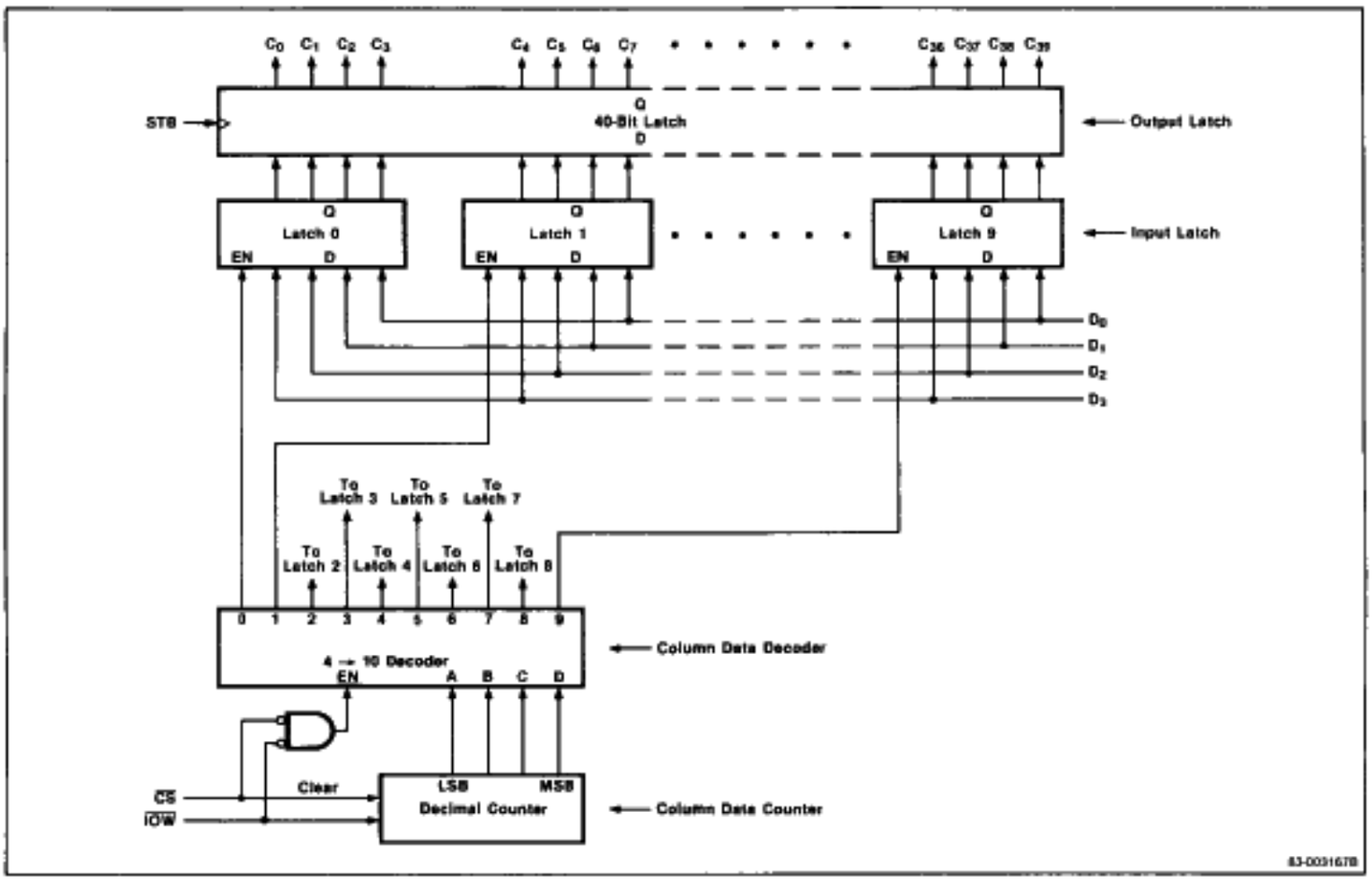
Table 1. C_0-C_{39} Output Levels

Function	+ (FRM' = 1)	− (FRM' = 0)
Select (Data = 1)	V_{LC5}	V_{LC0}
Clears (Data = 0)	V_{LC3}	V_{LC2}

Column Data Counter/Decoder Circuit

The column data counter/decoder circuit is shown in figure 1. This decimal circuit generates latch enable pulses to the input latches, which latch 40 bits of data (four bits at a time, a total of 10 times). The number of decoder outputs can be increased by cascading μPD6308s under the control of $\overline{CS}$. The counter value increments at the leading edge of $\overline{IOW}$, and clears when $\overline{CS}$ goes high.

Figure 1. Internal Block Diagram



Input Latch Circuit

The input latch circuit is shown in figure 1. The input latches display data four bits at a time until 40 bits are latched and displayed. When $\overline{CS}$ is active low, each $\overline{IOW}$ active low pulse input to the decimal counter causes 1 of 10 latch enable signals to be generated from the column data decoder. Latches 0 to 9 are enabled consecutively to load data D_0-D_3 until 40 bits are latched.

Output Latch Circuit

The output latch circuit is shown in figure 1. The 40 bits output from the input latch circuit are transferred to the output latch circuit at the leading edge of the STB signal and appear on the column drive outputs. Note that D_0 is output to C_3, D_1 to C_2, D_2, to C_1, and D_3 to C_0.