ROCKWELL SCIENTIFIC

RTH010

9 GHz Bandwidth 1 GS/s Dual Track-and-Hold

Features

- 9 GHz Small-Signal Input Bandwidth
- 6 GHz Large-Signal Input Bandwidth (1 Vpp)
- 200 - 1000 MHz Sampling Rate
- -63 dB Hold Mode Distortion (0.5 GHz 1 Vpp V_{IN})
- -59 dB Hold Mode Distortion (1.0 GHz 1 Vpp V_{IN})
- -45 dB Hold Mode Distortion (3.0 GHz 0.5 Vpp V_{IN})
- < 100 fs Aperture Jitter
- < 250 ps Acquisition Time
- < 50 ps Rise Time (20 – 80%)
- Differential Analog Input/Output
- 100 – 1000 MHz Output Data Rate
- Output Held more than Half Clock Cycle
- Track Mode Select

Applications

- Test Instrumentation Equipment
- RF Demodulation Systems
- Radar
- Software Radio
- Digital Receiver Systems
- High-Speed DAC Deglitching
- THA for Differential ADCs
- Digital Sampling Oscilloscopes

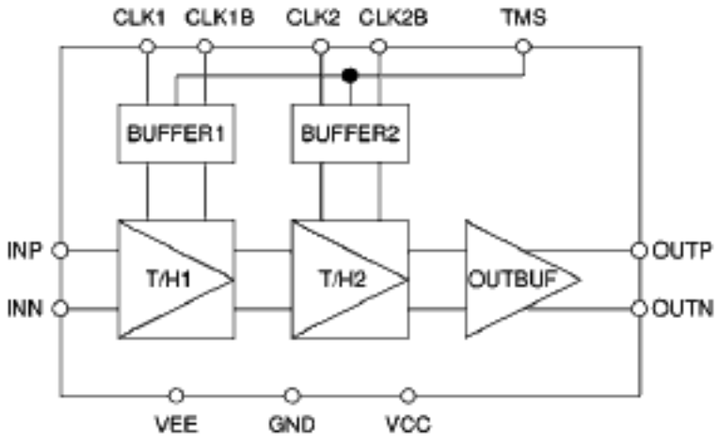


Figure 1. Functional Diagram

Product Description

RTH010's unprecedented bandwidth and aperture jitter enable 10-bit 1-GS/s sampling of DC to multi-GHz signals. The differential-to-differential dual track-and-hold cascades two track-and-hold circuits, TH1 and TH2. It is a monolithic circuit fabricated in an 80-GHz f_T GaAs HBT process. The RTH010 provides a held output for more than half a clock cycle, easing bandwidth requirements of subsequent circuitry relative to the case of a single track-and-hold (TH). The option to independently clock TH1 and TH2 (as low as 100 MHz) further relaxes this requirement for sub-sampling applications.

Absolute Maximum Ratings

Supply Voltages

VCC to GND	-1 V to +6 V
VEE to GND	-6 V to +1 V
VCC to VEE	-1 to +11 V

Input Voltages

INP, INN to GND	-1 to +1 V
CLK1, CLK1B, CLK2, CLK2B to GND	-1 to +1 V
TMS to GND	-6 V to +1 V

Output Voltages

Vterm (Output Termination Voltage) to GND	-2.5 to +3 V

Temperature

Operating Temperature	-30 to +70 °C
Case Temperature	-15 to +85 °C
Junction Temperature	+125 °C
Lead, Soldering (10 Seconds)	+220 °C
Storage	-40 to 125 °C

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Electrical Specification

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
ANALOG INPUT							
Full Scale Range	FSR		4		1000		mVpp
Common Mode Voltage	V_{CM}		2	-100	0	100	mV
Input Resistance		Each Lead to GND	2	46	50	54	Ω
Input Capacitance		Each Lead to GND	2	200	250	300	fF
CLOCK INPUTS, CLK1(B) AND CLK2(B)							
Amplitude[1]			2	200	600	1000	mVpp
Common Mode Voltage			2	-250	0	250	mV
Input Resistance		Each Lead to GND	2	46	50	54	Ω
Input Capacitance		Each Lead to GND	2	200	250	300	fF
DIGITAL INPUT, TRACK-MODE SELECT							
TMS High		Track Mode	3	-0.65	0	1	V
TMS Low		Sampled Mode. Open TMS ≈ –2.8V	3	-5	Open	-2.05	V
Max. Current Draw		Into Lead, TMS High	3		0.75		mA
ANALOG OUTPUT							
Ext. Termination Voltage	Vterm		3	0	0	2	V
Ext. Termination Resistor	Rterm	Required From Outputs To Vterm	3		50		Ω
Swing		Into 50 Ω Rterm, FSR Input	2	0.76	0.80	0.84	Vpp
Common Mode Voltage		Relative to Vterm	3	-1.1	-1.0	-0.9	V
Average Current		Into Each Output Lead	3		20		mA
Maximum Current		Into Output Lead	3		30		mA
DC CHARACTERISTICS							
Gain			1	0.76	0.80	0.84	
Offset Voltage			3			±15	mV
DYNAMIC TRACK MODE PERFORMANCE, SINEWAVE INPUT							
Track Bandwidth		-3dB Gain, TH1 & TH2 In Track Mode	2	800	1000	1200	MHz
Gain Flatness Deviation			2			±0.5	dB
Integrated Noise		Input Referred	4		400		µV
Noise Floor		Input Referred	4		3.9		nV/√ns
DYNAMIC HOLD MODE PERFORMANCE, SINEWAVE INPUT[2]							
Bandwidth, Small Signal	bw	-3dB Gain, Small Signal (< 0.1 Vpp)	2	8.5	9	9.5	GHz
Bandwidth, Half Signal		-3dB Gain, -6dBfs (0.5 Vpp)	2	7.5	8	8.5	GHz
Bandwidth, Large Signal	BW	-3dB Gain, Large Signal (1 Vpp)	2	5.5	6	6.5	GHz
Gain Flatness Deviation			2			±1	dB
Integrated Noise		Input Referred	4		550		µV
Noise Floor		Input Referred	4		5.3		nV/√ns
TH1 Hold Feedthrough[3]		500 MHz 1 Vpp Input	2		-72	-70	dB
TH1 Hold Feedthrough[3]		1 GHz 1 Vpp Input	2		-68	-65	dB
-THD/SFDR 20 MHz		1 Vpp Input	2	68/71	71/72		dB
-THD/SFDR 520 MHz		1 Vpp Input	2	62/65	63/66		dB
-THD/SFDR 1020 MHz		1 Vpp Input	2	58/59	59/60		dB
-THD/SFDR 1520 MHz		1 Vpp Input	2	44/45	46/47		dB
-THD/SFDR 3020 MHz		1 Vpp Input	2	34/34	35/35		dB
-THD/SFDR 5020 MHz		1 Vpp Input	2	22/24	25/27		dB
-THD/SFDR 20 MHz		0.5 Vpp Input	1	75/78	77/82		dB
-THD/SFDR 520 MHz		0.5 Vpp Input	1	63/65	65/67		dB
-THD/SFDR 1020 MHz		0.5 Vpp Input	1	62/63	64/65		dB
-THD/SFDR 1520 MHz		0.5 Vpp Input	1	55/57	57/58		dB
-THD/SFDR 3020 MHz		0.5 Vpp Input	1	43/44	45/46		dB
-THD/SFDR 5020 MHz		0.5 Vpp Input	1	29/29	32/32		dB
-THD/SFDR 5020 MHz		0.25 Vpp Input	2	35/35	38/38		dB
-THD/SFDR 5020 MHz		0.015 Vpp Input	2	49/54	52/57		dB

[1] For > 500 MHz sinusoidal CLK1(B), 500 to 700 mVpp (–2 to 1 dBm,pp) amplitude is recommended for combined aperture jitter and clock feed-through performance. At lower clock frequencies, use high amplitude for minimum jitter. See Theory of Operation.

[2] For out-of-phase clocking of TH1 and TH2 with 50% duty cycle, using a low jitter 500-MHz 0-dBm sinusoidal clock passed through a passive single-to-differential balun. Distortion numbers may worsen by several dB if single-ended clocking is used.

[3] Measured with TH2 in track mode and comparing the DTH output for TH1 in track and hold mode. See Theory of Operation.

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Electrical Specification (Continued)

PARAMETER	SYMBOL	CONDITIONS, NOTE	TEST LEVEL	MIN	TYP	MAX	UNITS
TRACK-TO-HOLD SWITCHING AND HOLD STATE, TH1							
Aperture Delay	ta	After V(CLK1) - V(CLK1B) Goes Neg.	4		+60		ps
Aperture Jitter	Δt	Jitter Free 1-GHz 0.5-Vpp CLK1(B)[4,5]	3	70	100	130	fs
Settling Time to 1 mV	ts	At Hold Capacitors. ttrack1,min Observed	4		300		ps
Differential Pedestal/V_{IN}[6]			4		-2		%
Diff. Droop Rate/V_{IN}			4		-1		%/ns
Hold Noise[7]		Per Sqrt(Hold Time)	4		50		μV/√ns
Minimum CLK1 Freq.	fclk1, min	50% Duty Cycle Clock	2			200	MHz
Maximum CLK1 Freq.	fclk1, max	50% Duty Cycle Clock	2	1000		1250	MHz
Maximum Hold Time[8]	thold1, max		3	5	8	12	ns
HOLD-TO-TRACK SWITCHING AND TRACK STATE, TH1							
Acquisition Time to 1 mV[9]	tacq	At Hold Caps, FSR Step At Input	4		250		ps
Max. Acq. Slew Rate[9]	dvdt,max	At Hold Caps, FSR Step At Input	4		15		V/ns
Rise Time[9]	tr	20 – 80%	3			50	ps
Minimum Track Time	ttrack1,min	thold1,max Observed	2		0.4		ns
Recovery Time		Required Accumulated Track Time After thold1,max Violation	3			4	ns
TRACK-TO-HOLD SWITCHING AND HOLD STATE, TH2							
Aperture Delay	ta2	After V(CLK2) - V(CLK2B) Goes Neg.	4		+60		ps
Settling Time to 1 mV[10]	ts2	At DTH Output. ttrack2,min Observed	4		300		ps
Differential Pedestal/V_{IN}[11]			4		±0.25		%
Diff. Droop Rate/V_{IN}			4		-0.12		%/ns
Hold Noise[7]		Per Sqrt(Hold Time)	4		25		μV/√ns
Minimum CLK2 Freq.	fclk2,min	50% Duty Cycle Clock	2			100	MHz
Maximum CLK2 Freq.	fclk2,max	50% Duty Cycle Clock	2	1000		1250	MHz
Maximum Hold Time[8]	thold2,max		3	10	15	20	ns
HOLD-TO-TRACK SWITCHING AND TRACK STATE, TH2							
Minimum Track Time after TH1 in Hold Mode[12]	ttrack2,min	thold2,max Observed	2		0.5		ns
Recovery Time		Required Accumulated Track Time After thold2,max Violation	3			4	ns
POWER SUPPLY REQUIREMENTS							
Positive Supply Voltage	VCC		1	4.75	5.0	5.25	V
VCC Current	ICC		1		130	180	mA
Negative Supply Voltage	VEE		1	-5.45	-5.2	-4.95	V
VEE Current	IEE		1		325	400	mA
Power Dissipation			1	2.2	2.35	2.5	W
Warm-up Time[13]		After Power-up	2			10	s

[4] The clock source jitter and the aperture jitter combine in an rms manner to yield the total sampling jitter. See Definition of Terms.
[5] Device aperture jitter increases as the V(CLK1) – V(CLK1B) slew rate at the zero crossing decreases. See Theory of Operation.
[6] The differential pedestal error is proportional to the input signal. For TH1 it corresponds to a track-to-hold gain ~ -0.17 dB. This gain loss may be observed at the DTH output if TH2 is in track mode during the TH1 track-to-hold transition.
[7] The variance of the hold noise is proportional to the hold time, thold. For example, for TH1, a 4-ns hold time, thold1, gives about 100 μV accumulated hold noise. TH1 and TH2 hold noise, up to the output sampling instant, should be rms added to the hold mode integrated noise of the DTH.
[8] Maximum hold time is determined by droop of single-ended hold capacitor voltages. The resulting shift of internal operating voltages is not directly observable at the DTH outputs but eventually causes device performance degradation.
[9] TH1 tacq, dvdt,max, and tr also apply to the reconstructed DTH output if sub-sampling a fast-edge repetitive wave form.
[10] Output is settled ta2 + ts2 after CLK2(B) downward transition.
[11] The differential pedestal error is proportional to the input signal. For TH2 it corresponds to a track-to-hold gain ~ ±0.02 dB.
[12] ttrack2,min > ts, since the buffered TH1 output onto the TH2 hold capacitors lags behind the TH1 hold capacitor signal.
[13] The part functions immediately and reaches specification after warm-up time.

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Test Levels

TEST LEVEL	TEST PROCEDURE
1	100% production tested at Ta = 25 C[1]
2	Sample tested at Ta = 25 C unless other temperature is specified[1]
3	Quaranteed by design and/or characterization testing
4	Typical value only

[1] All tests are continuous, not pulsed. Therefore, Tj (junction temperature) > Tc (case temperature) > Ta (ambient temperature). This is the normal operating condition and is more stressful than a pulsed test condition.

Pin Description and Pin Out

P/I/O	NAME	FUNCTION
P	GND	Power Supply Ground
I	TMS	Track Mode Select
I	INP	Analog Input
O	OUTP	Analog Output
I	CLK1	Clock Input 1, High = Track Mode
I	CLK2	Clock Input 2, High = Track Mode
P	VEE	Negative Power Supply, -5.2V ± 5%
P	VCC	Positive Power Supply, 5.0V ± 5%
I	INN	Complementary Analog Input
O	OUTN	Complementary Analog Output
I	CLK1B	Complementary Clock Input 1
I	CLK1B	Complementary Clock Input 2

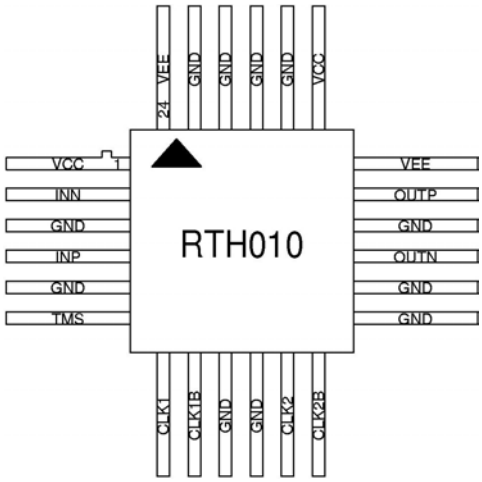


Figure 2. Pin configuration (top view, not to scale)24-lead glass-wall metallized ceramic quad flat pack

Definitions of Terms

Acquisition Time (tacq). The delay between the time that a track-and-hold circuit (TH) enters track mode and the time that the TH hold capacitor nodes track the input within some specified precision. The acquisition time sets a lower limit on the required track time during clocked operation.

Aperture Delay (ta). The average (or mean value) of the delay between the hold command (input clock switched from track to hold state) and the instant at which the analog input is sampled. The time is positive if the clock path delay is longer than the signal path delay. It is negative if the signal path delay is longer than the clock path delay.

Aperture Jitter (Δt). The standard deviation of the delay between the hold command (input clock switched from hold to track state) and the instant at which the analog input is sampled, excluding clock source jitter. It is the total jitter if the clock source is jitter free (ideal). Jitter diverges slowly as measurement time increases because of "1/f" noise, important at low frequencies (< 10 kHz). The specified jitter takes into account the white noise sources only (thermal and shot noise). For high-speed samplers this is reasonable, since even long data records span a time shorter than the time scale important for 1/f noise. For white-noise caused jitter, the clock and aperture jitter can be added in an rms manner to obtain the total sampling jitter.

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If the underlying voltage noise mechanism of the sampling jitter has a white spectrum, the sampled signal will display a white noise floor as well. In this case, the required aperture jitter, Δt, to achieve a certain SNR, for a full-scale sinewave at frequency, *f*, is given by (B. Razavi, Principles of Data Conversion, IEEE Press, 1995, Appendix 2.1):

$$SNR\,(dB) = -20\log(2\pi f \Delta t)$$

If this TH is used in front of an *n*-bit ADC, then the ideal ADC SNDR is given by:

$$SNDR(dB) = 10\log(3/2) + 20\log(2)n = 1.76 + 6.02n$$

In order that the TH jitter performance not limit the ADC performance, the jitter must fulfill:

$$\Delta t \le \frac{1}{\sqrt{6}\pi 2^n f}\,.$$

Note that this is independent of the sampling rate, so undersampling does not improve jitter tolerance. The averaging that is often combined with undersampling in test equipment, does improve jitter tolerance (and tolerance to other white noise effects).

The criterion above is sharper than the standard (incorrect) time-domain slope estimate by a factor √6. The reason is that *n*-bit quantization requires an rms error of (quantization step)/√12, which is considerably smaller than the quantization step error implicitly allowed in the usual time-domain estimates (another √2 comes from the energy of a sinewave relative to its amplitude squared).

The time-domain maximum slope argument can be appropriate for non-sinusoidal inputs, such as those encountered in instrumentation. If the rms error, ΔV, in the maximum slope region, slope FSR/(rise time), is used to define an effective number of bits, *n*, then the jitter simply needs to fulfill:

$$\Delta t \le \frac{rise\ time}{2^n}$$

Clock Jitter. The standard deviation of the instants of the mid-point of the relevant (rising or falling) edge of the clock source relative to the ideal instants (best fit). This jitter can be derived from the phase noise of the clock source, where the lower frequency bound of integration should correspond to the duration of a measurement record that the source will be used for.

Full Scale Range (FSR). The maximum difference between the highest and lowest input levels for which various device performance specifications hold, unless otherwise noted.

Gain. Ratio of output signal magnitude to input signal magnitude. For sinewave inputs, it is the ratio of the amplitude of the first (main) harmonic output (HD1) to the amplitude of the input.

Input Bandwidth (BW, bw). The input frequency at which the gain for sinewave inputs is reduced by 3 dB (factor 1/√2) relative to its average value at low frequencies. The low frequency range is defined as the range including DC over which the gain stays essentially constant. The high frequency range is characterized by an increase in gain variation versus frequency, at least including the eventual monotonic decrease of the gain ("roll-off"). The input bandwidth tends to be input amplitude dependent. It is normally largest for very small inputs (small signal bandwidth, bw) and smallest for FSR inputs (large signal bandwidth, BW).

Settling Time (ts). The delay between the time that a track-and-hold circuit (TH) enters hold mode and the time that the TH hold capacitor nodes settle to within some specified precision. The settling time sets a lower limit on the required hold time during clocked operation.

Spectrum. The finite Fourier transform (FFT) of the discrete-time-sampled TH output. Ideally, this is obtained with a very high-resolution ADC quantizing the TH output with a clock rate locked to the TH clock (the ADC may be clocked at a slower rate than the TH). In the case of a dual TH (DTH), we can also use the beat frequency test, where the input frequency is close to an integer multiple of the clock frequency, and the DTH output is fed directly into a spectrum analyzer. The DTH output then contains little high frequency energy and the low frequency part of the spectrum analyzer sweep accurately

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represents the TH spectrum that would have been obtained with the ADC method.

Spurious Free Dynamic Range (SFDR). The ratio of the magnitude of the first (main) harmonic, HD1, and the highest other harmonic (or nonharmonic other tone, if present), as observed in the TH spectrum. The input is FSR, unless otherwise noted. SFDR in dB is given by 20 log(SFDR as amplitude ratio), and is generally positive.

Total Harmonic Distortion (THD). The ratio of the square root of the sum of the harmonics 2 to 5 to the amplitude of the first (main) harmonic in the TH spectrum. THD in dB is given by 20 log(THD as amplitude ratio), and is generally negative.

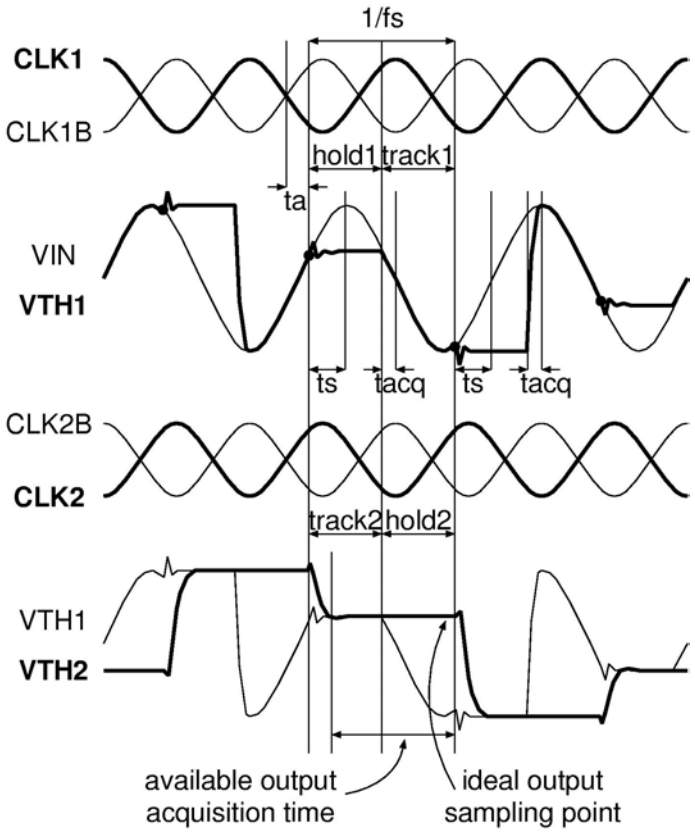


Figure 3. Timing diagram for out-of-phase clocking of TH1 and TH2

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Theory of Operation

The DTH chip contains two TH's, TH1 and TH2, in series, together with clock shaping circuitry, BUFFER1 and BUFFER2, and a 50-ohm output driver, OUTBUF (Figure 1). To maximize dynamic range and insensitivity to noise, all non-DC internal circuits and all non-DC inputs and outputs are differential. TH1 determines the dynamic sampled-mode performance of the DTH. Its sampling bridges exploit the ultra-high speed of the Schottky diodes available in the GaAs HBT process. TH1 clock inputs, CLK1 and CLK1B, should be driven by a low-jitter clock source. TH2 is similar to TH1, except that its bandwidth requirement is lower and its gain is closer to unity.

The DTH receives a differential analog input signal at inputs INP and INN, which is sampled on the TH1 hold capacitors upon a falling transition of its differential clock voltage V(CLK1) – V(CLK1B), after an aperture delay, ta, see Figure 2. TH1's aperture delay is positive, nominally 60 ps.

The sampling instant is affected by clock source jitter (off-chip) and aperture jitter (caused by on-chip noise). From the Definition of Terms, the required total sampling jitter for sampling a 1-GHz 1-Vpp sine wave with 10-bit accuracy is 127 fs. The aperture jitter of the RTH010 is less than 100 fs for a 1-GHz 0.5-Vpp TH1 clock, CLK1(B). Using rms addition of jitter, the clock source jitter must be less than 80 fs (over the measurement record time) for direct 10-bit sampling of GHz range signals. Given a noise variance, ΔV, of the on-chip clock buffer, its aperture jitter, Δt, is inversely proportional to the clock buffer gain and the slew rate of the incoming clock at the zero-crossing point:

$$\Delta t = \frac{\Delta V}{gain \times slew\,rate}$$

For low slew rates or frequencies, the clock buffer gain is constant and its aperture jitter is inversely proportional to the input clock slew rate, improving with increasing slew rate. For high slew rates or high frequencies, the jitter increases again, because the buffer gain drops steeply. For the RTH010, the clock buffer gain is still roughly constant up to 1 GHz, so that the aperture jitter is inversely proportional with the slew rate of the incoming clock. In the above equation, we have $\Delta V/gain \approx 0.15$ mV. The RTH010 aperture jitter at various slew rates can then be estimated. For example, a 1-GHz 0.5-Vpp sinusoidal CLK1(B) signal corresponds to a slew rate ~ 1.6 V/ns, correctly yielding an aperture jitter < 100 fs.

The held and buffered output of TH1, VTH1, is sampled on the TH2 hold capacitors upon a falling transition of its differential clock voltage V(CLK2) – V(CLK2B), after an aperture delay closely equal to that of TH1. This allows simple out-of-phase clocking of TH1 and TH2 by having opposite phases for CLK1(B) and CLK2(B). Aperture jitter of TH2 is irrelevant, since the slew rate of the TH2 input is equal to the TH1 differential droop rate, about 1000x lower than the input slew rate for TH1 for a 1-GHz 1-Vpp sine wave. TH2 can be in track mode before TH1 switches to hold, but a minimum track time of TH2 after TH1 enters hold mode must be observed to ensure that TH2 has fully acquired the TH1 output (ttrack2,min).

Hold mode feedthrough, or in-to-out hold-mode gain in dB, again is important for TH1 and not for TH2, since any distortion on the held TH1 signal by a rapidly varying TH1 input will be sampled by TH2, and can not be removed. RTH010's TH1 hold mode feedthrough performance is more than sufficient for 10-bit sampling of GHz range signals.

After a TH1 postamplifier, TH2 produces an output VTH2. For out-of-phase clocking, the delay from the hold instant of TH1 to the ideal sampling time of circuitry after TH2 is close to one full clock cycle, for example 1 ns at a 1-GHz sampling rate. The TH2 output is flat for more than half a clock cycle, which eases the bandwidth requirement of subsequent circuitry. This is true, even though a small glitch will be present at the transition from track to hold of

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TH2 and the output is only 10-bit accurate during the latter part of half a clock cycle.

Lower limits for the sampling rates of TH1 and TH2 are set by single-ended hold-mode droop rates, and lead to the specification of maximum hold times (thold1,max and thold2,max). For longer hold times, the DTH must be allowed sufficient recovery time during track phase (or a sequence of track phases), so it can return to normal operation mode. The bandwidth of subsequent circuitry can be minimal if TH2 is clocked at its lowest recommended frequency, 100 MHz. Since TH1 should be clocked at least at 200 MHz, and possibly faster to meet jitter requirements, CLK1(B) and CLK2(B) can be chosen different, as long as they are locked to each other with a proper phase relationship. Minimum required single-pole bandwidth at the output for 10-bit precision is $(10\ln 2/2\pi) \times f_{CLK2}$, or approximately $1.1 f_{CLK2}$. In practice, <200 MHz bandwidth of subsequent circuitry would be sufficient, if f_{CLK2} is 100 MHz.

One digital input, Track Mode Select (TMS), is provided to put both TH's in track mode, independent of the clock signals. The bandwidth of the DTH is substantially lower in this mode than in the sampled mode. The TMS is useful for low sample-rate operation, including DC testing

Signal Descriptions

The RTH010 inputs are terminated on-chip with 50 Ω to GND. This automatically protects against off-chip high-impedance high-voltage disturbances. The absolute maximum rated voltage at input termination resistors is ±1 V, at 20 mA current. The RTH010 is designed for 1-Vpp differential input signals, and can accept common-mode offsets up to ±100 mV. If operated in single-ended mode, terminate the complementary input off-chip with 50 Ω to the same common mode as the driven input. The single-ended FSR is half that of the differential FSR. Distortion in the single-ended mode can be up to 6 dB higher than in differential mode, and differential input should be used for optimal performance. The INP and INN inputs are equivalent, except for the polarity of their effect on OUTP and OUTN.

All four clock input signals are terminated on-chip with 50 Ω to GND. For lowest clock source jitter, use a sinusoidal clock source. Use differential clock signals for optimal performance. Large CLK1(B) amplitude benefits aperture jitter performance, small CLK1(B) and CLK2(B) amplitudes minimizes distortion due to clock feed-through in the higher clock frequency range (500 to 1000 MHz). Independent of the clock waveform, clock slew rates < 2 V/ns are recommended to minimize clock feed-through related distortion. In case of single-ended clocking the complementary input(s) can be terminated directly to GND (lowest noise, clock waveform distortion is not critical). Distortion for single-ended clocks can be several dB higher than for differential clocks, and differential clocks should be used for optimal performance.

The track-mode select, TMS, can simply be left open for the (default) sampled-mode operation of the RTH010. Grounding the TMS puts both track-and-holds, TH1 and TH2, in track-mode. In this state, the TMS draws up to 0.75 mA of current.

Due to its highly differential design, the RTH010 requires relatively modest power supply decoupling. The 0.01 μF capacitors VEE-to-GND and VEE-to-VCC (Figure 4) should be placed as close to the package as possible. Larger low frequency power supply decoupling capacitors, VEE-to-GND and VCC-to-GND, should be placed within 1 inch of the RTH010. Depending on the expected noise on the supplies more capacitors in parallel may need to be used. With low-impedance supplies that are very quiet (no digital circuitry), the RTH010 can also perform well with no external decoupling at all.

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Typical Operating Circuit

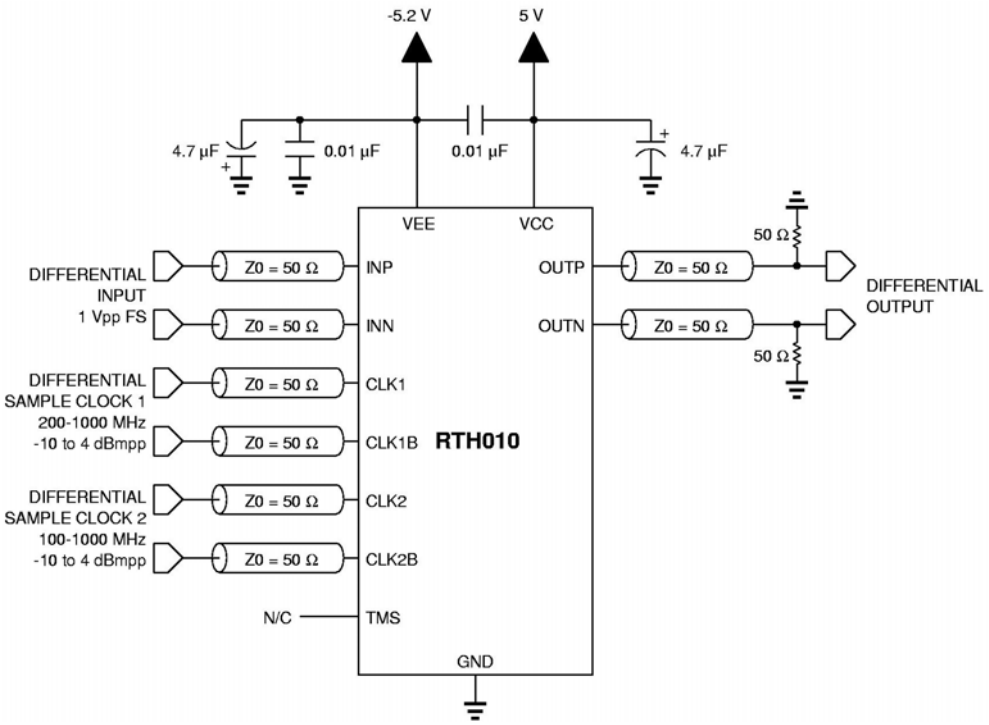


Figure 4. Typical interface circuit (sampled mode, connect TMS to GND for track mode). All differential inputs are terminated on-chip with 50 Ω to GND

Die Plot and Pad Arrangement

The inputs and output of the RTH010 are arranged in signal-ground-signal (SGS) configurations on opposite sides of the die (Figure 5). The clock signals come in under an orthogonal direction, which reduces inductive coupling to the signal path, both for bond wires and for package leads. The part does not require other components inside the package, since sufficient bypass capacitance is supplied on-chip.

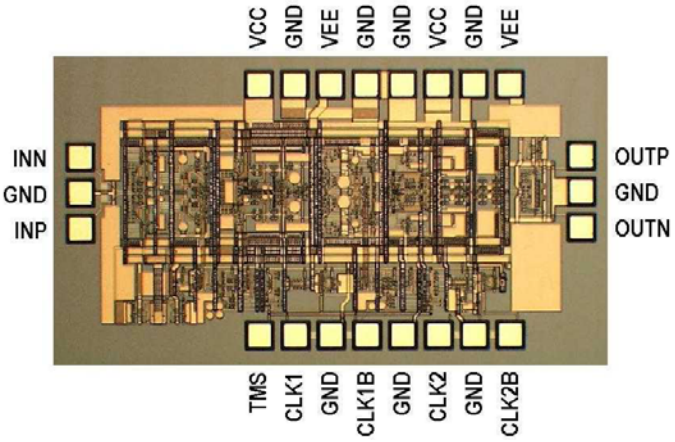


Figure 5. RTH010 die photo and pad arrangement Die size: 104 x 60 x 7 mils (2.650 x 1.525 x 0.178 mm) Pad pitch: 5.91 mil (0.150 mm)

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Typical Performance Characteristics

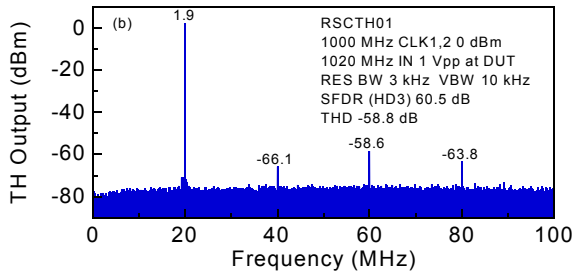


Figure 6. Beat frequency spectrum for 500 MS/s and 1020-MHz 1-Vpp input sine wave (floor set by source and spectrum analyzer)

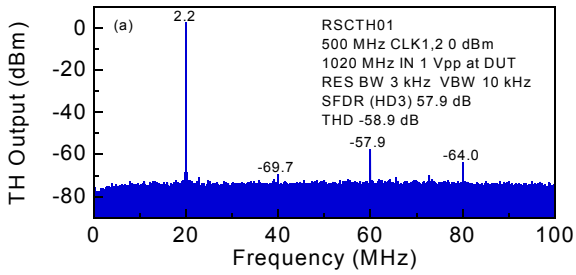


Figure 7. Beat frequency spectrum for 1 GS/s and 1020-MHz 1-Vpp input sine wave (floor set by source and spectrum analyzer)

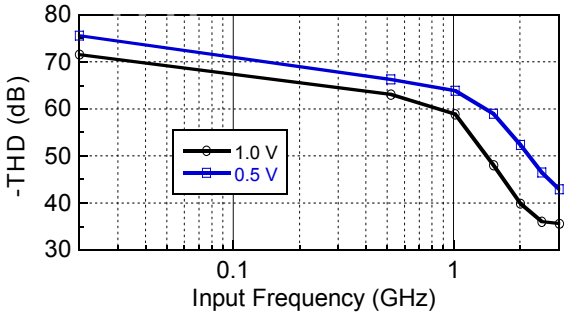


Figure 8. THD vs. input frequency for full and half scale input power (500 MS/s)

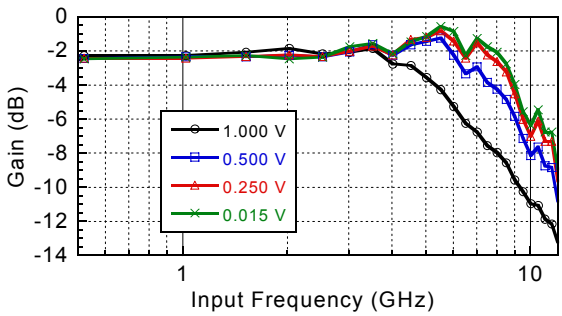


Figure 9. Gain vs. input frequency for various input power levels (500 MS/s)

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Package Information

The package is a 24-lead metallized ceramic-base glass-sidewall Quad Flat-Pack. The leads are trimmed to 0.150 inch (3.81 mm) length. The thermal impedance (junction to base) is approximately 15 °C/W. The lid is sealed with epoxy.

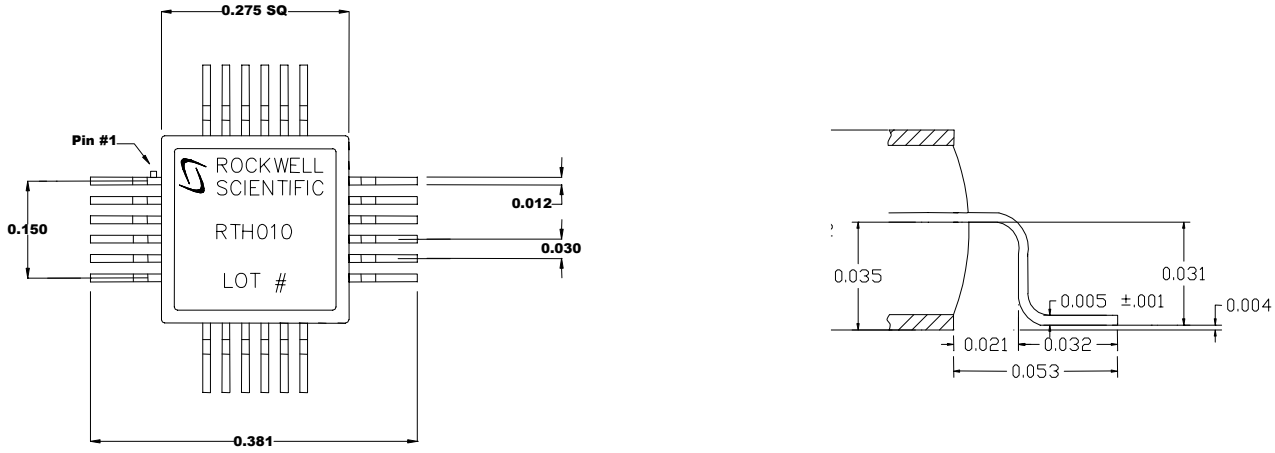


Figure 10. RTH010 package outline. Dimensions shown in inches, tolerance ±0.002 inch

Ordering Information

PART NUMBER	PACKAGE TYPE	TEMPERATURE RANGE
RTH010QFP	24-Lead Ceramic Quad FP	-30 to +70 °C
RTH010DIE	Die[14]	0 to +100 °C

[14] Die performance is as good as or better than that of the packaged part. On-wafer measurements show large/small-signal bandwidths, BW/bw, and THD at 5-GHz 0.5-Vpp equal to 6/9.3 GHz and –42 dB vs. 6/9 GHz and –32 dB for the packaged part.

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