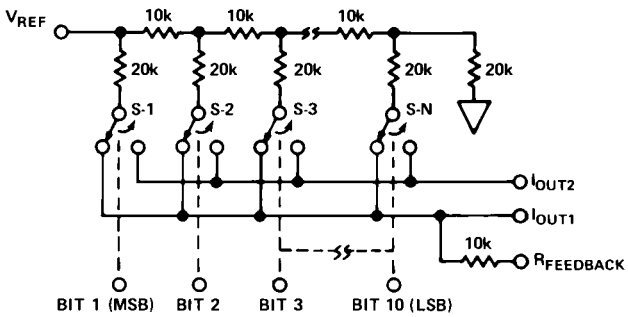
CMOS Low Cost 10-Bit Multiplying DAC

AD7533

FEATURES
Lowest Cost 10-Bit DAC
Low Cost AD7520 Replacement
Linearity: 1/2, 1 or 2LSB
Low Power Dissipation
Full Four-Quadrant Multiplying DAC
CMOS/TTL Direct Interface
Latch Free (Protection Schottky not Required)
End-Point Linearity

APPLICATIONS
Digitally Controlled Attenuators
Programmable Gain Amplifiers
Function Generation
Linear Automatic Gain Control

Functional Block Diagram



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

Logic: A switch is closed to I_{OUT1} for its digital input in a "HIGH" state.

ORDERING GUIDE[1]

Model[2]	Temperature Range	Nonlinearity (% FSR max)	Package Option[3]
AD7533JN	−40°C to +85°C	±0.2	N-16
AD7533KN	−40°C to +85°C	±0.1	N-16
AD7533LN	−40°C to +85°C	±0.05	N-16
AD7533JP	−40°C to +85°C	±0.2	P-20A
AD7533KP	−40°C to +85°C	±0.1	P-20A
AD7533LP	−40°C to +85°C	±0.05	P-20A
AD7533JR	−40°C to +85°C	±0.2	R-16
AD7533KR	−40°C to +85°C	±0.1	R-16
AD7533LR	−40°C to +85°C	±0.05	R-16
AD7533AQ	−40°C to +85°C	±0.2	Q-16
AD7533BQ	−40°C to +85°C	±0.1	Q-16
AD7533CQ	−40°C to +85°C	±0.05	Q-16
AD7533SQ	−55°C to +125°C	±0.2	Q-16
AD7533TQ	−55°C to +125°C	±0.1	Q-16
AD7533UQ	−55°C to +125°C	±0.05	Q-16
AD7533SE	−55°C to +125°C	±0.2	E-20A
AD7533TE	−55°C to +125°C	±0.1	E-20A
AD7533UE	−55°C to +125°C	±0.05	E-20A

NOTES
[1]Analog Devices reserves the right to ship ceramic (package outline D-16) packages in lieu of cerdip (package outline Q-16) packages.
[2]To order MIL-STD-883, Class B processed parts, add /883B to part number. Contact your local sales office for military data sheet.
[3]E = Leadless Ceramic Chip Carrier; N = Plastic DIP; P = Plastic Leaded Chip Carrier; Q = Cerdip; R = SOIC.

REV. A

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Tel: 617/329-4700 **Twx: 710/394-6577**
Telex: 174059 **Cables: ANALOG NORWOODMASS**

AD7533—SPECIFICATIONS (V_{DD} = +15V, V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Relative Accuracy[1]			
AD7533JN, AD, SD, AQ, SQ	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD, BQ, TQ	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD, CQ, UQ	±0.05% FSR max	±0.05% FSR max	
Gain Error[2,3]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[4]			
$\Delta Gain/\Delta V_{DD}$	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1}	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2}	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[4]	800ns[5]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[5]	±0.1% FSR max[5]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sine wave.
REFERENCE INPUT			
Input Resistance (Pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[6]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1}	100pF max[5]	100pF max[5]	Digital Inputs = V_{INH}
C_{OUT2}	35pF max[5]	35pF max[5]	
C_{OUT1}	35pF max[5]	35pF max[5]	Digital Inputs = V_{INL}
C_{OUT2}	100pF max[5]	100pF max[5]	
DIGITAL INPUTS			
Input High Voltage			
V_{INH}	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	8pF max[5]	8pF max[5]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[5]	+5V to +16V	+5V to +16V	Functionality with Degraded Performance
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}

NOTES
[1]"FSR" is Full-Scale Range.
[2]Full Scale (FS) = (V_{REF})
[3]Max gain change from T_A = +25°C to T_{min} or T_{max} is ±0.1% FSR.
[4]AC parameter, sample tested to ensure specification compliance.
[5]Guaranteed, not tested.
[6]Absolute temperature coefficient is approximately −300ppm/°C.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

V_{DD} to GND	−0.3V, +17V
R_{FB} to GND	±25V
V_{REF} to GND	±25V
Digital Input Voltage Range	−0.3V to V_{DD} +0.3V
OUT 1, OUT 2 to GND	−0.3V to V_{DD}
Power Dissipation (Any Package)	
To +75°C	450mW
Derates above +75°C by	6mW/°C
Operating Temperature Range	
Plastic (JN, KN, LN versions)	0 to +70°C
Hermetic (AD, BD, CD, AQ, BQ, CQ versions)	−25°C to +85°C
Hermetic (SD, TD, UD, SQ, TQ, UQ versions)	−55°C to +125°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10sec)	+300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION:
ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The foam should be discharged to the destination socket before devices are removed.



TERMINOLOGY

RELATIVE ACCURACY: Relative accuracy or end-point nonlinearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for ideal zero and full scale and is expressed in % of full-scale range or (sub) multiples of 1LSB.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution fo $[2^{-(n-1)}]$ $(V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2LSB for a given digital input stimulus, i.e., 0 to Full Scale.

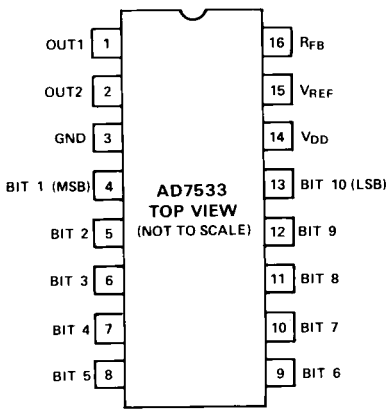
GAIN ERROR: Gain error is a measure of the output error between an ideal DAC and the actual device output. It is measured with all 1s in the DAC after offset error has been adjusted out and is expressed in Least Significant Bits. Gain error is adjustble to zero with an external potentiometer.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

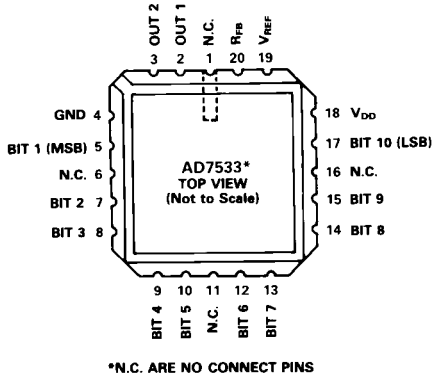
OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

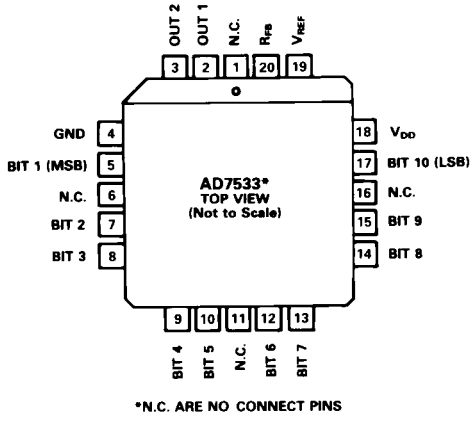
PIN CONFIGURATIONS



DIP



LCCC



PLCC

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

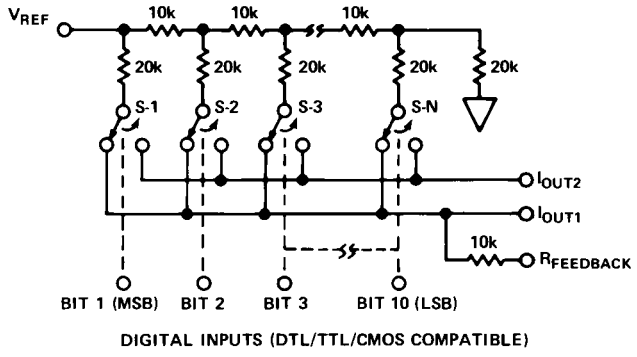


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20Ω, switch 2 for 40Ω, and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

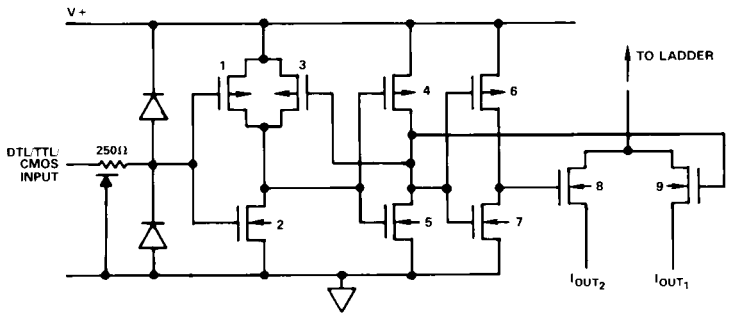


Figure 2. CMOS Switch

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 100pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 35pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

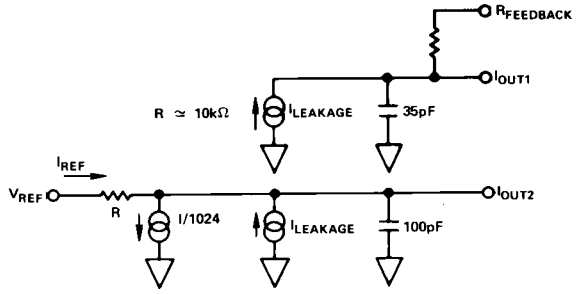


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

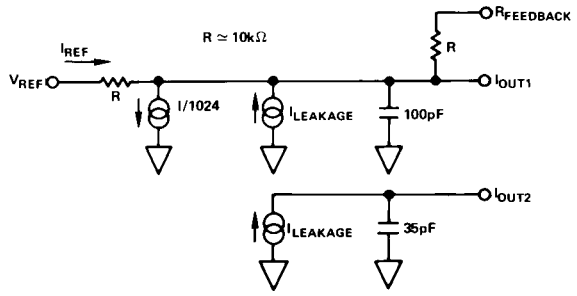


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 5)
1 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1023}{1024}\right)$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{513}{1024}\right)$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{1024}\right)=\frac{V_{REF}}{2}$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{511}{1024}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{1}{1024}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{0}{1024}\right)=0$

NOTE:
1. Nominal LSB magnitude for the circuit of Figure 5 is given by $LSB = V_{REF}\left(\frac{1}{1024}\right)$

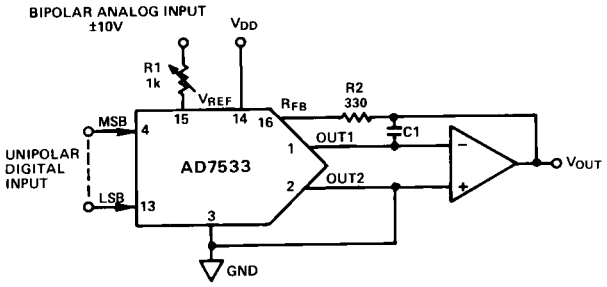
Table I. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT (V_{OUT} as shown in Figure 6)
1 1 1 1 1 1 1 1 1 1	$+V_{REF}\left(\frac{511}{512}\right)$
1 0 0 0 0 0 0 0 0 1	$+V_{REF}\left(\frac{1}{512}\right)$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$-V_{REF}\left(\frac{1}{512}\right)$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}\left(\frac{511}{512}\right)$
0 0 0 0 0 0 0 0 0 0	$-V_{REF}\left(\frac{512}{512}\right)$

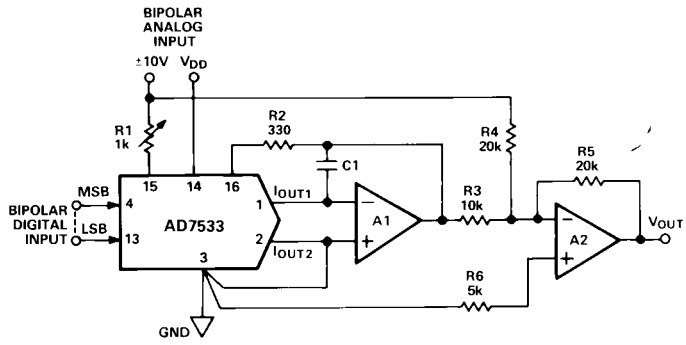
NOTE
1. Nominal LSB magnitude for the circuit of Figure 6 is given by $LSB = V_{REF}\left(\frac{1}{512}\right)$

Table II. Bipolar (Offset Binary) Code Table



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

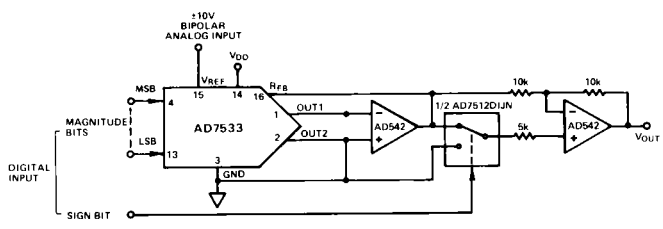


NOTES
1. R3, R4 AND R5 SELECTED FOR MATCHING AND TRACKING.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. C1 PHASE COMPENSATION (5-15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.

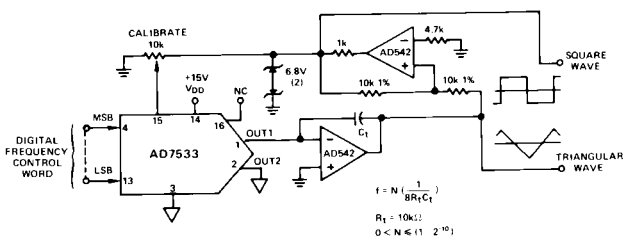
Figure 6. Bipolar Operation (4-Quadrant Multiplication)

APPLICATIONS

10-BIT AND SIGN MULTIPLYING DAC

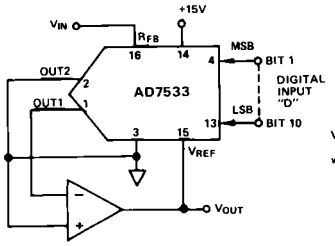


PROGRAMMABLE FUNCTION GENERATOR



APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



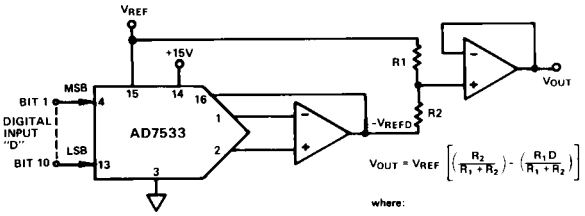
$$V_{OUT} = \frac{-V_{IN}}{D}$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$0 < D \leq \frac{1023}{1024}$$

MODIFIED SCALE FACTOR AND OFFSET



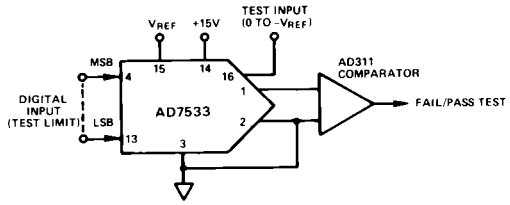
$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1+R_2}\right) - \left(\frac{R_1 D}{R_1+R_2}\right)\right]$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$\left(0 \leq D \leq \frac{1023}{1024}\right)$$

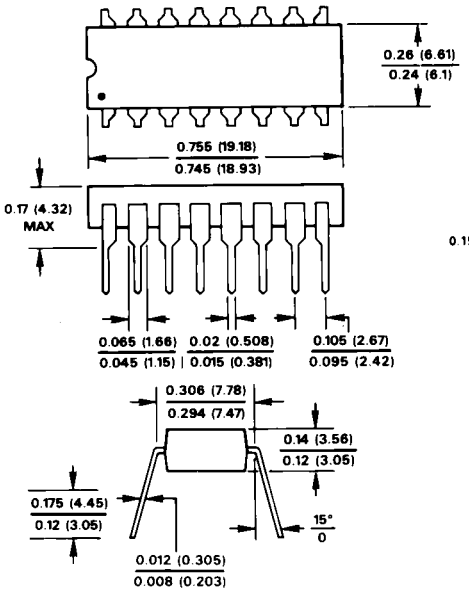
DIGITALLY PROGRAMMABLE LIMIT DETECTOR



OUTLINE DIMENSIONS

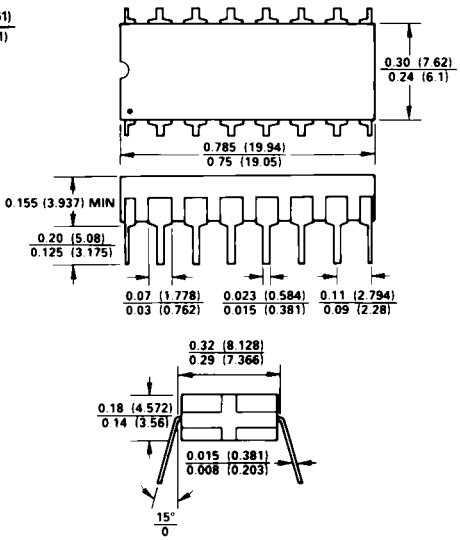
Dimensions shown in inches and (mm).

16-PIN PLASTIC DIP (SUFFIX N)



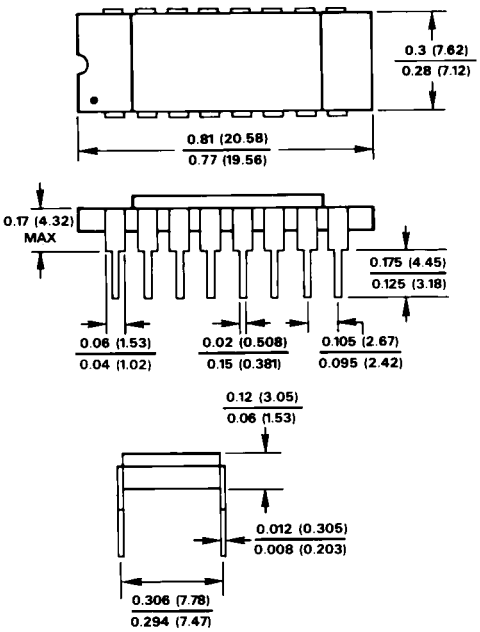
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16-PIN CERDIP (SUFFIX Q)



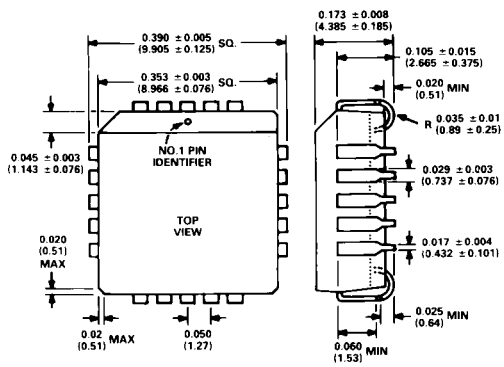
NOTES
LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER OR TIN-PLATED KOVAR OR ALLOY 42

16-PIN CERAMIC DIP (SUFFIX D)

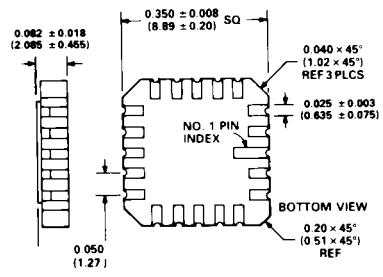


LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS WILL BE EITHER GOLD OR TIN PLATED
IN ACCORDANCE WITH MIL-M38510 REQUIREMENTS

20-TERMINAL PLASTIC LEADED CHIP CARRIER (SUFFIX P)



20-TERMINAL LEADLESS CHIP CARRIER (SUFFIX E)



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