HAMAMATSU

InGaAs linear image sensors

G9211 to G9214 series
G9205 to G9208 series

Near infrared image sensors (0.9 to 1.67 µm / 2.55 µm)

The G9211 to G9214/G9205 to G9208 series InGaAs linear image sensors are specifically designed for near infrared multichannel spectrophotometry. These linear image sensors consist of an InGaAs photodiode array, a charge amplifier array, an offset compensation circuit, a shift register and a timing generator formed on a CMOS chip. The charge amplifier array is made up of CMOS transistors connected to each pixel of the InGaAs photodiode array. Signals from each pixel are read out in charge integration mode to achieve high sensitivity and stable operation in the near infrared spectral range. The package is hermetically sealed for high reliability.
Signal processing circuits on the CMOS chip can be selected from two conversion efficiencies (CE) by external voltage. The image sensor operates over a wide dynamic range when CE=16 nV/e^- and delivers high gain when CE=320 nV/e^-.

Features

- **Wide dynamic range**
- **Low noise and low dark current**
- **Two selectable conversion efficiencies**
- **Anti-saturation circuit**
- **CDS circuit** *1
- **Offset compensation circuit**
- **Simple operation (by built-in timing generator)** *2
- **High resolution: 25 µm pitch (512 ch)**
- **Low cross-talk**
- **256 ch: 1 video line**
  512 ch: 2 video lines

Applications

- **Near infrared multichannel spectrophotometry**
- **Radiation thermometry**
- **Non-destructive inspection**

Related products

- **InGaAs multichannel detector head C8061-01, C8062-01**
- **Multichannel detector head controller C7557**

*1: A major source of noise in charge amplifiers is the reset noise generated when the integration capacitance is reset. A CDS (correlated double sampling) circuit greatly reduces this reset noise by holding the signal immediately after reset to find the noise differential.

*2: Different signal timings must be properly set in order to operate a shift register. In conventional image sensor operation, external PLDs (programmable logic device) are used to input the required timing signals. However, the G9211 to G9214/G9205 to G9208 series image sensors internally generate all timing signals on the CMOS chip just by supplying CLK and RESET pulses. This makes it simple to set the timings.

Selection guide

Type No.	Cooling	Number of pixels	Pixel pitch (µm)	Pixel size [µm (H) × µm (V)]	Spectral response range (µm)	Defective pixel
G9211-256S	One-stage TE-cooled	256	50	50 × 250	0.9 to 1.67 (-10 °C)	1 % Max. *3
G9212-512S		512	25	25 × 250		
G9213-256S		256	50	50 × 500		
G9214-512S		512	25	25 × 500		
G9205-256W	Two-stage TE-cooled	256	50	50 × 250	0.9 to 1.85 (-20 °C)	5 % Max.
G9206-256W					0.9 to 2.05 (-20 °C)	
G9207-256W					0.9 to 2.25 (-20 °C)	
G9208-256W					0.9 to 2.55 (-20 °C)	

*3: If your application requires sensors with no defective pixels, please select G9201 series.

Absolute maximum ratings

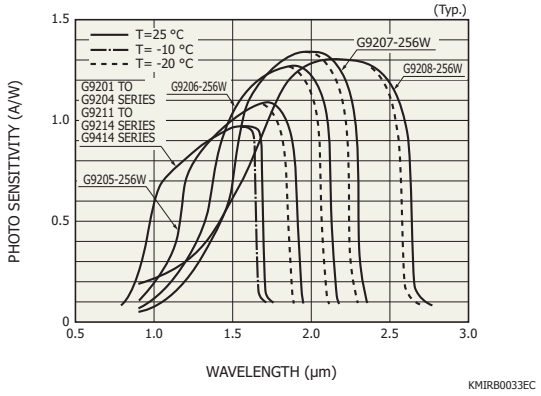
Parameter	Symbol	Value	Unit
Clock pulse voltage	Vϕ	5.5	V
Operating temperature *4	Topr	-40 to +70	°C
Storage temperature *4	Tstg	-40 to +85	°C

*4: Non condensation

Electrical characteristics (Ta=25 °C, Vϕ=5 V)

Parameter		Symbol		Min.	Typ.	Max.	Unit
Supply voltage		Vdd		4.9	5.0	5.1	V
		Vref		-	1.26	-	
Supply current		I(Vdd)	256 ch	-	45	50	mA
			512 ch	-	90	100	
		I(Vref)		-	-	1	mA
Ground		Vss		-	0	-	V
Element bias		INP		3.5	4.5	4.6	V
Element bias current		I(INP)		-	-	1	mA
Clock frequency		f		0.1	-	4	MHz
Clock pulse voltage	High	Vϕ		Vϕ - 0.5	Vϕ	Vϕ + 0.5	V
	Low			0	0	0.4	V
Clock pulse rise time		trϕ		0	20	100	ns
Clock pulse fall time		tfϕ					
Clock pulse width		tpwϕ		100	-	-	ns
Reset pulse voltage	High	V(RES)		Vϕ - 0.5	Vϕ	Vϕ + 0.5	V
	Low			0	0	0.4	V
Reset pulse rise time		tr(RES)		0	20	100	ns
Reset pulse fall time		tf(RES)					
Reset pulse width		tpw(RES)		6000	-	-	ns
Video output voltage	High	VH		-	4.5	-	V
	Low	VL		0	1.26	-	
Video data rate		fv		-	f/8	-	Hz

Spectral response



Electrical and optical characteristics (G9211 to G9214 series: T=25 °C, G9205 to G9208 series: T=-20 °C)

Parameter	Symbol	G9211 to G9214 series			G9205 to G9208 series				Unit
		Min.	Typ.	Max.		Min.	Typ.	Max.	
Peak sensitivity wavelength	λp	-	1.55	-	G9205	-	1.75	-	μm
					G9206	-	1.95	-	
					G9207	-	2.05	-	
					G9208	-	2.3	-	
Saturation charge *5	Qsat	-	30	-		-	30	-	pC
RMS noise voltage (Readout noise)	N	-	180	300		-	180	300	μV rms
Photo response non-uniformity	PRNU	-	-	±5 *6		-	-	±10 *7	%

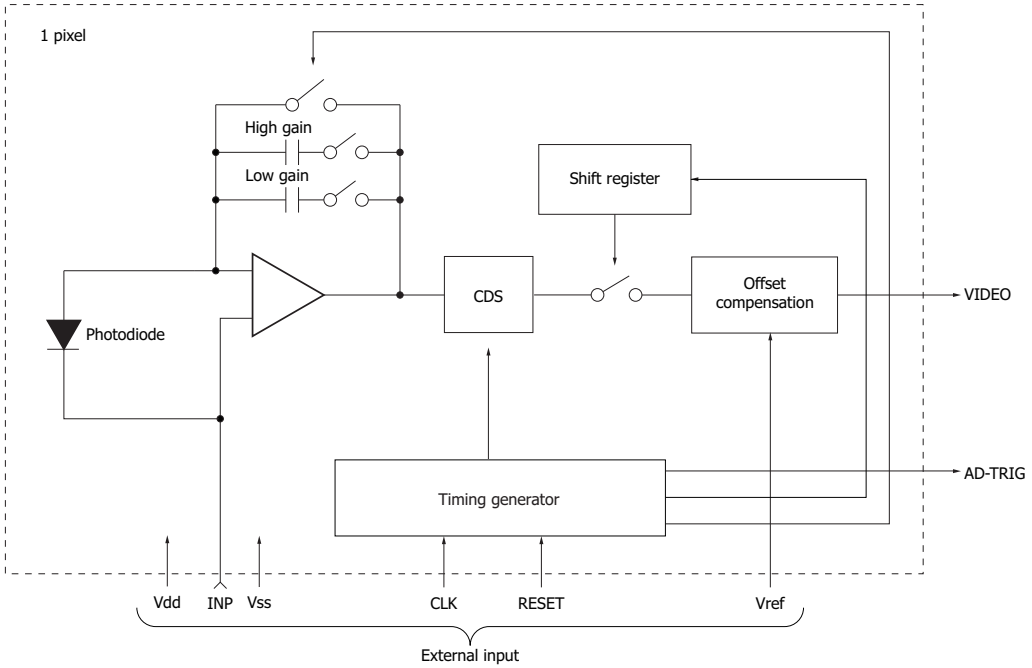
*5: Vϕ=5 V, CE=16 nV/e⁻
*6: 50 % of saturation, integration time: 10 ms, after dark output subtraction, excluding first and last pixels
*7: 50 % of saturation, integration time: 3 ms, after dark output subtraction, excluding first and last pixels

Dark current characteristics (T=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
G9211-256S	I_D	-	2	10	pA
G9212-512S		-	1	5	
G9213-256S		-	4	20	
G9214-512S		-	1	5	
G9205-256W *5		-	15	60	
G9206-256W *5		-	30	120	
G9207-256W *5		-	200	800	
G9208-256W *5		-	500	2000	

*5: T_D=-20 °C

Equivalent circuit



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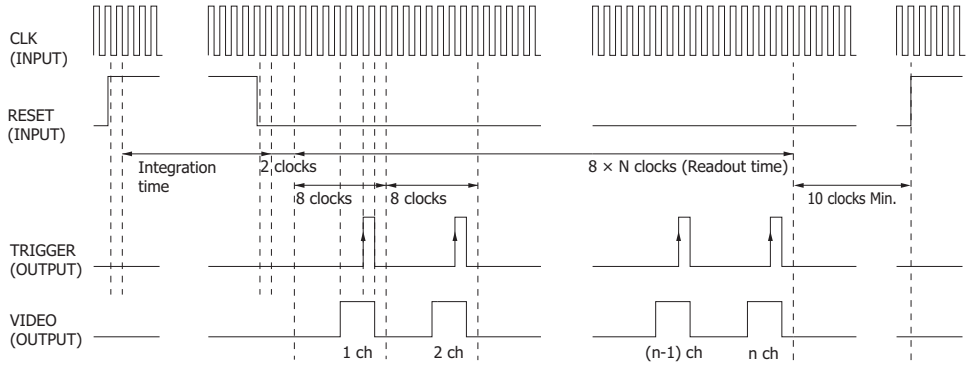
Timing chart



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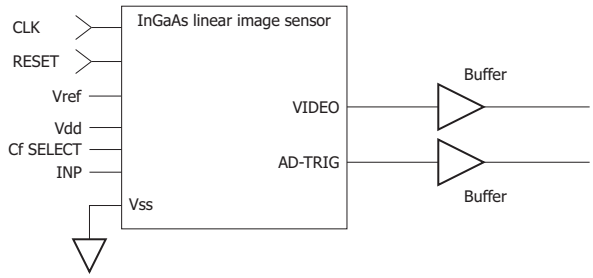
Connection example



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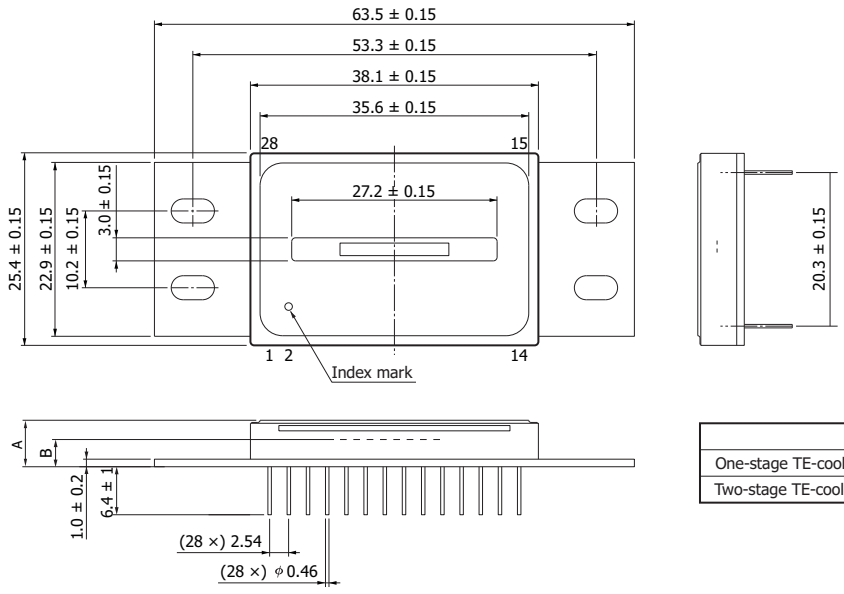
Dimensional outline (unit: mm)



	A	B
One-stage TE-cooled	6.15	3.6
Two-stage TE-cooled	7.25	4.5

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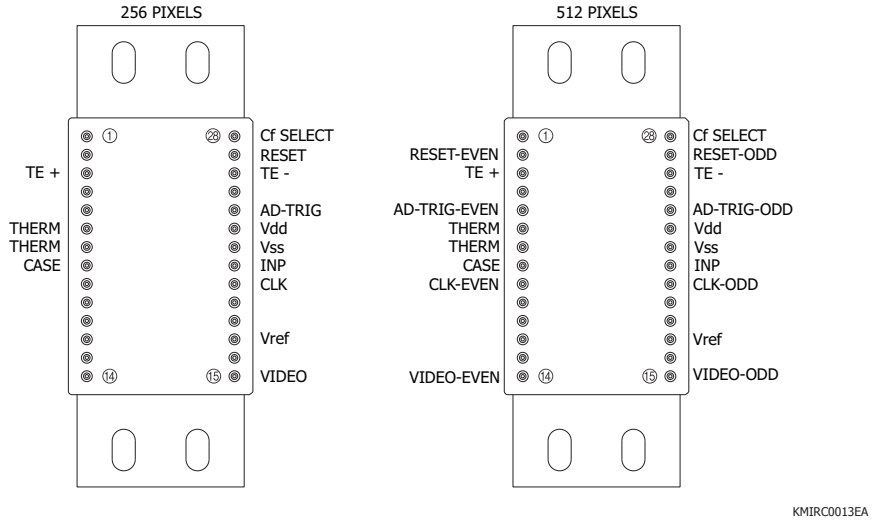
Pin connection (top view)



Terminal name	Input/Output	Function and recommended connection
CLK	Input (CMOS logic compatible)	Clock pulse for operating the CMOS shift register
RESET	Input (CMOS logic compatible)	Reset pulse for initializing the feedback capacitance in the charge amplifier formed in the CMOS chip. The width of the reset pulse is integration time.
Vdd	Input	Supply voltage for operating the signal processing circuit in the CMOS chip
Vss	Input	Ground for the signal processing circuit in the CMOS chip
INP	Input	Reset voltage for the charge amplifier array in the CMOS chip
Cf SELECT	Input	Voltage that determines the conversion efficiency in the CMOS chip. Low gain (CE=16 nV/e^-) at 0 V, and high gain (CE=320 nV/e^-) at 5 V.
CASE	-	This terminal is electrically connected to the package.
THERM	Output	Thermistor for monitoring temperature inside the package
TE+, TE-	Input	Power supply terminal for the thermoelectric cooler that cools the photodiode array. No connection for room temperature operation type.
AD-TRIG	Output	Digital signal for AD conversion; positive polarity
VIDEO	Output	Analog video signal; positive polarity
Vref	Input	Reset voltage for the offset compensation circuit in the CMOS chip

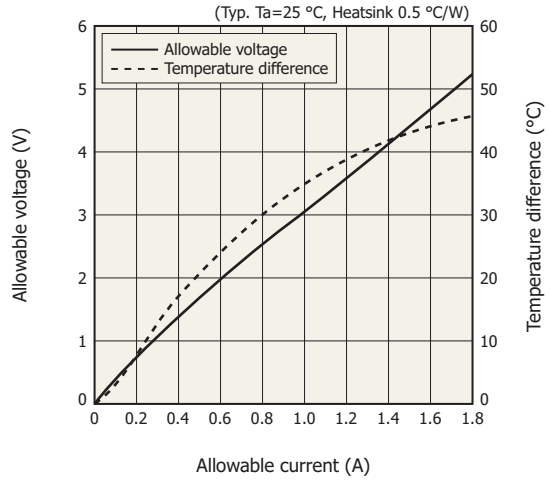
Specifications of TE-cooler (Ta=25 °C, Vdd=5 V, INP=4.5 V)

Parameter	Condition	Symbol	One-stage TE-cooler			Two-stage TE-cooler			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
TE-cooler allowable current		Ic Max.	-	-	1.8	-	-	2.8	A
TE-cooler allowable voltage		Vc Max.	-	-	5.0	-	-	4.0	V
Temperature difference *6	*7	ΔT	40	-	-	50	-	-	°C
Thermistor resistance		Rth	4.85	5.00	5.15	4.85	5.00	5.15	kΩ
Thermistor power dissipation		Pth	-	-	0.2	-	-	0.2	mW

*6: This is a temperature difference between the surface of active area and the heat radiating portion of package.
*7: One-stage thermoelectrically cooled type: Ic=1.4 A, two-stage thermoelectrically cooled type: Ic=2.6 A.

TE-cooler temperature characteristics

One-stgae TE-cooler



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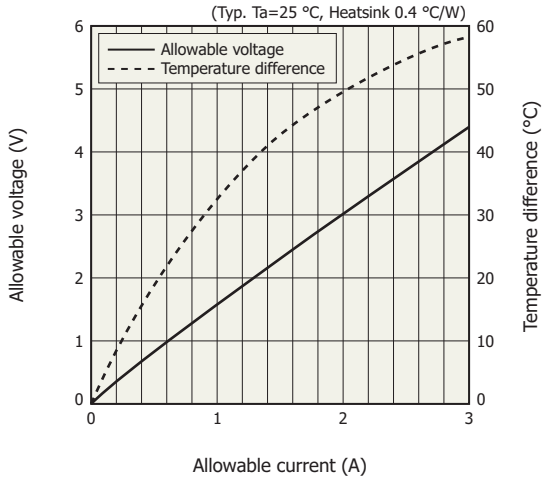
Two-stgae TE-cooler



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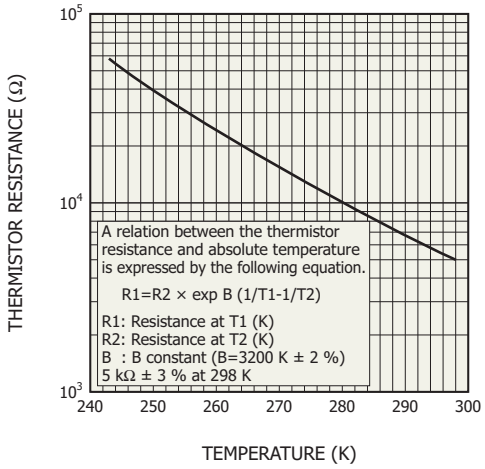
Thermistor temperature characteristic



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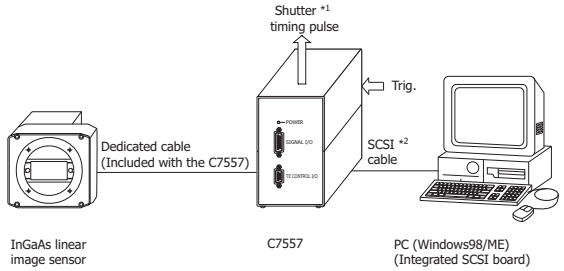
Connection of related products



*1: Shutter, etc. are not available.
*2: SCSI cable and SCSI board (card) are not supplied with the C7557.

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