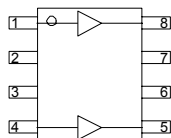




Product Description

Sirenza Microdevice's CGA-3318 is a high performance Silicon Germanium HBT MMIC Amplifier. Designed with SiGe process technology for excellent linearity at an exceptional price. A Darlington configuration is utilized for broadband performance. The heterojunction increases breakdown voltage and minimizes leakage current between junctions. The CGA-3318 contains two amplifiers for use in wideband Push-Pull CATV amplifiers requiring excellent second order performance. The second and third order non-linearities are greatly improved in the push pull configuration.

Amplifier Configuration



ELECTRICAL SPECIFICATIONS

Symbol	Parameter	Freq.(MHz)	Min.	Typ.	Max.	Units
G	Small Signal Gain *See 5-100 MHz Application Circuit, pg. 7.	*5		13.2		dB
		50		12.5		
		500		12.5		
		870	10.0	12.0		
OIP2	Output Second Order Intercept Point Tone Spacing = 1 MHz, Pout per tone = +6 dBm	50		69.0		dBm
		250		71.5		
		500	67.0	69.0		
OIP3	Output Third Order Intercept Point Tone Spacing = 1 MHz, Pout per tone = +6 dBm	50		36.5		dBm
		500		38.0		
		870	36.0	38.0		
P1dB	Output Power at 1dB Gain Compression	50		20.0		dBm
		500		21.0		
		870	18.6	20.6		
IRL	Input Return Loss	500		17.0		dB
		50-870	10			
ORL	Output Return Loss	500		12.0		dB
		50-870	10			
NF	Noise Figure Balun Insertion Loss Included	50		4.2		dB
		500		4.3		
		870		5.0	6.0	
CSO	Worst Case Over Band, 79 Ch., Flat, +34dBmV			70		dBc
CTB	Worst Case Over Band, 79 Ch., Flat, +34dBmV			68		dBc
XMOD	Worst Case Over Band, 79 Ch., Flat, +34dBmV			63		dBc
V_D	Device Operating Voltage		3.9	4.1	4.3	V
I_D	Device Operating Current		135	150	165	mA
$R_{TH(J-L)}$	Thermal Resistance (Junction to Lead)			50		°C/W

Test Conditions: $V_S = 8\text{ V}$ $R_{BIAS} = 51\text{ Ohms}$ $I_D = 150\text{ mA Typ. @ } T_L = 25^\circ\text{C}$ $Z_S = Z_L = 75\text{ Ohms}$ Push Pull Application Circuit

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CGA-3318

Dual CATV Broadband High Linearity SiGe HBT Amplifier



Product Features

- Excellent CSO/CTB/XMOD Performance at +34 dBmV Output Power per Tone
- Dual Devices in each SOIC-8 Package simplify Push-Pull configuration PC board layout
- 5 to 900 MHz operation

Applications

- CATV Head End Driver and Predriver Amplifier

Absolute Maximum Ratings

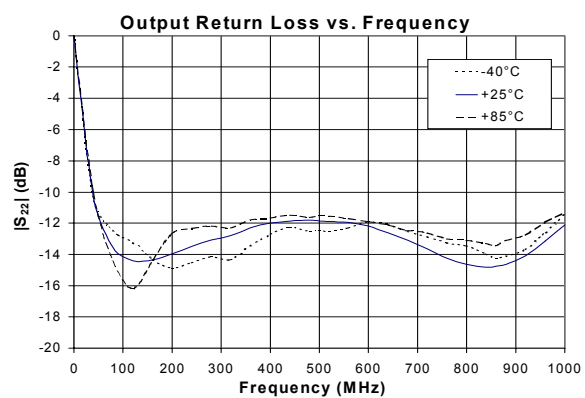
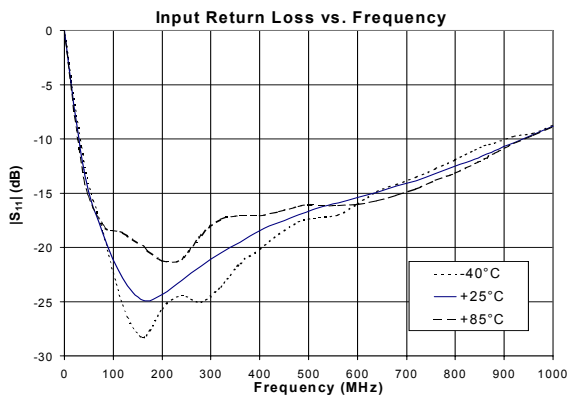
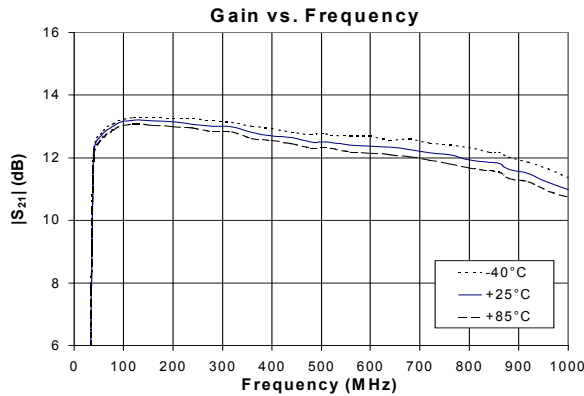
Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:

$$I_D V_D < (T_J - T_L) / R_{TH} j-I$$

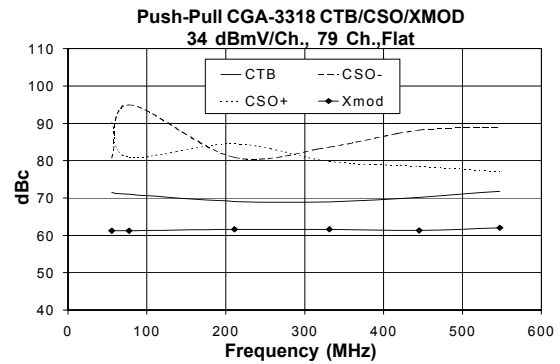
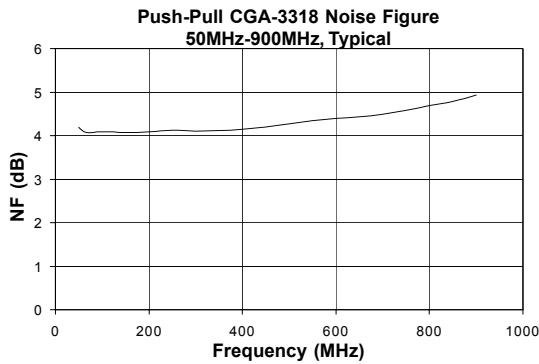
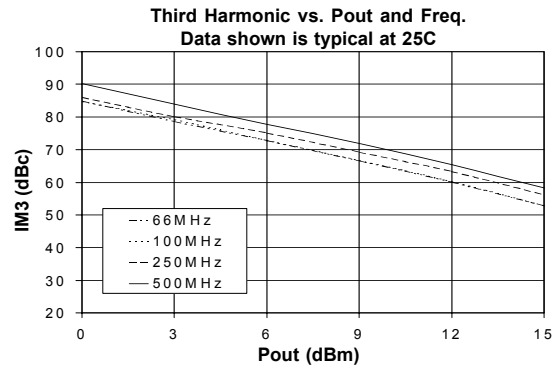
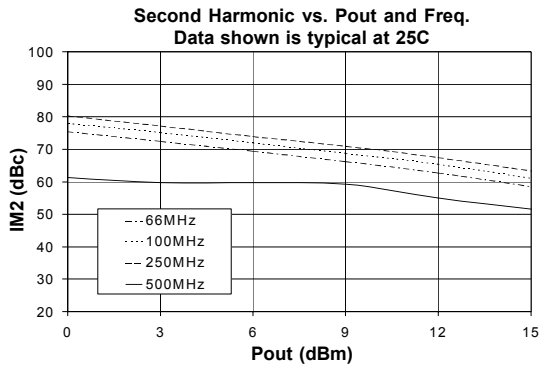
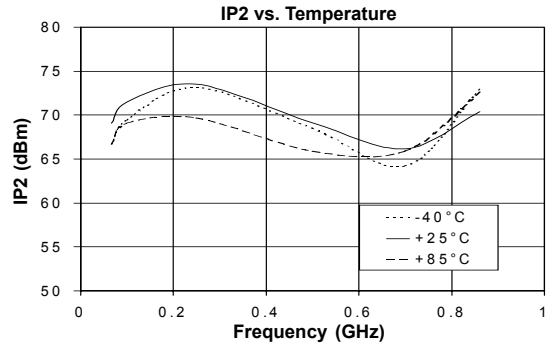
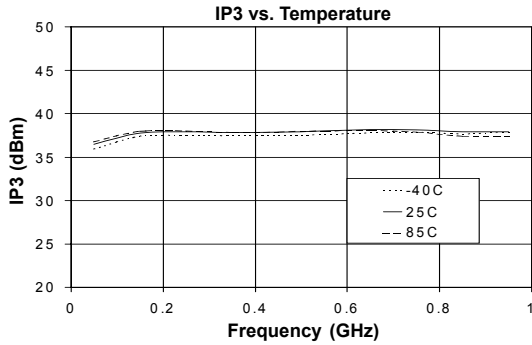
Parameter	Absolute Limit
Max. Device Current (I_D)	225 mA
Max. Device Voltage (V_D)	7 V
Max. RF Input Power	+18 dBm
Max. Junction Temp. (T_J)	+150°C
Operating Temp. Range (T_L)	-40°C to +85°C
Max. Storage Temp.	+150°C

Typical RF Performance: $V_S=8V$, $I_D=150mA$ @ $T_L=+25^\circ C$, $R_{BIAS}=51$ Ohms, Push-Pull Config.



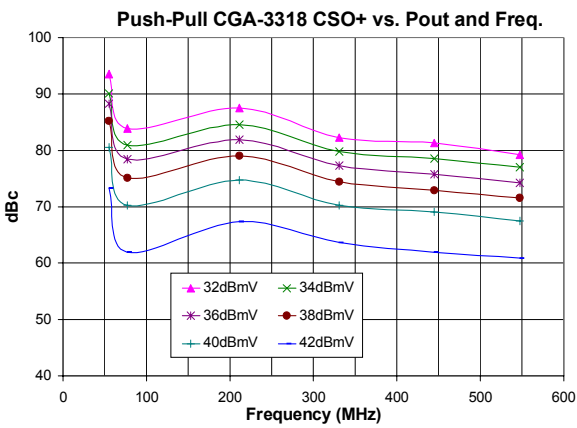
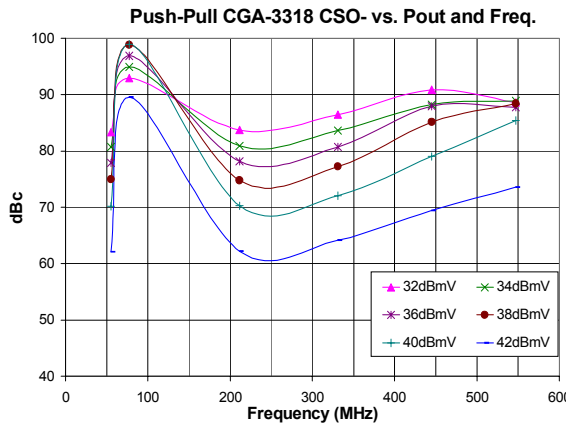
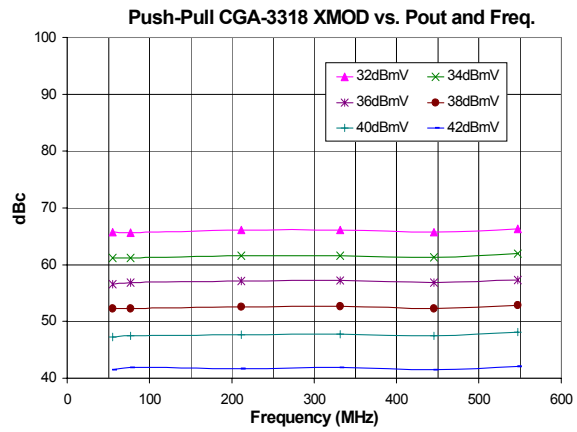
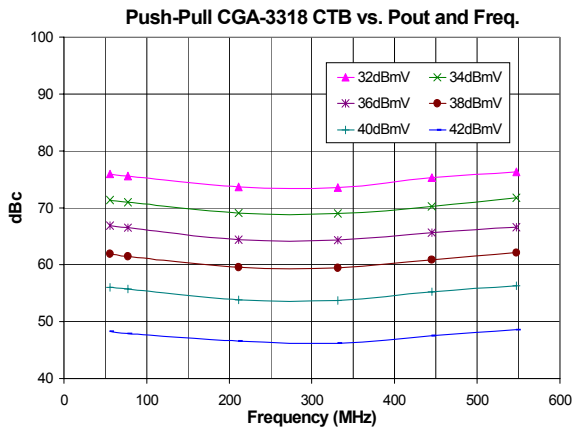
75 Ohm Push Pull S-parameters are available for download at www.sirenza.com

Typical RF Performance: $V_s=8V$, $I_D=150mA$ @ $T_L=+25^\circ C$, $R_{BIAS}=51$ Ohms, Push-Pull Config.



CSO/CTB/XMOD Performance:

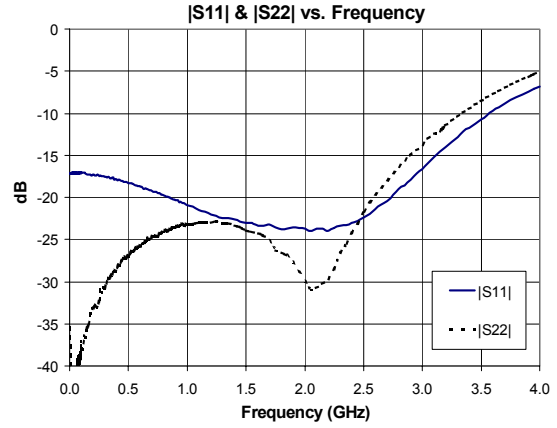
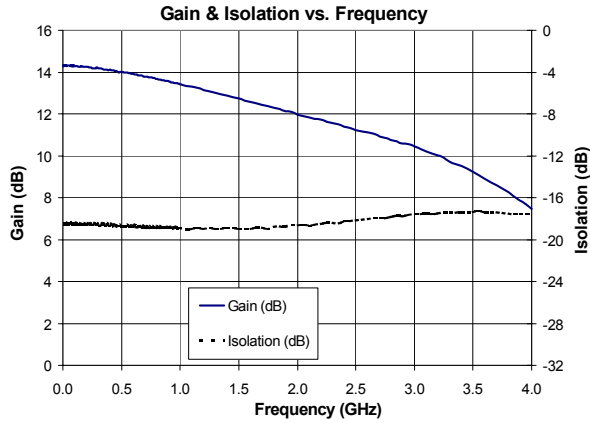
$V_S=8V$, $I_D=150mA$ @ $T_L=+25^\circ C$, $R_{BIAS}=51$ Ohms, Push-Pull Config, 79 Ch. Flat Analog, No Digital Channels.



Note: CSO measurements > 85 dBc can be limited by system noise.

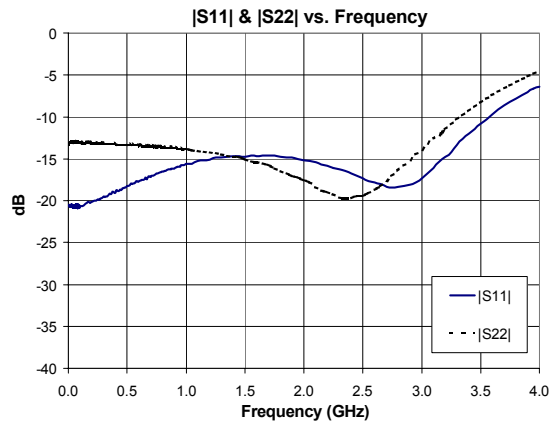
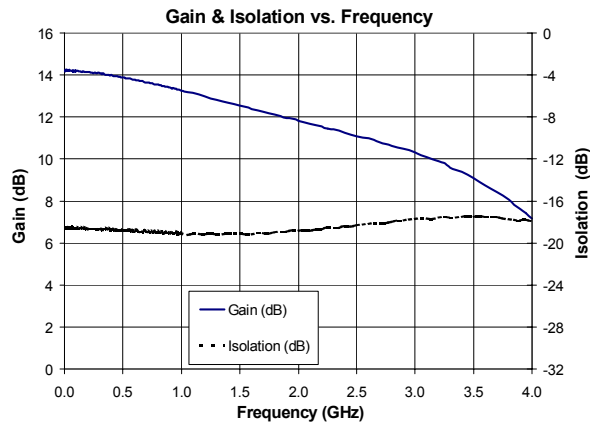
Typical RF Performance - Single Ended - 50 Ohm System

$V_s=8V$, $I_D=75mA$ (one amp biased), $T_L=+25^\circ C$, $R_{BIAS}=51$ Ohms



Typical RF Performance - Single Ended - 37.5 Ohm System

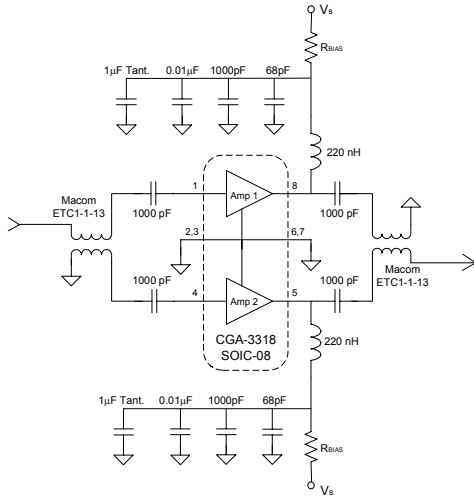
$V_s=8V$, $I_D=75mA$ (one amp biased), $T_L=+25^\circ C$, $R_{BIAS}=51$ Ohms



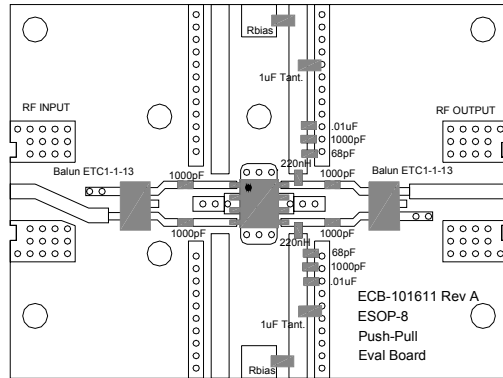
50 Ohm and 37.5 Ohm Single Ended S-parameter files are available for download at www.sirenza.com

Pin #	Function	Description	Device Pin Out
1	RF IN Device 1	RF input pin. This pin requires the use of an external DC blocking capacitor as shown in the schematic.	
2,3	Ground	Connection to ground. Use via holes for best performance to reduce lead inductance as close to ground leads as possible.	
4	RF IN Device 2	Same as pin 1	
5	RF OUT / Vcc Device 2	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of the bias network should be well bypassed.	
6,7	Ground	Same as pins 2 and 3	
8	RF OUT / Vcc Device 1	Same as pin 5	
EPAD	Ground	Exposed area on the bottom side of the package must be soldered to the ground plane of the board for optimum thermal and RF performance. Several vias should be located under the EPAD as shown in the recommended land pattern on page 5.	

Basic Application Schematic 50-870 MHz



Evaluation Board Layout 50-870 MHz



Recommended Bias Resistor Values for $I_D=150mA$				
Supply Voltage(V_s)	8V	9V	12V	15V
R_{BIAS}	51Ω	62Ω	100Ω	150Ω
R_{BIAS} Power Rating	1/2W	1/2W	1W	1W

$$R_{BIAS} = \frac{2(V_s - V_D)}{I_D}$$

Part Number Ordering Information

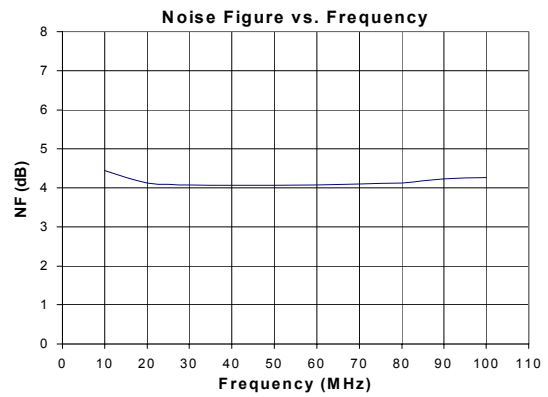
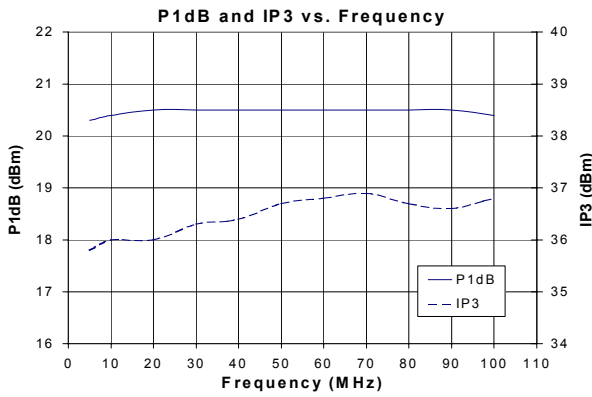
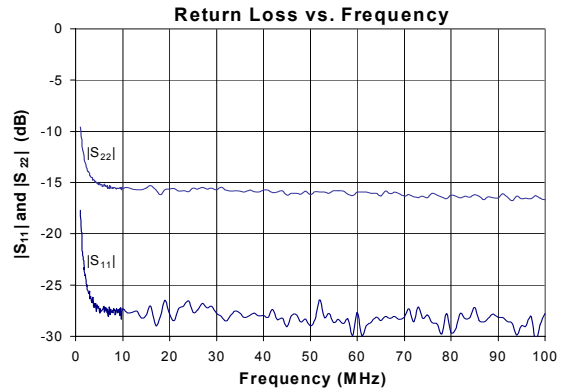
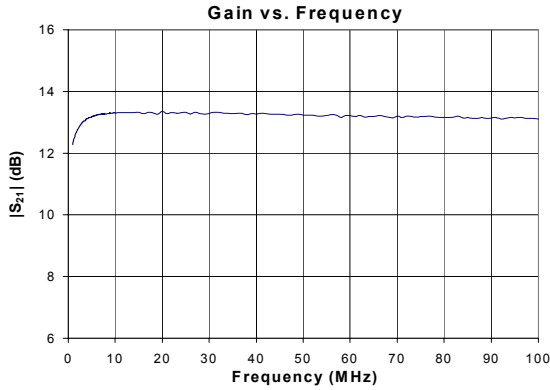
Part Number	Devices Per Reel	Reel Size
CGA-3318	500	7"



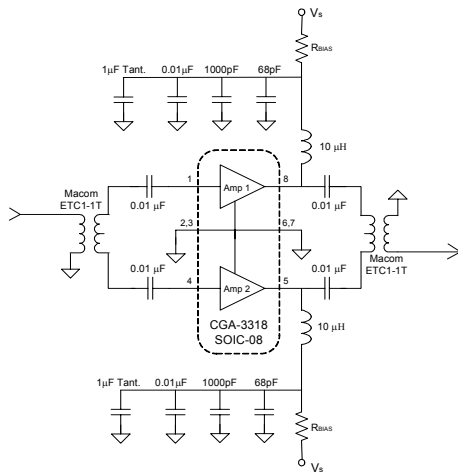
Caution: ESD sensitive

Appropriate precautions in handling, packaging and testing devices must be observed.

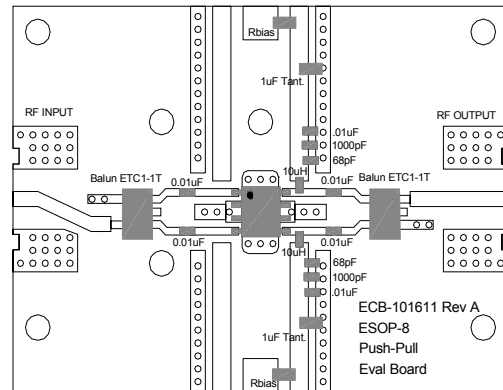
5 - 100 MHz Application Circuit: $V_s=8V$, $I_D=150mA$ @ $T_L=+25^\circ C$, Push-Pull Config.

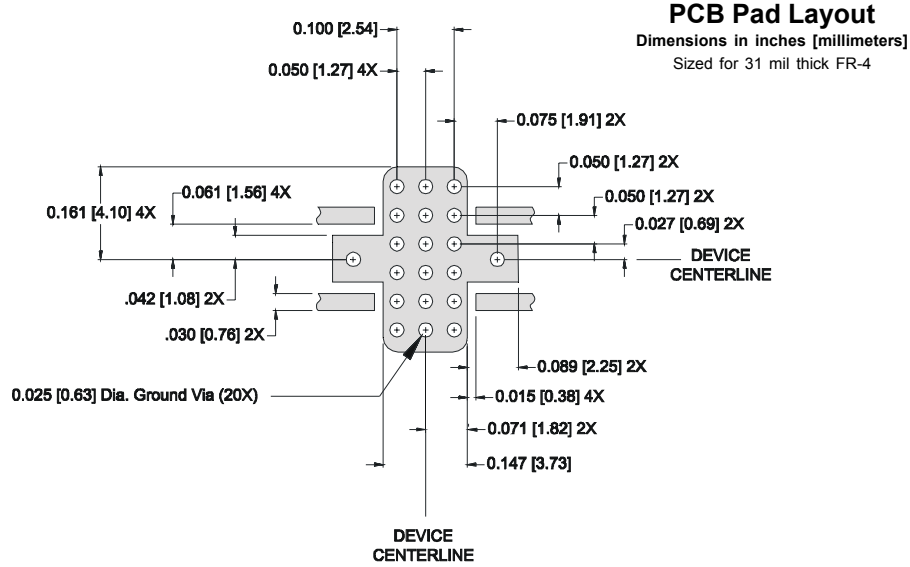


5-100 MHz Application Schematic



5-100 MHz Evaluation Board Layout





Nominal Package Dimensions & Package Marking

Dimensions in inches [millimeters]
Refer to package drawing posted at www.sirenza.com for tolerances.

