USB Power Delivery 3.0 Adaptive Source Charging Controller

FUSB3307

FUSB3307 is a highly integrated USB Power Delivery (PD) power source controller that can control a DC−DC port power regulator or the opto−coupler in the secondary side of an AC−DC adapter. It implements the Source finite state machines of USB Power Delivery 3.0 (PD 3.0) and Type−C™ which includes Programmable Power Supplies (PPS). In order to meet the PPS specification, FUSB3307 supports minimum 3.3 V and maximum 21 V output voltage control. It includes Constant Voltage (CV) and Constant Current Limit (CL) control blocks. The references are supported from internal D/A converters.

FUSB3307 supports various protections, Under Voltage Protection (UVP), Over Voltage Protection(OVP), Over Current Protection (OCP), CC1 and CC2 Over Voltage Protection (CC_OVP), VCONN Over Current Protection (VCONN_OCP), and internal and external Over Temperature protection (I_OTP and E_OTP). With a 10−bit A/D converter, output voltage, output current, IC internal temperature and external temperature via an NTC resistor can be monitored.

FUSB3307 is capable of controlling a single or back−to−back N−Channel MOSFETs as a load switch, which results in a lower cost and easier design.

Features

- PD 3.0 v2.0 and Type−C 2.0 Compliant
- Constant Voltage (CV) and Constant Current Limit (CL) Regulation
- Small Current Sensing Resistor (5 mΩ) for High Efficiency
- Gate Driver for N−Channel MOSFET as a Load Switch
- CC1/CC2 Pin Protection up to 26 V
- Selectable Resistor Divider or Battery Charging (BC1.2) Modes
- Built−in Output Capacitor Discharging Resistance
- Adaptive UVP, Adaptive OVP, I_OTP, E_OTP, CC_OVP and VCONN_OCP Fault Detection
- 14−pin SOIC and 20−pin QFN Packages Available

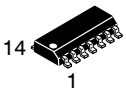
Applications

- Wall Chargers for Tablet PC's and Laptop Batteries
- AC−DC PD 3.0 Compliant Adapters
- DC−DC Car Chargers for Individual Port Power Control

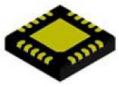
This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.

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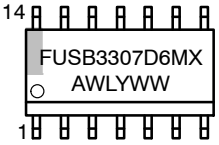


SOIC−14 NB
CASE 751A−03



QFNW20 4x4, 0.5P
CASE 484AT
(In Development)

GENERIC MARKING DIAGRAMS





FUSB3307D6MX = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN DESCRIPTION

See detailed pin description information on page 5 of this data sheet.

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

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APPLICATION DIAGRAM

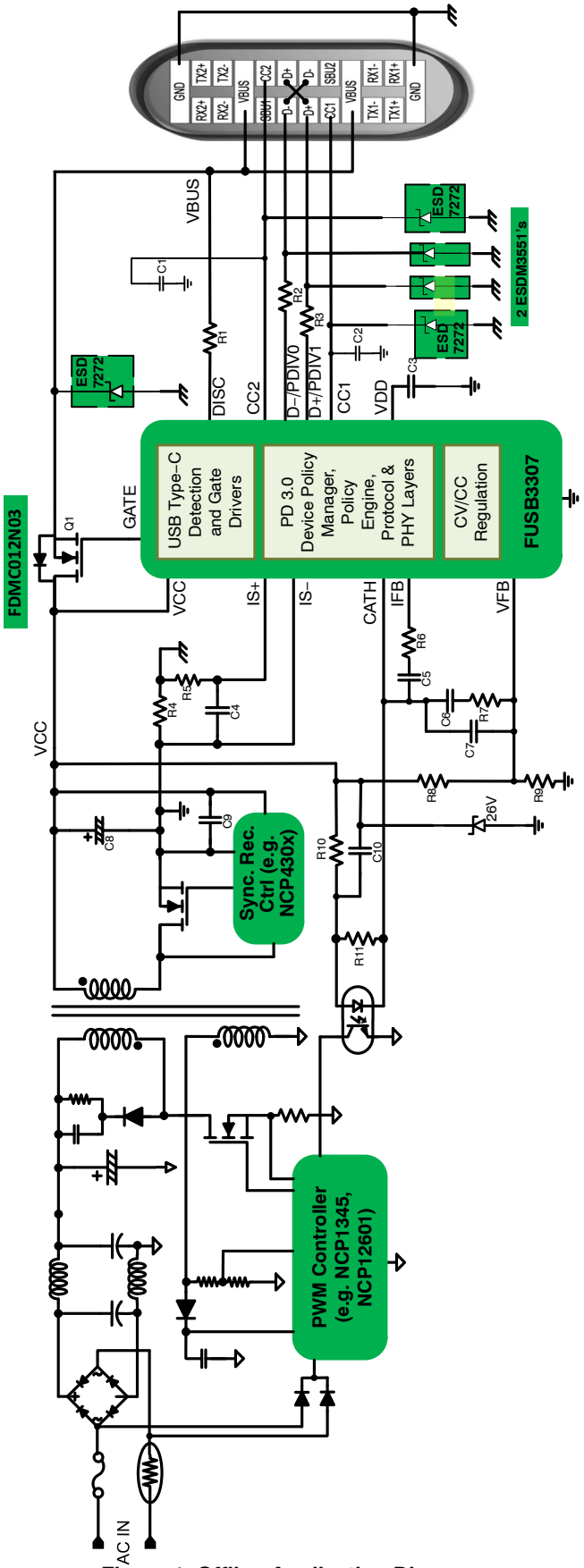


Figure 1. Offline Application Diagram

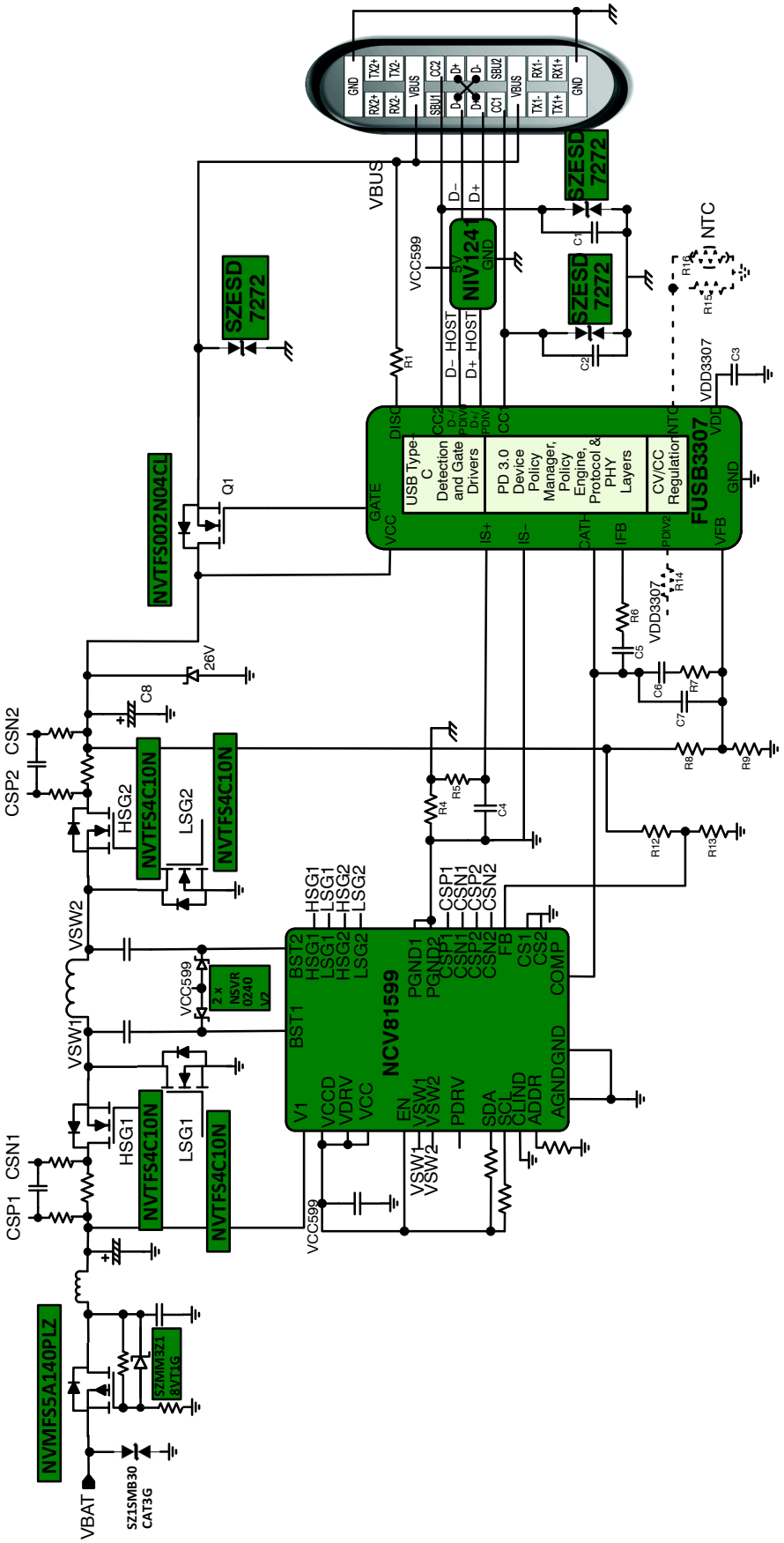


Figure 2. Automotive Application Diagram

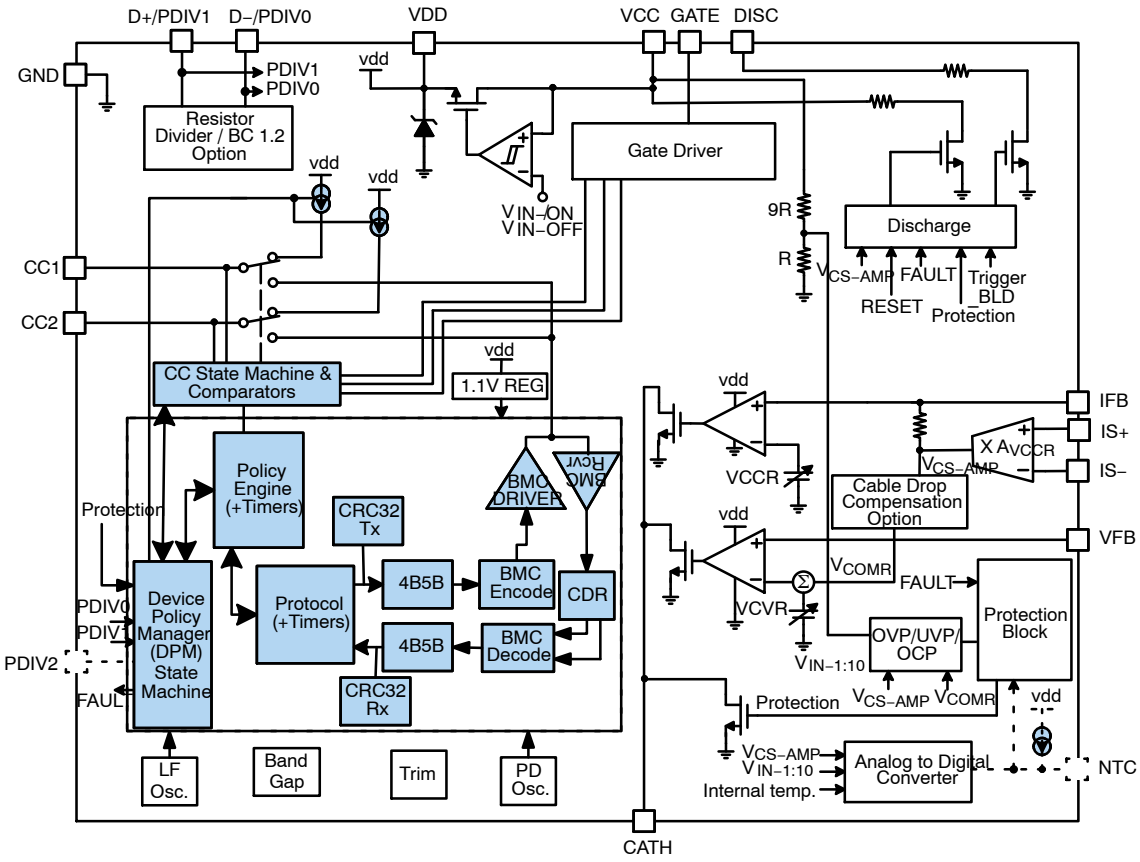


Figure 3. Block Diagram

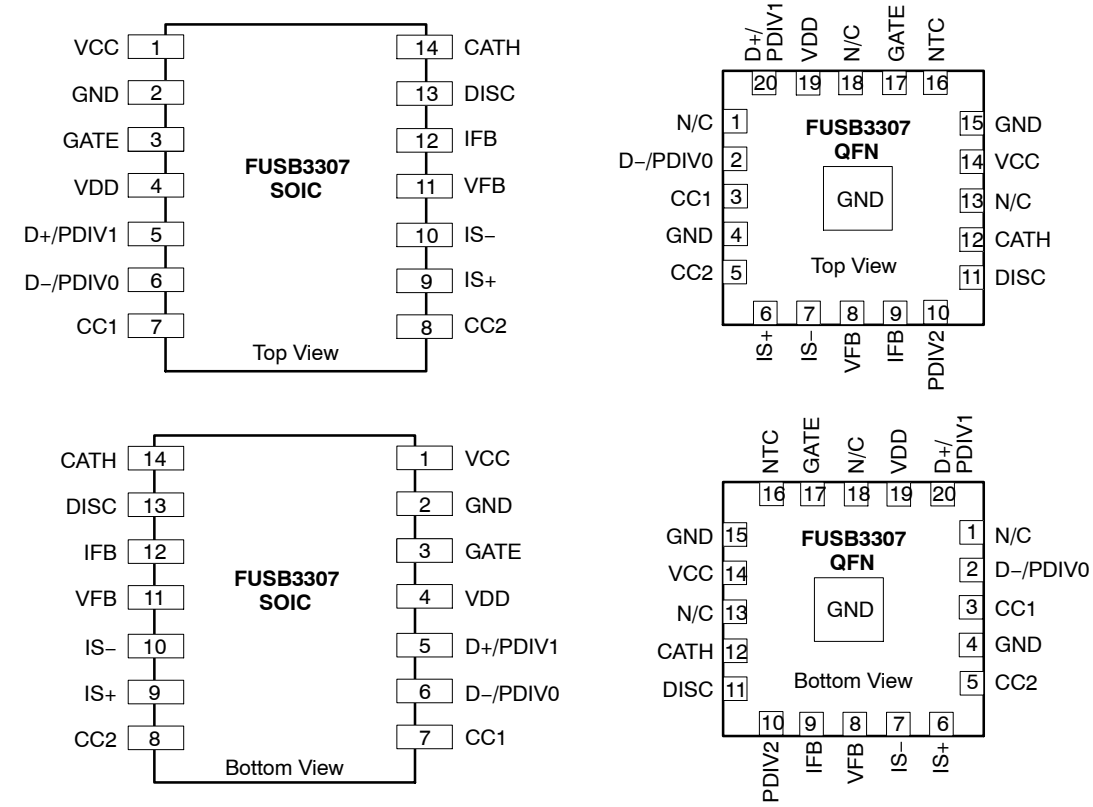


Figure 4. Pin Diagrams

PIN FUNCTION DESCRIPTION

SOIC Pin Number	QFN Pin Number	Pin Name	I/O Type	Description
1	14	VCC	Supply	Output voltage (Input voltage to the FUSB3307). This pin is tied to the output of the power source to monitor its output voltage and supply internal bias to the FUSB3307 via the VDD pin.
4	19	VDD	Supply	Internal supply voltage regulator output. This pin should be connected to an 1 μF external capacitor
2	4, 15, DAP	GND	Ground	Ground
14	12	CATH	Open Drain Output	Feedback to control the power supply. Typically an opto−coupler cathode on the secondary side is connected to this pin to provide feedback signal to the primary side PWM controller. Alternatively, this can be connected to the error amplifier output of a DC−DC regulator (often called the compensation pin) or with an inverting circuit to the DC−DC feedback (FB) pin.
11	8	VFB	Input	Output Voltage Sensing Signal. This pin is used for constant voltage (CV) regulation, and it is tied to the internal CV loop amplifier non−inverting input terminal. It is tied to the output voltage external 1:10 resistor divider and a compensation circuit
12	9	IFB	Input	Constant Current Amplifying Signal. The voltage level at this pin is the amplified current sense signal used for providing an external compensation circuit. Internally this pin is tied to the non−inverting input of the current loop error amplifier.
10	7	IS−	Input	Current sensing amplifier negative terminal. Connect this pin directly to the negative end of the current sense resistor with a short PCB trace
9	6	IS+	Input	Current sensing amplifier positive terminal. Connect this pin directly to the positive end of the current sense resistor with a short PCB trace
3	17	GATE	Output	Gate drive signal to drive the gate of an NFET load switch
13	11	DISC	Open Drain I/O	Discharge pin. This pin should be tied to a small (40 Ω) external resistor that is connected to VBUS after the load switch to discharge VBUS at the connector
7	3	CC1	I/O	Configuration Channel 1. This pin is used to detect USB Type−C devices and communicate over USB PD
8	5	CC2	I/O	Configuration Channel 2. This pin is used to detect USB Type−C devices and communicate over USB PD
5	20	D+/PDIV1	D+: I/O PDIV1: Input	Different functionality available with Trim option (see **Application Information** section and note at the bottom of Table 6 below): D+: Connected to D+ for BC1.2 or resistor divider mode PDIV1: Programmable pin to select different USB Power Delivery Power (PDP) values
6	2	D−/PDIV0	D−: I/O PDIV0: Input	Different functionality available upon request: D−: Connected to D− for BC1.2 or resistor divider mode PDIV0: Programmable pin to select different USB Power Delivery Power (PDP) values
N/A	10	PDIV2	Input	Programmable pin to select different USB Power Delivery Power (PDP) values
N/A	16	NTC	I/O	Pin connected to external NTC resistor to sense PCB or connector temperature

ORDERING INFORMATION

Part Number	Top Mark	Operating Temperature Range	Package	Packing Method
FUSB3307D6MX	FUSB3307D6MX	−40°C to 85°C	SOIC−14 NB (Pb−Free)	Tape and Reel
FUSB3307D6VMNWTWG (In Development)	3307 D6V	−40°C to 105°C	QFNW20 (Pb−Free)	Tape and Reel
FUSB3307D6MNWTWG (In Development)	3307 D6	−40°C to 85°C	QFNW20 (Pb−Free)	Tape and Reel
Other trim (see note at the bottom of Table 6) or package options	−	−	Please contact ON Semiconductor sales	−

Table 1. MAXIMUM RATINGS (Notes 1, 2)

Rating	Symbol	Value	Unit
VCC, CATH, DISC, CC1, CC2 Pin Voltage	V_{CC}	−0.3 to 26	V
GATE Pin Voltage	V_{GATE}	−0.3 to 30	V
IFB, VFB, IS+, IS−, NTC, D+/PDIV1, D−/PDIV0, PDIV2 Pin Voltage	$V_{I/O}$	−0.3 to 6	V
VDD Pin Voltage	V_{DD}	−0.3 to 6	V
Power Dissipation (T_A = 25°C)	P_D	1.5	W
Operating Junction Temperature	T_J	−40 to 150	°C
Storage Temperature Range	T_{STG}	−40 to 150	°C
Lead Temperature, (Soldering, 10 Seconds)	TL	260	°C
Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 (Note 3)	ESD_{HBM}	2	kV
Charged Device Model, JESD22−C101 (Note 3)	ESD_{CDM}	0.5	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. All voltage values, except differential voltages, are given with respect to the GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.
3. Meets JEDEC standards JS−001−2012 and JESD 22−C101.

Table 2. THERMAL CHARACTERISTICS (Note 4)

Rating		Symbol	Value	Unit
Thermal Characteristics,	Thermal Resistance, Junction−to−Air, SOIC14	$R_{\theta JA}$	75	°C/W
	Thermal Reference, Junction−to−Top, SOIC14	$R_{\theta JT}$	41.6	
	Thermal Resistance, Junction−to−Air, QFNW20	$R_{\theta JA}$	36.1	
	Thermal Reference, Junction−to−Top, QFNW20	$R_{\theta JT}$	2.3	

4. T_A=25°C unless otherwise specified with JEDEC 2S2P board with no thermal vias.

Table 3. RECOMMENDED OPERATING RANGES

Rating	Symbol	Min	Max	Unit
Input Voltage	V_{CC}	3.3 − 5%	21 + 5%	V
Output Current Through Load Switch	I_{OUT}		5	A
Adjustable Type−C Connector VBUS Output Voltage	VBUS	3.3 − 5%	21 + 5%	V
Ambient Temperature	T_A	−40	85 (Commercial) 105 (Automotive)	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 4. ELECTRICAL CHARACTERISTICS V_{CC} = 5 V, T_J = −40°C to 125°C unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VDD SECTION						
VDD Operating Voltage at VCC = 20 V	V_{CC} = 20 V, I_{VDD} = 0 mA	V_{DD}	4.75	5.2	5.5	V
VDD Source Current	V_{CC} = 3.3 V, V_{DD} = 2.9 V	I_{DD}	10			mA
VCC SECTION						
Continuous Operating Voltage (Note 5)		V_{CC-OP}			21 + 5%	V
Operating Supply Current at 5 V	V_{CC} = 5 V, sense resistor voltage difference (V_{CS}) = 25 mV, sense resistor (R_{CS}) = 5 mΩ	$I_{CC-OP-5V}$		2.4		mA
Operating Supply Current at 20 V	V_{CC} = 20 V, V_{CS} = 25 mV, Rcs = 5 mΩ	$I_{CC-OP-20V}$		3.1		mA
Turn−On Threshold Voltage	V_{CC} increasing	V_{CC-ON}	2.9	3.2	3.4	V
Turn−Off Threshold Voltage	V_{CC} decreasing after $V_{CC} \geq V_{CC-ON}$	V_{CC-OFF}	2.80	2.87	3.10	V
Turn−Off to Turn−On Hysteresis	V_{CC} decreasing after $V_{CC} \geq V_{CC-ON}$	V_{CC-OFF_HYS}	100	260	360	mV

Table 4. ELECTRICAL CHARACTERISTICS V_{CC} = 5 V, T_J = −40°C to 125°C unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
VCC SECTION						
Standby Operating Supply Current	V_{CC} = 5 V, V_{CS} = 0 mV ($I_{P-CC1-330}$ and $I_{P-CC2-330}$ not flowing since CC1 and CC2 are HIGH)	$I_{CC-STBY}$		0.85	1.1	mA
VCC−UVP SECTION						
Ratio V_{CC} Under−Voltage−Protection (UVP) to V_{CC}	V_{CS} = 0 mV	K_{CC-UVP}	60	65	70	%
UVP Debounce Time		t_{D-UVP}	45	60	75	ms
UVP Blanking Time during a Voltage Transition	Whenever a voltage change occurs from lower VBUS to a higher VBUS	$t_{BNK-UVP}$	160	200	240	ms
VCC−OVP SECTION						
Ratio V_{CC} Over−Voltage−Protection (OVP) to V_{CC}	V_{CS} = 0 mV	K_{CC-OVP}	116.0	121	127.0	%
V_{CC} Maximum Over−Voltage−Protection		$V_{CC-OVP-MAX}$	23	23.8	24.8	V
OVP Debounce Time		t_{D-OVP}	35	75	110	μs
OVP Blanking Time during a Voltage Transition (Note 5)	VBUS voltage transition step (V_{STEP}) ≤ 0.5 V, Final VBUS > 13 V	$t_{BNK-OVP1}$		7		ms
OVP Blanking Time during a Voltage Transition (Note 5)	V_{STEP} ≤ 0.5 V, Final VBUS < 13 V	$t_{BNK-OVP2}$		19		ms
OVP Blanking Time during a Voltage Transition (Note 5)	V_{STEP} > 0.5 V, Final VBUS > 13 V	$t_{BNK-OVP3}$		56		ms
OVP Blanking Time during a Voltage Transition (Note 5)	V_{STEP} > 0.5 V, Final VBUS < 13 V	$t_{BNK-OVP4}$		221		ms
CONSTANT CURRENT LIMIT SENSING SECTION (100% Constant Current)						
Current−Sense Amplifier Gain (Note 5)	R_{CS} = 5 mΩ	A_{V-CCR}		40		V/V
Current threshold on sensing resistor between IS+ and IS− at I_{OUT} = 1.00 A	Constant Current Limit mode and V_{CC} = 5 V, 20 V	I_{CS-1A}	0.85	1.00	1.15	A
Current threshold on sensing resistor between IS+ and IS− at I_{OUT} = 2.00 A	Constant Current Limit mode and V_{CC} = 5 V, 20 V	I_{CS-2A}	1.85	2.00	2.15	A
Current threshold on sensing resistor between IS+ and IS− at I_{OUT} = 3.00 A	Constant Current Limit mode and V_{CC} = 5 V, 20 V	I_{CS-3A}	2.85	3.00	3.15	A
Current threshold on sensing resistor between IS+ and IS− at I_{OUT} = 4.00 A	Constant Current Limit mode and V_{CC} = 5 V, 20 V	I_{CS-4A}	3.80	4.00	4.20	A
Current threshold on sensing resistor between IS+ and IS− at I_{OUT} = 5.00 A	Constant Current Limit mode and V_{CC} = 5 V, 20 V	I_{CS-5A}	4.75	5.00	5.25	A
Current threshold on sensing resistor between IS+ and IS− at ΔI_{OUT} = 50 mA	Constant Current Limit mode and V_{CC} = 5 V	$I_{CS-STEP}$	48	50	52	mA
OVER CURRENT PROTECTION SENSING SECTION						
Over Current Protection (OCP) threshold on sensing resistor between IS+ and IS−	Constant Voltage mode, PD Request Message = 3 A and V_{CC} = 5 V	I_{CS-3A}	3.42	3.60	3.78	A
Over Current Protection (OCP) threshold on sensing resistor between IS+ and IS−	Constant Voltage mode, PD Request Message = 5 A and V_{CC} = 5 V	I_{CS-5A}	5.7	6.0	6.3	A
OCP Debounce Time		$t_{OCP-DEB}$	50	60	70	ms
Current threshold on sensing resistor between IS+ and IS− for enabling discharge on DISC pin during a voltage transition	VBUS is decreasing	$I_{CS-EN-DSCG}$		330		mA
Debounce time for enabling discharge on DISC pin during a voltage transition		$t_{CS-EN-DSCG}$		0.6	1.0	ms
CONSTANT VOLTAGE SENSING SECTION						
VFB Reference Voltage at 3.3 V	V_{CC} = 3.3 V, V_{CS} = 0 V	$V_{CVR-3.3V}$	0.320	0.330	0.340	V

Table 4. ELECTRICAL CHARACTERISTICS V_{CC} = 5 V, T_J = −40°C to 125°C unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
CONSTANT VOLTAGE SENSING SECTION						
VFB Reference Voltage at 5.0 V (Power−on reset, default)	V_{CC} = 5.0 V, V_{CS} = 0 V	$V_{CVR-5.0V}$	0.485	0.500	0.515	V
VFB Reference Voltage at 9 V	V_{CC} = 9 V, V_{CS} = 0 V	V_{CVR-9V}	0.873	0.900	0.927	V
VFB Reference Voltage at 12 V	V_{CC} = 12 V, V_{CS} = 0 V	$V_{CVR-12V}$	1.164	1.200	1.236	V
VFB Reference Voltage at 15 V	V_{CC} = 15 V, V_{CS} = 0 V	$V_{CVR-15V}$	1.455	1.500	1.545	V
VFB Reference Voltage at 20 V	V_{CC} = 20 V, V_{CS} = 0 V	$V_{CVR-20V}$	1.940	2.000	2.060	V
VFB Reference Voltage of 20 mV step	ΔV_{CC} = 20 mV, V_{CS} = 0 V	$V_{CVR-STEP-20mV}$	1.940	2.000	2.060	mV
FEEDBACK SECTION						
CATH Pin Sink Current (Note 5)	Minimum guaranteed sink current expected from CATH pin	$I_{CATH-Sink}$	2			mA
DISCHARGE SECTION						
VBUS to GND leakage resistance when VBUS is not being sourced	GATE = 0 V	$R_{DISC-BUS}$	72.4	155		kΩ
VCC Pin Sink Current when discharging (Note 5)	Discharging current on VCC after a fault has triggered at VCC = 20 V	$I_{VCC\ -Sink}$	170			mA
DISC Pin Sink Current when discharging (Note 5)	Discharging current on DISC during a voltage transition at VCC = 20 V, $I_{OUT} < I_{CS-EN-DSCG}$	$I_{DISC\ -Sink}$	250			mA
Discharge Time (Note 5)	VBUS voltage transition step (V_{STEP}) ≤ 0.5 V, Final VBUS > 13 V, $I_{OUT} < I_{CS-EN-DSCG}$	t_{DISC1}		7		ms
Discharge Time (Note 5)	V_{STEP} ≤ 0.5 V, Final VBUS < 13 V, $I_{OUT} < I_{CS-EN-DSCG}$	t_{DISC2}		19		ms
Discharge Time (Note 5)	V_{STEP} > 0.5 V, Final VBUS > 13 V, $I_{OUT} < I_{CS-EN-DSCG}$	t_{DISC3}		56		ms
Discharge Time (Note 5)	V_{STEP} > 0.5 V, Final VBUS < 13 V, $I_{OUT} < I_{CS-EN-DSCG}$	t_{DISC4}		221		ms
OVER TEMPERATURE PROTECTION SECTION						
Current Source on NTC pin (Note 6)	Resistance to ground on NTC = 3.293 kΩ	I_{NTC}	55	60	65	μA
Debounce time for External Over Temperature Protection (E_OTP) (Note 6)		$t_{NTC-DEB}$		90		ms
Internal Die Warning Temperature Threshold (Note 5)		T_{I_WARN}		125		°C
Internal Die Over−Temperature Threshold (Note 5)		T_{I_OTP}		135		°C
PROTECTION RECOVERY SECTION						
VCC Voltage Release Threshold	UVP fault causing release when VCC < V_{LATCH}	V_{LATCH}	0.9			V
Duration for Disabling Load Switch When Fault Removed in Normal Mode (Note 5)	After fault OVP, UVP, OCP, E_OTP, I_OTP or CC_OVP has recovered	$t_{2S_AR_NM}$	1.8	2	2.2	sec
Duration for Disabling Load Switch When Fault Removed in Debug Test Mode		$t_{2S_SR_DM}$		100		ms
INPUTS SECTION						
PDIV2, PDIV1 and PDIV0 input LOW voltage	Input LOW	V_{IL}			0.4	V
PDIV2, PDIV1 and PDIV0 input HIGH voltage	Input HIGH	V_{IH}	V_{DD} − 0.4			V

Table 4. ELECTRICAL CHARACTERISTICS V_{CC} = 5 V, T_J = −40°C to 125°C unless otherwise specified.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
TYPE C SECTION						
330 μA Source Current on CC1 Pin	V_{CC} = 5 V, V_{CC1} = 0 V	$I_{P-CC1-330}$	304	330	356	μA
180 μA Source Current on CC1 Pin	Used for USB PD to signal that the Sink can communicate, V_{CC} = 5 V, V_{CC1} = 0 V	$I_{P-CC1-180}$	166	180	194	μA
330 μA Source Current on CC2 Pin	V_{CC} = 5 V, V_{CC2} = 0 V	$I_{P-CC2-330}$	304	330	356	μA
180 μA source current on CC2 Pin	Used for USB PD to signal that the Sink can communicate, V_{CC} = 5 V, V_{CC2} = 0 V	$I_{P-CC2-180}$	166	180	194	μA
Input Impedance on CC1 Pin	V_{CC} = 0 V, Sourcing 330 μA on CC1	$Z_{OPEN-CC1}$	126			kΩ
Input Impedance on CC2 Pin	V_{CC} = 0 V, Sourcing 330 μA on CC2	$Z_{OPEN-CC2}$	126			kΩ
Ra Impedance Detection Voltage Threshold on CC1 Pin	V_{CC} = 5 V, V_{CC2} = 5 V, Decreasing V_{CC1}	V_{RA-CC1}	0.75	0.80	0.85	V
Ra Impedance Detection Voltage Threshold on CC2 Pin	V_{CC} = 5 V, V_{CC1} = 5 V, Decreasing V_{CC2}	V_{RA-CC2}	0.75	0.80	0.85	V
Rd Impedance Detection Voltage Threshold on CC1 Pin	V_{CC} = 5 V, V_{CC2} = 5 V, Decreasing V_{CC1}	V_{RD-CC1}	2.45	2.60	2.75	V
Rd Impedance Detection Voltage Threshold on CC2 Pin	V_{CC} = 5 V, V_{CC1} = 5 V, Decreasing V_{CC2}	V_{RD-CC2}	2.45	2.60	2.75	V
Sink Attach Debounce Time (Note 5)	V_{CC} = 5 V	$t_{CCDebounce}$	100	150	200	ms
GATE High Voltage at 3.3 V	V_{CC} = 3.3 V	$V_{GATE-3.3V}$	5.3			V
GATE High Voltage at 21 V	V_{CC} = 21 V	$V_{GATE-21V}$	24.5			V
GATE High Voltage at $V_{IN-OVP-MAX}$	V_{CC} = $V_{CC-OVP-MAX}$	$V_{GATE-MAX}$			30	V
V_{CONN} supply voltage		V_{CONN}	3.0		5.5	V
V_{CONN} OCP voltage		I_{CONN_OCP}	50			mA
V_{CONN} OCP debounce time		t_{VCONN_OCP}	2.6	3.6	4.7	ms
V_{CONN} supply current	V_{CC} = 4.75 V, VCONN = 3 V	IV_{CONN}	34			mA
CC1 Pin Over−Voltage Protection		$V_{CC1-OVP}$	5.5	5.75	6.0	V
CC2 Pin Over−Voltage Protection		$V_{CC2-OVP}$	5.5	5.75	6.0	V
CC1/CC2 OVP Debounce Time		$t_{CC-OVP-DEB}$		28		μs
Safe Operating Voltage at 0 V		VSafe0V	0.66	0.73	0.80	V
USB PD BMC TRANSMITTER SECTION						
Unit internal	1/fBitRate	tUI	3.03		3.70	μs
Logic High Voltage	IOH = −165 μA or 293 μA	V_{OH}	1.05	1.125	1.2	V
Logic Low Voltage	IOL = 763 μA	V_{OL}			0.075	V
Rise time	VDD = 4.7 μF	$t_{Rise-TX}$	300	500	700	ns
Fall time	VDD = 4.7 μF	$t_{Fall-TX}$	300	500	700	ns
Transmitter output impedance		zDriver	33		75	Ω
USB PD BMC RECEIVER SECTION						
Rx bandwidth limiting filter		$t_{RxFilter}$	100			ns
CC receiver capacitance		cReceiver		15		pF
Receiver Input Impedance		zBmcRx	1			MΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Guaranteed by Design
6. QFN package only where NTC pin is available

Application Information

FUSB3307 has the entire PD Device Policy Manager (DPM), PD Policy Engine, Protocol and PHY layers within hardware and it responds to all the messages typical for PD Power Sources. No external processor is needed and it is completely USB PD 3.0 with PPS compliant.

Two Reference Design Examples

Below are two reference design example applications of the FUSB3307. One is an AC/DC design on the secondary side of the offline design and the other is a DC/DC design where the FUSB3307 directly controls the DC/DC controller. In the descriptions that follow, both of these designs are discussed when describing the operation of the FUSB3307. Interspersed within these descriptions is how it relates to USB Power Delivery (PD) and Type C specifications. These are just two example designs since there are considerably more use cases of the FUSB3307 in reference designs for power source applications. For more information on specific design needs, please contact your ON Semiconductor field application engineers.

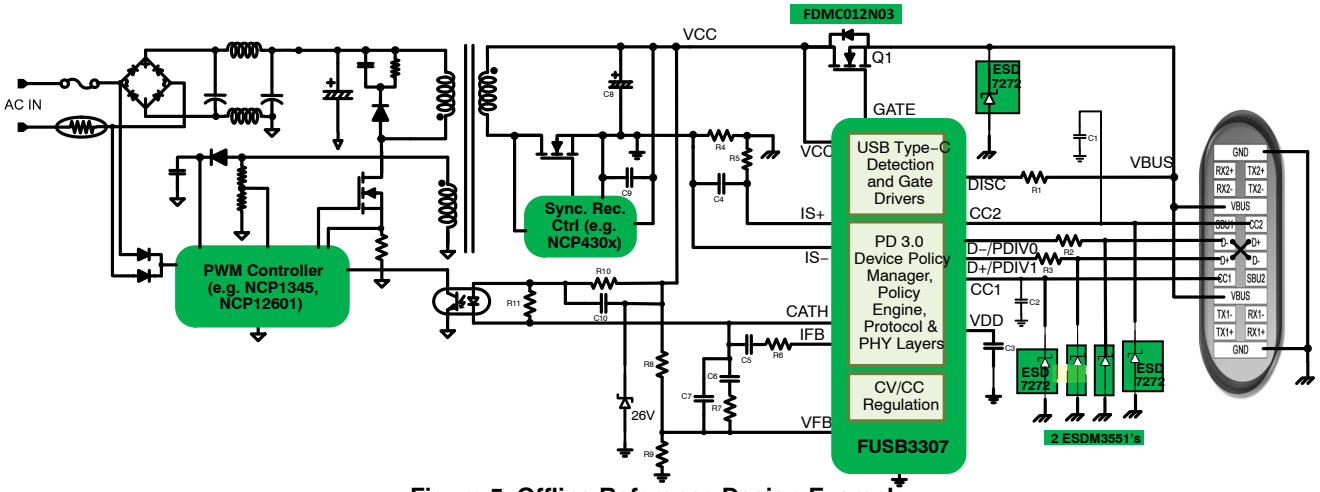


Figure 5. Offline Reference Design Example

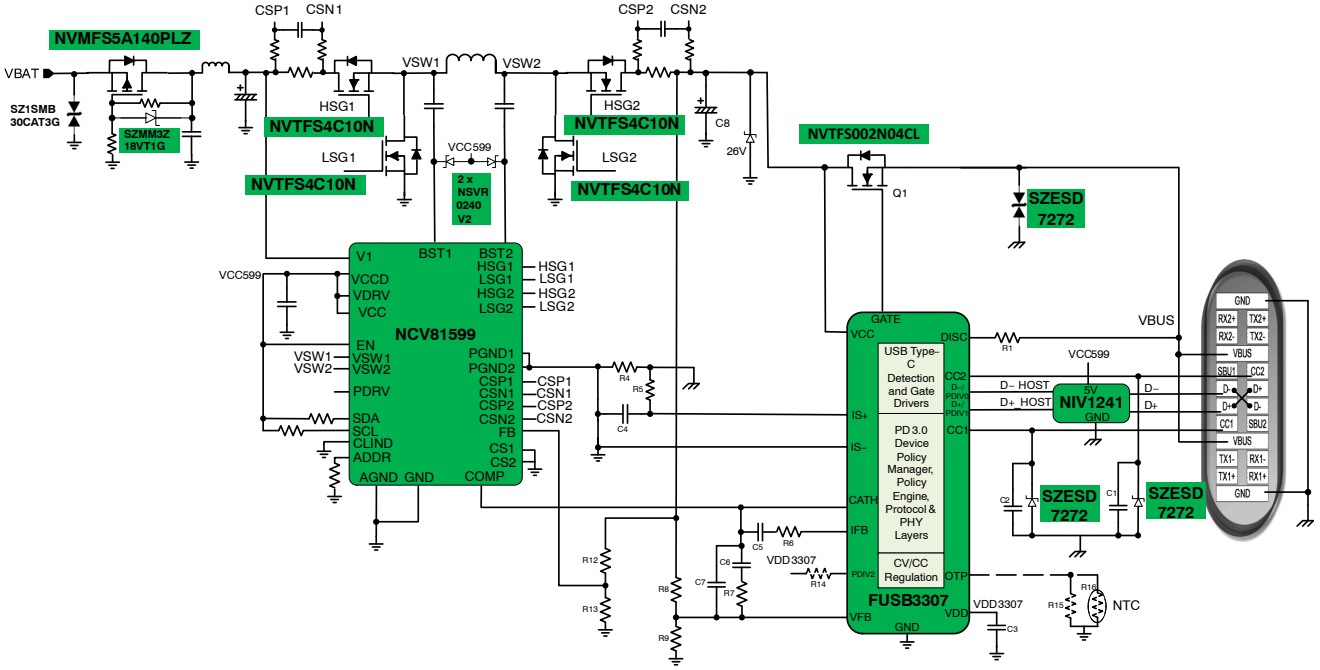


Figure 6. Automotive DC/DC Reference Design Example

Power Up and Assumptions

For Figure 5, the focus is on only the secondary side of this power source and only on the interactions with the FUSB3307 device. For Figure 6, only the interconnections of the FUSB3307 with the buck−boost shown will be discussed, not the buck−boost operation. It is assumed all other functionality of these AC/DC and DC/DC designs is known.

For Figure 5, upon application of an AC source, the secondary side VCC starts at 5 V and for Figure 6, upon application of input VBAT, the buck−boost regulates VCC at 5 V for USB−C operation. The FUSB3307 takes its input from the resistor divider ratio comprising of R8 and R9 in Figure 5 and Figure 6 above. In Figure 5, FUSB3307 controls the CATH pin current through the opto−coupler, R11 and R10 resistors for providing the feedback to the primary side controller to regulate to 5 V as shown in Figure 7.

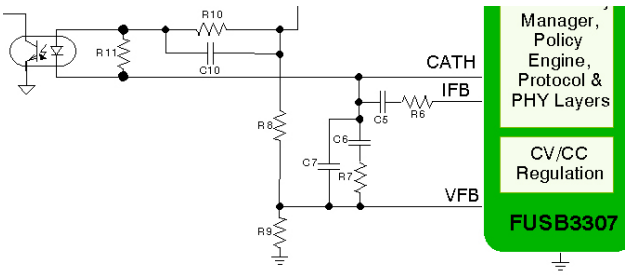


Figure 7. Constant Voltage / Constant Current (CV/CC) section of Application Diagram

In Figure 6, FUSB3307 controls the CATH pin voltage which is tied to the COMP pin of the buck−boost which directly regulates the output voltage to 5 V. The ratio of R9:(R8+R9) is expected to be 1:10 to achieve 5 V on VCC upon power up which is typically R8 = 120 kohms and R9 = 13.3 kohms.

In Figure 6, the buck−boost has its feedback FB pin which has the resistor that also expects a 1:10 resistor divider in typical default operation. However this buck−boost resistor divider is set to 1:50 ratio to set the upper limit of the voltage while the FUSB3307 directly controls the PWM operation within the buck−boost. If direct COMP pin control of the buck−boost is not desirable, then the FUSB3307 can control the FB pin via a simple external circuit. Please contact ON Semiconductor Field Application Engineers for more details.

FUSB3307 will not attach to any Sink devices unless 5 V (4.75 V to 5.5 V voltage range) is first attained on its VCC pin since that is the basis of both the USB Type C and USB Power Delivery (PD) specifications. From this 5 V on VCC, the FUSB3307 derives its VDD voltage which is used for powering the internal circuitry as illustrated by this section of the block diagram shown in Figure 8.

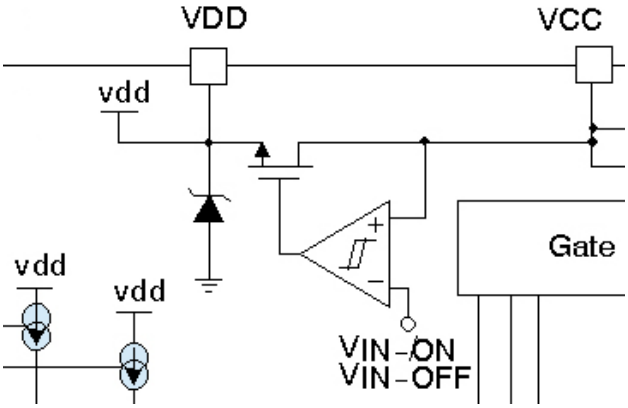


Figure 8. VDD Generation with FUSB3307

It is expected that a capacitor, C3 is connected externally (typically 1 μF) from VDD to ground to provide energy storage. VDD is regulated to be at the appropriate voltage for the internal circuitry for any USB PD contract from 3.3 V when in a USB PD Programmable Power Supply (PPS) contract to the highest PPS voltage of 21 V.

CC1 and CC2 Lines and USB−C Receptacle Assumptions

If a USB−C receptacle is used, CC1 and CC2 are connected from the receptacle to the FUSB3307's CC1 and CC2 pins. If a hardwired connection (called "captive cable" in Type−C and USB PD specifications) is desired, the CC line is connected to CC1 (or CC2 if more convenient for routing) and the VCONN line is connected to CC2 (or CC1) pin not used above.

The design in the figures above assumes a Type C receptacle (as opposed to captive cable) and all the following descriptions are consistent with this configuration. Also assumed is USB 2.0 only receptacle (D+ and D−) for a power source application without data (that is, the USB D+ and D− do not go to a USB PHY). All SuperSpeed lines (TX1+, TX1−, RX1+, RX1−, TX2+, TX2−, RX2+, RX2−) are left unconnected and the SBU1 (Side Band Use) and SBU2 pins are not used.

Internally, the FUSB3307 pulls up CC1 and CC2 individually to VDD with currents that advertise 3 A capability for this power source per USB Type C specification. When a Sink device is connected to the USB−C receptacle, the voltages on CC1 and CC2 will drop down per Type C specification. The FUSB3307 will detect a legitimate attach with the Sink and accordingly turn on the VBUS FET Q1 (see **VBUS Operation** descriptions below).

If this design needs high−voltage, short−to−VBUS protection on CC1 and CC2, the FUSB3307 protects the CC1 and CC2 lines internally to the highest VBUS voltage that is possible for USB PD. FUSB3307 also detects CC1 and CC2 pins in this over−voltage state and goes into the Type C Disabled state. But it will take a finite amount of time to detect an over−voltage event on CC1 or CC2, turn off the load switch FET Q1 and discharge VBUS and thus the over−voltage protection on CC1 and CC2 to protect these I/Os. The CC1 and CC2 connector pins are physically close to the VBUS connector pins which is why this need arises more often than not as highlighted in Figure 9.

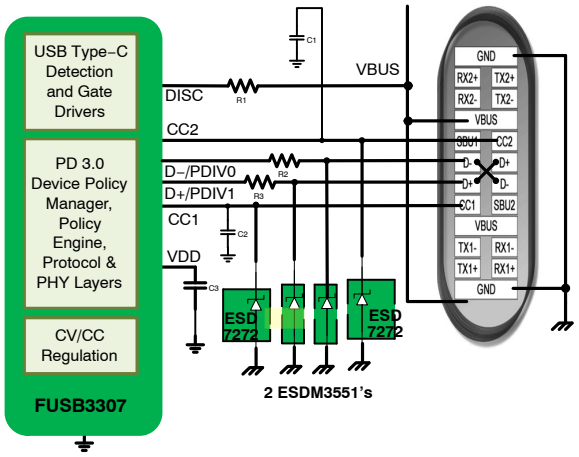


Figure 9. CC1 and CC2 Proximity to VBUS Within Type−C Connector

For USB PD traffic, per specification, the CC1 (and CC2) line needs a capacitor to ground that is between 200 pF and 600 pF to minimize noise coupling from other signals within the connector (especially if D+ and D− USB 2.0 data is sent through the USB−C connector). Since the FUSB3307 has very little internal capacitance on the CC1 and CC2 lines (cReceiver in the electrical tables above), most of this has to be supplied externally. The recommended value is 390 pF capacitors from CC1 to ground and CC2 line to ground (C1 and C2 in Figure 5 and Figure 6) and the voltage rating is dependent on the decision for high voltage protection above.

VBUS Operation

VBUS from the USB−C connector is typically connected to a load switch NFET (Q1) source terminal whose gate terminal is driven by the FUSB3307 gate driver via the GATE pin. There isn't a need for putting a resistor between GATE pin and the gate of Q1 since when the load switch is first turned on, upon attach of a Sink device via the USB−C connector, the Sink device is not allowed to draw more than 500 mA. However, if desired for a soft turn−on of the FET, a small (10 ohms typical) resistor can be placed between the FUSB3307 GATE pin and the gate terminal of Q1. The drain terminal of Q1 is connected to the power VCC which is at 5 V in the normal detached operation or in an initial USB−C attach.

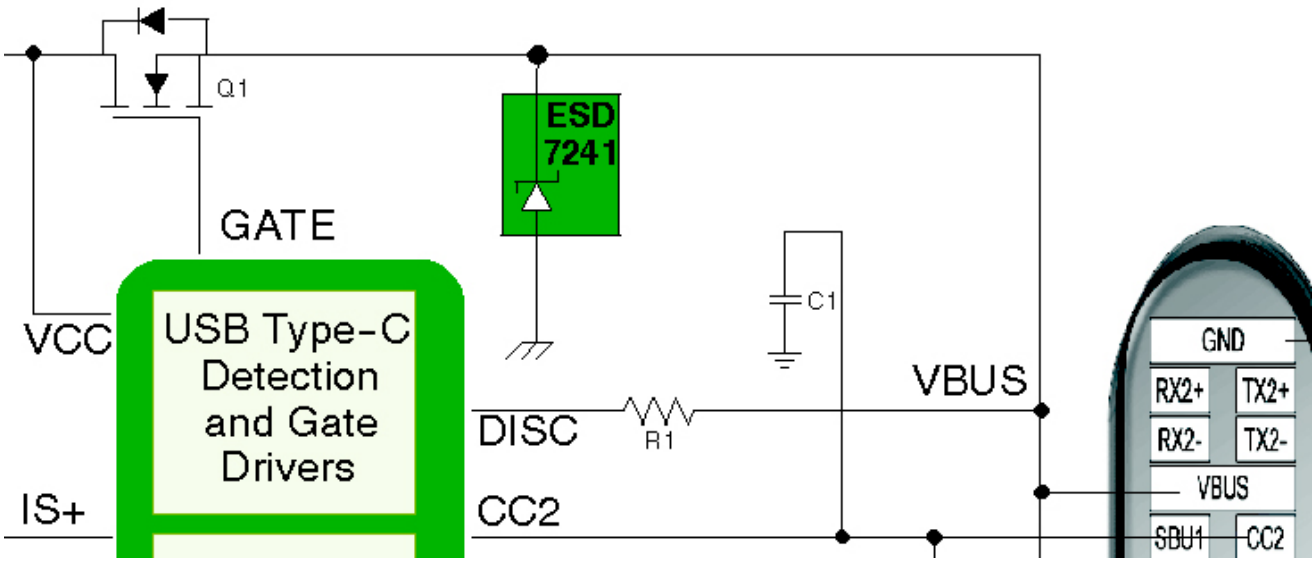


Figure 10. VBUS Discharge by FUSB3307 via DISC Pin

VBUS is discharged through a resistor (R1) via the DISC pin of the FUSB3307 as shown in the highlighted section in Figure 10.

The external resistor R1 value is dependent on the total bulk capacitance (C8) of this power source so that VBUS is discharged within the time limits dictated by USB PD. A typical value for R1 is 39 Ω, 1 W and in addition, there is internal resistance that causes a expected discharge current within the FUSB3307 in its discharge path ($I_{DISC-Sink}$ in the electrical tables above). If the load current to the Sink is sufficient (exceeds $I_{CS-EN-DSCG}$ for $t_{CS-EN-DSCG}$ debounce time) such that the internal discharge is not needed, then the FUSB3307 will automatically disable internal discharge.

Upon power up, the FUSB3307 will discharge VBUS in case there is any voltage on VBUS since the only way a Sink can be attached per Type C specification is if VBUS is discharged to ground (below VSafe0V) upon attach. The discharge resistance limits are governed by the Type C specification when not sourcing power on VBUS ($R_{DISC-BUS}$ in the electrical tables above). It is preferred that no external load/discharge resistor is connected to VBUS other than R1 to the FUSB3307 discharge DISC pin.

A TVS diode connected from VBUS to ground and shown in the figures ([SZ]ESD7241) allow operating voltages up to 24 V covering the entire VBUS range of 3.3 V to 21 V for a USB PD PPS contract. This can be replaced by a TVS that covers the VBUS range for the use case of this design if needed.

USB Type C specification requires that the supply voltage is not sourced on VBUS until an attach per Type C specification has been determined. Dual back−to−back FET's for the load switch are not needed for reverse voltage protection since it is unlikely that VBUS is charged from an external source. For interoperability with legacy connectors, there is a case where a Type A to Type C cable is first plugged into a Type A port of a power source which then supplies 5 V on VBUS of the cable. Then the Type C connector is plugged into this design which is not plugged into the AC outlet nor gets it power from the DC input depending on the design. The 5 V from the cable will forward conduct through the Q1 FET and charge the bulk capacitor C8. This doesn't cause an issue, since the FUSB3307 will power up, check the CC1 and CC2 lines and realize it is not a legitimate Sink device plugged in and stay detached. Upon unplugging the A to C cable, the discharge resistance ($R_{DISC-BUS}$ in the electrical tables above) will discharge VBUS to ground if the input voltage is still unavailable. Even if the input power is supplied to this design during this incorrect connection, VCC will regulate to 5 V which will prevent the previously forward bias body diode of Q1 FET from conducting and the FUSB3307 will wait for a legitimate Sink to be attached before turning on FET Q1. The maximum bulk capacitance is specified in the Type C specification to handle this fault case as shown in Table 5 from the USB Type C specification so as to allow for just one FET use for optimum efficiency.

Table 5. TYPE−C SPECIFICATION FOR VBUS BULK CAPACITANCE

Symbol	Notes	Min	Max	Units
VBUS Capacitance	Capacitance for source−only ports between VBUS and GND pins on receptacle when VBUS is not being sourced.		3000	μF
	Capacitance for DRP ports between VBUS and GND pins on receptacle when VBUS is not being sourced.		10	μF

Capacitance to ground on the connector side VBUS connection (source of Q1) can be added if needed but it hasn't been shown in the application diagrams above. If added, it is recommended it doesn't exceed 1 μF for recovery from the source−source case mentioned above.

Voltage and Current Sensing Operation

As mentioned above (see **Power Up and Assumptions**), the resistor ratio from VCC to ground formed by resistors R8 and R9 (typically 1:10 ratio where R8=120k and R9=13.3k) and sensed via FUSB3307 VFB pin will sense the voltage for VCC in order to set a new voltage. For Figure 5 offline design, this will be done via the FUSB3307 CATH pin, the opto−coupler, resistor R10 and the primary side PWM controller operation. R11 provides a bias current to the CATH pin feedback circuit within the FUSB3307 and is optional. For Figure 6 buck−boost design, this will be done via the FUSB3307 CATH pin controlling the buck−boost PWM via its COMP pin. The FUSB3307 will automatically control the CATH pin based on the desired voltage as determine by the USB PD contract and the existing VCC voltage sensed by VFB. If FUSB3307's PD communication is not responded to by the Sink upon initial attach, the FUSB3307 will continue with 5 V VBUS Type C operation until the Sink detaches. The external compensation network formed by C6/R7/C7 and R6/C5 need to be selected to achieve stable operation over the range of VBUS voltage and current transitions as shown in Figure 11.

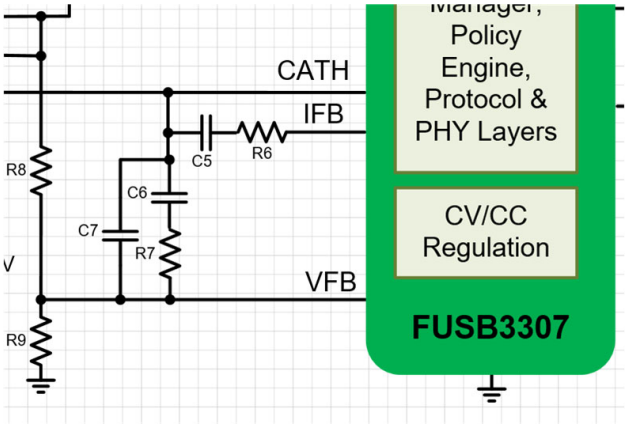


Figure 11. Compensation Network for Constant Voltage / Constant Current (CV/CC) Feedback

For the offline design, C10 may be needed as well. For the DC/DC design, there may be a need for additional compensation networks from COMP pin to ground or from COMP to the NCV81599 supply.

The current is sensed via a small resistor R4 (5 mΩ typically) connected between the USB−C connector ground and the main ground plane of the power source (secondary side ground for offline design) as shown in Figure 12.

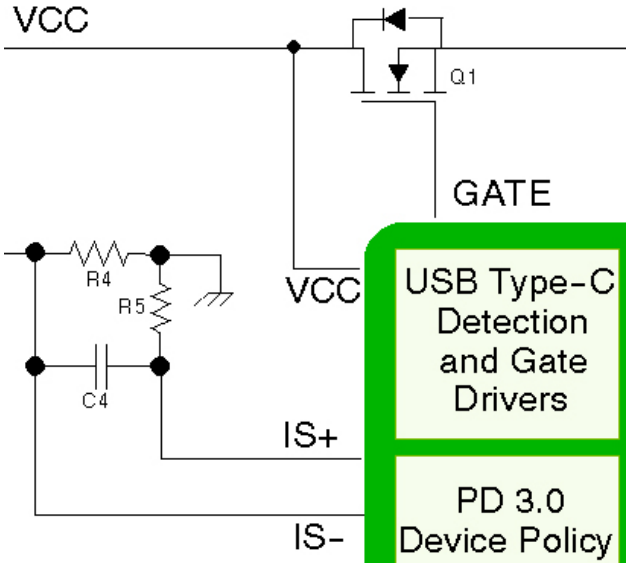


Figure 12. Current Sense Network

A low pass filter formed by R5/C4 provides a stable signal for IS+ and IS− pins of the FUSB3307 to sense this current for over−current protection for fixed voltage PD contracts, constant current operation for PPS contracts and cable compensation if selected from the trim table (Table 6). It is expected that the USB−C connector ground is connected only to the current sense network resistors R4 and R5 and the connector TVS ground connections and not to the main ground plane of the NCV81599 for the DC/DC design or secondary side power ground for the offline design (FUSB3307 ground connection). However, the FUSB3307 consumes very little current and so it should have a negligible impact on this current sensing if the FUSB3307 ground connection is on the USC−C connector ground if it is more convenient in the Printed Circuit Board (PCB) layout.

When in a PPS contract, if a PPS_Status message is requested, the FUSB3307 will measure the current with an internal 10−bit Analog to Digital Converter (ADC) based on the above description and report it back to the Sink on the PPS_Status message. The voltage is also reported back but it is measured off VCC with the ADC not VFB pin since the VFB pin is only used for voltage feedback. Thus if the voltage feedback resistor divider connected to VFB is modified to be slightly different from the 1:10 ratio expected, the voltage sensing for this PPS_Status message will not be affected.

USB 2.0 Data Lines

The USB 2.0 Data Lines D+ and D− can be externally connected together via a 100 ohms resistor to provide the maximum power, a legacy USB device can take, which is 1.5 A per USB Battery Charging v1.2 (BC1.2) specification. This will usually be the case when a USB−C to micro−B cable is plugged into this design where this adapter cable has the required Sink Rd resistors within it to allow the FUSB3307 to recognize a Type C attach and to source 5 V on VBUS. The Sink will go through BC1.2 steps of primary and secondary detection to detect a Dedicated Charging Port (DCP) via this resistor connection of D+ and D− and takes 1.5 A maximum from VBUS.

If selected by the Trim table (Table 6), to attach to certain phones that require resistor dividers on D+ and D− then connect D+ and D− to the FUSB3307 with small (22 Ω typical) resistors which auto−detects which type of legacy Sink is plugged in and automatically provides the legacy device with the appropriate power level it needs to charge. Note this power level is controlled by the device itself not the power source which is typical of most legacy USB power systems. The FUSB3307 will allow for 5 V at a maximum of 3 A for even legacy devices which will take at most either 1.5 A or 2.4 A for most legacy devices.

D+ and D− can also be connected to a USB Physical Layer (PHY) controller for using these lines for data traffic. In that case, the USB PHY is expected to advertise itself as a Charging Downstream Port (CDP) per BC1.2 so that the Sink can take a maximum of 1.5 A of power.

D+ and D− are low voltage pins (6 V absolute maximum voltage) and are not expected to be shorted to VBUS when VBUS goes higher than 6 V. The TVS diodes connected to D+ and D− shown in the figure (ESD7104) allow operating voltages up to 5 V for the offline design (Figure 5) and typically D+ and D− are 3.3 V signals when used for USB 2.0 data signals. For the automotive buck−boost design (Figure 6), short−to−VBUS protection is shown via the NIV1241 that contain TVS diodes and FETs to keep the FUSB3307 D+ and D− lines less than 5 V as shown in Figure 13.

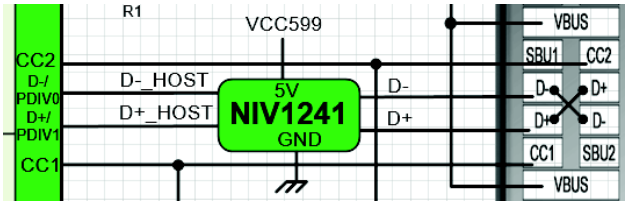


Figure 13. D+ and D− Pin Protection Provided by the NIV1241

Power Delivery Operation

FUSB3307 advertises source capabilities and responds to PD message completely autonomously following the USB PD 3.0 with PPS and Type C specifications. For more details on the USB PD messages please refer to the specification references mentioned below (See **Specification References** on page 19). Similarly the references mention the Type C and the BC1.2 specifications as well for further information.

To allow for a variety of designs, the following table has a number of trim options to accommodate almost every design. The following Table 6 lists out the various options. While all these options exist, they can only be obtained from ON Semiconductor if requested and once delivered, the trim option cannot be changed. The default trim option column below is for a 60 W design that uses 3 A cables and is for a USB Power Delivery (PD) 3.0 design with Programmable Power Supplies (PPS) and Fixed Supplies. In the future more default options will be available for general purpose use with likely 30 W, 45 W and 90 W power levels in addition to the 60 W option.

Table 6. FUSE TRIM (NOTE 7) OPTION TABLE

#	Function	Trim Option	Default Option
1	Output Power	PD Power (PDP) from 16 W to 100 W in 1W increments	60 W
2	Cable Compensation	Four choices of 50 mV/A, 100 mV/A, 150 mV/A and Disabled	Disabled
3	5 A Power Source	0 = Max current is 3 A, no eMarker detection 1 = Max current is 5 A, eMarker detection needed	0 = Max current = 3 A, no eMarker detection
4	Charging Output OVP	Four choices of OVP thresholds: 115%, 120%, 125% and 130%	120% OVP
5	Charging Output UVP	Four choices of UVP thresholds: 60%, 65%, 70% and Disabled	65% UVP
6	D+/D− versus PDIV0/PDIV1	00: D+/PDIV1=D+, D−/PDIV0=D− (SOIC package without PDIV2 pin) 01: D+/PDIV1=PDIV1, D−/PDIV0=PDIV0 (SOIC package without PDIV2 pin) 10: D+/PDIV1=PDIV1, D−/PDIV0=PDIV0 PDIV2 standalone pin (QFN package) 11: D+/PDIV1=D+, D−/PDIV0=D− PDIV2 standalone pin (QFN package)	00 for SOIC package 11 for QFN package
7	Support PD 3.0	0 = Enable PD 2.0 1 = Enable PD 3.0	1 = Enable PD 3.0

7. "Trim Options" means feature programmability to create new functional options in a manufacturing test program by trimming semiconductor fuses.

When a Sink device is connected via the USB−C connector, as mentioned above, the FUSB3307 will detect a legitimate Type C attach and drive the GATE pin to turn on the VBUS load switch Q1. The initial voltage on VBUS is always 5 V (4.75 V to 5.5 V voltage range) and the CC pin will advertise 3 A capability which is the maximum power allowed by a Type C (without PD) port. FUSB3307 is not expected to be used below 15 W power level since ON Semiconductor has other Type C only controllers such as the FUSB303. Subsequent to the initial attach, the FUSB3307 will send out PD packets to advertise source capabilities as selected by the trim options in Table 6. Using the Default FUSB3307 Trim options, the FUSB3307 will source 60 W by sending out a PD Source_Capabilities message on the CC line (either CC1 or CC2 depending on connector plug orientation) using PD communication messages. The supplies advertised for the default trim option are fixed supplies and PPS supplies shown in Table 7:

Table 7. DEFAULT TRIM OPTION ADVERTISED PD SOURCE CAPABILITIES

[Augmented] Power Data Object	Output Voltage	Maximum Sink Current Expected	Current Protection
PDO1	5 V	3 A	Over Current Protection
PDO2	9 V	3 A	Over Current Protection
PDO3	12 V	3 A	Over Current Protection
PDO4	15 V	3 A	Over Current Protection
PDO5	20 V	3 A	Over Current Protection
APDO1	3.3 V min, 21 V max	3 A	Current Limit Protection

The Sink will select one of these offerings and enter into a PD explicit contract with the FUSB3307 which is the first step of all subsequent PD communication. If the Sink selects an illegal data object number or requests an illegal current level, the FUSB3307 will reject the request. A short amount of time after this reject message is sent, the FUSB3307 will resend its Source_Capabilties message and expect a valid request.

If a 5 A capability is chosen from the trim table (Table 6) above then the FUSB3307 will use USB PD Discover Identity messages to interrogate the capabilities of the cable attached to it to ensure that it is a 5 A capable cable before the FUSB3307 advertises 5 A source capabilities. The FUSB3307 supplies the VCONN power needed to support this discovery process as specified in the USB PD and Type C specification which eliminates the need for an external VCONN power source and multiple power switches. If the cable is only 3 A, even though the FUSB3307 can support 5 A, the advertised capabilities will all drop down to 3 A. This will be done on the first source capabilities advertised but there is an indication in the USB PD Status message sent to indicate that the source is 5 A capable but the cable has limited the source capabilities to 3 A. In Table 8 the section of the SOP Status Data Block (SDB) is shown that communicates this power limitation.

Table 8. PD Status Message to Sink Showing Power is Limited by the Cable

Offset	Field	Bit	Description
5	Power Status	0	...
		1	Source power limited due to cable supported current
		2	...
		6...7	...

The FUSB3307 follows all USB PD specifications including dropping down to USB PD 2.0 operation when it detects a USB PD 2.0 Sink and a USB PD 2.0 cable eMarker (if applicable). All subsequent operation will follow the USB PD 2.0 specification until the FUSB3307 is reset via a Hard Reset message or undergoes a power cycle.

Standby Operation

When the FUSB3307 is in standby, where the source power supply still has to be maintained at 5 V via the CATH pin for a typical Type C connection but no Sink device has been attached to the FUSB3307, then the current consumed is just $I_{CC-GREEN}$ (< 870 μA typical). This low standby current allows for all the energy standard specifications to be well exceeded for offline designs (typically the FUSB3307 within the offline design can achieve 21 mW standby power).

PDIV0, PDIV1 and PDIV2 Options

FUSB3307 can adjust the output power from the trim table (Table 6) to have any PDP (Power Delivery Power) from 16 W to 100 W (called TrimPDP here) in 1 W increments. However, in some applications in may be advantageous to trim all FUSB3307 devices to 60 W PDP and use them in both single port and dual port configurations. For the dual port configuration, the PDP would need to be halved for assured capacity charger ports and PDIV2 pin does just that – cuts the trimmed 60 W PDP in half to 30 W. For further divider ratios, PDIV1 and PDIV0 can be used as well.

PDIV2 is available only in the QFN version of the FUSB3307 while PDIV0 and PDIV1 share their functionality with the D− and D+ pins respectively in both the QFN and SOIC package options. For the PDIV2 pin, the selection of power is shown in Table 9.

Table 9. PDIV2 Pin Changing Advertised PD Power

PDIV2 Pin State	Advertised PDP (Power Delivery Power)
1	100% of TrimPDP
0	50% of TrimPDP

With the SOIC package and PDIV0 and PDIV1 pins selected, the power can be controlled as shown below. In this case there is no PDIV2 pin and the PDIV0 and PDIV1 pins are used to trim power, as shown in Table 10.

Table 10. PDIV0 and PDIV1 Pins Changing Advertised PD Power

PDIV1 Pin State	PDIV0 Pin State	Advertised PDP (Power Delivery Power)
1	1	100% of TrimPDP
1	1	75% of TrimPDP
0	1	50% of TrimPDP
0	0	25% of TrimPDP

If PDIV2 is also available (i.e. QFN package) and in the above trim table (Table 6) the pins D+/PDIV1 and D−/PDIV0 allow PDIV0 and PDIV1 to be available as pins, then this is the PDP advertised, as shown in Table 11.

Table 11. PDIV0, PDIV1 and PDIV2 Pins Changing Advertised PD Power

PDIV2 Pin State	PDIV1 Pin State	PDIV0 Pin State	Advertised PDP (Power Delivery Power)
1	1	1	100% of TrimPDP
1	1	0	87.5% of TrimPDP
1	0	1	75% of TrimPDP
1	0	0	62.5% of TrimPDP
0	1	1	50% of TrimPDP
0	1	0	37.5% of TrimPDP
0	0	1	25% of TrimPDP
0	0	0	12.5% of TrimPDP

In all the above calculations, no Advertised PDP will ever go below 16 W minimum if in a USB PD contract. For example, if TrimPDP=100 and when PDIV0, PDIV1 and PDIV2 pins are available and they are [PDIV2:PDIV1:PDIV0] = 001 then Advertised PDP is 25 W (100W*25%). However if TrimPDP=60, then Advertised PDP is 16 W not 15 W (60W*25%).

When any of these pins, PDIV0, PDIV1 and PDIV2 are changed, the connected PD Sink has to ask for Source Capabilities to get these new capabilities or if this Sink or the FUSB3307 executes a Soft_Reset or Hard Reset which causes the new advertised capabilities to be sent by the FUSB3307. Alternatively recovery from any protection operation would cause the FUSB3307 to advertise the new PDP values based on the PDIV0, PDIV1 and PDIV2 pins setting.

Protection Operation

FUSB3307 has a number of ways it protects itself as shown in Table 12.

Table 12. Protection Modes Available

Symbol	Description	Pin(s) Used	Package
OVP	Output Voltage Over Voltage Protection	VCC	SOIC & QFN
UVP	Output Voltage Under Voltage Protection	VCC	SOIC & QFN
OCP	Over Current Protection	IS+ & IS−	SOIC & QFN
I_OTP	Internal Over Temperature Protection	none	SOIC & QFN
E_OTP	External Over Temperature Protection	NTC	QFN only
CC_OVP	CC1 or CC2 Over Voltage Protection	CC1 / CC2	SOIC & QFN
VCONN_OCP	CC1 or CC2 VCONN Over Current Protection	CC1 / CC2	SOIC & QFN

OVP and UVP are sensed via an internal resistor divider that divides VCC by 10 to determine the voltage from the power source. CC1 and CC2 are directly sensed for over voltage. For E_OTP (QFN package option only), a pin NTC is available that is connected to an NTC resistor to ground usually in parallel with another resistor to ground for linearity. For I_OTP (SOIC and QFN packages), an internal temperature monitor is used. For all faults except VCONN_OCP fault, upon detection, the FUSB3307 will disable the Type C connection with the Sink (no pull−up on CC), shut off VBUS load switch and keep monitoring the fault. Once the fault has been removed, the FUSB3307 starts up at 5 V after $t_{2S_AR_NM}$ seconds and reconnects with the Sink.

Output Over Voltage Protection (OVP)

FUSB3307 has built−in OVP based on the Trim Table (Table 6). For the default OVP case, whenever VCC, as sensed by an internal 1:10 resistor divider, exceeds K_{CC-OVP} (typically 120%) of the requested VCC from the power source for a debounce time of t_{D-OVP}, then the OVP fault would be triggered. Upon detection, the FUSB3307 will disable the Type C connection with the Sink (no pull−up on CC), shut off VBUS load switch and keep monitoring VCC to determine if the OVP is still present. When OVP is removed, a timer is started which when expired in t_{2S_AR} seconds, causes the FUSB3307 to reestablish the Sink Type C connection with the initial 5 V VBUS supplied as if it were initially attached.

During transitions between VCC voltages, the OVP circuitry is blanked or disabled for $t_{BNK-OVP}$ time to ensure that false triggering of OVP doesn't occur. To ensure safe operation over all voltages of VCC, the maximum VCC voltage is limited to $V_{CC-OVP-MAX}$.

Output Under Voltage Protection (UVP)

FUSB3307 has a built−in UVP based on the Trim Table (Table 6). For the default UVP case, whenever VCC, as sensed internally, is below K_{CC-UVP} (typically 65%) of the requested output voltage from the power source for a debounce time of t_{D-UVP}, then the UVP fault would be triggered. No PD Alert messages are sent for this fault.

During transitions between VCC voltages, the UVP circuitry is blanked or disabled for $t_{BNK-UVP}$ time to ensure that false triggering of UVP doesn't occur.

For PPS contracts, if current limiting causes the voltage to decrease, the UVP fault will not trigger at 65% of VCC since all voltages from the requested voltage to V_{CC-OFF}, the lowest voltage, are valid.

For compliance with the USB PD specification, the FUSB3307 will trigger UVP whenever VCC is below V_{CC-OFF}. This allows protection for a direct short of VBUS to ground separately or in conjunction with the OCP fault described below. If VCC < V_{CC-OFF} fault is triggered, then to resume normal operation, VCC has to go below V_{LATCH} to reset the FUSB3307 to exit this fault condition.

Over Current Protection (OCP) and Constant Current Limit (CL)

If VBUS is shorted to ground, either the UVP fault described above could trigger or the OCP fault, or both. FUSB3307 senses the current via a small R4 resistor (5 mΩ typical) as described in the **Voltage and Current Sensing** section above. The OCP fault is triggered at 120% of the maximum current for the requested Power Data Object (PDO) for fixed supplies only (I_{CS-3A} typically 3.6 A for a 3 A maximum fixed supply current). Once this OCP fault occurs, the FUSB3307 protects the system as described in the **Protection Operation** section above. An Alert message is sent upon the FUSB3307 establishing an explicit contract with the Sink and a PD "Status" message from the FUSB3307 will include the OCP history.

For PPS APDO's (Augmented Power Data Objects), Constant Current Limiting (CL) is used as specified in the USB PD specification where the voltage will drop to a low value based on keeping the current constant and equal to the requested PPS current. In this case UVP described above will trigger if VCC drops below V_{CC-OFF} since any voltage from the lowest 3.3 V – 5% to the PPS requested voltage could occur with current limiting. If the PPS current limit is changed with a new PD Request message, the VCC voltage may change accordingly to a new value based on the current limiting function. An Alert message is sent whenever there is a switch from Constant Current Limit (CL) to Constant Voltage (CV) mode and vice versa. For PPS_Status messages, this flag that shows whether the FUSB3307 is in CL or CV mode, is sent along with the VCC voltage and load current as sensed by R4 to monitor the FUSB3307 while it provides PPS voltages and currents.

Over Temperature Protection (I_OTP and E_OTP)

FUSB3307 has two different over temperature faults, E_OTP and I_OTP. For E_OTP, when the QFN package is used, there is a NTC pin that is expected to be connected to an NTC resistor in parallel with a regular resistor for linearity. The FUSB3307 provides a I_{NTC} current source (typically 60 μA) on the NTC pin to bias this NTC resistor so that an internal A/D converter measures the external temperature as shown in Figure 14.

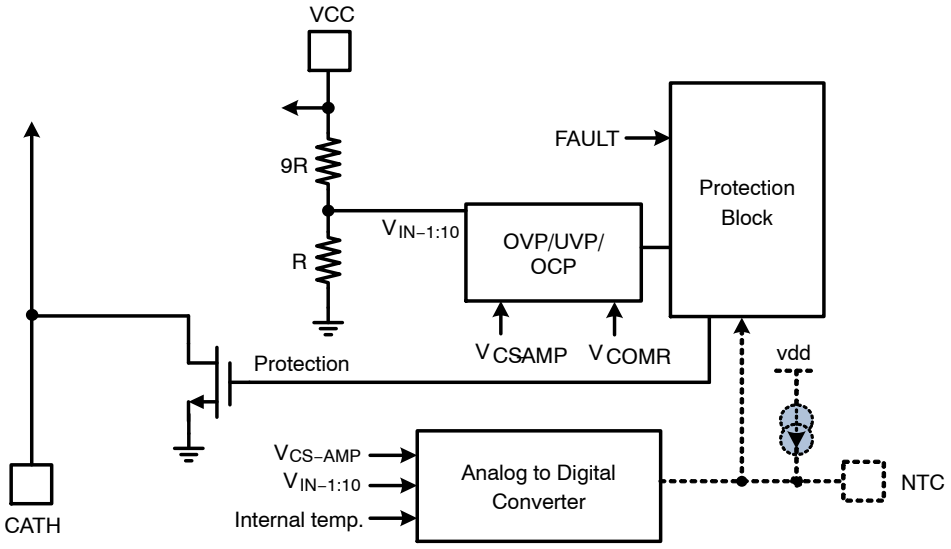


Figure 14. Protection Section of Block Diagram for UVP, OVP, OCP, and OTP Faults

This NTC measured temperature is useful for dynamic monitoring by the Sink via FUSB3307 provided PD Status messages which contains this NTC temperature in this package option. If this temperature exceeds a warning threshold (100°C for a NTC resistor of 100 kΩ ± 1%, B25/50 = 4300K ± 1% to ground in parallel with a 20 kΩ ± 1% to ground) for $t_{NTC-DEB}$ debounce time, then a PD Alert message is sent to the Sink indicating this temperature warning. If however, the E_OTP threshold is exceeded (110°C for a NTC resistor of 100 kΩ ± 1%, B25/50 = 4300K ± 1% to ground in parallel with a 20 kΩ ± 1% to ground) for $t_{NTC-DEB}$ debounce time, then an E_OTP fault is triggered as described in the **Protection Operation** section above. Upon re−establishing an explicit contract with the Sink, the FUSB3307 sends an Alert to let the Sink know it previously experienced an Over Temperature Protection event.

The SOIC package version of the FUSB3307 doesn't have an NTC pin and so the internal die temperature is monitored. When the die temperature exceeds T_{INT-W} threshold for $t_{NTC-DEB}$ debounce time, then a PD Alert message is sent to the Sink indicating this temperature warning. If however, the $T_{INT-OTP}$ threshold is exceeded for $t_{NTC-DEB}$ debounce time, then an I_OTP fault is triggered and executing protection as described in **Protection Operation** section above. The FUSB3307 sends an Alert to let the Sink know it previously experienced an Over Temperature Protection event. This internal die temperature is monitored also in the QFN package option and either an E_OTP fault (based off the NTC pin voltage) or an I_OTP fault causes the FUSB3307 to disconnect and shut off VBUS. The temperature warning for the QFN package is only triggered via the NTC resistor not the internal die temperature.

CC1 and CC2 Over Voltage Protection (CC_OVP)

FUSB3307 protects against the CC1 and CC2 connector pins being shorted to VBUS up to 26 V and it has the ability to start protecting the system when the CC voltage is beyond it normal operating range. If the CC voltage is above $V_{CC1-OVP}$ (if CC is CC1 pin) or above $V_{CC2-OVP}$ (if CC is CC2 pin) threshold for $t_{CC-OVP-DEB}$ debounce time, then the FUSB3307 protects the system by triggering this fault and executing protection as described in **Protection Operation** section above.

VCONN Over Current Protection (VCONN_OCP)

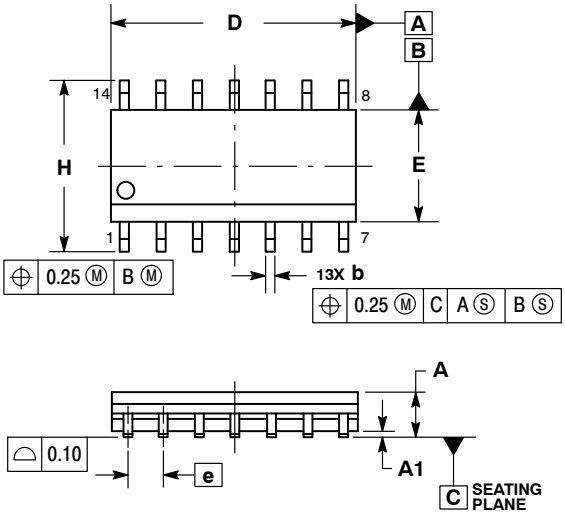
FUSB3307 will turn on VCONN whenever it needs to read the eMarker in the cable only if 5 A capability is chosen from the trim table (Table 6) above and this design has a Type C connector and not a hardwired captive cable. When VCONN is sourced, per USB PD specification only 100 mW maximum (5 V with 20 mA for the FUSB3307) needs to be supplied for a USB 2.0 source application. If the VCONN current exceeds I_{CONN_OCP} (typical 50 mA) for t_{VCONN_OCP} then the FUSB3307 will disable the VCONN supply and abort the eMarker discovery process. The default maximum current of 3 A will be used for all source capabilities for USB PD messages in the latter case and the normal PD messaging will occurs without interruption. No Alert messages will be sent but the PD Status message will have a bit to indicate that the cable limited the FUSB3307 from advertising 5 A source capabilities.

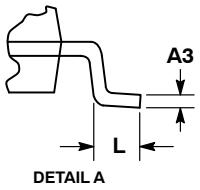
Specifications References

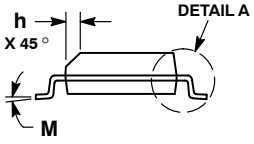
- Universal Serial Bus Power Delivery specification revision 3.0 version 2.0 + ECNs up to 07 February, 2020
- Universal Serial Bus Type C Cable and Connection Specification release 2.0, dated August, 2019
- USB Battery Charging Specification, revision 1.2, dated December 7, 2010
- Universal Serial Bus Power Delivery specification revision 2.0 version 1.3, dated 12 January, 2017

PACKAGE DIMENSIONS

SOIC−14 NB
CASE 751A−03
ISSUE L



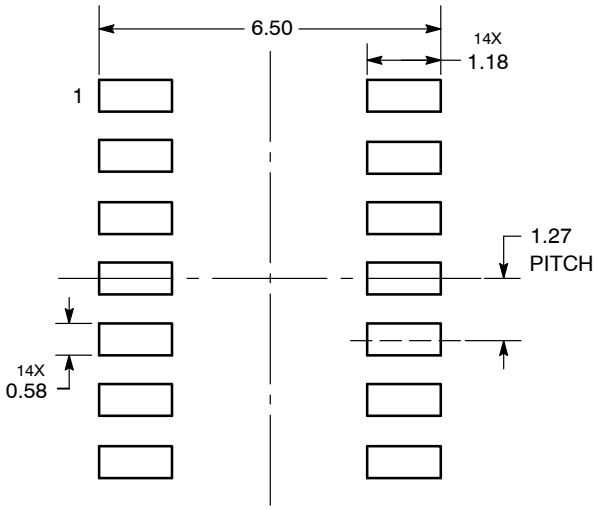




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
A3	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7 °	0 °	7 °

SOLDERING FOOTPRINT*

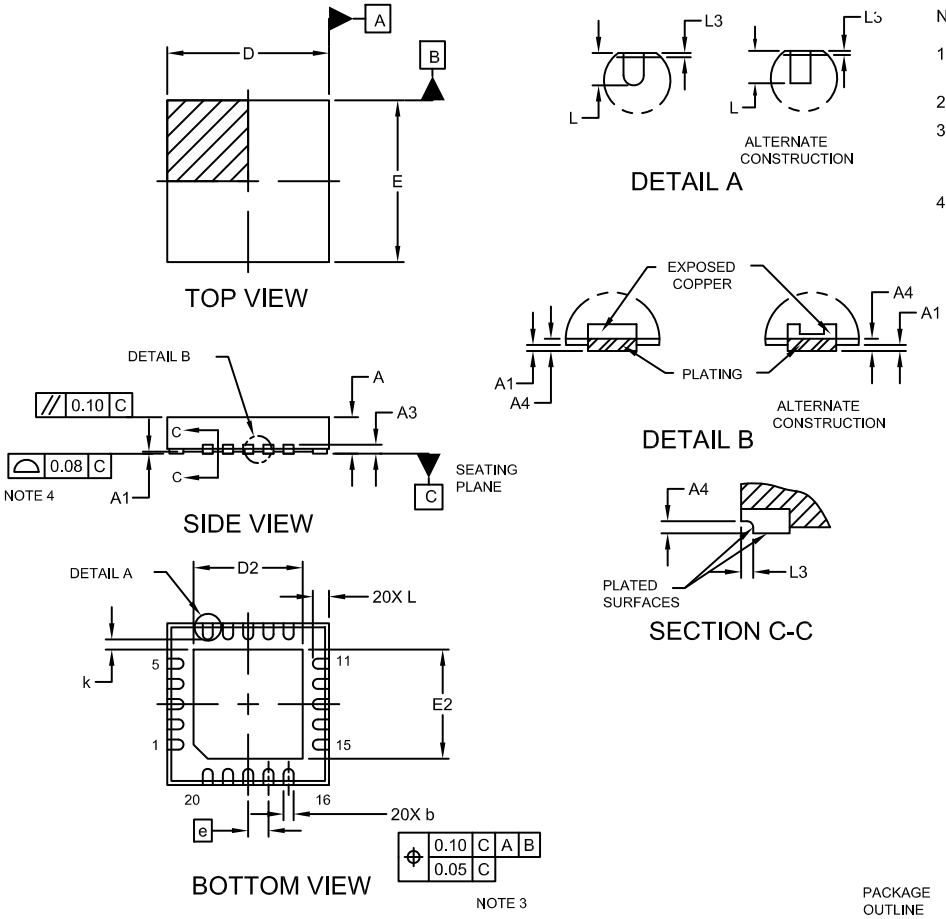


DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

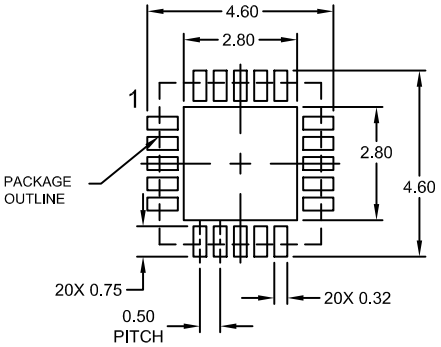
QFNW20 4x4, 0.5P
CASE 484AT
ISSUE O



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2008.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO THE PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
A4	0.10	---	---
b	0.20	0.25	0.30
D	3.90	4.00	4.10
D2	2.60	2.70	2.80
E	3.90	4.00	4.10
E2	2.60	2.70	2.80
e	0.50 BSC		
k	0.20	---	---
L	0.35	0.40	0.45
L3	---	---	0.090



RECOMMENDED MOUNTING FOOTPRINT*

*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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