

512K x 32 SRAM

SRAM Memory Array MCM

FEATURES

- Fast access times: 10, 12, 15, 17 and 20ns
- Fast OE\ access times: 6ns
- Ultra-low operating power < 1W worst case
- Single +3.3V $\pm 0.3V$ power supply
- Fully static -- no clock or timing strobes necessary
- All inputs and outputs are TTL-compatible
- Easy memory expansion with CE\ and OE\ options
- Automatic CE\ power down
- High-performance, low-power consumption, CMOS

OPTIONS

- Timing

10ns	-10
12ns	-12
15ns	-15
17ns	-17
20ns	-20
- Package

Ceramic Quad Flatpak	Q	No. 702
Ceramic Quad Flatpak(.054min SO)	Q1	
Pin Grid Array	P	No.904
- Operating Temperature Ranges

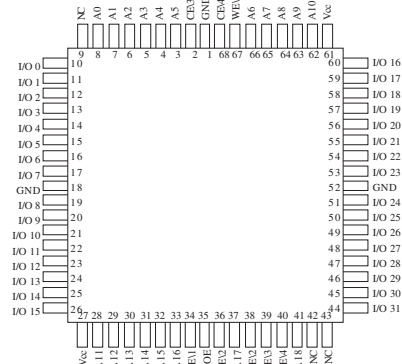
Military (-55°C to +125°C)	XT
Industrial (-40°C to +85°C)	IT
- 2V data retention/low power L

MARKINGS

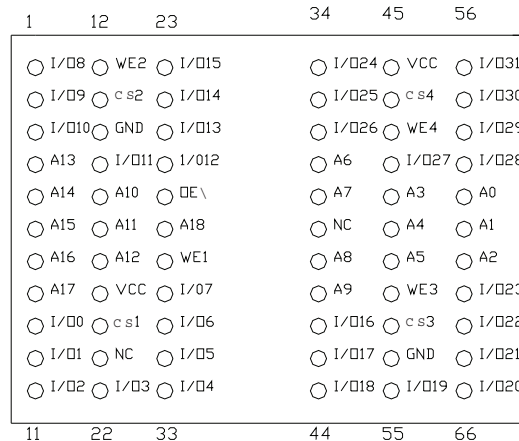
PIN ASSIGNMENT

(Top View)

68 Lead CQFP (Q & Q1)



66 Lead PGA (P)

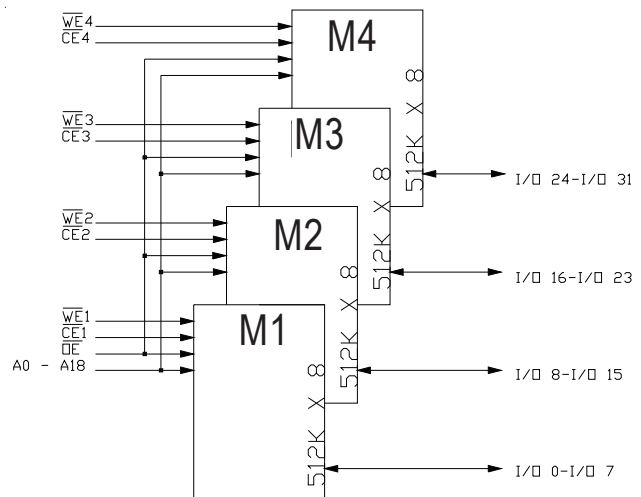


GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8SLC512K32 is a 3.3V 16 Megabit CMOS SRAM Module organized as 512Kx32 bits. The AS8SLC512K32 achieves very high speed access, low power consumption and high reliability by employing advanced CMOS memory technology.

This military temperature grade product is ideally suited for commercial, industrial, and military applications when asynchronous high speed switching and low ACTIVE opening power & ultra Fast Asynchronous Access is mandated.

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BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Voltage of Vcc Supply Relative to Vss.....-0.5V to +4.6V
 Storage Temperature.....-65°C to +150°C
 Short Circuit Output Current(per I/O).....20mA
 Voltage on Any Pin Relative to Vss.....-5V to Vcc+4.6V
 Maximum Junction Temperature**.....+150°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device.

This is a stress rating only and functional operation on the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow. See the Application Information section at the end of this datasheet for more information.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(-55°C ≤ T_A ≤ 125°C and -40°C to +85°C; Vcc = 3.3V ±0.3V)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
Input High (logic 1) Voltage		V _{IH}	2.2	V _{CC} +0.3	V	1
Input Low (logic 1) Voltage		V _{IL}	-0.3	0.8	V	1
Input Leakage Current _{ADD,OE}	0V < V _{IN} < V _{CC}	I _{LI1}	-10	10	μA	
Input Leakage Current _{WE,CE}		I _{LI2}	-10	10	μA	
Output Leakage Current _{I/O}	Output(s) Disabled 0V < V _{OUT} < V _{CC}	I _{LO}	-10	10	μA	
Output High Voltage	I _{OH} = -4.0mA	V _{OH}	2.4		V	1
Output Low Voltage	I _{OL} = 8.0mA	V _{OL}		0.5	V	1

DESCRIPTION	CONDITIONS	SYMBOL	MAX					UNITS	NOTES
			-10	-12	-15	-17	-20		
High Speed Power Supply Current: Operating	CS\ < V _{IL} ; V _{CC} = MAX f = MAX = 1/ t _{RC} (MIN) Outputs Open, OE\ = V _{IH}	I _{CC1}	350	320	280	260	240	mA	2, 3, 13
	Low Power (L)		280	240	200	180	160		
Low Speed Power Supply Current: Operating	CS\ < V _{IL} ; V _{CC} = MAX f = 10 MHz, OE\ = V _{IH}	I _{CC2}	---	---	---	---	---	mA	2
	Low Power (L)		120	80	80	80	80		
Low Speed Power Supply Current: Operating	CS\ < V _{IL} ; V _{CC} = MAX f = 1 MHz, OE\ = V _{IH}	I _{CC3}	---	---	---	---	---	mA	2
	Low Power (L)		80	40	40	40	40		
Power Supply Current: Standby	CS\ > V _{IH} ; V _{CC} = MAX f = MAX = 1/ t _{RC} (MIN) Outputs Open, OE\ = V _{IH}	I _{SBT1}	100	80	80	80	80	mA	3, 13
	Low Power (L)		80	60	60	60	60		
CMOS Standby	V _{IN} = V _{CC} - 0.2V, or V _{SS} + 0.2V V _{CC} = Max; f = 0Hz	I _{SBT2}	80	60	60	60	60	mA	
	Low Power (L)		50	36	36	36	36		

CAPACITANCE ($V_{IN} = 0V$, $f = 1MHz$, $T_A = 25^{\circ}C$)*

SYMBOL	PARAMETER	MAX	UNITS
C_{ADD}	A0 - A18 Capacitance	40	pF
C_{OE}	OE\ Capacitance	40	pF
C_{WE}, C_{CS}	WE\ and CS\ Capacitance	12	pF
C_{IO}	I/O 0- I/O 31 Capacitance	15	pF

NOTE:

*This parameter is sampled.

AC TEST CONDITIONS

TEST SPECIFICATIONS

Input pulse levels.....VSS to 3V
 Input rise and fall times.....1ns/V
 Input timing reference levels.....1.5V
 Output reference levels.....1.5V
 Output load.....See Figure 1, 2

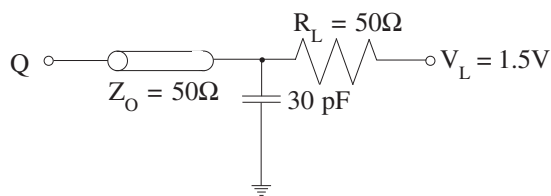


FIGURE 1

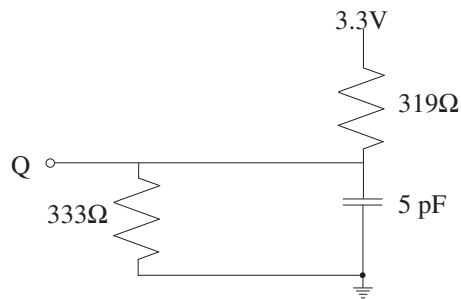


FIGURE 2

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

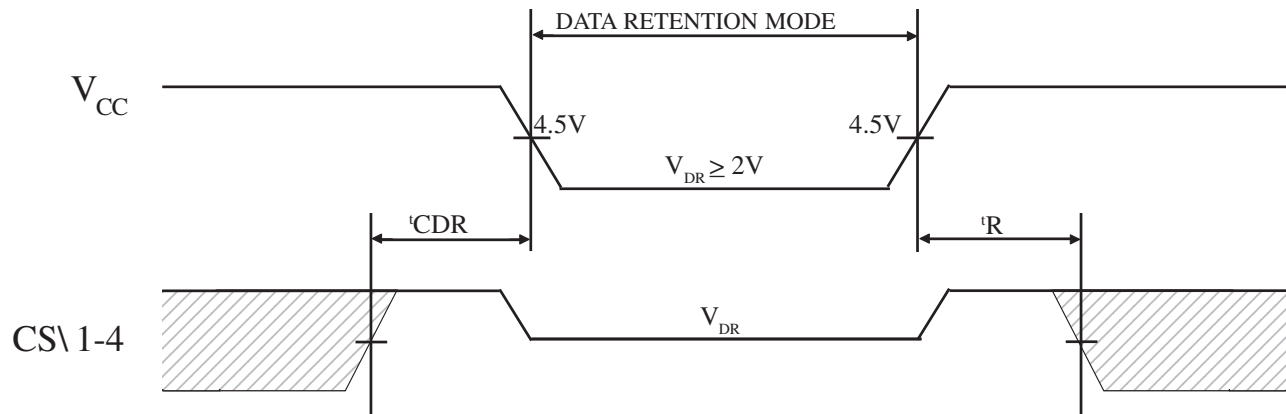
(NOTE 5) ($-55^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ and -40°C to $+85^{\circ}\text{C}$; $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$)

DESCRIPTION	SYMBOL	-10		-12		-15		-17		-20		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
READ CYCLE													
READ cycle time	^t RC	10		12		15		17		20		ns	
Address access time	^t AA		10		12		15		17		20	ns	
Chip select access time	^t ACS		10		12		15		17		20	ns	
Output hold from address change	^t OH	1		2		2		2		2		ns	
Chip select to output in Low-Z	^t LZCS	1		2		2		2		2		ns	4,6,7
Chip select to output in High-Z	^t HZCS		5		6		7		7.5		8	ns	4,6,7
Output enable access time	^t AOE	0	5	0	6	0	7		7.5	0	8	ns	
Output enable to output in Low-Z	^t LZOE	0		0		0		0		0		ns	4,6
Output disable to output in High-Z	^t HZOE		5		6		7		7.5		8	ns	4,6
WRITE CYCLE													
WRITE cycle time	^t WC	10		12		15		17		20		ns	
Chip select to end of write	^t CW	7		8		10		11		12		ns	
Address valid to end of write	^t AW	7		8		10		11		12		ns	
Address setup time	^t AS	0		0		0		0		0		ns	
Address hold from end of write	^t AH	0		0		0		0		0		ns	
WRITE pulse width, CS\ controlled	^t WP1	9		10		12		14		15		ns	
WRITE pulse width, WE\ controlled	^t WP2	9		10		12		14		15		ns	
Data setup time	^t DS	5		6		7		7.5		8		ns	
Data hold time	^t DH	1		1		1		1		1		ns	
Write disable to output in Low-z	^t LZWE	2		2		2		2		2		ns	4,6,7
Write enable to output in High-Z	^t HZWE	5		5		6		6.5		7		ns	4,6,7

LOW POWER CHARACTERISTICS (L Version Only)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS	NOTES
V_{CC} for Retention Data		V_{DR}	2		V	
Data Retention Current	All Inputs @ $V_{CC} \pm 0.2V$ or $V_{SS} \pm 0.2V$, $CS\backslash = V_{CC} \pm 0.2V$	$V_{CC} = 2V$ I_{CCDR}		24	mA	
		$V_{CC} = 3V$ I_{CCDR}		32	mA	
Chip Deselect to Data Retention Time		t_{CDR}	0		ns	4
Operation Recovery Time		t_R	20		ms	4, 11

LOW V_{CC} DATA RETENTION WAVEFORM



NOTES

1. All voltages referenced to V_{SS} (GND).
2. Worst case address switching.
3. I_{CC} is dependent on output loading and cycle rates.

$$\text{unloaded, and } f = \frac{1}{t_{RC(MIN)}} \text{ Hz.}$$

The specified value applies with the outputs

4. This parameter guaranteed but not tested.
5. Test conditions as specified with output loading as shown in Fig. 1 & 2 unless otherwise noted.
6. t_{HZCS} , t_{HZOE} and t_{HZWE} are specified with $C_L = 5pF$ as in Fig. 2. Transition is measured ± 200 mV typical from steady state voltage, allowing for actual tester RC time constant.

7. At any given temperature and voltage condition,

t_{HZCS} , is less than t_{LZCS} , and t_{HZWE} is less than t_{LZWE} .

8. $WE\backslash$ is HIGH for READ cycle.

9. Device is continuously selected. Chip selects and output enable are held in their active state.

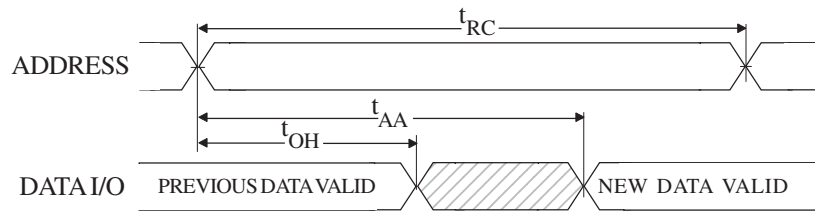
10. Address valid prior to or coincident with latest occurring chip enable.

11. t_{RC} = READ cycle time.

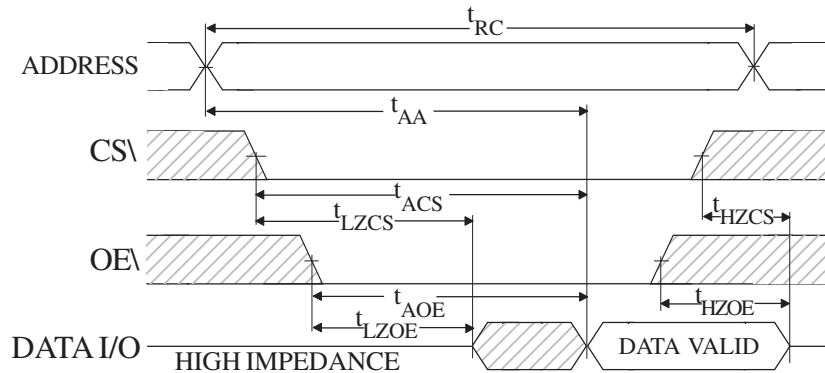
12. Chip enable ($CS\backslash$) and write enable ($WE\backslash$) can initiate and terminate a WRITE cycle.

13. I_{CC} is for full 32 bit mode.

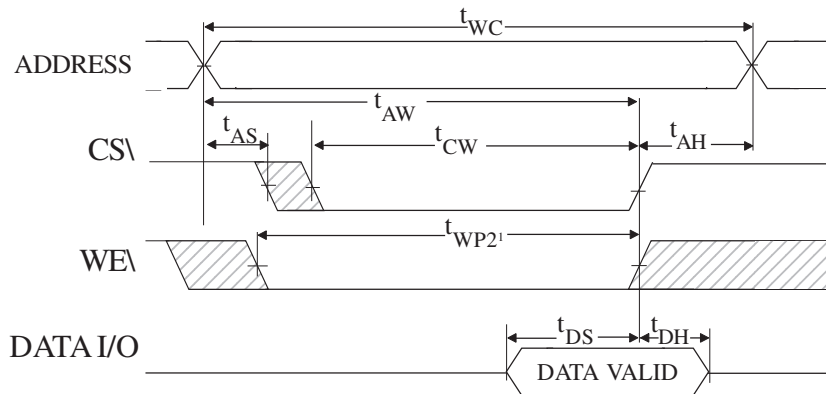
READ CYCLE NO. 1



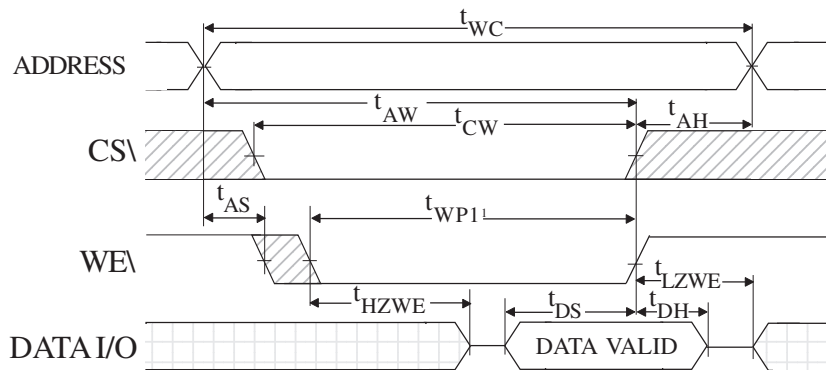
READ CYCLE NO. 2



WRITE CYCLE NO. 1
(Chip Select Controlled)



WRITE CYCLE NO. 2
(Write Enable Controlled)

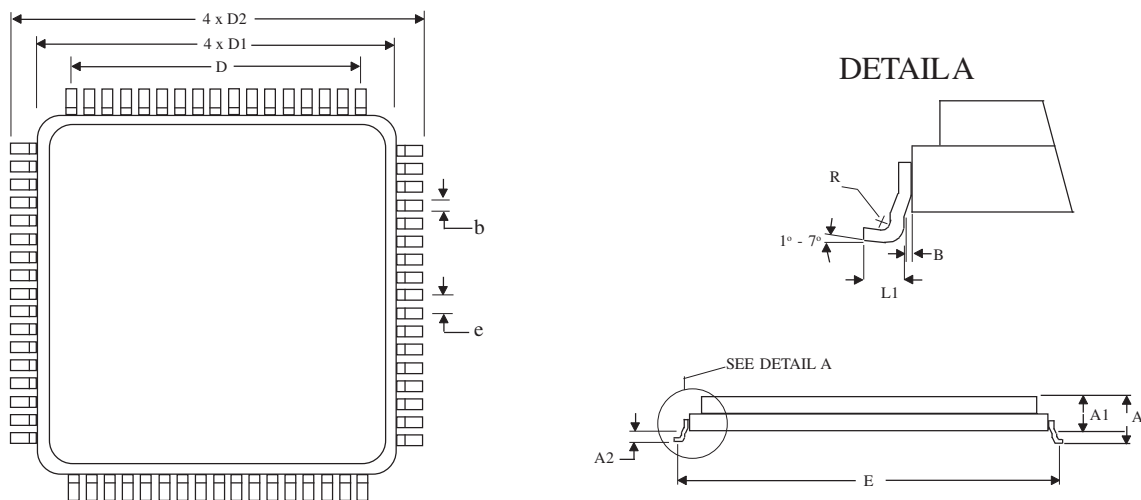


NOTES

1. All voltages referenced to V_{SS} (GND).

MECHANICAL DEFINITIONS*

ASI Case #702 (Package Designator Q)

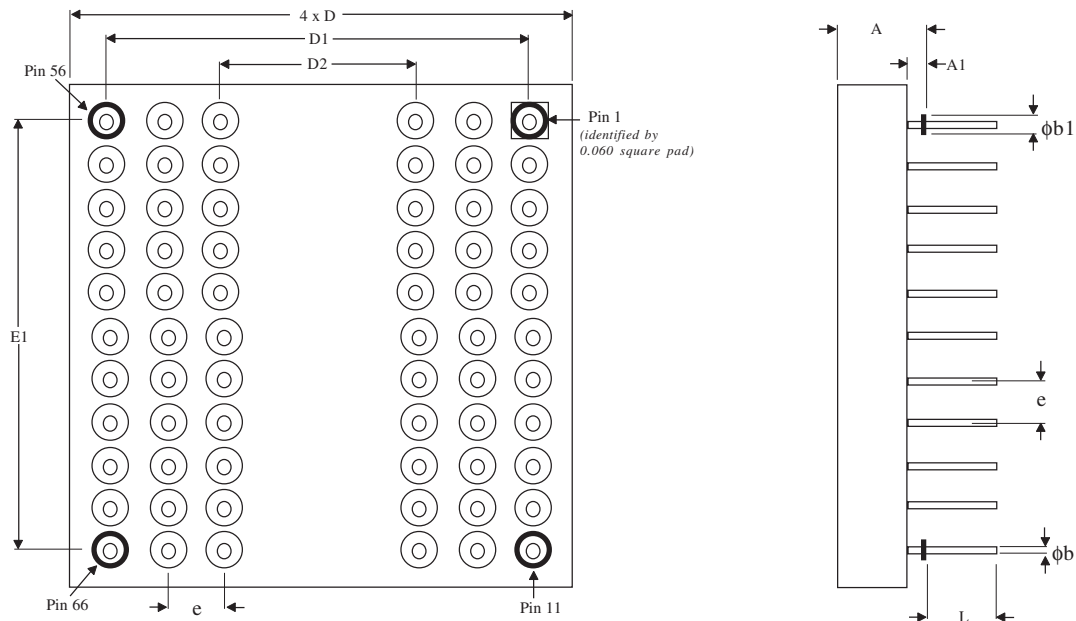


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.123	0.196
A1	0.118	0.186
A2	0.000	0.020
B	0.010 REF	
b	0.013	0.017
D	0.800 BSC	
D1	0.870	0.890
D2	0.980	1.000
E	0.936	0.956
e	0.050 BSC	
R	0.005	---
L1	0.035	0.045

*All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case #904 (Package Designator P)

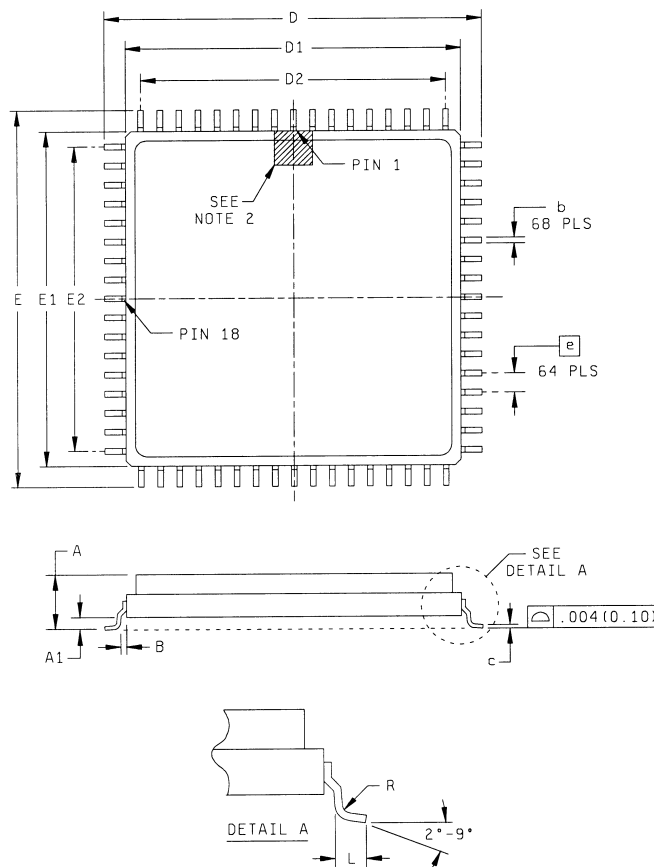


SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	0.144	0.181
A1	0.025	0.035
ϕb	0.016	0.020
$\phi b1$	0.045	0.055
D	1.065	1.085
D1/E1	1.000 TYP	
D2	0.600 TYP	
e	0.100 TYP	
L	0.145	0.155

*All measurements are in inches.

MECHANICAL DEFINITIONS*

ASI Case (Package Designator Q1) Case Outline A



SYMBOL	SMD SPECIFICATIONS	
	MIN	MAX
A	---	0.196
A1	0.054	---
b	0.013	0.017
B	0.010 TYP	
c	0.009	0.012
D/E	0.980	1.000
D1/E1	0.870	0.890
D2/E2	0.800 BSC	
e	0.050 BSC	
L	0.035	0.045
R	0.010 TYP	

*All measurements are in inches.

ORDERING INFORMATION

EXAMPLE: AS8SLC512K32Q-17L/XT				
Device Number	Package Type	Speed ns	Options	Process
AS8SLC512K32	Q	-10	L	/*
AS8SLC512K32	Q	-12	L	/*
AS8SLC512K32	Q	-15	L	/*
AS8SLC512K32	Q	-17	L	/*
AS8SLC512K32	Q	-20	L	/*
EXAMPLE: AS8SLC512K32P-12/IT				
Device Number	Package Type	Speed ns	Options	Process
AS8SLC512K32	P	-10	L	/*
AS8SLC512K32	P	-12	L	/*
AS8SLC512K32	P	-15	L	/*
AS8SLC512K32	P	-17	L	/*
AS8SLC512K32	P	-20	L	/*
EXAMPLE: AS8SLC512K32Q1-12/XT				
Device Number	Package Type	Speed ns	Options	Process
AS8SLC512K32	Q1	-10	L	/*
AS8SLC512K32	Q1	-12	L	/*
AS8SLC512K32	Q1	-15	L	/*
AS8SLC512K32	Q1	-17	L	/*
AS8SLC512K32	Q1	-20	L	/*

*AVAILABLE PROCESSES

XT = Extended Temperature Rang

-55°C to +125°C

IT = Industrial Temperature Range

-40°C to +85°C

883C = Military Processing

-55°C to +125°C

OPTION DEFINITIONS

L = 2V data retention/low power



Austin Semiconductor, Inc.

SRAM
AS8SLC512K32

DOCUMENT TITLE

512K x 32 SRAM SRAM Memory Array MCM

REVISION HISTORY

<u>Rev #</u>	<u>History</u>	<u>Release Date</u>	<u>Status</u>
2.5	Updated Q & Q1 Package Specs Page 8 & 10	May 2009	Release