LMR36015 4.2-V to 60-V, 1.5-A Synchronous Step-Down Converter in HotRod™ Package

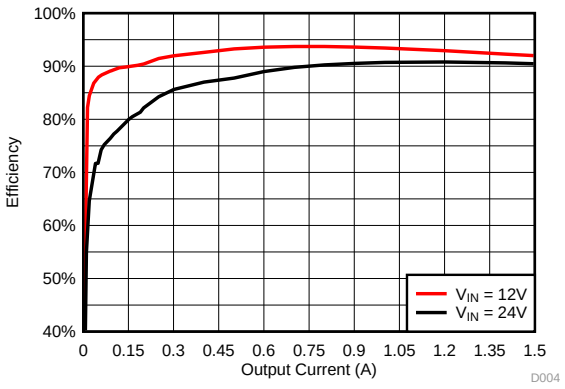
1 Features

- Designed for Reliable and Rugged Applications
  - Input Transient Protection up to 66 V
  - Junction Temperature Range –40°C to +150°C
  - Protection Features Like Thermal Shutdown, Input Undervoltage Lockout, Cycle-by-Cycle Current Limit, Hiccup Short-Circuit Protection
- Suited for Scalable Industrial Power Supplies
  - Pin Compatible With LMR36006 (60 V, 0.6 A) and LMR33620/30 (36 V, 2 A / 3 A)
  - 400-kHz, 1-MHz Frequency Options Available
- Integration Reduces Solution Size and Cost
  - Small, 3-mm × 2-mm HotRod™ Package
  - Few External Components with Integrated Rectification and Internal Compensation
- Low Power Dissipation Across Load Spectrum
  - 93% Efficiency at 400kHz (12 V_{IN}, 5 V_{OUT}, 1 A)
  - Increased Light Load Efficiency with Automatic Transition into PFM
  - Low Shutdown Quiescent Current of 3 µA
  - Low Operating Quiescent Current of 23 µA
- AEC-Q100 version available in 400 kHz and 2.1 MHz — contact TI for details
- Create a Custom Design Using the LMR36015 with the WEBENCH® Power Designer

2 Applications

- Field Transmitters, Machine Vision, PLC Modules
- Thermostats, Video Doorbells, HVAC Systems
- AC and Servo Drives, Rotary Encoders
- General-Purpose Wide Input Voltage Regulators

Efficiency vs Output Current
V_{OUT} = 5 V, 400 kHz



3 Description

The LMR36015 regulator is an easy-to-use, synchronous, step-down DC/DC converter. With integrated high-side and low-side power MOSFETs, up to 1.5 A of output current can be delivered over a wide input voltage range of 60 V, with transient tolerance up to 66 V. The transient tolerance reduces the necessary design effort to protect against overvoltages and meets the surge immunity requirements of IEC 61000-4-5.

The LMR36015 employs peak-current-mode control to provide optimal efficiency and output voltage accuracy. Load transient performance is improved with FPWM feature in the 1-MHz regulator. Precision enable provides flexibility by enabling a direct connection to the wide input voltage or precise control over device start-up and shutdown. The power-good flag, with built-in filtering and delay, offers a true indication of system status, and negates the requirement for an external supervisor.

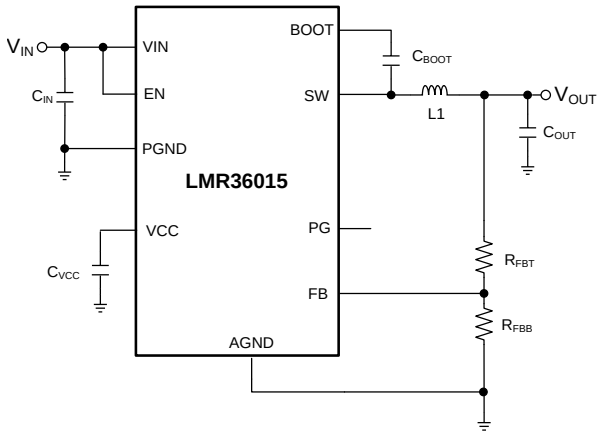
The device requires few external components and has a pinout designed for simple PCB layout. The small solution size and feature set of the LMR36015 is designed to simplify implementation for a wide range of end equipment, including space critical applications of ultra-small field transmitters and vision sensors.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LMR36015	VQFN-HR (12)	3.00 mm × 2.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



ADVANCE INFORMATION

Table of Contents

ADVANCE INFORMATION

4 Revision History

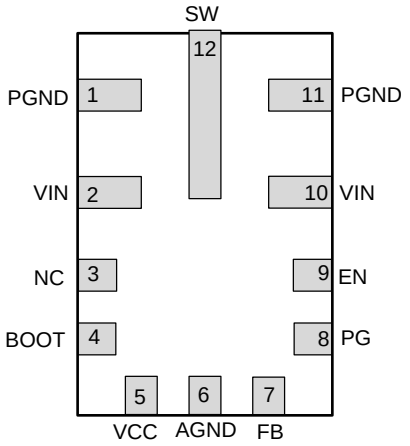
DATE	REVISION	NOTES
April 2018	*	Initial release

5 Device Comparison Table

ORDERABLE PART NUMBER	OUTPUT VOLTAGE	FPWM	F_{SW}	PACKAGE QTY
PLMR36015ARNXT	Adjustable	No	400 kHz	250
PLMR36015ARNXR	Adjustable	No	400 kHz	Contact TI for samples
PLMR36015FBRNXT	Adjustable	Yes	1 MHz	Contact TI for samples
PLMR36015FBRNXR	Adjustable	Yes	1 MHz	Contact TI for samples

6 Pin Configuration and Functions

RNX Package
12-Pin VQFN-HR
Top View



Pin Functions

NO.	NAME	TYPE	DESCRIPTION
1, 11	PGND	G	Power ground terminal. Connect to system ground and AGND. Connect to C_{IN} with short wide traces.
2, 10	VIN	P	Input supply to regulator. Connect a high-quality bypass capacitor(s) directly to this pin and PGND.
3	NC	—	Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin. This pin has no internal connection to the regulator.
4	BOOT	P	Boot-strap supply voltage for internal high-side driver. Connect a high-quality 100-nF capacitor from this pin to the SW pin. Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
5	VCC	P	Internal 5-V LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
6	AGND	G	Analog ground for regulator and system. Ground reference for internal references and logic. All electrical parameters are measured with respect to this pin. Connect to system ground on PCB.
7	FB	A	Feedback input to regulator. Connect to tap point of feedback voltage divider. DO NOT FLOAT. DO NOT GROUND.
8	PG	A	Open drain power-good flag output. Connect to suitable voltage supply through a current limiting resistor. High = power OK, low = power bad. Goes low when EN = Low. Can be open or grounded when not used.
9	EN	A	Enable input to regulator. High = ON, low = OFF. Can be connected directly to VIN; DO NOT FLOAT.
12	SW	P	Regulator switch node. Connect to power inductor. Connect the SW pin to NC on the PCB. This simplifies the connection from the C_{BOOT} capacitor to the SW pin.
A = Analog, P = Power, G = Ground			

ADVANCE INFORMATION

7 Specifications

7.1 Absolute Maximum Ratings

Over recommended operating junction temperature range of -40°C to 150°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	–0.3	66	V
	EN to AGND	–0.3	V_{IN} + 0.3	
	FB to AGND	–0.3	5.5	
	PG to AGND	–0.3	22	
	AGND to PGND	–0.3	0.3	
Output voltage	SW to PGND	–0.3	V_{IN} + 0.3	V
	SW to PGND less than 10-ns transients	–3.5	V_{IN} + 0.3	
	CBOOT to SW	–0.3	5.5	
	VCC to AGND	–0.3	5.5	
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40 ℃ to 150 ℃ (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	VIN to PGND	4.2	60	V
	EN to PGND(2)	0	V_{IN}	
	PG to PGND(2)	0	18	
Output voltage	V_{OUT} (3) (4)	1	28	V
Output current	I_{OUT}	0	1.5	A
Operating junction temperature, T_J (5)		–40	150	℃

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see *Electrical Characteristics.*
(2) The voltage on this pin must not exceed the voltage on the VIN pin by more than 0.3 V.
(3) Under no conditions should the output voltage be allowed to fall below zero volts.
(4) Maximum V_{OUT} ensured up to 90% of V_{IN} in final production.
(5) Maximum junction temperature to be ensured in final production.

ADVANCE INFORMATION

7.4 Thermal Information

THERMAL METRIC(1)		LMR36015 RNX (VQFN-HR) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	76.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.6	°C/W
$R_{\theta JC}$ (bottom)	Junction-to-case (bottom) thermal resistance	0.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	15.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
$I_{Q\text{-}nonSW}$	Operating quiescent current (non-switching)(2)	V_{EN} = 3.3 V	21	23	36	µA
I_{SD}	Shutdown quiescent current; measured at VIN pin	V_{EN} = 0 V		3	10	µA
ENABLE (EN PIN)						
$V_{EN\text{-}VCC\text{-}H}$	Enable input high level for V_{CC} output	V_{ENABLE} rising			1.14	V
$V_{EN\text{-}VCC\text{-}L}$	Enable input low level for V_{CC} output	V_{ENABLE} falling	0.3			V
$V_{EN\text{-}VOUT\text{-}H}$	Enable input high level for V_{OUT}	V_{ENABLE} rising	1.157	1.231	1.3	V
$V_{EN\text{-}VOUT\text{-}HYS}$	Enable input hysteresis for V_{OUT}	Hysteresis below $V_{ENABLE\text{-}H}$; falling		110		mV
$I_{LKG\text{-}EN}$	Enable input leakage current	V_{EN} = 3.3V		0.2		nA
INTERNAL LDO (VCC PIN)						
V_{CC}	Internal V_{CC} voltage	6 V ≤ V_{IN} ≤ 60 V	4.75	5	5.25	V
$V_{CC\text{-}UVLO\text{-}Rising}$	Internal V_{CC} undervoltage lockout	V_{CC} rising	3.7	3.9	4.1	V
$V_{CC\text{-}UVLO\text{-}Falling}$	Internal V_{CC} undervoltage lockout	V_{CC} falling	3.1	3.3	3.4	V
VOLTAGE REFERENCE (FB PIN)						
V_{FB}	Feedback voltage		0.985	1	1.015	V
$I_{LKG\text{-}FB}$	Feedback leakage current	FB = 1 V		0.2		nA
CURRENT LIMITS AND HICCUP						
I_{SC}	Short-circuit high-side current limit(3)		2	2.4	2.8	A
$I_{LS\text{-}LIMIT}$	Short-circuit low-side current limit(3)			1.8		A
$I_{L\text{-}ZC}$	Zero cross detector threshold			0.02		A
$I_{PEAK\text{-}MIN}$	Minimum inductor peak current(3)			0.48		A
$I_{L\text{-}NEG}$	Negative current limit(3)	FPWM variant only	–1.6	–1.2	–0.8	A

(1) MIN and MAX limits are 100% production tested at 25℃. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) The current limit values in this table are tested, open loop, in production. They may differ from those found in a closed loop application.

ADVANCE INFORMATION

Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD (PGOOD PIN)						
$V_{PG-HIGH-UP}$	Power-Good upper threshold - rising	% of FB voltage	105%	107%	110%	
$V_{PG-LOW-DN}$	Power-Good lower threshold - falling	% of FB voltage	90%	93%	95%	
V_{PG-HYS}	Power-Good hysteresis (rising & falling)	% of FB voltage		2%		
T_{PG}	Power-Good rising/falling edge deglitch delay		80		200	µs
$V_{PG-VALID}$	Minimum input voltage for proper Power-Good function				2	V
R_{PG}	Power-Good on-resistance	V_{EN} = 2.5 V		80	165	Ω
R_{PG}	Power-Good on-resistance	V_{EN} = 0 V		35	90	Ω
OSCILLATOR						
F_{OSC}	Internal oscillator frequency	1-MHz variant	0.85	1	1.15	MHz
F_{OSC}	Internal oscillator frequency	400-kHz variant	340	400	460	kHz
MOSFETS						
$R_{DS-ON-HS}$	High-side MOSFET ON-resistance	I_{OUT} = 0.5 A		225	435	mΩ
$R_{DS-ON-LS}$	Low-side MOSFET ON-resistance	I_{OUT} = 0.5 A		150	280	mΩ

7.6 Timing Requirements

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and Maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V.

		MIN	NOM	MAX	UNIT
t_{ON-MIN}	Minimum switch on-time		55	80	ns
$t_{OFF-MIN}$	Minimum switch off-time		53	73	ns
t_{ON-MAX}	Maximum switch on-time		7.5		µs
t_{SS}	Internal soft-start time	3	4.5	6	ms

ADVANCE INFORMATION

7.7 System Characteristics

The following specifications apply to a typical application circuit with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25℃ only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40℃ to 150℃. *These specifications are not ensured by production testing.*

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage range		4.2		60	V
V_{OUT}	Adjustable output voltage regulation(1)	PFM operation	–1.5%		2.5%	
V_{OUT}	Adjustable output voltage regulation(1)	FPWM operation	–1.5%		1.5%	
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 0 A, R_{FBT} = 1 MΩ, PFM variant		25		µA
D_{MAX}	Maximum switch duty cycle(2)			98%		
V_{HC}	FB pin voltage required to trip short-circuit hiccup mode			0.4		V
t_{HC}	Time between current-limit hiccup burst			94		ms
t_D	Switch voltage dead time			2		ns
T_{SD}	Thermal shutdown temperature	Shutdown temperature		170		°C
T_{SD}	Thermal shutdown temperature	Recovery temperature		158		°C

(1) Deviation in V_{OUT} from nominal output voltage value at V_{IN} = 24 V, I_{OUT} = 0 A to 1.5 A.
(2) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: F_{MIN} = 1 / (t_{ON-MAX} + $t_{OFF-MIN}$). D_{MAX} = t_{ON-MAX} /(t_{ON-MAX} + $t_{OFF-MIN}$).

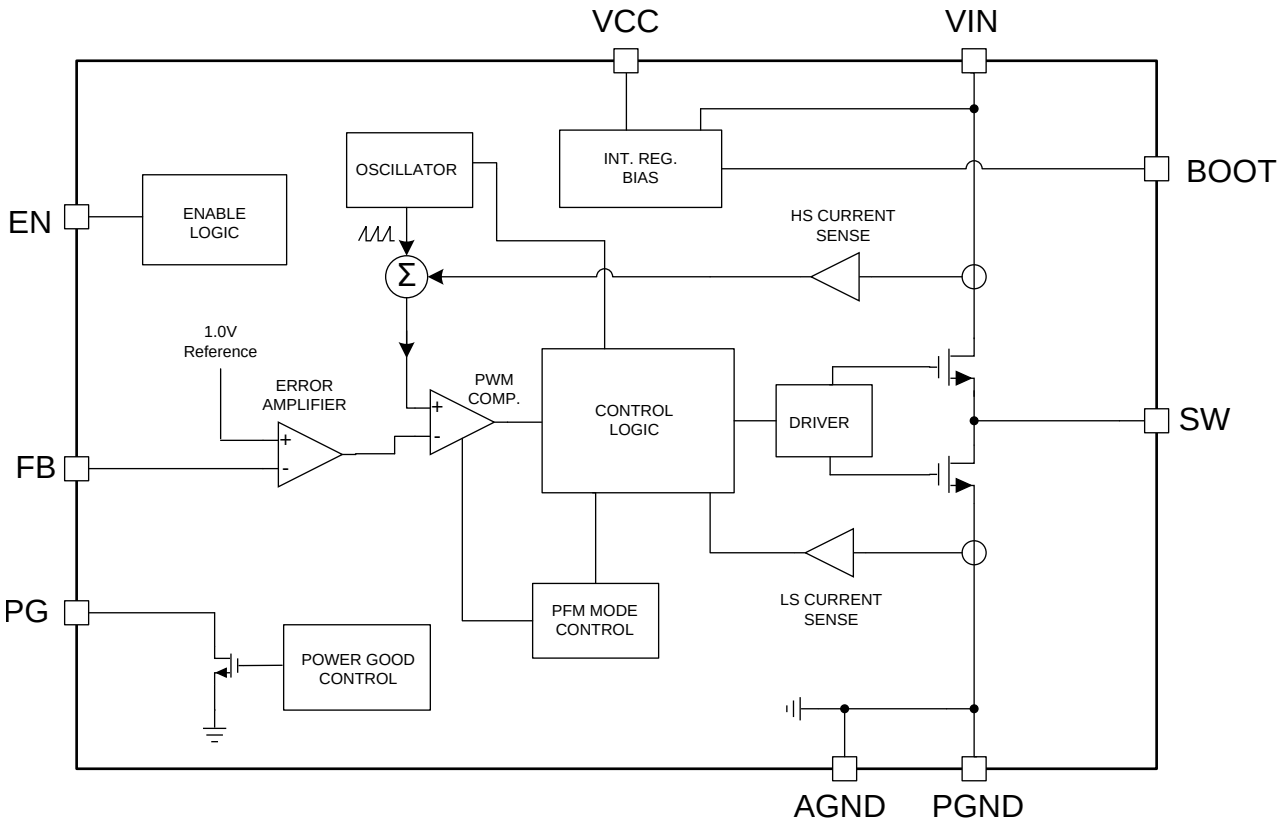
ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The LMR36015 is a synchronous peak-current-mode buck regulator designed for a wide variety of industrial applications. The regulator automatically switches modes between PFM and PWM depending on load. At heavy loads, the device operates in PWM at a constant switching frequency. At light loads the mode changes to PFM, with diode emulation allowing DCM. This reduces the input supply current and keeps efficiency high. The device features internal loop compensation which reduces design time and requires fewer external components than externally compensated regulators.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Power-Good Flag Output

The power-good flag function (PG output pin) of the LMR36015 can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output goes low under fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for short excursions of the output voltage, such as during line and load transients. The timing parameters of the glitch filter are found in the table. Output voltage excursions lasting less than t_{PG} do not trip the power-good flag. Power-good operation can best be understood by reference to Figure 1 and Figure 2. Note that during initial power-up a delay of about 4 ms (typical) is inserted from the time that EN is asserted to the time that the power-good flag goes high. This delay only occurs during start-up and is not encountered during normal operation of the power-good function.

Feature Description (continued)

The power-good output consists of an open drain NMOS; requiring an external pullup resistor to a suitable logic supply. It can also be pulled up to either VCC or V_{OUT}, through an appropriate resistor, as desired. If this function is not needed, the PG pin must be grounded. When EN is pulled low, the flag output is also forced low. With EN low, power good remains valid as long as the input voltage is ≥ 2 V (typical). Limit the current into this pin to ≤ 4 mA.

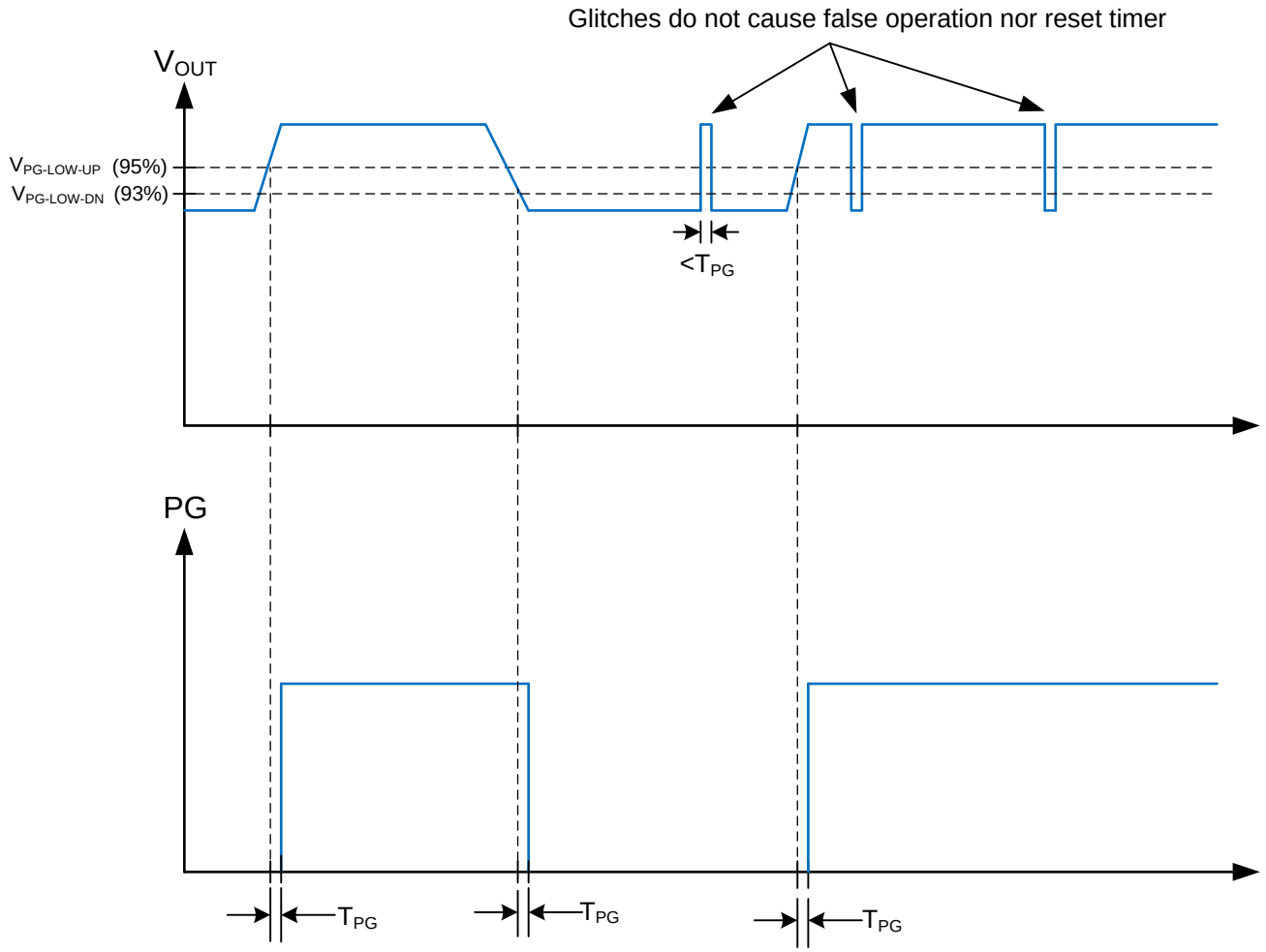


Figure 1. Static Power-Good Operation

ADVANCE INFORMATION

Feature Description (continued)

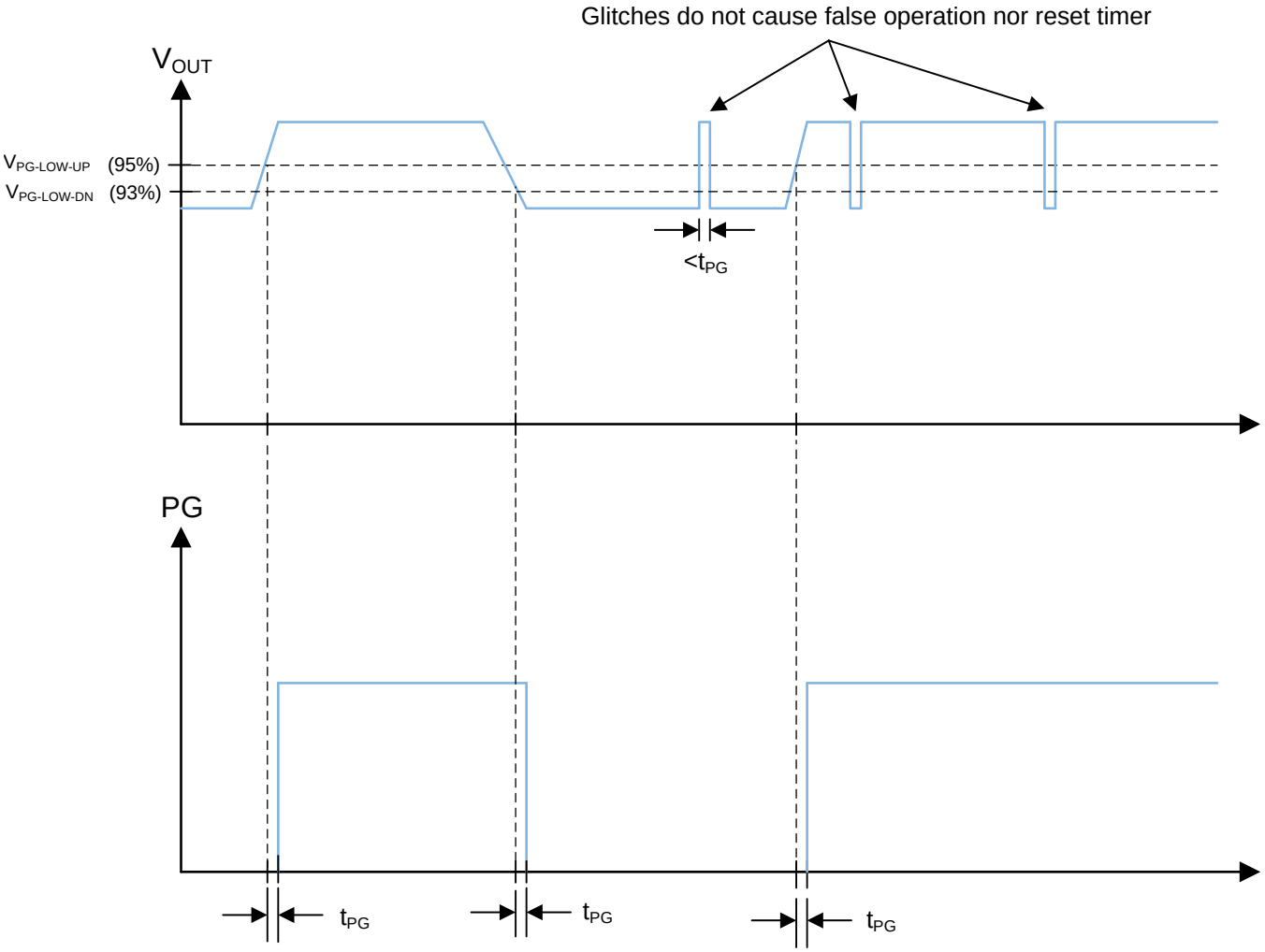


Figure 2. Power-Good-Timing Behavior

8.3.2 Enable and Start-up

Start-up and shutdown are controlled by the EN input. This input features precision thresholds, allowing the use of an external voltage divider to provide an adjustable input UVLO (see the *External UVLO* section). Applying a voltage of ≥ V_{EN-VCC_H} causes the device to enter standby mode, powering the internal VCC, but not producing an output voltage. Increasing the EN voltage to V_{EN-H} fully enables the device, allowing it to enter start-up mode and beginning the soft-start period. When the EN input is brought below V_{EN-H} by V_{EN-HYS}, the regulator stops running and enters standby mode. Further decrease in the EN voltage to below $V_{EN-VCC-L}$ completely shuts down the device. This behavior is shown in Figure 3. The EN input may be connected directly to VIN if this feature is not needed. This input must not be allowed to float. The values for the various EN thresholds can be found in the table.

The LMR36015 utilizes a reference-based soft start that prevents output voltage overshoots and large inrush currents as the regulator is starting up. A typical start-up waveform is shown in Figure 4 along with typical timings. The rise time of the output voltage is about 4 ms.

ADVANCE INFORMATION

Feature Description (continued)

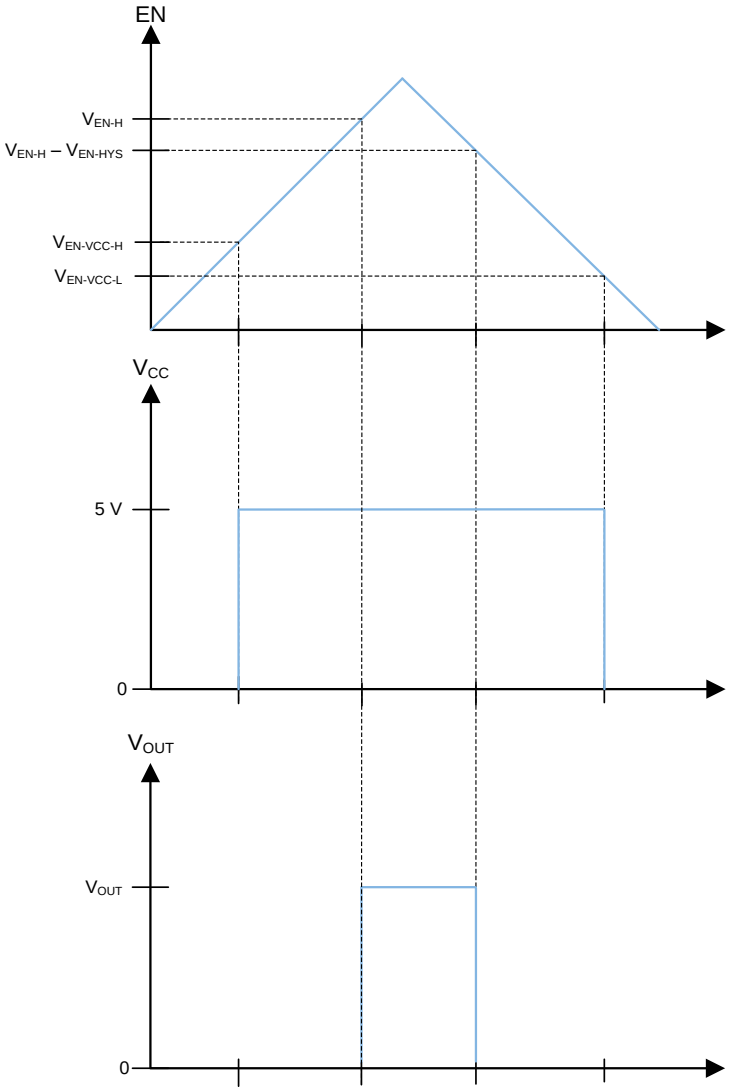


Figure 3. Precision Enable Behavior

ADVANCE INFORMATION

Feature Description (continued)

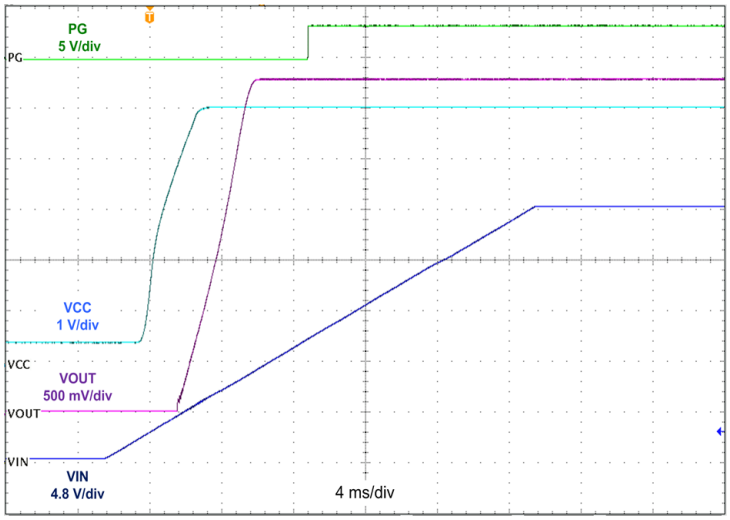


Figure 4. Typical Start-up Behavior
V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 1.5 A

8.3.3 Current Limit and Short Circuit

The LMR36015 incorporates valley current limit for normal overloads and for short-circuit protection. In addition the high-side power MOSFET is protected from excessive current by a peak current limit circuit. Cycle-by-cycle current limit is used for overloads, while hiccup mode is used for short circuits. Finally, a zero current detector is used on the low-side power MOSFET to implement DEM at light loads (see *Glossary*).

During overloads the low-side current limit, I_{LIMIT}, determines the maximum load current that the LMR36015 can supply. When the low-side switch turns on, the inductor current begins to ramp down. If the current does not fall below I_{LIMIT} before the next turnon cycle, then that cycle is skipped, and the low-side MOSFET is left on until the current falls below I_{LIMIT}. This is somewhat different than the more typical peak current limit and results in Equation 1 for the maximum load current.

$$I_{OUT}\big|_{max} = I_{LIMIT} + \frac{(V_{IN} - V_{OUT})}{2 \cdot f_{SW} \cdot L} \cdot \frac{V_{OUT}}{V_{IN}} \quad (1)$$

where

- f_{SW} = switching frequency
- L = inductor value

If, during current limit, the voltage on the FB input falls below about 0.4 V due to a short circuit, the device enters into hiccup mode. In this mode the device stops switching for t_{HC}

The high-side-current limit trips when the peak inductor current reaches I_{SC}. This is a cycle-by-cycle current limit and does not produce any frequency or load current fold back. It is meant to protect the high-side MOSFET from excessive current. Under some conditions, such as high input voltages, this current limit may trip before the low-side protection. Under this condition, I_{SC} determines the maximum output current. Note that I_{SC} varies with duty cycle.

ADVANCE INFORMATION

Feature Description (continued)

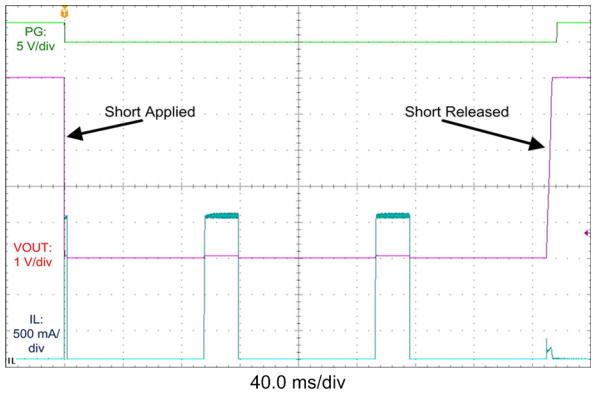


Figure 5. Short-Circuit Transient and Recovery

8.3.4 Undervoltage Lockout and Thermal Shutdown

The LMR36015 incorporates an undervoltage-lockout feature on the output of the internal LDO (at the VCC pin). When VCC reaches about 3.7 V the device is ready to receive an EN signal and start up. When VCC falls below about 3 V, the device shuts down, regardless of EN status. Because the LDO is in dropout during these transitions, the previously mentioned values roughly represent the input voltage levels during the transitions.

Thermal shutdown is provided to protect the regulator from excessive junction temperature. When the junction temperature reaches about 165°C the device shuts down; re-start occurs when the temperature falls to about 148°C .

8.4 Device Functional Modes

8.4.1 Auto Mode

In auto mode the device moves between PWM and PFM as the load changes. At light loads the regulator operates in PFM. At higher loads the mode changes to PWM.

In PWM the regulator operates as a constant frequency, current mode, full synchronous converter using PWM to regulate the output voltage. While operating in this mode the output voltage is regulated by switching at a constant frequency and modulating the duty cycle to control the power to the load. This provides excellent line and load regulation and low output voltage ripple.

In PFM the high-side MOSFET is turned on in a burst of one or more pulses to provide energy to the load. The duration of the burst depends on how long it takes the inductor current to reach $I_{PEAK-MIN}$. The frequency of these bursts is adjusted to regulate the output, while diode emulation (DEM) is used to maximize efficiency (see *Glossary*). This mode provides high light-load efficiency by reducing the amount of input supply current required to regulate the output voltage at small loads. This trades off very good light-load efficiency for larger output voltage ripple and variable switching frequency. Also, a small increase in output voltage occurs at light loads. The actual switching frequency and output voltage ripple depends on the input voltage, output voltage, and load. Typical switching waveforms in PFM and PWM are shown in Figure 6 and Figure 7. See the *Application Curves* for output voltage variation with load in Auto mode.

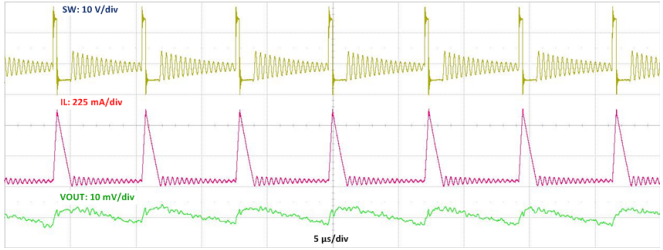


Figure 6. Typical PFM Switching Waveforms
V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 200 mA

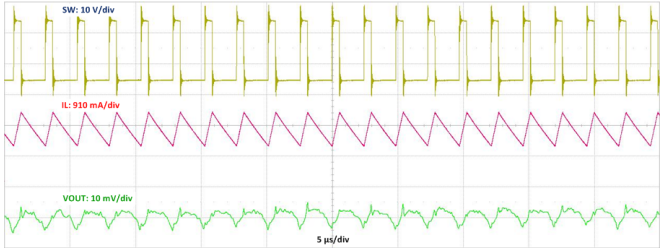


Figure 7. Typical PWM Switching Waveforms
V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 1.5 A, f_S = 400 kHz

ADVANCE INFORMATION

Device Functional Modes (continued)

8.4.2 Dropout

The dropout performance of any buck regulator is affected by the R_{DSON} of the power MOSFETs, the DC resistance of the inductor, and the maximum duty cycle that the controller can achieve. As the input voltage is reduced to near the output voltage, the off-time of the high-side MOSFET starts to approach the minimum value. Beyond this point the switching may become erratic and/or the output voltage will fall out of regulation. To avoid this problem the LMR36015 automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation. In this data sheet the dropout voltage is defined as the difference between the input and output voltage when the output has dropped by 1% of its nominal value. Under this condition the switching frequency has dropped to its minimum value of about 140 kHz. Typical dropout characteristics can be found in Figure 8.

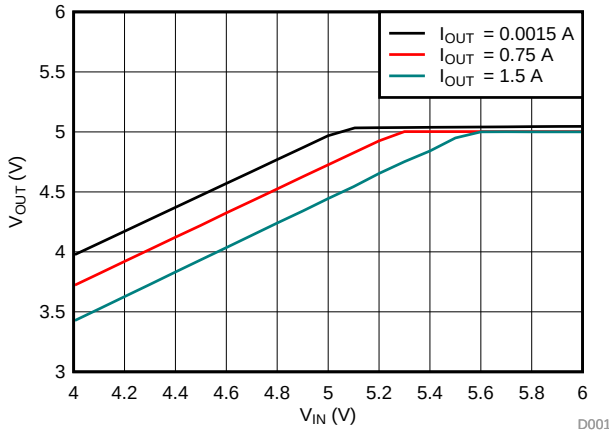


Figure 8. Overall Dropout Characteristic
V_{OUT} = 5 V

8.4.3 Minimum Switch On-Time

Every switching regulator has a minimum controllable on-time dictated by the inherent delays and blanking times associated with the control circuits. This imposes a minimum switch duty cycle and therefore a minimum conversion ratio. The constraint is encountered at high input voltages and low output voltages. To help extend the minimum controllable duty cycle, the LMR36015 automatically reduces the switching frequency when the minimum on-time limit is reached. In this way the converter can regulate the lowest programmable output voltage at the maximum input voltage. An estimate for the approximate input voltage, for a given output voltage, before frequency fold-back occurs is found in Equation 2. As the input voltage is increased, the switch on-time (duty cycle) reduces to regulate the output voltage. When the on-time reaches the limit, the switching frequency drops, while the on-time remains fixed.

$$V_{IN} \leq \frac{V_{OUT}}{t_{ON} \cdot f_{SW}} \quad (2)$$

ADVANCE INFORMATION

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

NOTE

All of the capacitance values given in the following application information refer to *effective* values; unless otherwise stated. The *effective* value is defined as the actual capacitance under D.C. bias and temperature; not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X5R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under D.C. bias the capacitance drops considerably. Large case sizes and/or higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank should be made in order to ensure that the minimum value of *effective* capacitance is provided.

9.1 Application Information

The LMR36015 step-down DC-to-DC converter is typically used to convert a higher DC voltage to a lower DC voltage with a maximum output current of 1.5 A. The following design procedure can be used to select components for the LMR36015. Alternately, the WEBENCH® Design Tool may be used to generate a complete design. This tool utilizes an iterative design procedure and has access to a comprehensive database of components. This allows the tool to create an optimized design and allows the user to experiment with various options.

ADVANCE INFORMATION

9.2 Typical Application

Figure 9 shows a typical application circuit for the LMR36015. This device is designed to function over a wide range of external components and system parameters. However, the internal compensation is optimized for a certain range of external inductance and output capacitance. As a quick start guide, *Table 1* provides typical component values for a range of the most common output voltages.

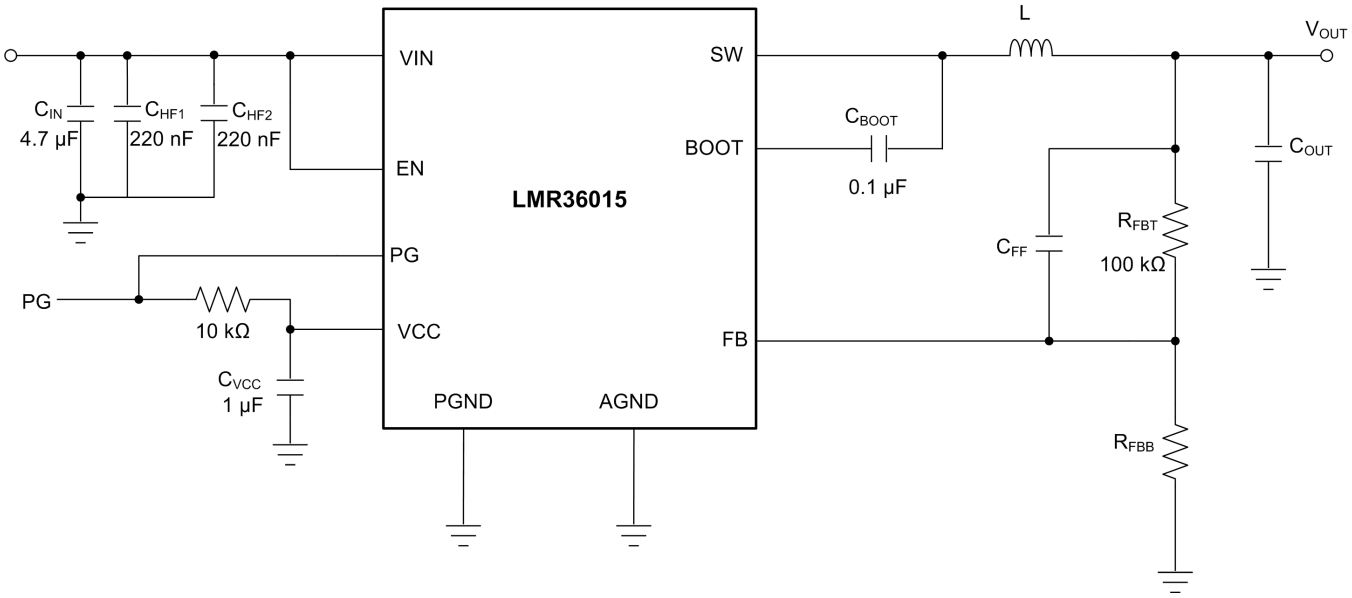


Figure 9. Example Application Circuit

Table 1. Typical External Component Values

f_{SW} (kHz)	V_{OUT} (V)	L (µH)	C_{OUT} (rated capacitance)	R_{FBT} (Ω)	R_{FBB} (Ω)	C_{IN}	C_{BOOT}	C_{VCC}	C_{FF}
400	3.3	18	2 × 47 µF	100 k	43.2 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	20 pF
1000	3.3	6.8	3 × 22 µF	100 k	43.2 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	20 pF
400	5	27	3 × 22 µF	100 k	24.9 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	20 pF
1000	5	10	2 × 22 µF	100 k	24.9 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	20 pF
400	12	56	3 × 22 µF	100 k	9.09 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	20 pF
1000	12	22	4 × 10 µF	100 k	9.09 k	4.7 µF + 2 × 220 nF	100 nF	1 µF	20 pF

9.2.1 Design Requirements

The following provides a detailed design procedure based on Table 2.

Table 2. Detailed Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage	24 V (6 V to 60 V)
Output voltage	5 V
Maximum output current	0 A to 1.5 A
Switching frequency	400 kHz

ADVANCE INFORMATION

9.2.2 Detailed Design Procedure

The following design procedure applies to Figure 9 and Table 2.

9.2.2.1 Custom Design With WEBENCH Tools

Click here to create a custom design using the LMR36015 device and the WEBENCH Power Designer.

1. Start by entering the input voltage, output voltage, and output current requirements
2. Optimize the design for key performance such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases the following features are available with this tool:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to help understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print full design reports in PDF.

Get more information at ti.com

9.2.2.2 Choosing the Switching Frequency

The choice of switching frequency is a compromise between conversion efficiency and overall solution size. Lower switching frequency implies reduced switching losses and usually results in higher system efficiency. However, higher switching frequency allows the use of smaller inductors and output capacitors, and hence a more compact design. For this example 400 kHz is used.

9.2.2.3 Setting the Output Voltage

The output voltage of LMR36015 is externally adjustable using a resistor divider network. The range of recommended output voltage is found in the table. The divider network is comprised of R_{FBT} and R_{FBB}, and closes the loop between the output voltage and the converter. The converter regulates the output voltage by holding the voltage on the FB pin equal to the internal reference voltage, V_{REF}. The resistance of the divider is a compromise between excessive noise pick-up and excessive loading of the output. Smaller values of resistance reduce noise sensitivity but also reduce the light-load efficiency. The recommended value for R_{FBT} is 100 kΩ; with a maximum value of 1 MΩ. If a 1 MΩ is selected for R_{FBT}, then a feed-forward capacitor must be used across this resistor to provide adequate loop phase margin (see *C_{FF} Selection*). Once R_{FBT} is selected, Equation 3 is used to select R_{FBB}. V_{REF} is nominally 1 V.

$$R_{FBB} = \frac{R_{FBT}}{\left[\frac{V_{OUT}}{V_{REF}} - 1\right]} \quad (3)$$

For this 5-V example values are: R_{FBT} = 100 kΩ and R_{FBB} = 24.9 kΩ.

ADVANCE INFORMATION

9.2.2.4 Inductor Selection

The parameters for selecting the inductor are the inductance and saturation current. The inductance is based on the desired peak-to-peak ripple current and is normally chosen to be in the range of 20% to 40% of the maximum output current. Experience shows that the best value for inductor ripple current is 30% of the maximum load current. Note that when selecting the ripple current for applications with much smaller maximum load than the maximum available from the device, use the the maximum device current. Equation 4 can be used to determine the value of inductance. The constant K is the percentage of inductor current ripple. For this example we choose K = 0.4 and find an inductance L = 16 µH; we select the next standard value of 10 µH.

$$L = \frac{(V_{IN} - V_{OUT})}{f_{SW} \cdot K \cdot I_{OUT\,max}} \cdot \frac{V_{OUT}}{V_{IN}} \tag{4}$$

Ideally, the saturation current rating of the inductor is at least as large as the high-side switch current limit, I_{SC}. This ensures that the inductor does not saturate even during a short circuit on the output. When the inductor core material saturates, the inductance falls to a very low value, causing the inductor current to rise very rapidly. Although the valley current limit, I_{LIMIT}, is designed to reduce the risk of current runaway, a saturated inductor can cause the current to rise to high values very rapidly. This may lead to component damage; do not allow the inductor to saturate! Inductors with a ferrite core material have very *hard* saturation characteristics, but usually have lower core losses than powdered iron cores. Powered iron cores exhibit a *soft* saturation, allowing some relaxation in the current rating of the inductor. However, they have more core losses at frequencies above about 1 MHz. In any case, the inductor saturation current must not be less than the device low-side current limit, I_{LIMIT}. In order to avoid sub-harmonic oscillation, the inductance value must not be less than that given in Equation 5:

$$L_{MIN} \geq 0.28 \cdot \frac{V_{OUT}}{f_{SW}} \tag{5}$$

9.2.2.5 Output Capacitor Selection

The value of the output capacitor, and its ESR, determine the output voltage ripple and load transient performance. The output capacitor bank is usually limited by the load transient requirements, rather than the output voltage ripple. can be used to estimate a lower bound on the total output capacitance, and an upper bound on the ESR, required to meet a specified load transient.

$$C_{OUT} \geq \frac{\Delta I_{OUT}}{f_{SW} \cdot \Delta V_{OUT} \cdot K} \cdot \left[(1-D) \cdot (1+K) + \frac{K^2}{12} \cdot (2-D) \right]$$

$$ESR \leq \frac{(2+K) \cdot \Delta V_{OUT}}{2 \cdot \Delta I_{OUT} \left[1+K+\frac{K^2}{12} \cdot \left(1+\frac{1}{(1-D)} \right) \right]}$$

$$D = \frac{V_{OUT}}{V_{IN}}$$

where

- ΔV_{OUT} = output voltage transient
- ΔI_{OUT} = output current transient
- K = Ripple factor from *Inductor Selection* (6)

Once the output capacitor and ESR have been calculated, Equation 7 can be used to check the output voltage ripple.

$$V_r \cong \Delta I_L \cdot \sqrt{ESR^2 + \frac{1}{(8 \cdot f_{SW} \cdot C_{OUT})^2}}$$

where

- V_r = peak-to-peak output voltage ripple (7)

The output capacitor and ESR can then be adjusted to meet both the load transient and output ripple requirements.

In practice the output capacitor has the most influence on the transient response and loop phase margin. Load transient testing and Bode plots are the best way to validate any given design and must always be completed before the application goes into production. In addition to the required output capacitance, a small ceramic placed on the output can help to reduce high frequency noise. Small case size ceramic capacitors in the range of 1 nF to 100 nF can be very helpful in reducing spikes on the output caused by inductor and board parasitics.

Limit the maximum value of total output capacitance to about 10 times the design value, or 1000 µF, whichever is smaller. Large values of output capacitance can adversely affect the start-up behavior of the regulator as well as the loop stability. If values larger than noted here must be used, then a careful study of start-up at full load and loop stability must be performed.

9.2.2.6 Input Capacitor Selection

The ceramic input capacitors provide a low impedance source to the regulator in addition to supplying the ripple current and isolating switching noise from other circuits. A minimum ceramic capacitance of 4.7-µF is required on the input of the LMR36015. This must be rated for at least the maximum input voltage that the application requires; preferably twice the maximum input voltage. This capacitance can be increased to help reduce input voltage ripple and/or maintain the input voltage during load transients. In addition a small case size 220-nF ceramic capacitor must be used at the input, as close a possible to the regulator. This provides a high frequency bypass for the control circuits internal to the device. For this example a 4.7-µF, 100-V, X7R (or better) ceramic capacitor is chosen. The 220 nF must also be rated at 100-V with an X7R dielectric. The VQFN package provides two input voltage pins and two power ground pins on opposite sides of the package. This allows the input capacitors to be split, and placed optimally with respect to the internal power MOSFETs, thus improving the effectiveness of the input bypassing. In this example, place two 220-nF ceramic capacitors at each VIN-PGND location.

It is often desirable to use an electrolytic capacitor on the input in parallel with the ceramics. This is especially true if long leads/traces are used to connect the input supply to the regulator. The moderate ESR of this capacitor can help damp any ringing on the input supply caused by the long power leads. The use of this additional capacitor also helps with voltage dips caused by input supplies with unusually high impedance.

Most of the input switching current passes through the ceramic input capacitor(s). The approximate RMS value of this current can be calculated from Equation 8 and should be checked against the manufacturers' maximum ratings.

$$I_{RMS} \cong \frac{I_{OUT}}{2} \tag{8}$$

9.2.2.7 C_{BOOT}

The LMR36015 requires a bootstrap capacitor connected between the BOOT pin and the SW pin. This capacitor stores energy that is used to supply the gate drivers for the power MOSFETs. A high-quality ceramic capacitor of 100 nF and at least 16 V is required.

9.2.2.8 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-µF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see *Power-Good Flag Output*). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 5 V.

ADVANCE INFORMATION

9.2.2.9 C_{FF} Selection

In some cases a feed-forward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT}, in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help to mitigate this effect. Equation 9 can be used to estimate the value of C_{FF}. The value found with Equation 9 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The application report *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed-forward Capacitor* is helpful when experimenting with a feed-forward capacitor.

$$C_{FF} < \frac{V_{OUT} \cdot C_{OUT}}{120 \cdot R_{FBT} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (9)$$

9.2.2.9.1 External UVLO

In some cases an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in Figure 10 can be used. The input voltage at which the device turns on is designated V_{ON}; while the turnoff voltage is V_{OFF}. First a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ and then Equation 10 is used to calculate R_{ENT} and V_{OFF}.

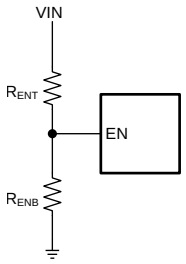


Figure 10. Set-up for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-H}} - 1 \right) \cdot R_{ENB}$$

$$V_{OFF} = V_{ON} \cdot \left(1 - \frac{V_{EN-HYS}}{V_{EN}} \right)$$

where

- $V_{ON} = V_{IN}$ turnon voltage
- $V_{OFF} = V_{IN}$ turnoff voltage (10)

ADVANCE INFORMATION

9.2.2.10 Maximum Ambient Temperature

As with any power conversion device, the LMR36015 dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the converter above ambient. The internal die temperature (T_J) is a function of the ambient temperature, the power loss and the effective thermal resistance, $R_{\theta JA}$ of the device and PCB combination. The maximum internal die temperature for the LMR36015 must be limited to 125°C. This establishes a limit on the maximum device power dissipation and therefore the load current. Equation 11 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The converter efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions can not be found in one of the curves, then interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in *Semiconductor and IC Package Thermal Metrics*, the values given in *Thermal Information* are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}\big|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \cdot \frac{\eta}{(1-\eta)} \cdot \frac{1}{V_{OUT}} \quad (11)$$

where

- η = Efficiency

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as power dissipation, air temperature/flow, PCB area, copper heat-sink area, number of thermal vias under the package, and adjacent component placement; to mention just a few. Due to the ultra-miniature size of the VQFN (RNX) package, a DAP is not available. This means that this package exhibits a somewhat greater $R_{\theta JA}$.

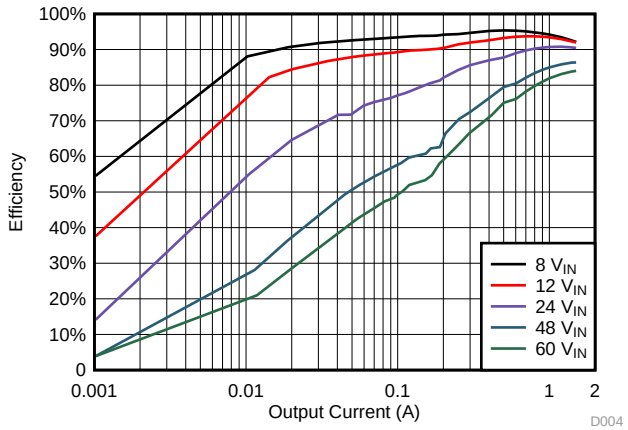
Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
- *Semiconductor and IC Package Thermal Metrics*
- *Thermal Design Made Simple with LM43603 and LM43602*
- *SLMA002 PowerPAD™ Thermally Enhanced Package*
- *PowerPAD Made Easy*
- *SBVA025 Using New Thermal Metrics*

ADVANCE INFORMATION

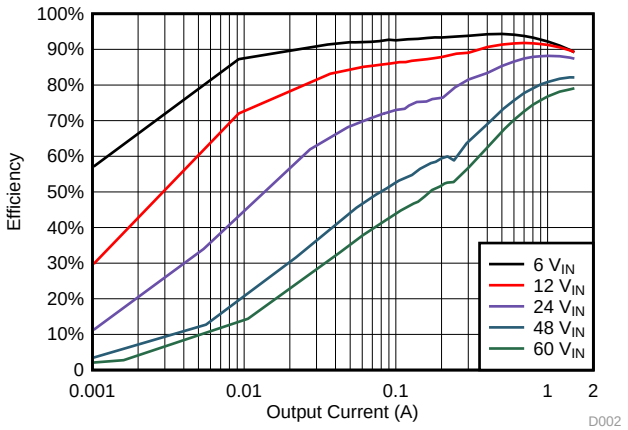
9.2.3 Application Curves

Unless otherwise specified the following conditions apply: V_{IN} = 24 V, T_A = 25°C. The circuit is shown in Figure 9, with the appropriate BOM from Table 3.



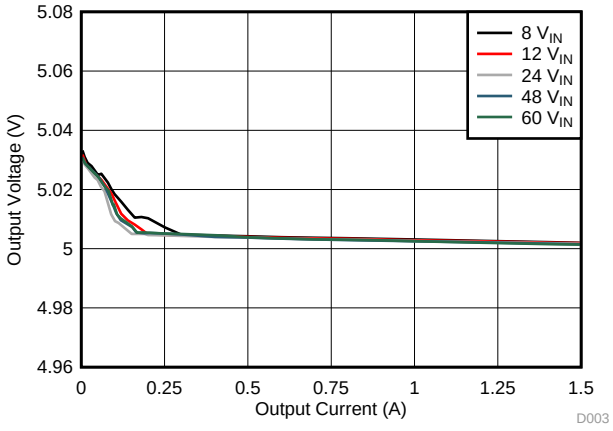
V_{OUT} = 5 V 400 kHz

Figure 11. Efficiency



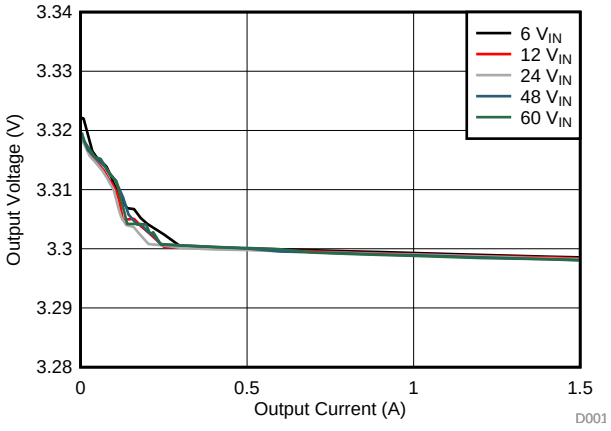
V_{OUT} = 3.3 V 400 kHz

Figure 12. Efficiency



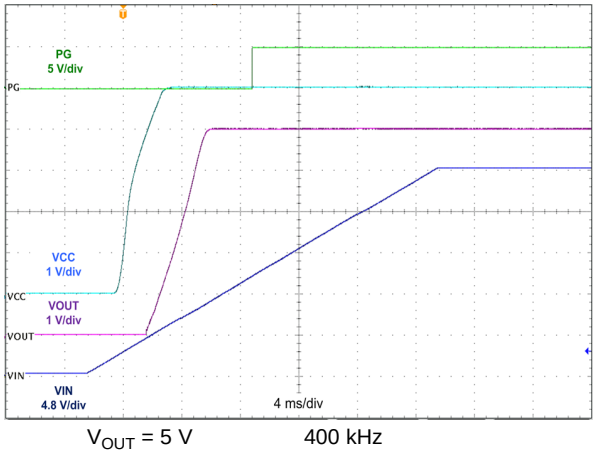
V_{OUT} = 5 V 400 kHz

Figure 13. Load Regulation



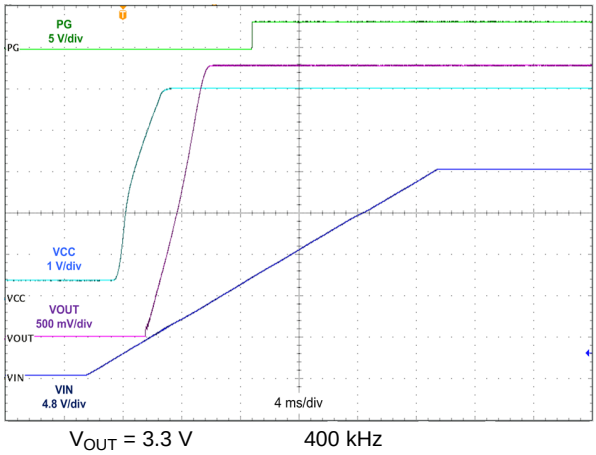
V_{OUT} = 3.3 V 400 kHz

Figure 14. Load Regulation



V_{OUT} = 5 V 400 kHz

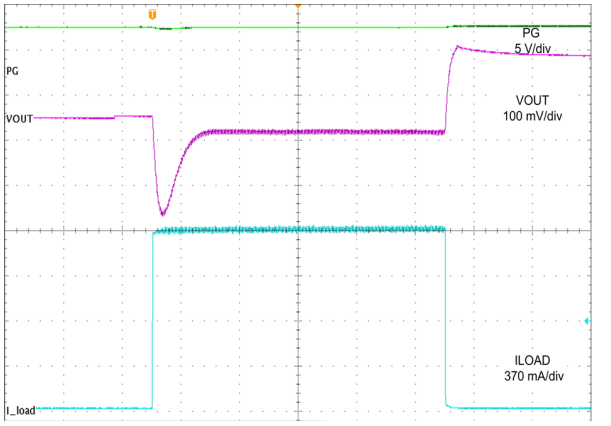
Figure 15. Start-Up Waveform



V_{OUT} = 3.3 V 400 kHz

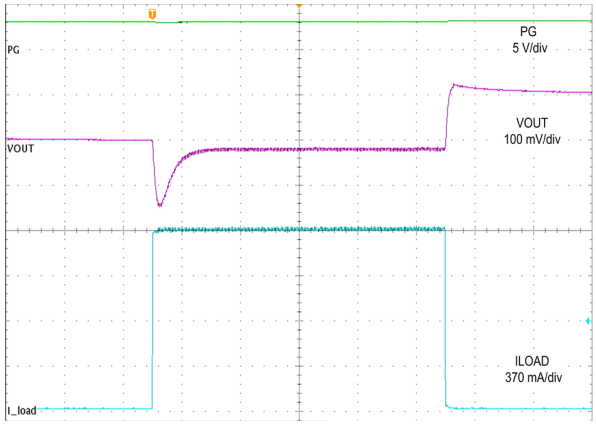
Figure 16. Start Up Waveform

Unless otherwise specified the following conditions apply: V_{IN} = 24 V, T_A = 25°C. The circuit is shown in Figure 9, with the appropriate BOM from Table 3.



V_{OUT} = 5 V 400 kHz I_{LOAD}= 0 A - 1.5 A
t_R=t_F=1µs

Figure 17. Load Transient



V_{OUT} = 3.3 V 400 kHz I_{LOAD}= 0 A - 1.5 A
t_R=t_F=1µs

Figure 18. Load Transient

Table 3. BOM for Typical Application Curves

V_{OUT}	FREQUENCY	R_{FBB}	C_{OUT}	L	U1
3.3 V	400 kHz	43.3 kΩ	4 × 22 µF	10 µH, 45 mΩ	LMR36015ARNX
5 V	400 kHz	24.9 kΩ	4 × 22 µF	10 µH, 45 mΩ	LMR36015ARNX

9.3 Do's and Don'ts

- **Don't:** Exceed the *Absolute Maximum Ratings*
- **Don't:** Exceed the *ESD Ratings*
- **Don't:** Allow the EN input to float.
- **Don't:** Allow the output voltage to exceed the input voltage, nor go below ground.
- **Don't:** Use the thermal data given in the *Thermal Information* table to design your application.
- **Do:** Follow all the guidelines and/or suggestions found in this data sheet before committing the design to production. TI application engineers are ready to help critique your design and PCB layout to help make your project a success (see *Community Resources*).

ADVANCE INFORMATION

10 Power Supply Recommendations

The characteristics of the input supply must be compatible with the and found in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator. The average input current can be estimated with Equation 12.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (12)$$

where

- η is the efficiency

If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low-ESR, ceramic input capacitors, can form an underdamped resonant circuit, resulting in overvoltage transients at the input to the regulator. The parasitic resistance can cause the voltage at the VIN pin to dip whenever a load transient is applied to the output. If the application is operating close to the minimum input voltage, this dip may cause the regulator to momentarily shutdown and/or reset. The best way to solve these kind of issues is to reduce the distance from the input supply to the regulator and/or use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of these types of capacitors help to damp the input resonant circuit and reduce any overshoots. A value in the range of 20 µF to 100 µF is usually sufficient to provide input damping and help to hold the input voltage steady during large load transients.

Sometimes, for other system considerations, an input filter is used in front of the regulator. This can lead to instability, as well as some of the effects mentioned above, unless it is designed carefully. The user guide *AN-2162 Simple Success With Conducted EMI From DCDC Converters* provides helpful suggestions when designing an input filter for any switching regulator.

In some cases a transient voltage suppressor (TVS) is used on the input of regulators. One class of this device has a *snap-back* characteristic (thyristor type). The use of a device with this type of characteristic is not recommended. When the TVS fires, the clamping voltage falls to a very low value. If this voltage is less than the output voltage of the regulator, the output capacitors discharge through the device back to the input. This uncontrolled current flow may damage the device.

ADVANCE INFORMATION

11 Layout

11.1 Layout Guidelines

The PCB layout of any DC/DC converter is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the converter regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent the EMI performance of the regulator is dependent on the PCB layout. In a buck converter the most critical PCB feature is the loop formed by the input capacitor(s) and power ground, as shown in Figure 19. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the converter. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. Figure 20 shows a recommended layout for the critical components of the LMR36015.

1. *Place the input capacitor(s) as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement.
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Use wide traces for the C_{BOOT} capacitor.* Place C_{BOOT} close to the device with short/wide traces to the BOOT and SW pins. Route the SW pin to the N/C pin and used to connect the BOOT capacitor to SW.
4. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, this latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
5. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and also act as a heat dissipation path.
6. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.
7. *Provide enough PCB area for proper heat-sinking.* As stated in the *Maximum Ambient Temperature* section, enough copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper; and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
8. *Keep switch area small.* Keep the copper area connecting the SW pin to the inductor as short and wide as possible. At the same time the total area of this node must be minimized to help reduce radiated EMI.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies*
- *Simple Switcher PCB Layout Guidelines*
- *Construction Your Power Supply- Layout Considerations*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x*

ADVANCE INFORMATION

Layout Guidelines (continued)

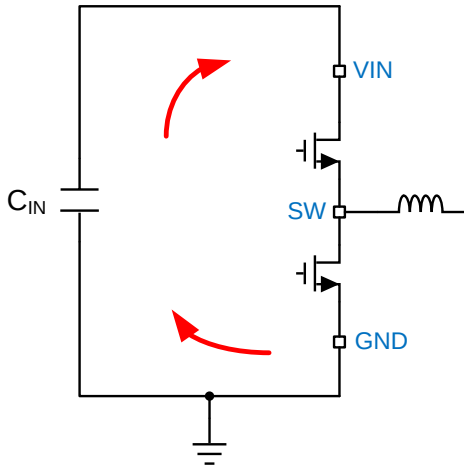


Figure 19. Current Loops with Fast Edges

11.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the AGND and PGND pins to the ground planes using vias next to the bypass capacitors. PGND pins are connected directly to the source of the low side MOSFET switch and also connected directly to the grounds of the input and output capacitors. The PGND net contains noise at the switching frequency and may bounce due to load variations. The PGND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat sinking by utilizing the thermal pad (PAD) of the device as the primary thermal path. Use a minimum 4 × 3 array of 10 mil thermal vias to connect the PAD to the system ground plane heat sink. The vias must be evenly distributed under the PAD. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

11.2 Layout Example

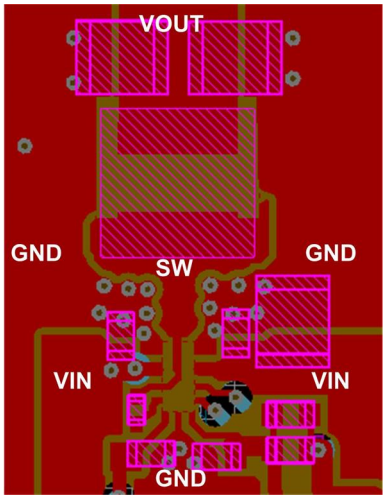


Figure 20. Example Layout

ADVANCE INFORMATION

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

12.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LMR36015 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *Thermal Design by Insight not Hindsight*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages*
- *Semiconductor and IC Package Thermal Metrics*
- *Thermal Design Made Simple with LM43603 and LM43602*
- *PowerPAD™ Thermally Enhanced Package*
- *PowerPAD Made Easy*
- *SBVA025 Using New Thermal Metrics*
- *Layout Guidelines for Switching Power Supplies*
- *Simple Switcher PCB Layout Guidelines*
- *Construction Your Power Supply- Layout Considerations*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

ADVANCE INFORMATION

12.5 Trademarks

HotRod, PowerPAD, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PLMR36015ARNXT	ACTIVE	VQFN-HR	RNX	12	250	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

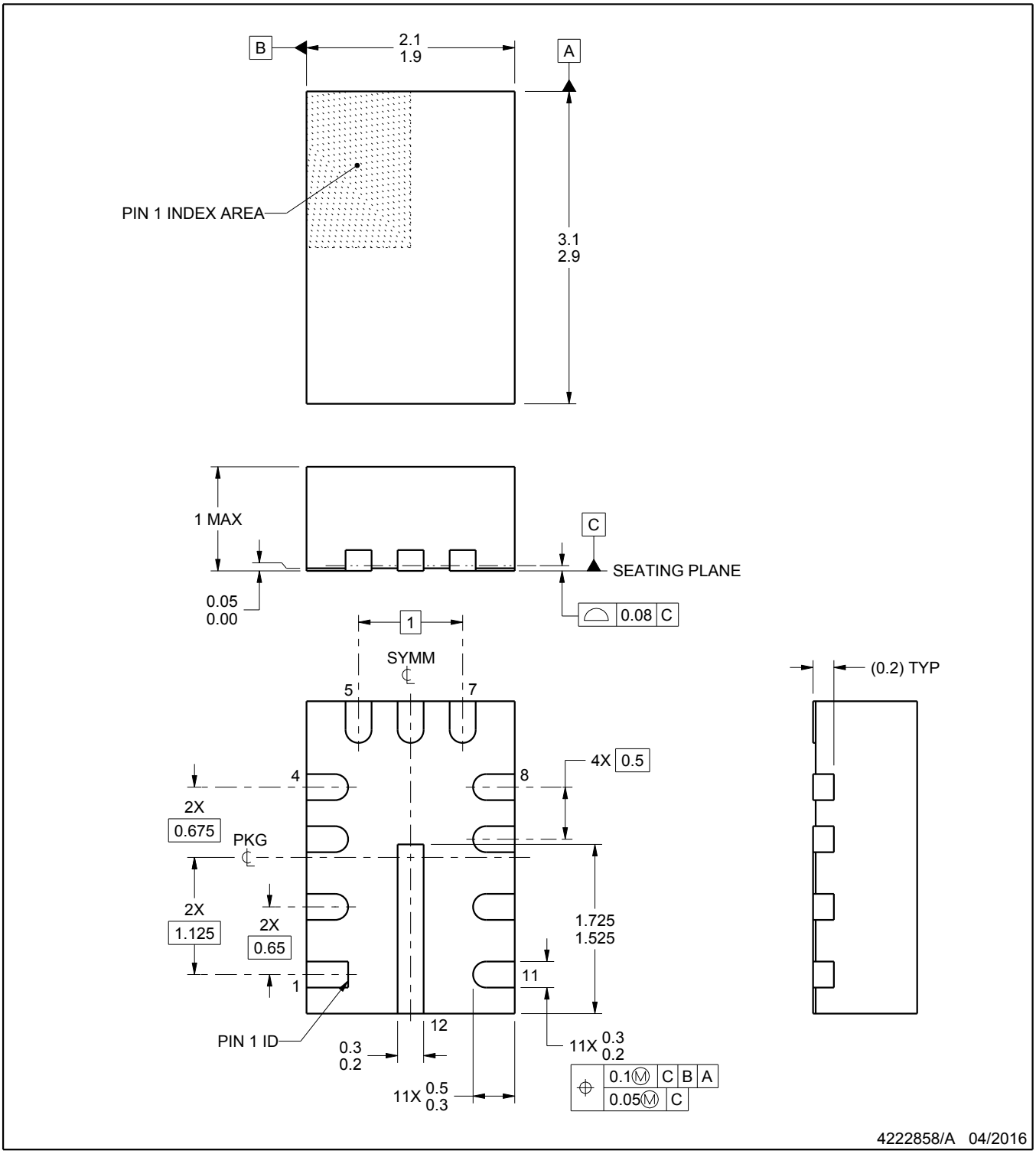
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RNX0012A

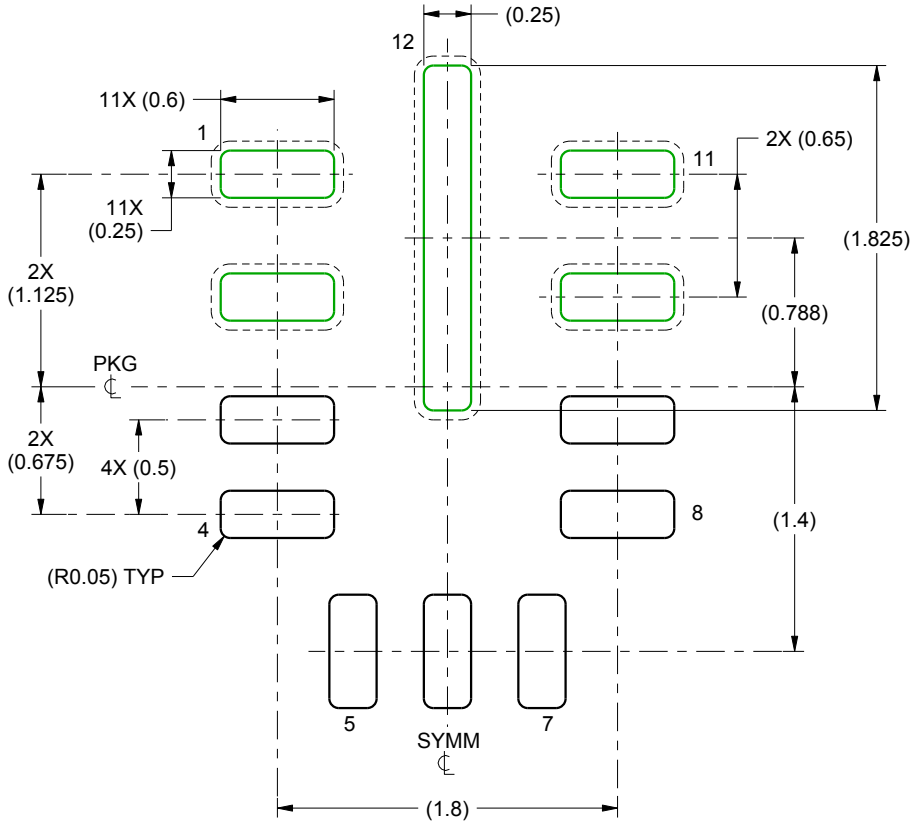
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

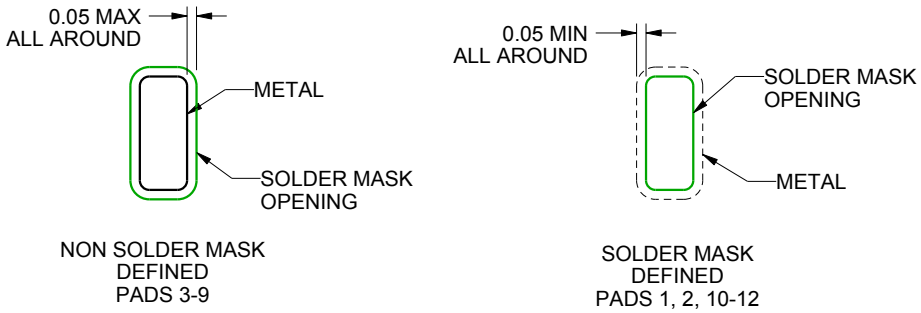


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

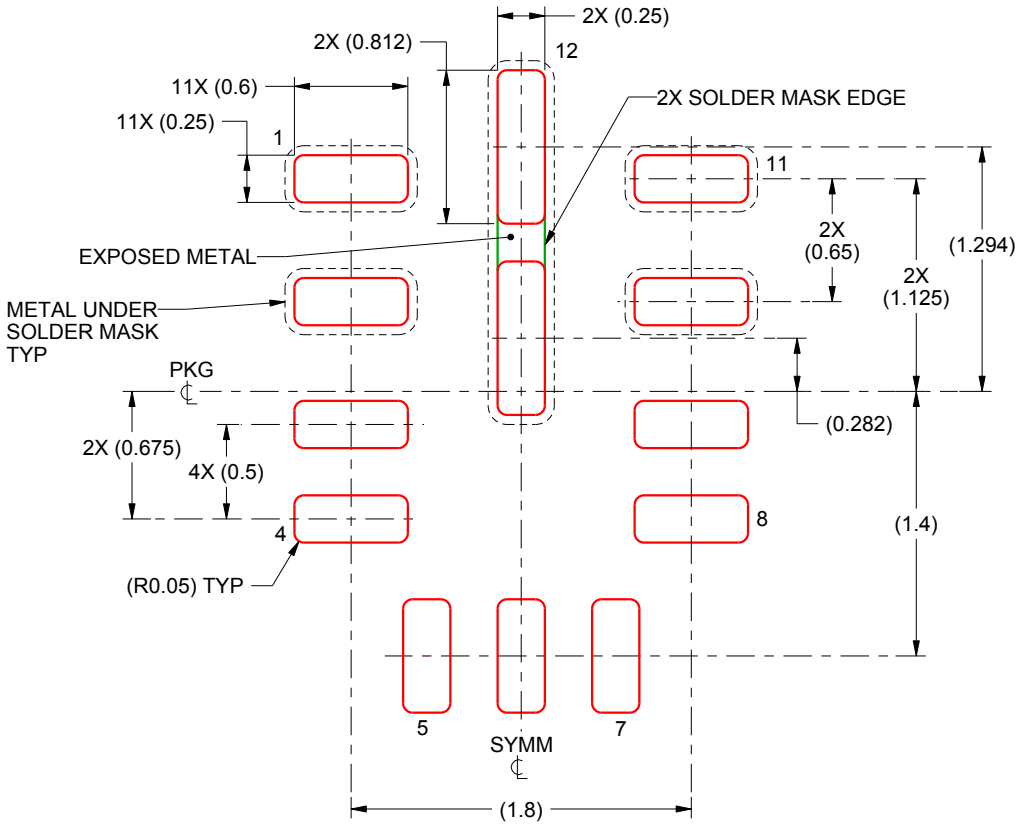


SOLDER MASK DETAILS

4222858/A 04/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

FOR PAD 12
87.7% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4222858/A 04/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265