MCP Specification

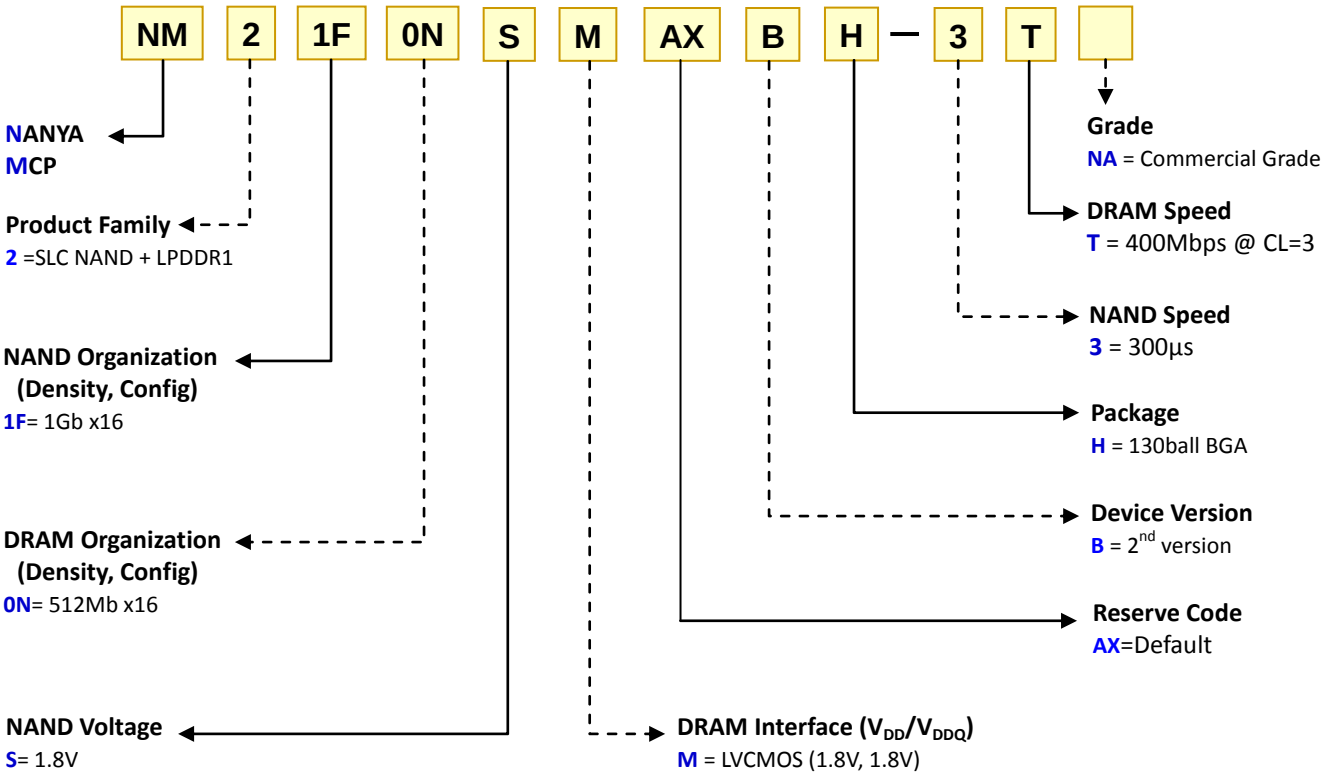
1Gb SLC NAND Flash (X16) + 512Mb LPDDR (X16)

Nanya Technology Corporation

Ordering Information

MCP	NAND				DRAM			
Part Number	Type	Density (Org.)	Program Time	Erase Time	Type	Density (Org.)	Speed	CL
NM21F0NSMAXBH-3T	SLC	1Gb (64Mb X16)	300µs	3.5ms	LPDDR	512Mb (32Mb X 16)	400	3

NANYA MCP Part Numbering Guide



Features

MCP

- **Separate SLC NAND and LPDDR RAM interfaces**
- **Lead-free (RoHS compliant) and Halogen-free Package :** 130-ball VFBGA (9.00mm x 8.00mm, pitch 0.65mm)
- **Operating temperature range:** –25°C to +85°C

1Gb X16 SLC NAND

- **Voltage Supply: 1.70V ~ 1.95V**
- **Organization**
  - Memory Cell Array: 1088 x 64K x 16
  - Data Register: 1088 x 16
  - Page Program: 1088 Words
  - Block Erase: (64K + 4K) Words
- **Modes**

  Read, Reset, Auto Page Program, Auto Block Erase, Status Read, Page Copy
- **Mode control**
  - Serial input/output
  - Command control
- **Number of valid blocks**
  - Min 1004 blocks
  - Max 1024 blocks
- **Access time**
  - Cell array to register: 25µs max
  - Serial Read Cycle: 25ns min (CL=30pF)
- **Program/Erase time**
  - Auto Page Program: 300µs/page typical
  - Auto Block Erase: 3.5ms/block typical
- **Operating current**
  - Read (25ns cycle): 30 mA max
  - Program (avg.): 30 mA max
  - Erase (avg.): 30 mA max
  - Standby: 50 µA max
- **8 bit ECC for each 512 Bytes is required.**

512Mb X16 LPDDR

- **Speed, Addressing and Retention Specification**

Organization	32Mb X 16
Speed Grade	400-3-3-3
Number of Banks	4
Bank Address	BA[1:0]
Row	A[12:0]
Column	A[9:0]
tREFI	7.8µs
tRFC	110ns

- **JEDEC LPDDR Compliant**
  - Low Power Consumption
  - Double-data rate on DQs, DQS and DM
  - 2n Prefetch Architecture
- **LVCMOS interface and Power Supply**
  - VDD/VDDQ= 1.70 to 1.95V
- **Signal Integrity**
  - Configurable DS for system compatibility
- **Data Integrity**
  - DRAM built-in Temperature Sensor for Temperature Compensated Self Refresh (TCSR)
  - Auto Refresh, Self Refresh and PASR Modes
- **Power Saving Modes**
  - Deep Power Down Mode (DPD)
  - Partial Array Self Refresh (PASR)
  - Clock Stop capability during idle period
- **Programmable Mode Register Function**
  - Output Drive Impedance (full, 3/4, 1/2, 1/4)
  - Burst Lengths (2, 4, 8, 16)
  - Burst Type (Sequential, Interleaved)
  - Partial Array Self Refresh (1, 1/2, 1/4, 1/8, 1/16)

130b Ball Assignment– Flash X16 + DRAM X16

Part Number: NM21F0NSMAXBH-XXX

	1	2	3	4	5	6	7	8	9	10	
A	NC	NC	$\overline{RE}$	CLE	VCC	$\overline{CE}$	$\overline{WE}$	VDD	VSS	NC	A
B	VSS	A4	$\overline{WP}$	ALE	VSS	R/$\overline{B}$	DQ15	DQ14	VDDQ	VSSQ	B
C	VDD	A5	A7	A9	DQ9	DQ11	DQ13	DQ12	VSSQ	VDDQ	C
D	A6	A8	CKE	RFU	UDQS	RFU	UDM	DQ10	VDDQ	VSSQ	D
E	A12	A11	NC	RFU	RFU	DQ8	RFU	RFU	VSSQ	VDDQ	E
F	NC	$\overline{RAS}$	RFU	RFU	RFU	RFU	RFU	CK	VDDQ	VSSQ	F
G	VDD	$\overline{CAS}$	RFU	RFU	RFU	RFU	RFU	$\overline{CK}$	VSS	VDD	G
H	VSS	$\overline{CS}$	BA0	RFU	RFU	RFU	LDQS	LDM	VSSQ	VDDQ	H
J	$\overline{WE}$	BA1	A10	A0	DQ7	RFU	DQ6	DQ4	VDDQ	VSSQ	J
K	A1	A2	A3	DQ0	DQ1	DQ2	DQ3	DQ5	VDDQ	VSSQ	K
L	VDD	VSS	NC	RFU	I/O 3	I/O 5	I/O 14	I/O 7	VSSQ	VDDQ	L
M	I/O 0	I/O 1	I/O 2	I/O 10	VCC	I/O 6	I/O 13	I/O 15	VDDQ	VSSQ	M
N	RFU	I/O 8	I/O 9	I/O 11	I/O 12	VSS	I/O 4	VDD	VSS	RFU[1]	N
	1	2	3	4	5	6	7	8	9	10	

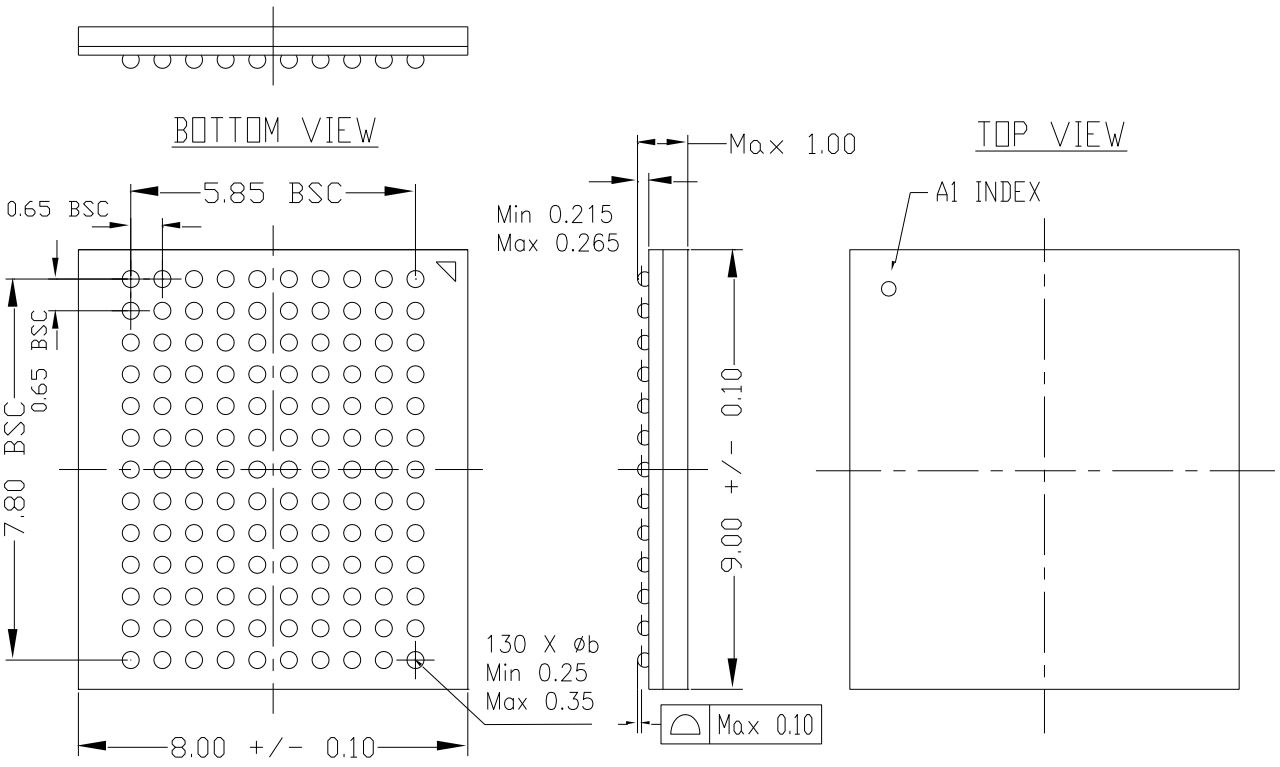
Power
Ground
DRAM
Flash
RFU
NC

NOTE 1 This pin is reserved for TEST purpose and it must be connected to Ground.

130b Package Outline Drawing (9.00mm x 8.00mm, pitch 0.65mm)

Unit: mm

* BSC (Basic Spacing between Center)



Ball Description – 1Gb X16 SLC NAND

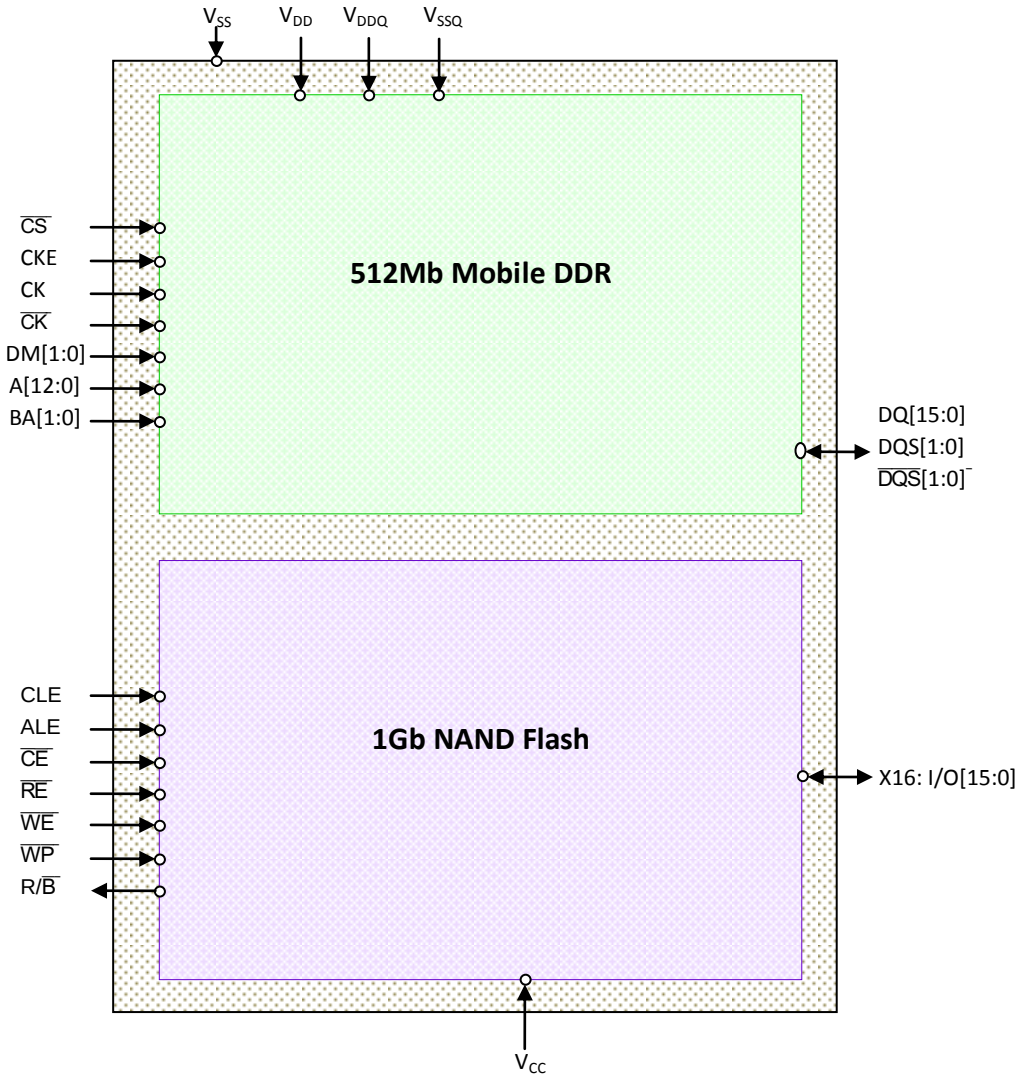
Symbol	Type	Function
X16: **I/O[15:0]**	Input/output	**Data Bus:** The I/O0 to 7 pins are used as a port for transferring address, command and input/output data to and from the device. The I/O8 to 15 pins are used as a port for transferring input/output data to and from the device. I/O8 to 15 pins must be low level (V_{IL}) when address and command are input.
CLE	Input	**Command Latch Enable:** The CLE input signal is used to control loading of the operation mode command into the internal command register. The command is latched into the command register from the I/O port on the rising edge of the $\overline{WE}$ signal while CLE is High
ALE	Input	**Address Latch Enable:** The ALE signal is used to control loading address information into the internal address register. Address information is latched into the address register from the I/O port on the rising edge of $\overline{WE}$ while ALE is High
$\overline{CE}$	Input	**Chip Enable:** The device goes into a low-power Standby mode when $\overline{CE}$ goes High during the device is in Ready state. The $\overline{CE}$ signal is ignored when device is in Busy state (RY / $\overline{BY}$ = L), such as during a Program or Erase or Read operation, and will not enter Standby mode even if the $\overline{CE}$ input goes High
$\overline{RE}$	Input	**Read Enable:** The $\overline{RE}$ signal controls serial data output. Data is available tREA after the falling edge of $\overline{RE}$. The internal column address counter is also incremented (Address = Address +1) on the falling edge.
$\overline{WE}$	Input	**Write Enable:** The $\overline{WE}$ signal is used to control the acquisition of data from the I/O port.
$\overline{WP}$	Input	**Write Protect:** The $\overline{WP}$ signal is used to protect the device from accidental programming or erasing. The internal voltage regulator is reset when $\overline{WP}$ is Low. This signal is usually used for protecting the data during the power-on/off sequence when input signals are invalid.
R/$\overline{B}$	Output	**Ready / Busy Output:** The RY / $\overline{BY}$ output signal is used to indicate the operating condition of the device. The RY / $\overline{BY}$ signal is in Busy state (RY / $\overline{BY}$ = L) during the Program, Erase and Read operations and will return to Ready state (RY / $\overline{BY}$ = H) after completion of the operation. The output buffer for this signal is an open drain and has to be pulled-up to Vccq with an appropriate resister. If RY / $\overline{BY}$ signal is not pulled-up to Vccq (“Open” state), device operation cannot guarantee
VCC	Supply	**Power Supply**
VSS	Supply	**Ground**
NC	—	**No Connect:** These pins should be left unconnected.

Ball Description – 512Mb X16 LPDDR

Symbol [1]	Type	Function
CK, $\overline{CK}$	Input	**Clock:** CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$. Input and output data is referenced to the crossing of CK and $\overline{CK}$ (both directions of crossing). Internal clock signals are derived from CK, $\overline{CK}$.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE LOW deactivates internal clock signals, and device input buffers and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operation (all banks idle), or ACTIVE POWERDOWN (row ACTIVE in any bank). CKE is synchronous for all functions except for SELF REFRESH EXIT, which is achieved asynchronously. Input buffers, excluding CK, $\overline{CK}$ and CKE, are disabled during power-down and self refresh mode which are contrived for low standby power consumption.
$\overline{CS}$	Input	**Chip Select:** $\overline{CS}$ enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external bank selection on systems with multiple banks. $\overline{CS}$ is considered part of the command code.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	**Command Inputs:** $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$) define the command being entered.
X16: **LDM, UDM**	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading matches the DQ and DQS loading.
X16:**DQ[15:0]**	Input/output	**Data Bus:** Bi-directional Input / Output data bus.
X16: **LDQS, UDQS**	Input/output	**Data Strobe:** Output with read data, input with write data. Edge-aligned with read data. Centered with write data to capture write data.
BA[1:0]	Input	**Bank Address Inputs:** BA0 and BA1 define to which bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0 and BA1 also determine which mode register is loaded during a LOAD MODE REGISTER command.
A[12:0]	Input	**Address Inputs:** provide the row address for ACTIVE commands, and the column address and auto precharge bit(A10) for READ or WRITE commands, to select one location out of the memory array in the respective bank. During a PRECHARGE command, A10 determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by Bank Address Inputs) or all banks (A10 HIGH). The address inputs also provide the opcode during a MODE REGISTER SET command.
VDD	Supply	**Power Supply**
VSS	Supply	**Ground**
VDDQ	Supply	**DQ Power Supply:** Isolated on the die for improved noise immunity.
VSSQ	Supply	**DQ Ground:** Provide isolated ground to DQs for improved noise immunity.
NC	-	**No Connect:** These pins should be left unconnected.

NOTE 1 The signal may show up in a different symbol but it indicates to the same thing. e.g., /CK = CK# = $\overline{CK}$ = CKb, /DQS = DQS# = $\overline{DQS}$ = DQSb

Functional Block Diagram



1Gb(X16) SLC NAND Flash

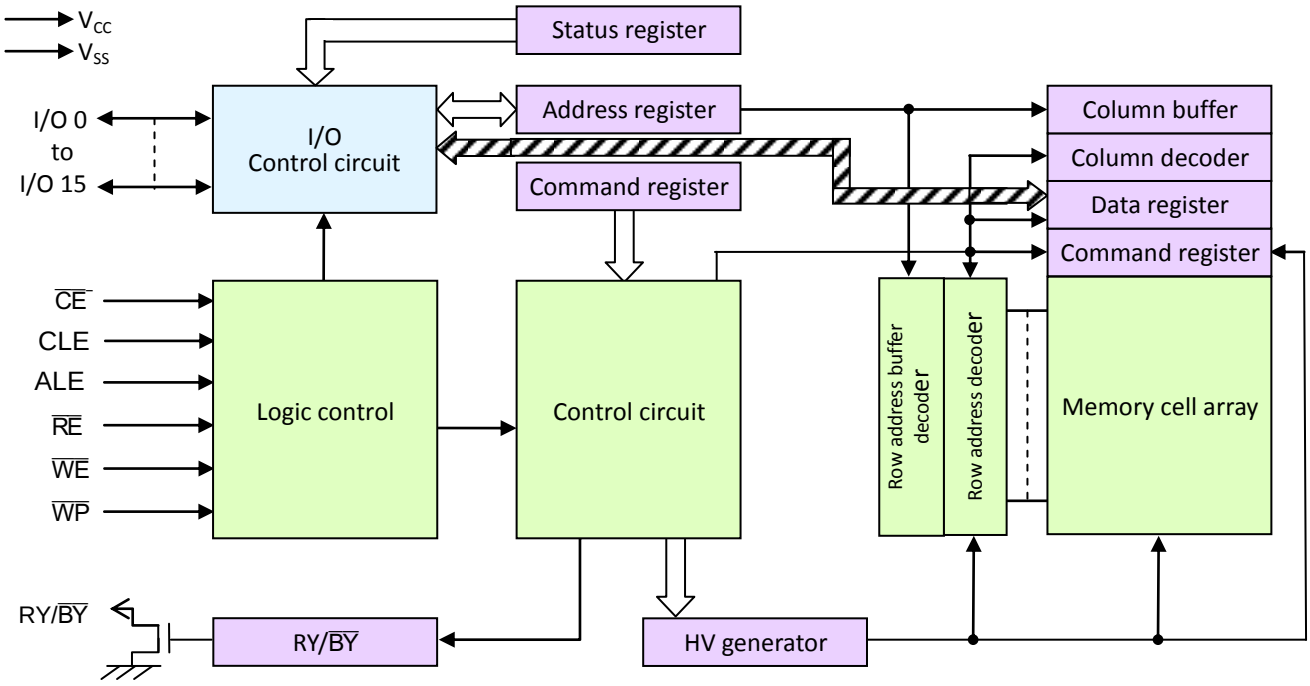
Descriptions

The device is a single 1.8V 1Gbit (1,140,850,688bits) NAND Electrically Erasable and Programmable Read-Only Memory (NAND E^2PROM) organized as (1024 + 64) words x 64 pages x 1024blocks.

The device has a 1088-word static registers which allow program and read data to be transferred between the register and the memory cell array in 1088 words increments. The Erase operation is implemented in a single block unit (64Kwords + 4Kwords: 1088 words x 64 pages).

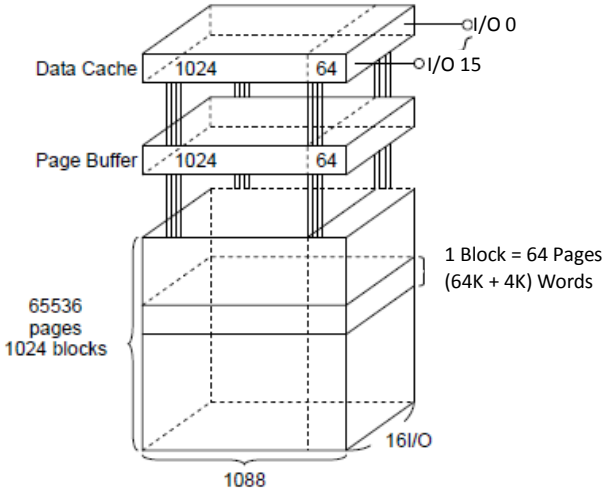
The device is a serial-type memory device which utilizes the I/O pins for both address and data input/output as well as for command inputs. The Erase and Program operations are automatically executed making the device most suitable for applications such as solid-state file storage, voice recording, image file memory for still cameras and other systems which require high-density non-volatile memory data storage.

Function Block Diagram (X16)



Array Organization (X16)

The Program operation works on page units while the Erase operation works on block units



A page consists of 1088 words in which 1024 words are used for main memory storage and 64 words are for redundancy or for other uses.
1 Page = 1088 Words
1 Block = 1088 Words x 64 Pages = (64K + 4K) Words
Capacity= 1088 Words x 64 Pages x1024 blocks

Array Address (X16)

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	I/O 8 ~ I/O 15	Address
1st cycle	CA_0	CA_1	CA_2	CA_3	CA_4	CA_5	CA_6	CA_7	L	Column Address
2nd cycle	CA_8	CA_9	CA_{10}	L	L	L	L	L	L	Column Address
3rd cycle	PA_0	PA_1	PA_2	PA_3	PA_4	PA_5	PA_6	PA_7	L	Page Address
4th cycle	PA_8	PA_9	PA_{10}	PA_{11}	PA_{12}	PA_{13}	PA_{14}	PA_{15}	L	Page Address

PA6 to PA16: Block address
PA0 to PA5: NAND address in block
Note I/O 8 ~ 15 must be held low when address is input.

Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{CC}	Power Supply Voltage	-0.6 to +2.5	V
V_{IN}	Input Voltage	-0.6 to +2.5	
$V_{I/O}$	Input / Output Voltage	-0.6 to Vcc + 0.3(≤2.5V)	
P_D	Power Dissipation	0.3	W
T_{SOLDER}	Soldering Temperature (10 s)	260	°C
T_{STG}	Storage Temperature	-55 to +125	°C

Capacitance[1]

(T_A=25℃, f=1.0MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input	V_{IN}=0V	—	10	pF
C_{OUT}	Output	V_{OUT}=0V	—	10	pF

NOTE 1 This parameter is periodically sampled and is not tested for every device.

Valid Blocks

Symbol	Parameter	Min	Typ.	Max	Unit
N_{VB}	Number of Valid Blocks	1,004	–	1,024	Blocks

NOTE 1 The device occasionally contains unusable blocks.
The first block (Block 0) is guaranteed to be a valid block at the time of shipment.
The specification for the minimum number of valid blocks is applicable over lifetime.

Recommended DC Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Unit
V_{CC}	Power Supply Voltage	1.70	–	1.95	V
V_{IH}	High Level Input Voltage	V_{CC} x 0.8	–	V_{CC} + 0.3	V
V_{IL}	Low Level Input Voltage	-0.3[1]	–	V_{CC} x 0.2	V

NOTE 1 -2 V (pulse width lower than 20 ns)

DC and Operation Characteristics

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Test Conditions	Min	Typ.	Max	Unit
I_{IL}	Input Leakage Current	V_{IN}=0 to V_{CC}	–	–	±10	µA
I_{LO}	Output Leakage Current	V_{OUT}=0 to V_{CC}	–	–	±10	µA
I_{CCO1}	Serial Read Current	$\overline{CE}$=V_{IL},I_{OUT}= 0 mA, tcycle=25ns	–	–	30	mA
I_{CCO2}	Programming Current	–	–	–	30	mA
I_{CCO3}	Erasing Current	–	–	–	30	mA
I_{CCS}	Standby Current	$\overline{CE}$ = V_{CC} - 0.2 V, $\overline{WP}$ = 0 V/V_{CC}	–	–	50	µA
V_{OH}	High Level Output Voltage	I_{OH} = -0.1mA	V_{CC} - 0.2	–	–	V
V_{OL}	Low Level Output Voltage	I_{OL} = 0.1mA	–	–	0.2	V
I_{OL} (RY/$\overline{BY}$)	Output Current of (RY/$\overline{BY}$) pin	V_{OL}=0.2V	–	4	–	mA

AC Timing Characteristics for Command / Address / Data Input

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Min	Max	Unit
tCLS	CLE Setup Time	12	–	ns
tCLH	CLE Hold Time	5	–	ns
tCS	$\overline{CE}$ Setup Time	20	–	ns
tCH	$\overline{CE}$ Hold Time	5	–	ns
tWP	Write Pulse Width	12	–	ns
tALS	ALE Setup Time	12	–	ns
tALH	ALE Hold Time	5	–	ns
tDS	Data Setup Time	12	–	ns
tDH	Data Hold Time	5	–	ns
tWC	Write Cycle Time	25	–	ns
tWH	$\overline{WE}$ High Hold Time	10	–	ns

AC Characteristics for Operation

Symbol	Parameter	Min	Max	Unit
tWW	$\overline{WP}$ High to $\overline{WE}$ Low	100	–	ns
tRR	Ready to $\overline{RE}$ Falling Edge	20	–	ns
tRW	Ready to $\overline{WE}$ Falling Edge	20	–	ns
tRP	Read Pulse Width	12	–	ns
tRC	Read Cycle Time	25	–	ns
tREA	$\overline{RE}$ Access Time	–	20	ns
tCEA	$\overline{CE}$ Access Time	–	25	ns
tCLR	CLE Low to $\overline{RE}$ Low	10	–	ns
tAR	ALE Low to $\overline{RE}$ Low	10	–	ns
tRHOH	$\overline{RE}$ High to Output Hold Time	25	–	ns
tRLOH	$\overline{RE}$ Low to Output Hold Time	5	–	ns
tRHZ	$\overline{RE}$ High to Output High Impedance	–	60	ns
tCHZ	$\overline{CE}$ High to Output High Impedance	–	20	ns
tCSD	$\overline{CE}$ High to ALE or CLE Don't care	0	–	ns
tREH	$\overline{RE}$ High Hold Time	10	–	ns
tIR	Output-High-impedance-to-$\overline{RE}$ Falling Edge	0	–	ns
tRHW	$\overline{RE}$ High to $\overline{WE}$ Low	30	–	ns
tWHC	$\overline{WE}$ High to $\overline{CE}$ Low	30	–	ns
tWHR	$\overline{WE}$ High to $\overline{RE}$ Low	60	–	ns
tR	Memory Cell Array to Starting Address	–	25	µs
tDCBSYR1	Data Cache Busy in Read Cache (following 31h and 3Fh)	–	25	µs
tDCBSYR2	Data Cache Busy in Page Copy (following 3Ah)	–	30	µs
tWB	$\overline{WE}$ High to Busy	–	100	ns
tRST	Device Reset Time (Ready/Read/Program/Erase)	–	5/5/10/500	µs

NOTE1 tCLS and tALS cannot be shorter than tWP.

NOTE2 tCS should be longer than tWP + 8ns.

AC Test Conditions

Parameter	Condition
	VCC : 1.70 to 1.95V
Input level	VCC – 0.2 V, 0.2 V
Input pulse rise and fall time	3ns
Input comparison level	Vcc / 2
Output data comparison level	Vcc / 2
Output Load	1 TTL GATE and CL=30pF

NOTE 1 Busy to ready time depends on the pull-up resistor tied to the RY/$\overline{BY}$ pin.

Program / Erase Characteristics

(Ta= -25 to 85℃, V_{CC}=1.70 to 1.95V)

Symbol	Parameter	Min	Typ	Max	Unit
tPROG	Average Programming Time	–	300	700	µs
tDCBSYW2[1]	Data Cache Busy Time in Write Cache (following 15h)	–	–	700	µs
Nop	Number of Partial Program Cycles in the Same Page	–	–	4	cycle
tBERASE	Block Erase Time	–	3.5	10	ms

NOTE 1 $t_{DCBSYW2}$ depends on the timing between internal programming time and data in time.

Operation Mode: Logic and Command Tables

The operation modes such as Program, Erase, Read and Reset are controlled by operations shown in command table. Address input, command input and data input/output are controlled by the CLE, ALE, $\overline{CE}$, $\overline{WE}$, $\overline{RE}$ and $\overline{WP}$ signals, as shown in Mode Selection Table.

Mode Selection Table

CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	$\overline{WP}$	Mode
H	L	L	↑	H	∗	Command Input
L	L	L	↑	H	H	Data Input
L	H	L	↑	H	∗	Address Input
L	L	L	H	↓	∗	Serial Data Output
∗	∗	∗	∗	∗	H	During Program (Busy)
∗	∗	∗	∗	∗	H	During Erase (Busy)
∗	∗	H	∗	∗	∗	During Read (Busy)
∗	∗	L	H[1]	H[1]	∗	
∗	∗	∗	∗	∗	L	Program, Erase Inhibit
∗	∗	H	∗	∗	0V/V_{CC}	Stand-by

H: V_{IH}, L=V_{IL} ∗ : V_{IH} or V_{IL}.

Note 1: If $\overline{CE}$ is low during read busy. $\overline{WE}$ and $\overline{RE}$ must be held High to avoid unintended command/address input to device or read to device. Reset or Status Read command can be input during Read Busy.

Command Table

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Serial Data Input	80_H	—	
Read	00_H	30_H	
Column Address Change in Serial Data Output	05_H	$E0_H$	
Read with Data Cache	31_H	—	
Read Start for Last Page in Read Cycle with Data Cache	$3F_H$	—	
Auto Page Program	80_H	10_H	
Column Address Change in Serial Data Input	85_H	—	
Auto Program with Data Cache	80_H	15_H	
Read for Page Copy (2) with Data Out	00_H	$3A_H$	
Auto Program with Data Cache during Page Copy (2)	$8C_H$	15_H	
Auto Program for last page during Page Copy (2)	$8C_H$	10_H	
Auto Block Erase	60_H	$D0_H$	
ID Read	90_H	—	
Status Read	70_H	—	O
Reset	FF_H	—	O

Read mode operation states

	CLE	ALE	$\overline{CE}$	$\overline{WE}$	$\overline{RE}$	I/O0 to I/O15	Power
Output select	L	L	L	H	L	Data output	Active
Output Deselect	L	L	L	H	H	High impedance	Active

H: V_{IH}, L=V_{IL}

ID Read

The device contains ID codes which can be used to identify the device type, the manufacturer, and features of the device. The ID codes can be read out under the following timing conditions:

ID Definition Table (X16)

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0	Hex Data
1st Data	Maker Code	1	0	0	1	1	0	0	0	98_H
2nd Data	Device Code	1	0	1	1	0	0	0	1	$B1_H$
3rd Data	Internal Chip Number, Cell Type	–	–	–	–	–	–	–	–	See table
4th Data	Page Size, Block Size	–	–	–	–	–	–	–	–	See table
5th Data	Plane Number	–	–	–	–	–	–	–	–	See table

3rd ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		

4th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (w/o redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				

5th ID Data

Item	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1 Plane					0	0		
	2 Plane					0	1		
	4 Plane					1	0		
	8 Plane					1	1		

Status Read

The device automatically implements the execution and verification of the Program and Erase operations. The status Read function is used to monitor the Ready/Busy status of the device, determine the result (pass/fail) of a Program or Erase operation, and determine whether the device is in Protect mode. The device status is output via the I/O port using RE after a “70h” command input. The Status Read can also be used during a Read operation to find out the Ready/Busy status.

Status Register Definition for 70_H Command

I/O	Page Program	Block Erase	Read	Cache Read	Cache Program	Definition
I/O 0	Pass / Fail	Pass / Fail	Invalid	Invalid	Pass / Fail	Chip Status1 Pass : 0 / Fail : 1
I/O 1	Invalid	Invalid	Invalid	Invalid	Pass / Fail	Chip Status2 Pass : 0 / Fail : 1
I/O 2	0	0	0	0	0	Not Used
I/O 3	0	0	0	0	0	Not Used
I/O 4	0	0	0	0	0	Not Used
I/O 5	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Page Buffer Busy : 0 / Ready : 1
I/O 6	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Ready / Busy	Data Cache Busy : 0 / Ready : 1
I/O 7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect Protected :0 / Not Protected : 1
I/O8 to 15	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used

NOTE The Pass/Fail status on I/O0 and I/O1 is only valid during a Program/Erase operation when the device is in the Ready state.

Chip Status 1:

During a Auto Page Program or Auto Block Erase operation this bit indicates the pass/fail result.

During a Auto Page Programming with Data Cache operation, this bit shows the pass/fail results of the current page program operation, and therefore this bit is only valid when I/O5 shows the Ready state.

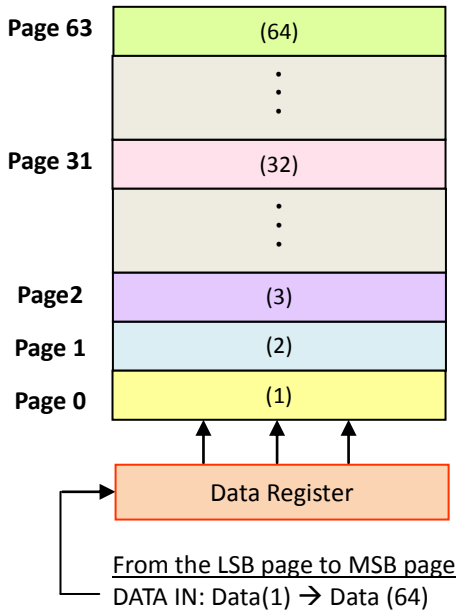
Chip Status 2:

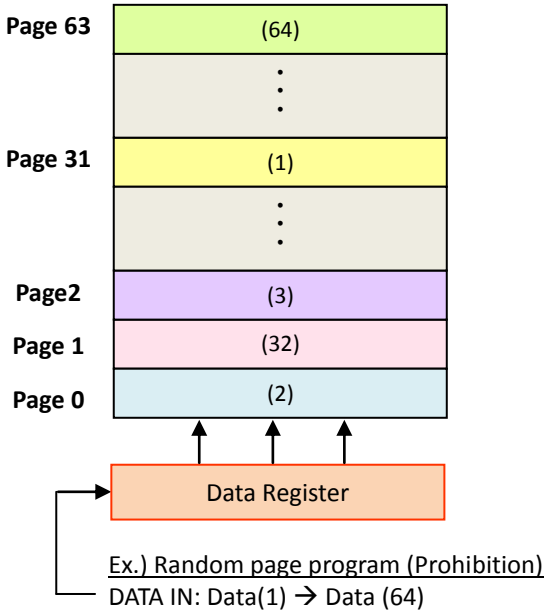
This bit shows the pass/fail result of the previous page program operation during Auto Page Programming with Data Cache. This status is valid when I/O6 shows the Ready State.

The status output on the I/O5 is the same as that of I/O6 if the command input just before the 70h is not 15h or 31h.

Addressing for Program Operation

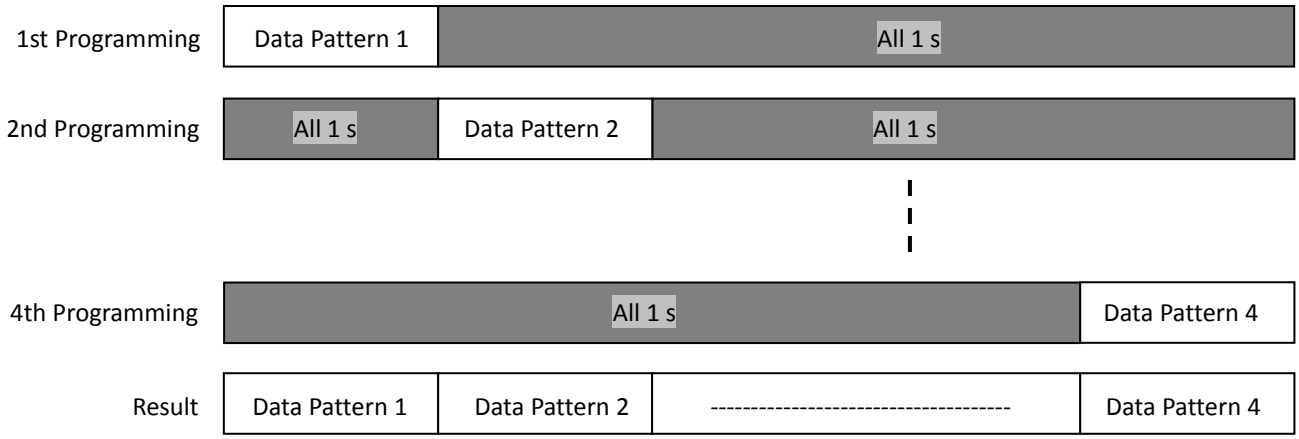
Within a block, the pages must be programmed consecutively from the LSB (least significant bit) page of the block to MSB (most significant bit) pages of the block. Random page address programming is prohibited.





Several programming cycles on the same page (Partial Page Program)

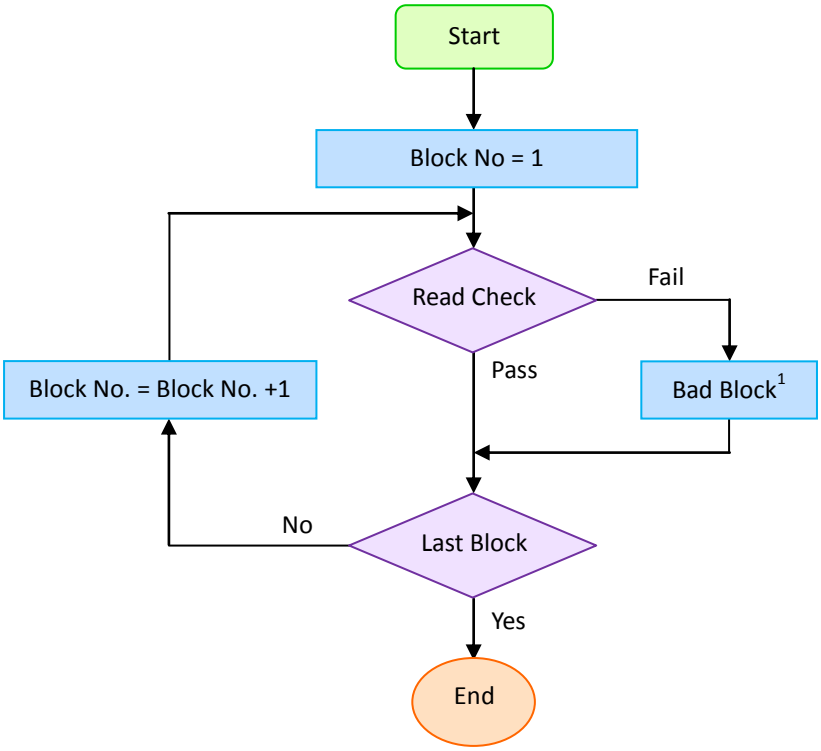
Each segment can be programmed individually as follows:



Bad Block Test Flow

Regarding invalid blocks, bad block mark is in whole pages.

Please read one column of any page in each block. It makes sure that every invalid block has Marjority “0” data at this column. If the data of the column is Marjority “0”, define the block as a bad block.



Note1: No erase operation is allowed to detected bad blocks

Failure phenomena for Program and Erase Operations

The device may fail during a Program or Erase operation.

The following possible failure modes should be considered when implementing a highly reliable system.

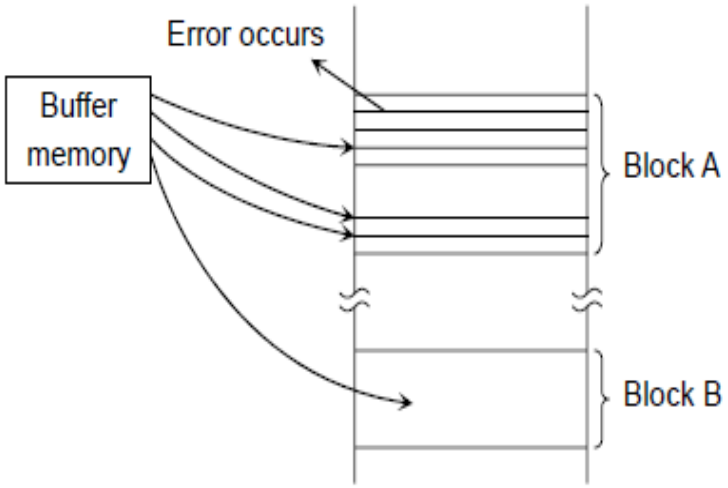
Failure Mode		Detection and Countermeasure Sequence
Block	Erase failure	Read Status after Erase → Block Replacement
Page	Program failure	Read Status after Program → Block Replacement
Read	Bit Error	ECC Correction / Block Refresh

NOTE 1 ECC: Error Correction Code. 8 bit correction per 512 Bytes is necessary.

Block Replacement

Program

When an error happens in Block A, try to reprogram the data into another Block (Block B) by loading from an external buffer. Then, prevent further system accesses to Block A (by creating a bad block table or by using anther appropriate scheme).



Erase

When an error occurs during an Erase operation, prevent future accesses to this bad block (again by creating a table within the system or by using another appropriate scheme).

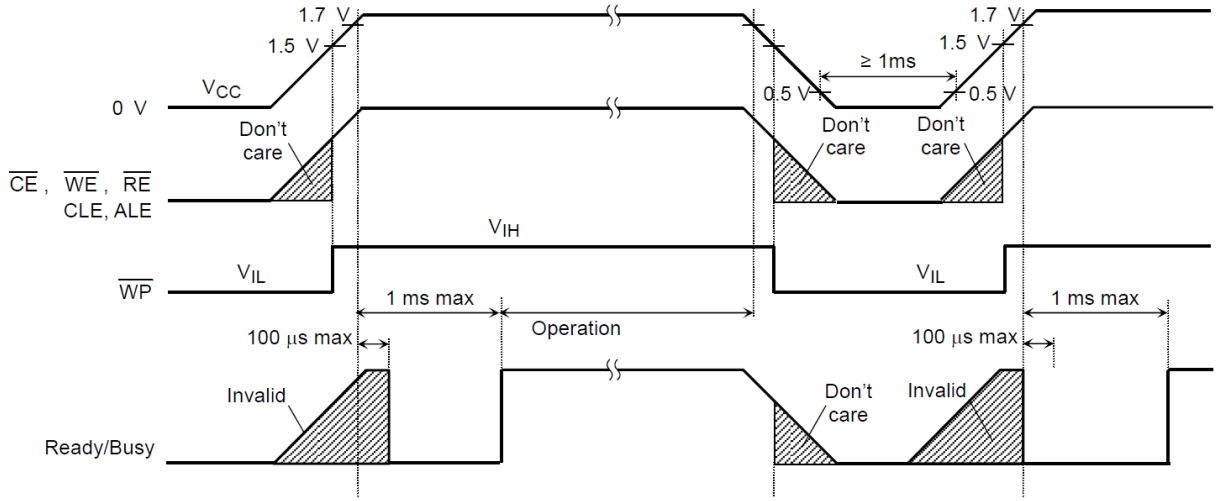
Power-on/off sequence

The timing sequence shown in the figure below is necessary for the power-on/off sequence.

The device internal initialization starts after the power supply reaches an appropriate level in the power on sequence.

During the initialization the device Ready/Busy signal indicates the Busy state as shown in the figure below. In this time period, the acceptable commands are FFh or 70h.

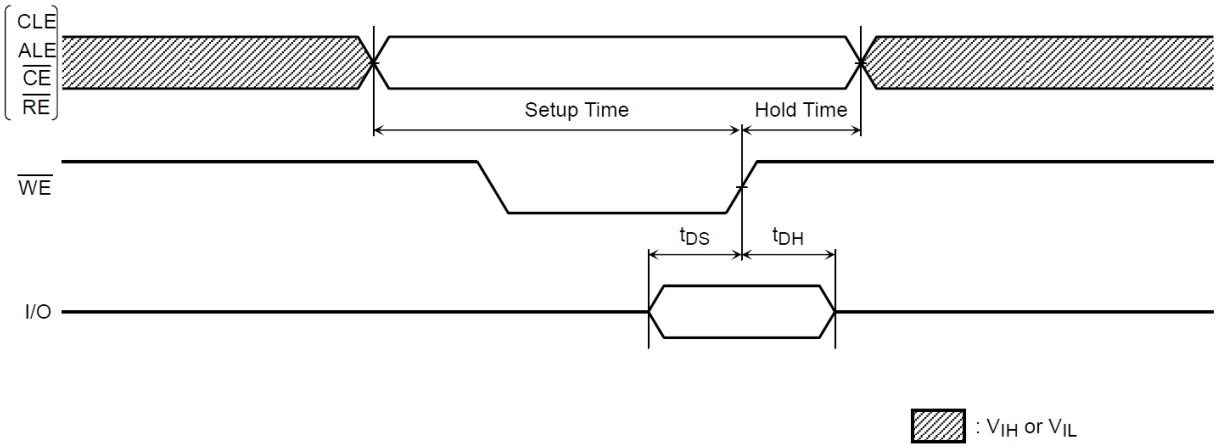
The $\overline{WP}$ signal is useful for protecting against data corruption at power-on/off.



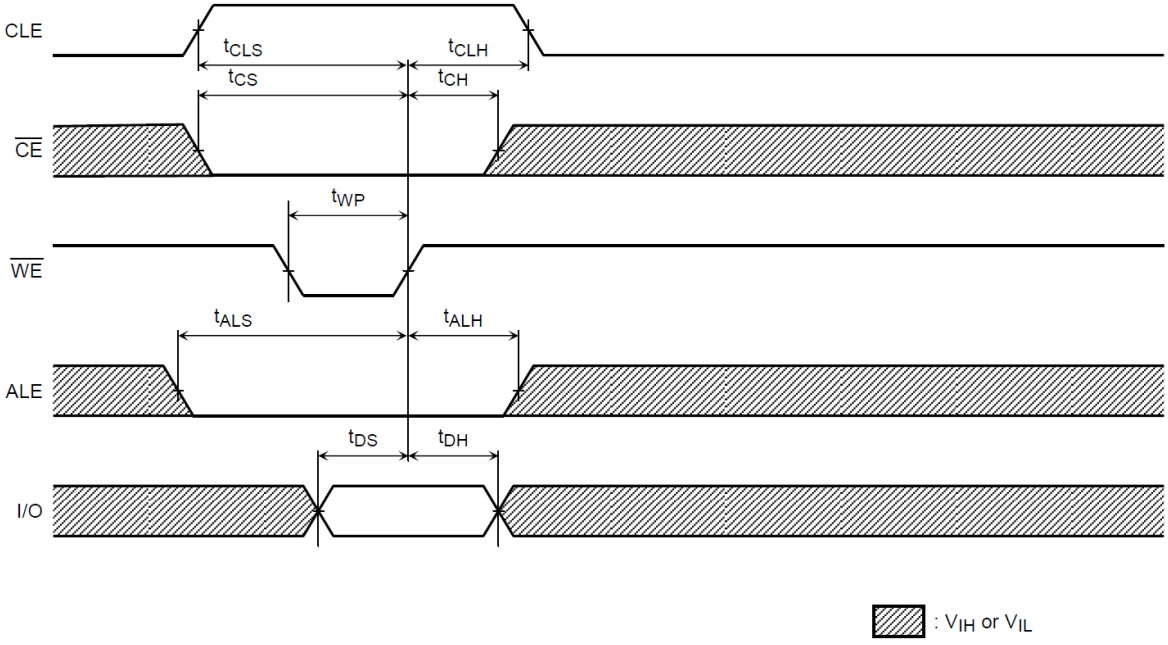
Do not turn off the power before write/erase operation is complete. Avoid using the device when the battery is low. Power shortage and/or power failure before write/erase operation is complete will cause loss of data and/or damage to data.

TIMING DIAGRAMS

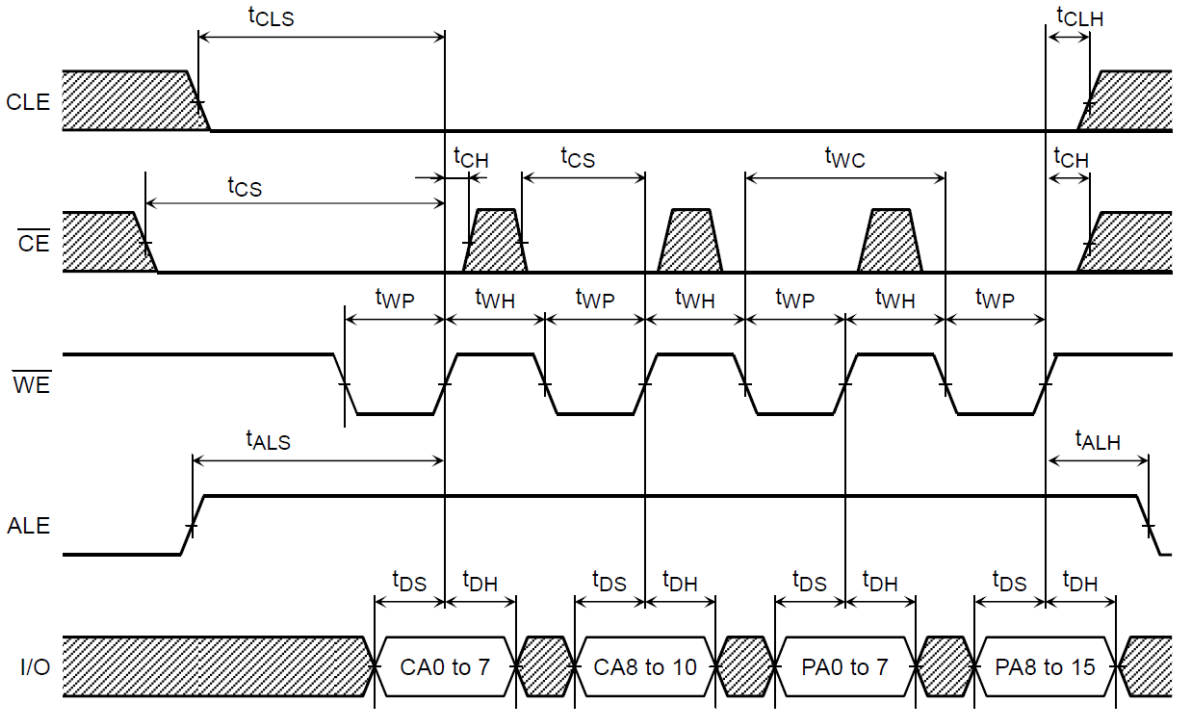
Latch Timing Diagram for Command/Address/Data



Command Input Cycle Timing Diagram

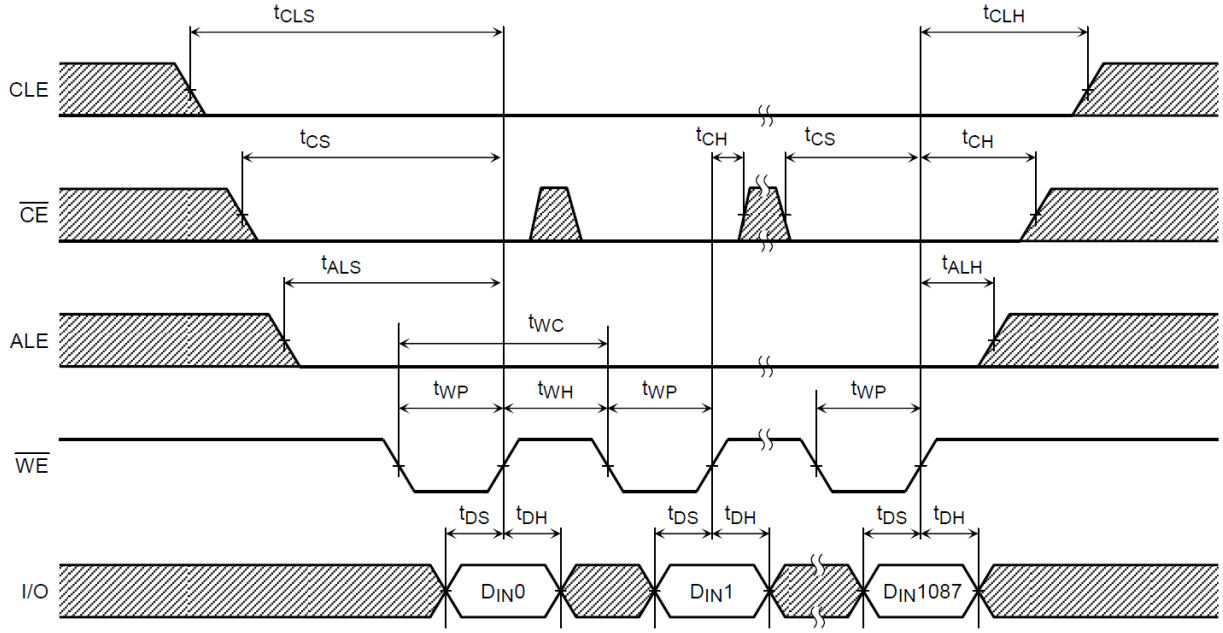


Address Input Cycle Timing Diagram

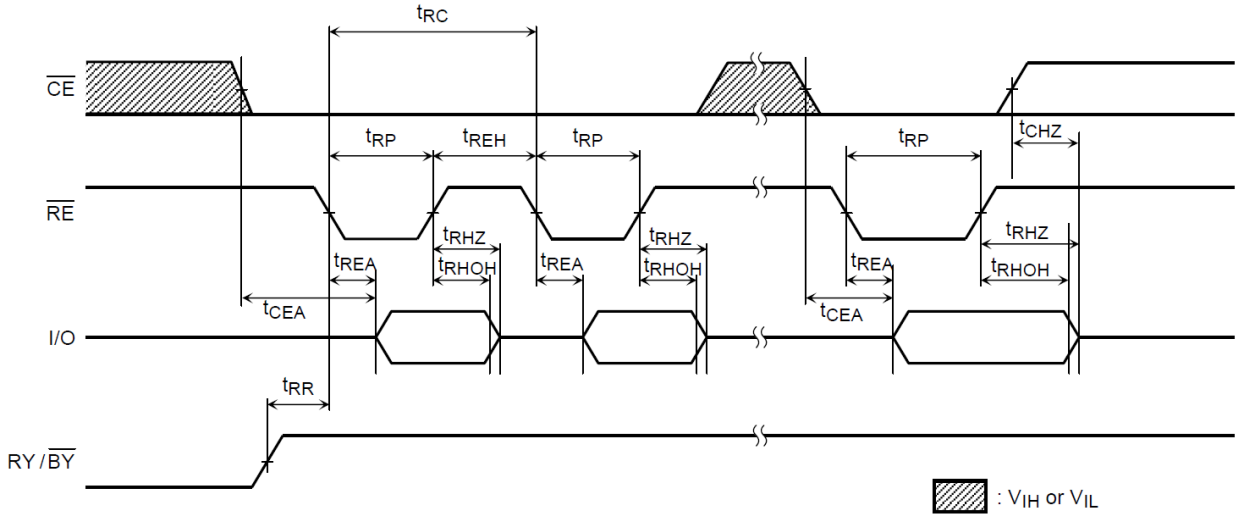


: V_{IH} or V_{IL}

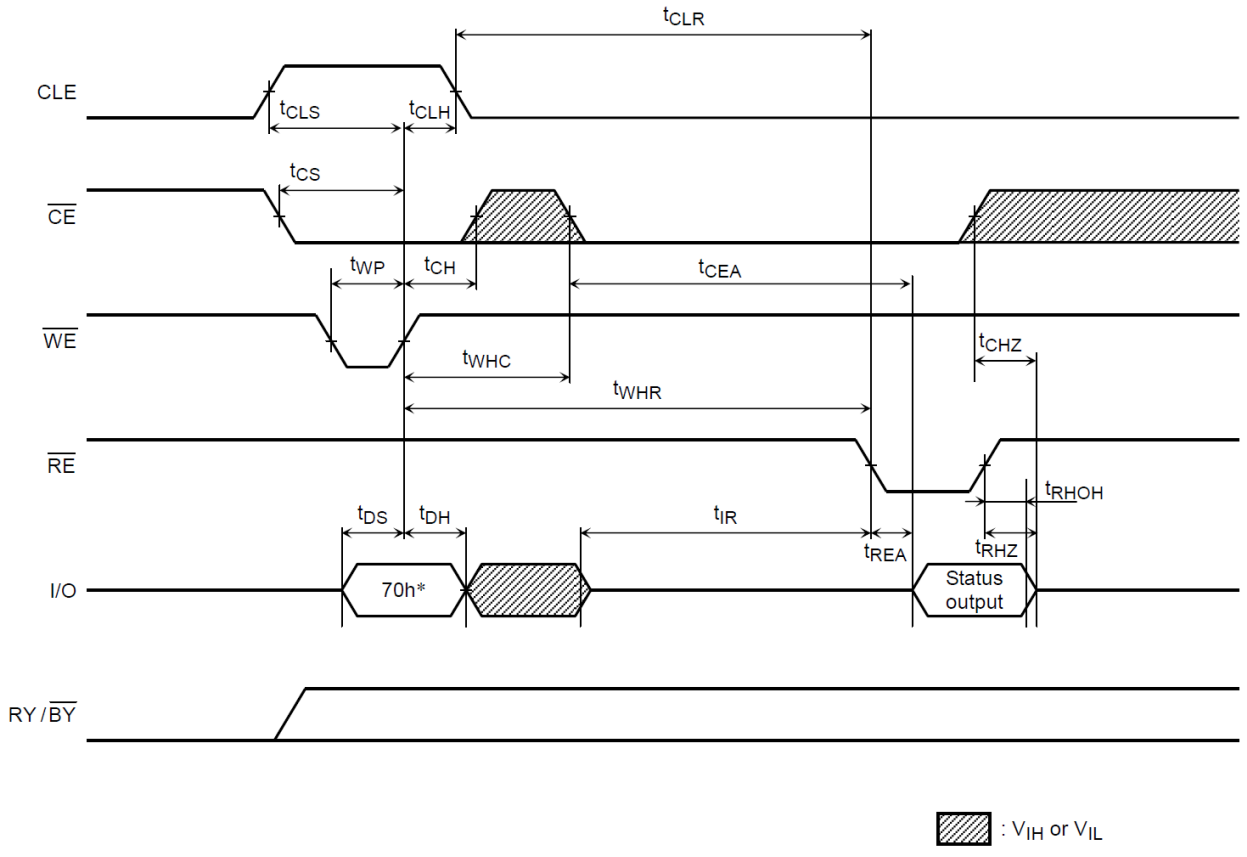
Data Input Cycle Timing Diagram



Serial Read Cycle Timing Diagram

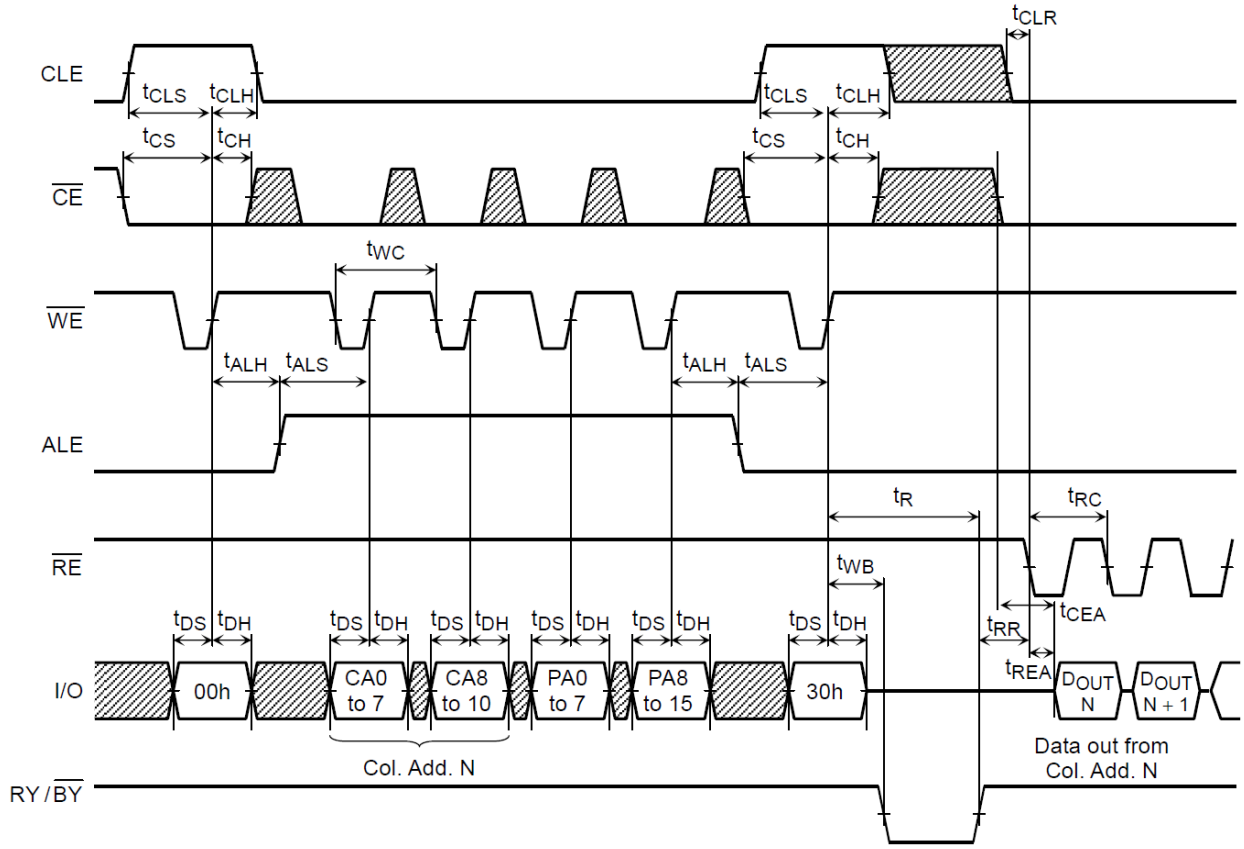


Status Read Cycle Timing Diagram

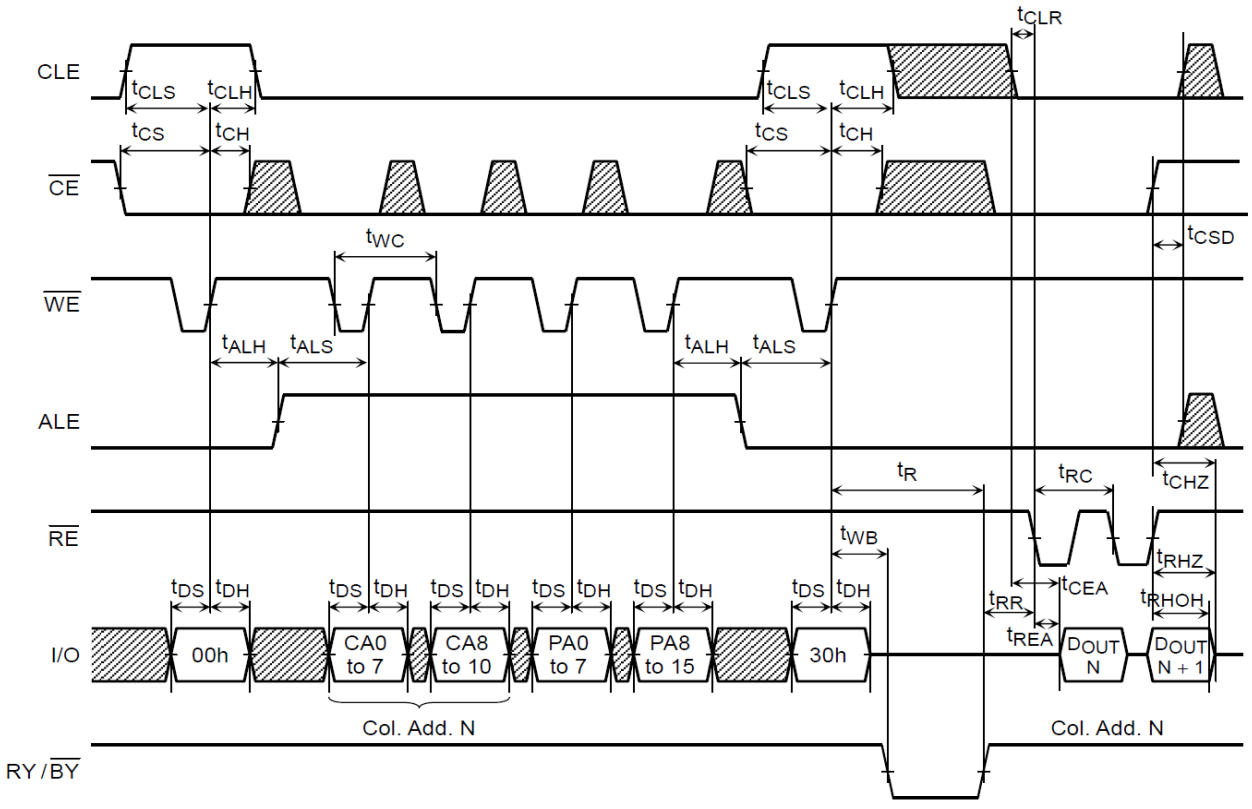


*: 70h represents the hexadecimal number

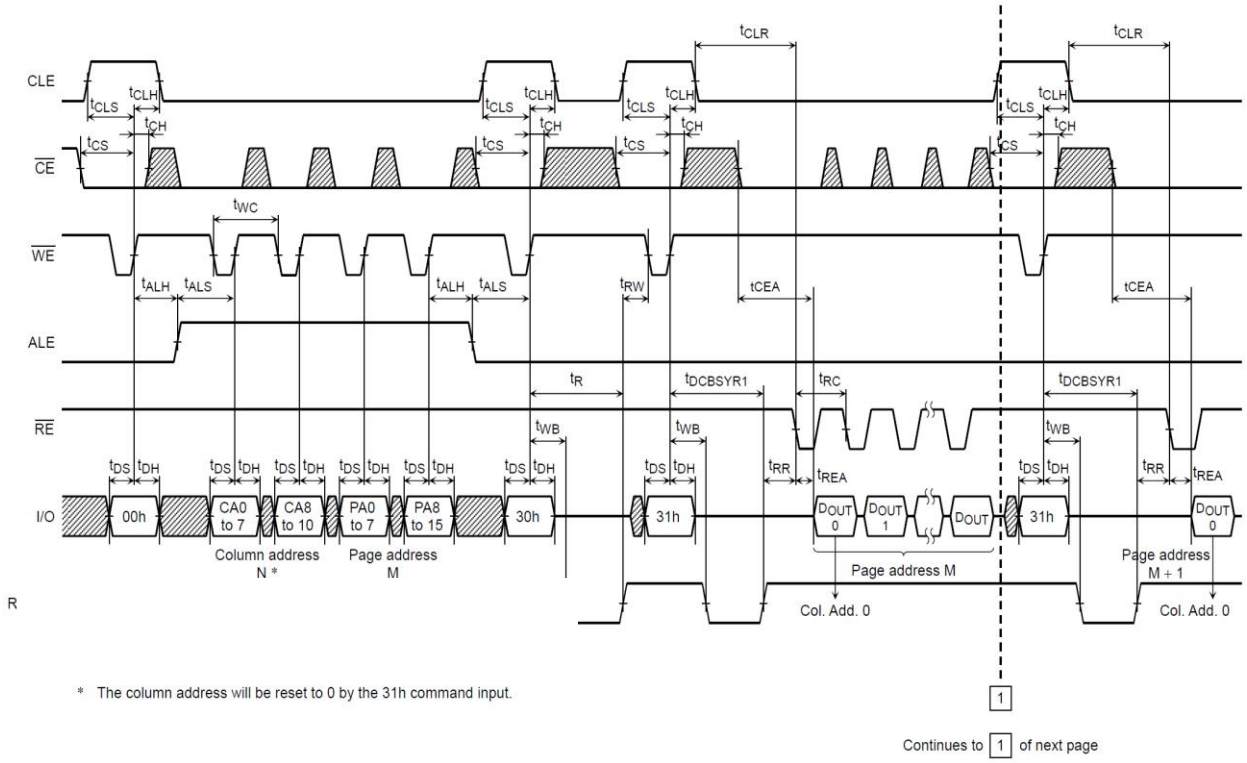
Read Cycle Timing Diagram



Read Cycle Timing Diagram: When Interrupted by $\overline{CE}$

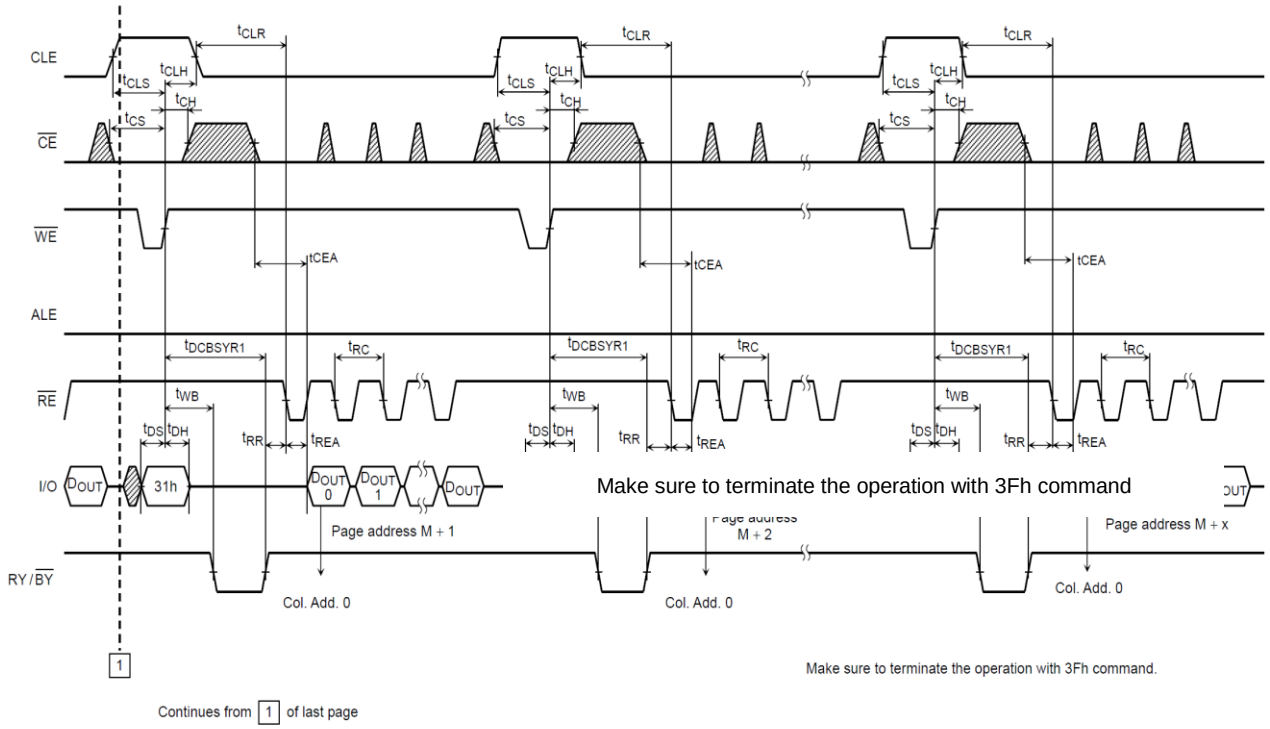


Read Cycle with Data Cache Timing Diagram (1/2)

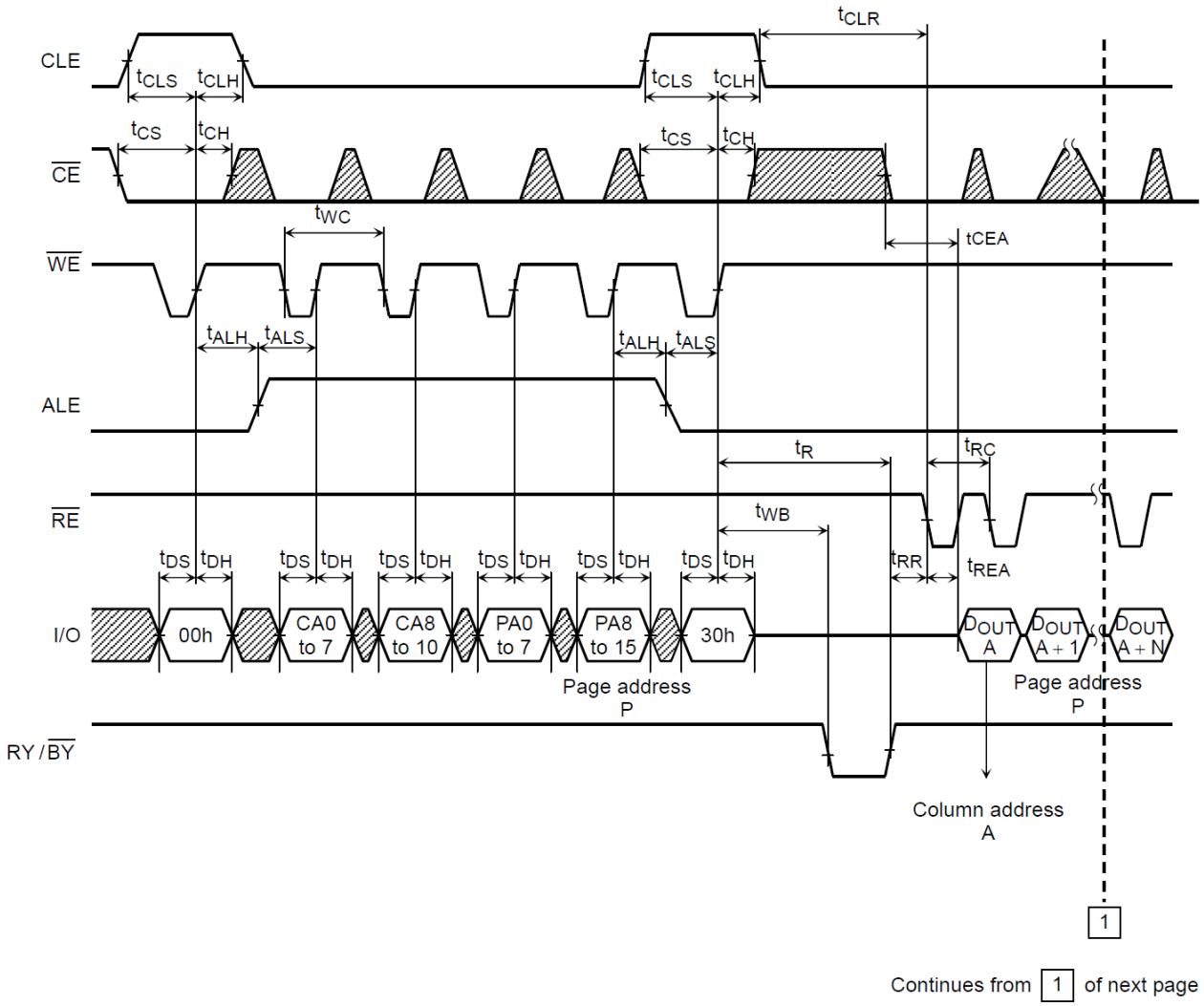


*: The column address will be reset to 0 by the 31h command input

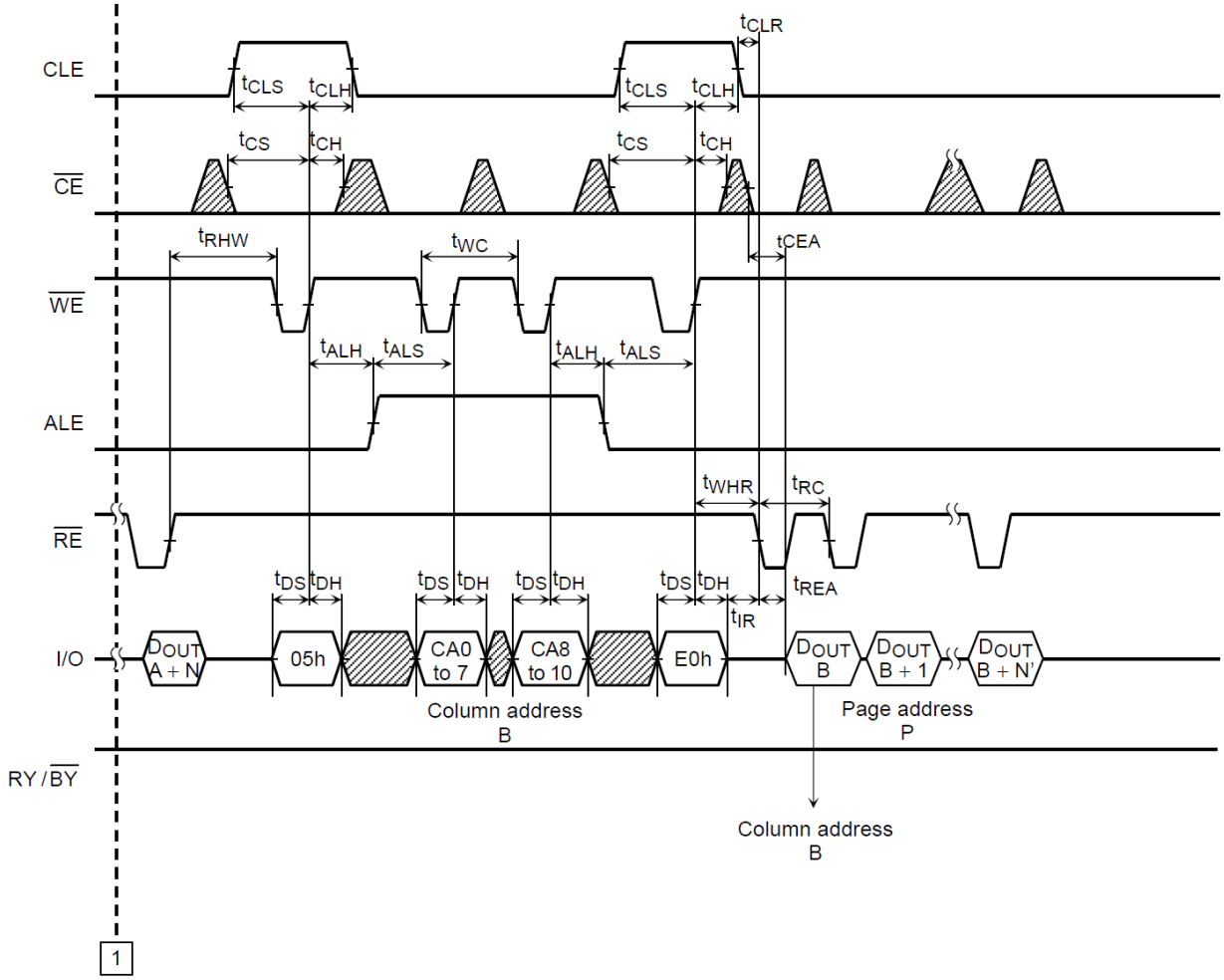
Read Cycle with Data Cache Timing Diagram (2/2)



Column Address Change in Read Cycle Timing Diagram (1/2)



Column Address Change in Read Cycle Timing Diagram (2/2)



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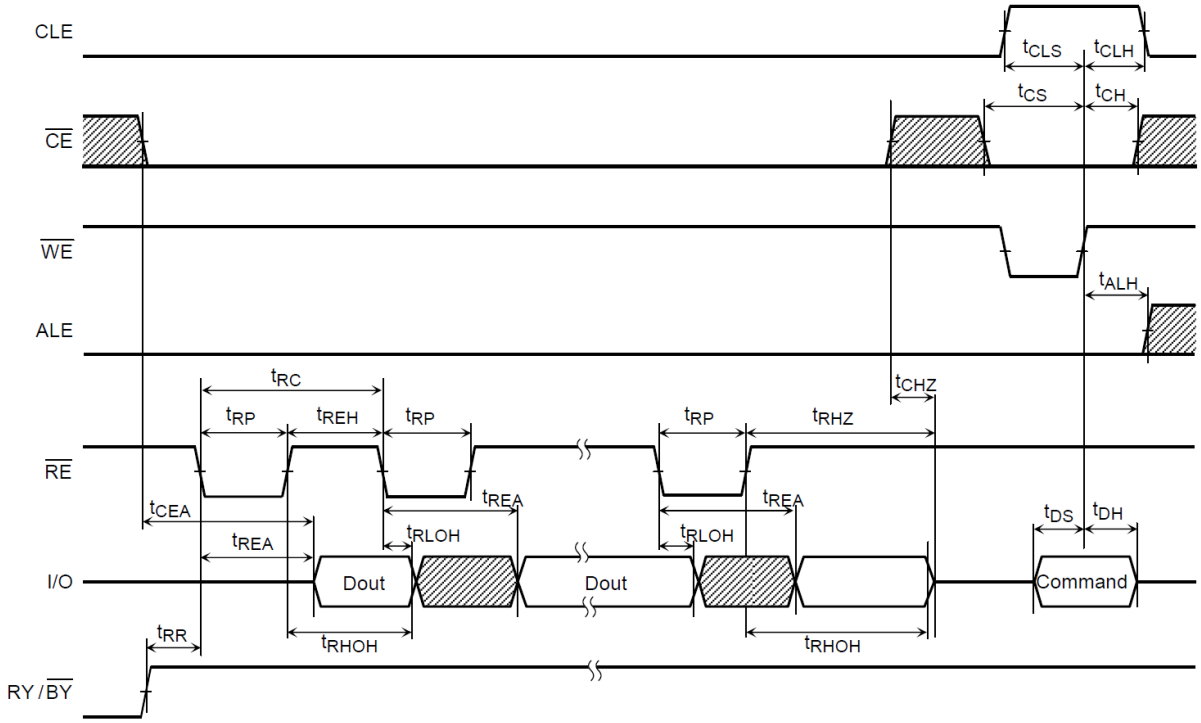
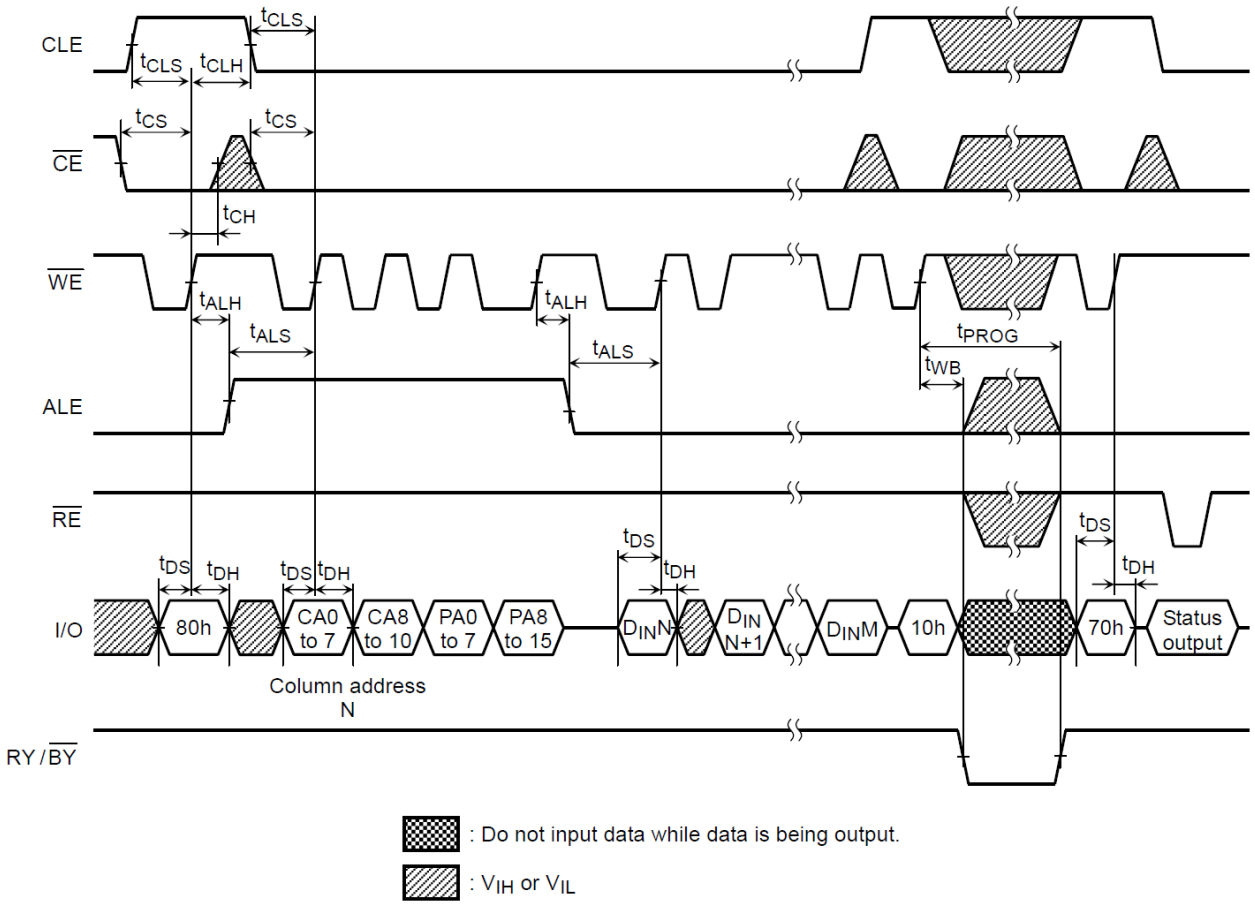
Data Output Timing Diagram

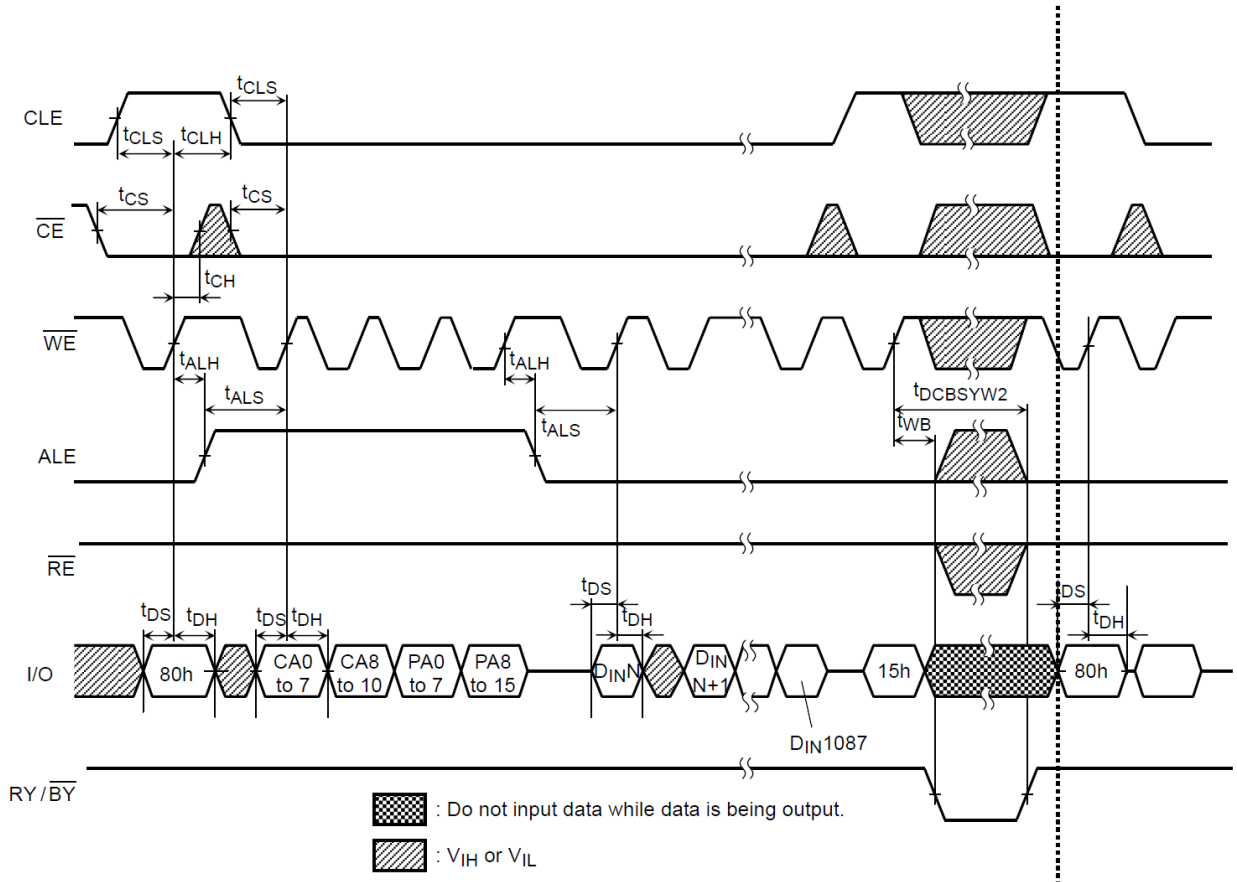


Auto-Program Operation Timing Diagram



*: M: up to 1087

Auto-Program Operation with Data Cache Timing Diagram (1/3)



CA0 to CA10 is 0 in this diagram.

1

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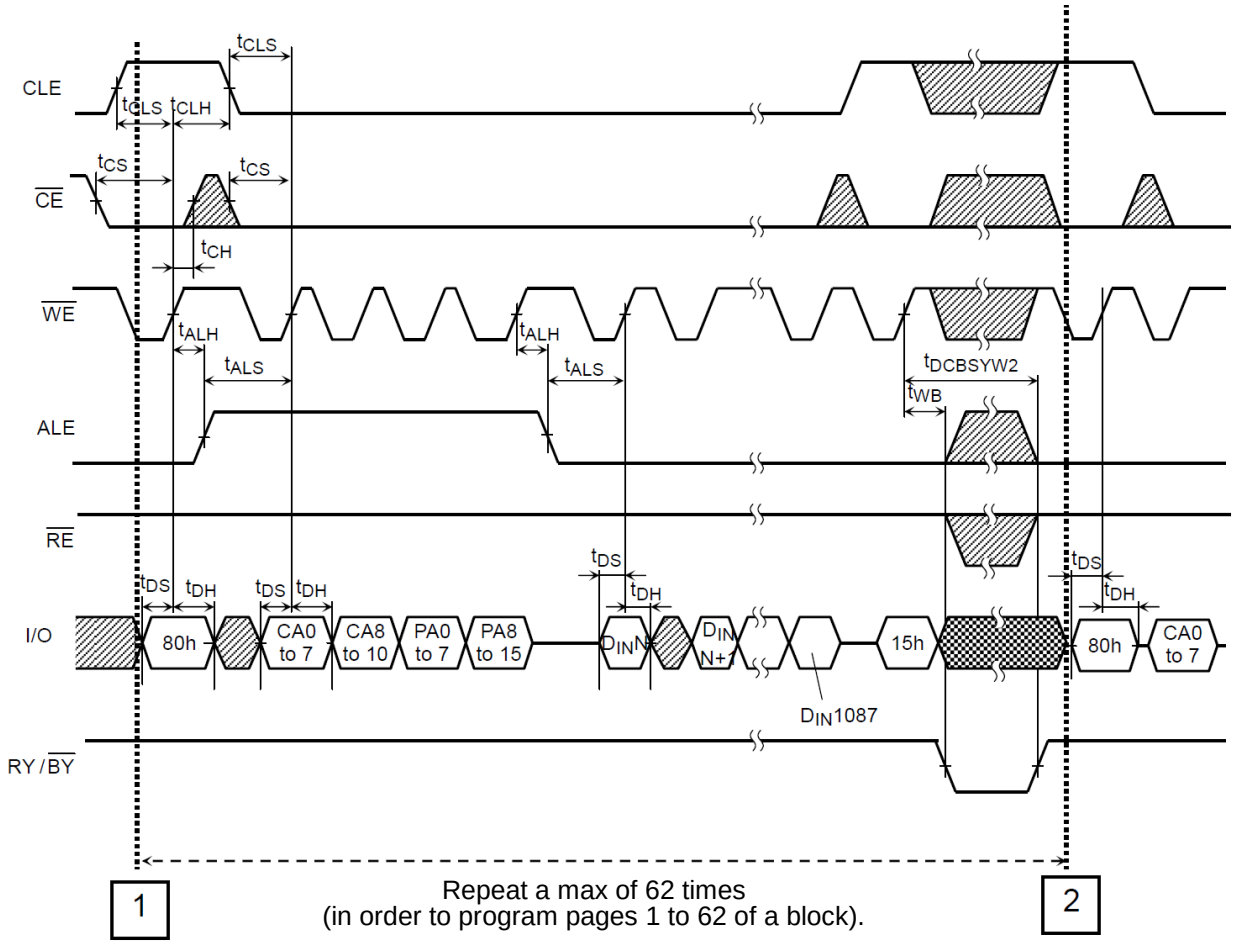
Auto-Program Operation with Data Cache Timing Diagram (2/3)



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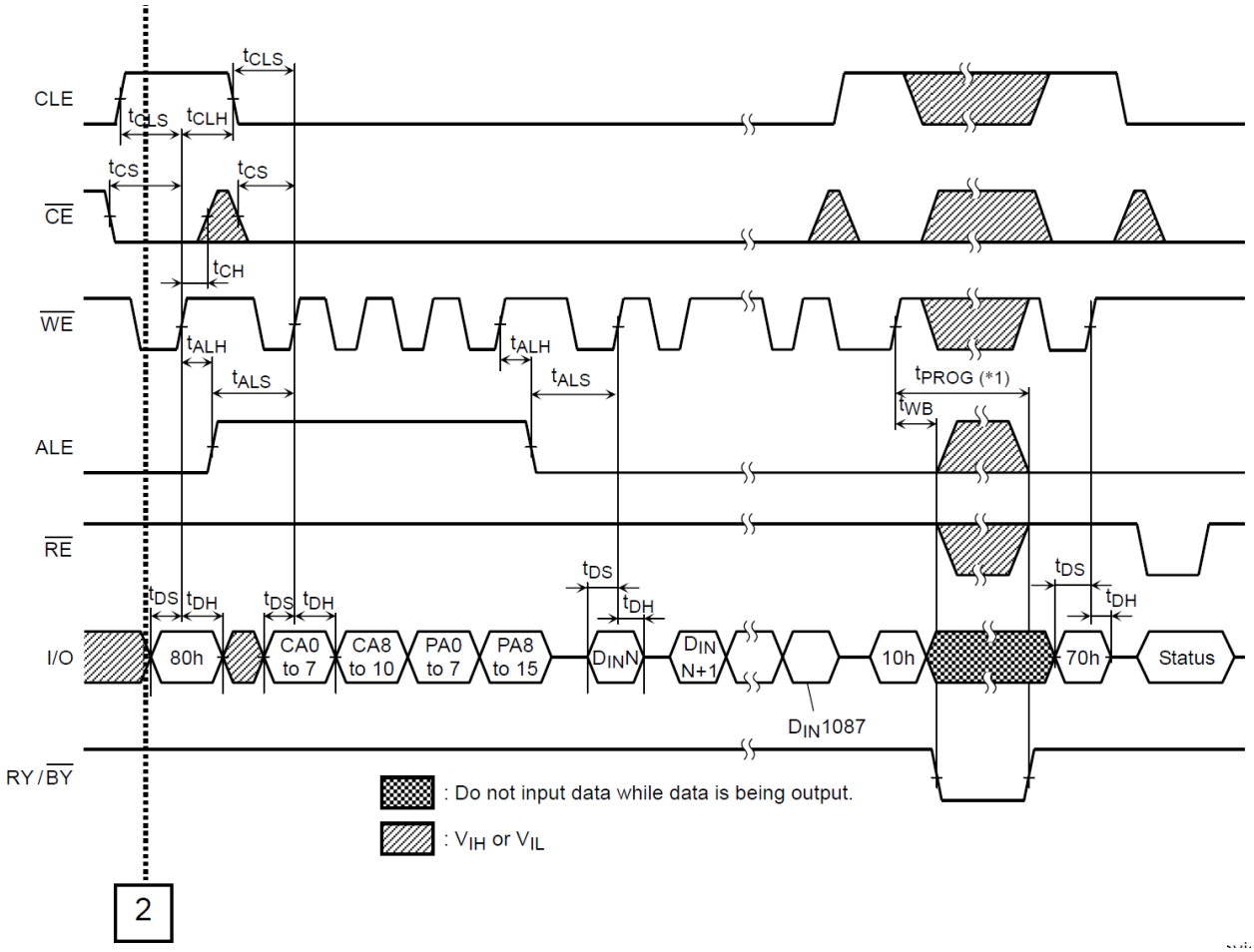
Auto-Program Operation with Data Cache Timing Diagram (3/3)



(*1)

tPROG: Since the last page programming by 10h command is initiated after the previous cache program, the tPROG during cache programming is given by the following equation.

tPROG = tPROG of the last page + tPROG of the previous page − A

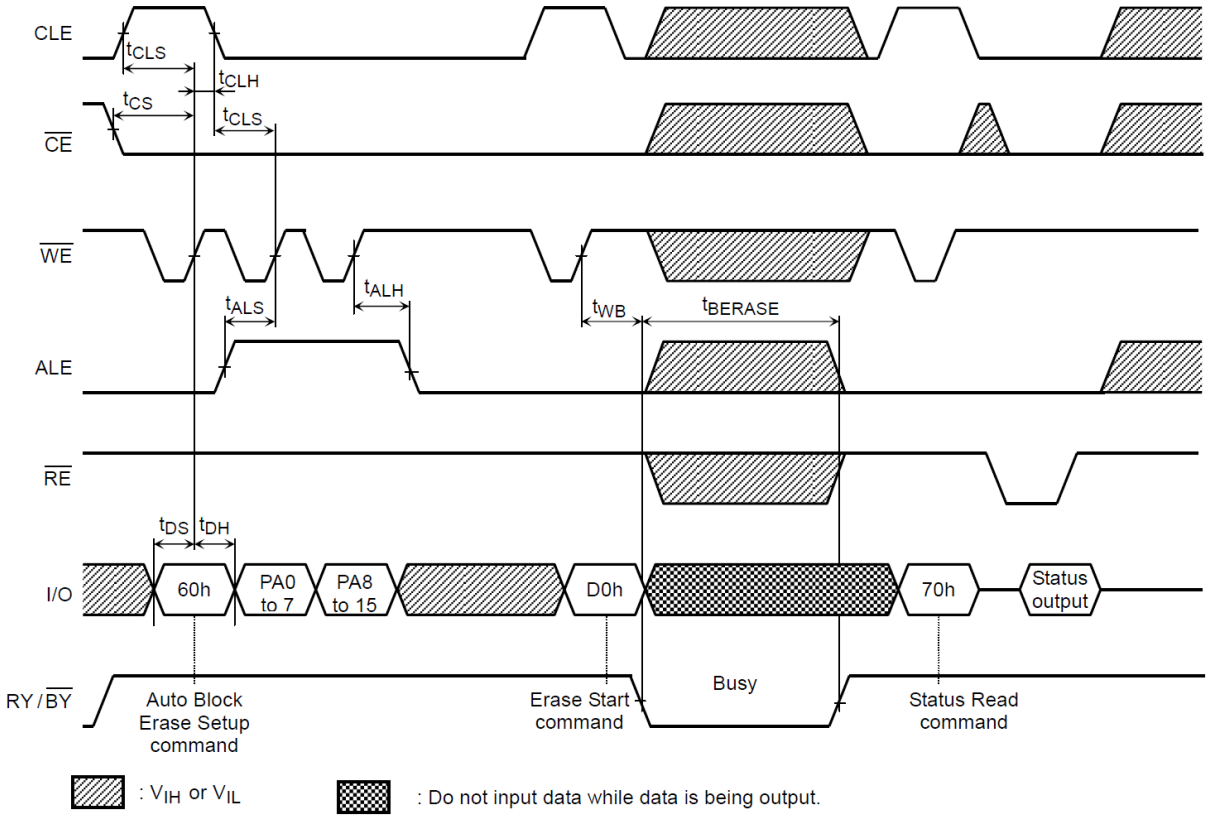
A = (command input cycle + address input cycle + data input cycle time of the last page)

If “A” exceeds the tPROG of previous page, tPROG of the last page is tPROG max.

NOTE: Make sure to terminate the operation with 80h-10h- command sequence.

If the operation is terminated by 80h-15h command sequence, monitor I/O 6 (Ready / Busy) by issuing Status Read command (70h) and make sure the previous page program operation is completed. If the page program operation is completed issue FFh reset before next operation.

Auto Block Erase Timing Diagram



ID Read Operation Timing Diagram

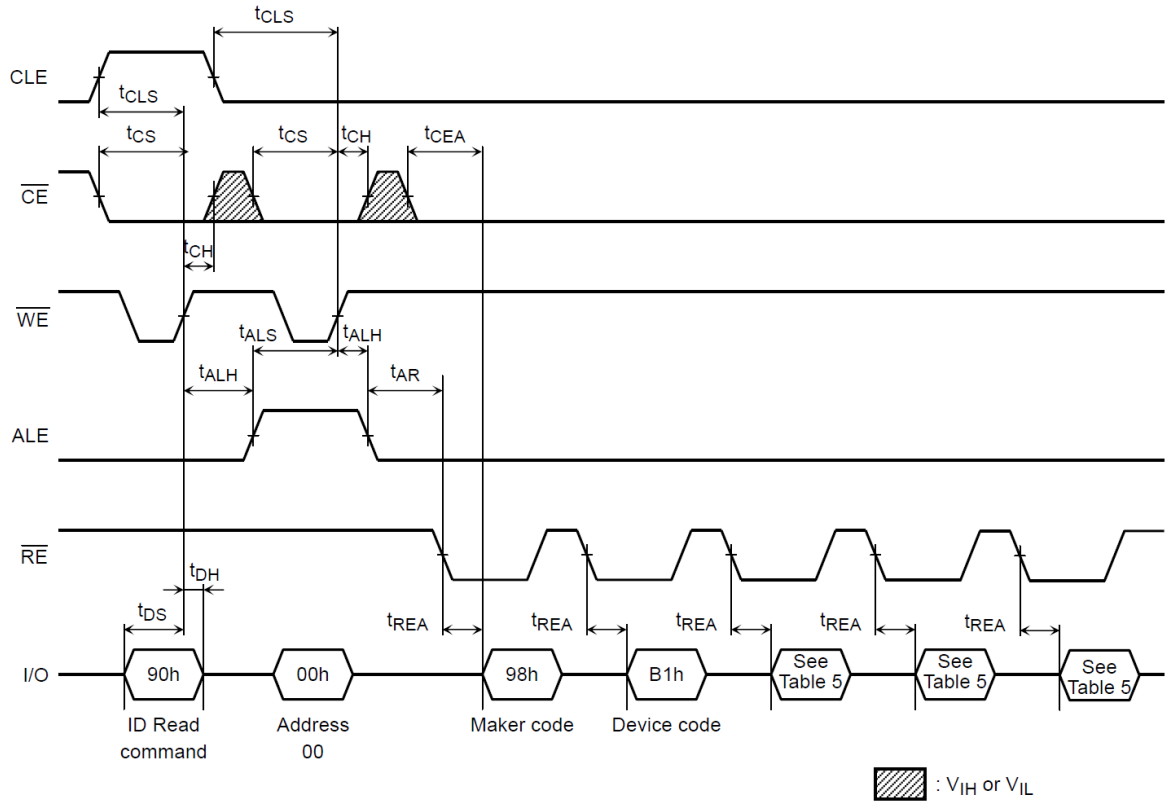


Table 5: ID Definition Table

512Mb(X16) LPDDR

Descriptions

The 512Mb Mobile LPDDR SDRAM is a high-speed CMOS, dynamic random-access memory containing 536,870,912 bits. It is internally configured as a quad-bank DRAM.

The 512Mb chip is organized as 8Mbit x 4 banks x 16 I/O. Each of the x16's 134,217,728-bit banks is organized as 8,192 rows by 1,024 columns by 16 bits. To achieve high-speed operation, our LPDDR SDRAM uses the double data rate architecture and adopt 2n-prefetch interface designed to transfer two data per clock cycle at the I/O pins.

The chip is designed to comply with all key Mobile Double-Data-Rate SDRAM key features. All of the control and address inputs are synchronized with a pair of externally supplied differential clocks, and latched at the cross point of differential clocks (CK rising and $\overline{CK}$ falling). The input data is registered at both edges of DQS, and the output data is referenced to both edges of DQS, as well as to both edges of CK. DQS is a bidirectional data strobe signal, transmitted by the LPDDR SDRAM during READs (edge-aligned with data), and by the memory controller during WRITEs (center-aligned with data).

LPDDR SDRAM, Read and Write access are burst oriented. The address bits registered coincident with the ACTIVE command to select the row in the specific bank. And then the address bits registered with the READ or WRITE command to select the starting column location in the bank for the burst access. The burst length can be programmed as 2, 4, 8 or 16. An Auto Precharge function may be enabled to provide a self-timed row precharge that is initiated at the end of burst access.

LPDDR SDRAM with Auto Refresh mode, and the Power-down mode for power saving. And the Deep Power Down Mode can achieve the maximum power reduction by removing the memory array power within Low Power DDR SDRAM. With this feature, the system can cut off almost all DRAM power without adding the cost of a power switch and giving up month-board power-line layout flexibility. Self Refresh mode with Temperature Compensated Self Refresh (TCSR) and Partial Array Self Refresh (PASR) options, which allow users to achieve additional power saving. The TCSR and PASR options can be programmed via the extended mode register. The two features may be combined to achieve even greater power saving. The DLL that is typically used on standard DDR devices is not necessary on the Mobile DDR SDRAM. It has been omitted to save power.

All inputs are LVCMOS compatible. Devices will have a V_{DD} and V_{DDQ} supply of 1.8V (nominal).

Absolute Maximum DC Ratings

Symbol	Parameter	Min	Max	Units
V_{DD} / V_{DDQ}	V_{DD} / V_{DDQ} supply voltage relative to Vss	-1.0	2.4	V
Vin	Voltage on any pin relative to Vss	-0.5	2.4 or (V_{DDQ} + 0.3V), Whichever is less	V
Tstg	Storage Temperature (plastic)	-55	+150	°C

Notes:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM.
3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times. V_{DDQ} must not exceed V_{DD}.

Input / Output Capacitance

Symbol	Parameter	Min	Max	Unit	Notes
CCK	Input capacitance: CK, $\overline{CK}$	1.5	3.0	pF	
CDCK	Input capacitance delta: CK, $\overline{CK}$	-	0.25	pF	2
CI	Input capacitance, all other input-only pins	1.5	3.0	pF	
CDI	Input capacitance delta, all other input-only pins	-	0.5	pF	2
CIO	Input/output capacitance, DQ, DM, DQS	3.0	5.0	pF	
CDIO	Input/output capacitance delta, DQ, DM, DQS	-	0.5	pF	3

Notes:

1. These values are guaranteed by design and are tested on a sample base only.
2. These capacitance values are for single monolithic devices only. Multiple die packages will have parallel capacitive loads.
3. Input capacitance is measured according to JEP147 procedure for measuring capacitance using a vector network analyzer. VDD, VDDQ are applied and all other pins (except the pin under test) floating. DQs should be in high impedance state. This may be achieved by pulling CKE to low level.
4. Although DM is an input-only pin, the input capacitance of this pin must model the input capacitance of the DQ and DQS pins. This is required to match signal propagation times of DQ, DQS and DM in the system.

AC/DC Electrical Characteristics and Operating Conditions

Apply Note 1-3 to whole the table.

Symbol	Parameter	Min	Max	Unit	Notes
V_{DD}	Supply voltage	1.70	1.95	V	-
V_{DDQ}	I/O Supply voltage	1.70	1.95	V	-
Address and Command inputs					
V_{IH}	Input voltage high	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	-
V_{IL}	Input voltage low	-0.3	0.2 x V_{DDQ}	V	-
Clock inputs (CK, $\overline{CK}$)					
V_{IN}	DC input voltage	-0.3	V_{DDQ} + 0.3	V	-
$V_{ID(DC)}$	DC input differential voltage	0.4 x V_{DDQ}	V_{DDQ} + 0.6	V	2
$V_{ID(AC)}$	AC Input Differential Voltage	0.6 x V_{DDQ}	V_{DDQ} + 0.6	V	2
V_{IX}	AC Differential Crosspoint Voltage	0.4 x V_{DDQ}	0.6 x V_{DDQ}	V	3
Data inputs					
$V_{IH(DC)}$	DC input high voltage	0.7 x V_{DDQ}	V_{DDQ} + 0.3	V	-
$V_{IL(DC)}$	DC input low voltage	-0.3	0.3 x V_{DDQ}	V	-
$V_{IH(AC)}$	AC input high voltage	0.8 x V_{DDQ}	V_{DDQ} + 0.3	V	-
$V_{IL(AC)}$	AC input low voltage	-0.3	0.2 x V_{DDQ}	V	-
Data outputs					
V_{OH}	DC output high voltage: Logic 1 (I_{OH} = -0.1mA)	0.9 x V_{DDQ}	-	V	-
V_{OL}	DC output low voltage: Logic 0 (I_{OL} = -0.1mA)	-	0.1 x V_{DDQ}	V	-
Leakage current					
I_I	Input leakage current Any input 0 $\leqq$ V_{IN} $\leqq$ V_{DD}, All other pins not under test = 0V	-1	1	uA	
I_{OZ}	Output leakage current DQs are disabled; 0 $\leqq$ V_{OUT} $\leqq$ V_{DDQ}	-5	5	uA	

Notes:

1. All voltages referenced to VSS and VSSQ must be same potential.
2. VID(DC) and VID(AC) are the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$.
3. The value of VIX is expected to be 0.5 * VDDQ and must track variations in the DC level of the same.

IDD Specifications and Measurement Conditions (32Mx16)

Notes 1 – 5 apply to all the parameters/conditions in this table

Symbol	Parameter/Condition		LPDDR400	Unit	Notes
IDD0	**Operating one bank active-precharge current:** tRC = tRCmin; tCK = tCKmin; CKE is HIGH; $\overline{CS}$ is HIGH between valid commands; address inputs are SWITCHING; data bus inputs are STABLE		70	mA	6
IDD2P	**Precharge power-down standby current:** all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE		300	uA	7,8
IDD2PS	**Precharge power-down standby current with clock stopped:** all banks idle, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		300	uA	7
IDD2N	**Precharge non power-down standby current:** all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE		15	mA	9
IDD2NS	**Precharge non power-down standby current with clock stopped:** all banks idle, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		10	mA	9
IDD3P	**Active power-down standby current:** one bank active, CKE is LOW; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE		5	mA	8
IDD3PS	**Active power-down standby current with clock stopped:** one bank active, CKE is LOW; $\overline{CS}$ is HIGH, CK = LOW, CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		4	mA	
IDD3N	**Active non power-down standby current:** one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, tCK = tCKmin; address and control inputs are SWITCHING; data bus inputs are STABLE		15	mA	6
IDD3NS	**Active non power-down standby current with clock stopped:** one bank active, CKE is HIGH; $\overline{CS}$ is HIGH, CK = LOW, CK = HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE		10	mA	6
IDD4R	**Operating burst read current:** one bank active; BL=4; CL=3; tCK = tCKmin; continuous read bursts; *I*OUT = 0 mA address inputs are SWITCHING; 50% data change each burst transfer		115	mA	6
IDD4W	**Operating burst write current:** one bank active; BL=4; tCK = tCKmin; continuous write bursts; address inputs are SWITCHING; 50% data change each burst transfer		115	mA	6
IDD5	**Auto Refresh current:** tCK = tCKmin; burst refresh; CKE is HIGH; address and control inputs are SWITCHING; data bus inputs are STABLE	tRC = tRFC	95	mA	10
IDD5A		tRC = tREFI	3	mA	10,11
IDD8	**Deep power-down current:** Address and control inputs are STABLE; data bus inputs are STABLE	25℃	10	uA	7,13
		85℃	20	uA	7

IDD6 Self-refresh and Partial Array Refresh current

Notes 1 – 5, 7, and 12 apply to all the parameters/conditions in this table

Symbol	Parameter/Condition	Temperature	PASR	Typical	Unit
IDD6	**Self refresh current:** CKE=LOW; ^{t}CK=^{t}CK(min); Address and control inputs are stable; Data bus inputs are stable.	85℃	Full Array	600	uA
			1/2 Array	480	uA
			1/4 Array	420	uA
			1/8 Array	420	uA
			1/16 Array	400	uA
		45℃	Full Array	300	uA
			1/2 Array	260	uA
			1/4 Array	250	uA
			1/8 Array	250	uA
			1/16 Array	250	uA

IDD Notes:

1. All voltages referenced to V_{SS}.
2. Tests for I_{DD} may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage and temperature range specified.
3. Timing and I_{DD} tests may use a V_{IL}-to-V_{IH} swing of up to 1.5V in the test environment, but input timing is still referenced to $V_{DDQ}/2$ (or, to the crossing point for CK and $\overline{CK}$). The output timing reference voltage level is $V_{DDQ}/2$.
4. I_{DD} is dependent on output loading and cycle rates. Specified values are obtained with minimum cycle time with the outputs open.
5. I_{DD} specifications are tested after the device is properly initialized, and are averaged at the defined cycle rate.
6. MIN (^{t}RC or ^{t}RFC) for IDD measurements is the smallest multiple of ^{t}CK that meets the minimum absolute value for the respective parameter. ^{t}RAS (MAX) for IDD measurements is the largest multiple of ^{t}CK that meets the maximum absolute value for ^{t}RAS.
7. Measurement is taken 500ms after entering into this operating mode to provide settling time for the tester.
8. V_{DD} must not vary more than 4 % if CKE is not active while any bank is active.
9. IDD2N specifies DQ, DQS, and DM to be driven to a valid HIGH or LOW logic level.
10. CKE must be active (HIGH) during the entire time a REFRESH command is executed. From the time the AUTO REFRESH command is registered, CKE must be active at each rising clock edge until ^{t}RFC later.
11. This limit is a nominal value and does not result in a fail. CKE is HIGH during REFRESH command period (^{t}RFC [MIN]) else CKE is LOW (for example, during standby).
12. Values for IDD6 85°C are guaranteed for the entire temperature range.
13. IDD8 are typical values.

AC Timings

Note 1-9 apply to all of the parameters in this table

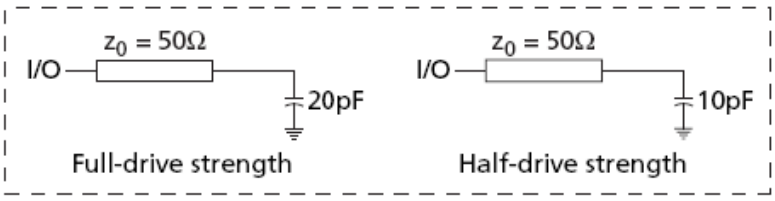
Symbol	Parameter		LPDDR400		Unit	Notes
			Min	Max		
tAC	Access window of DQs from CK,$\overline{CK}$		2.0	5.0	ns	
tDQSCK	Access window of DQS from CK, $\overline{CK}$		2.0	5.0	ns	
tCH	CK high-level width		0.45	0.55	tCK	
tCL	CK low-level width		0.45	0.55	tCK	
tHP	Half-clock period		min(tCH,tCL)	-	ns	10, 11
tCK	Clock cycle time	CL=3	5.0	100	ns	12
		CL=2(optional)	12	100		
tDSf	DQ and DM input setup time relative to DQS (fast slew rate)		0.48	-	ns	13,14,15
tDSs	DQ and DM input setup time relative to DQS (slow slew rate)		0.58	-	ns	13,14,16
tDHf	DQ and DM input hold time relative to DQS (fast slew rate)		0.48	-	ns	13,14,15
tDHs	DQ and DM input hold time relative to DQS (slow slew rate)		0.58	-	ns	13,14,16
tDIPW	DQ and DM input pulse width		1.8	-	ns	17
tISf	Address and Control input setup time (fast slew rate)		0.9	-	ns	15,18
tISs	Address and Control input setup time (slow slew rate)		1.1	-	ns	16,18
tIHf	Address and Control input hold time (fast slew rate)		0.9	-	ns	15,18
tIHs	Address and Control input hold time (slow slew rate)		1.1	-	ns	16,18
tIPW	Address and Control input pulse width		2.3	-	ns	17
tLZ	Data-out Low-z window from CK, $\overline{CK}$		1.0	-	ns	19
tHZ	Data-out high-z window from CK, $\overline{CK}$		-	5.0	ns	19
tDQSQ	DQS-DQ skew, DQS to last DQ valid, per group, per access		-	0.4	ns	20
tQH	DQ-DQS hold, DQS to first DQ to go non-valid, per access		tHP - tQHS	-	ns	11

Symbol	Parameter		LPDDR400		Unit	Notes
			Min	Max		
tQHS	Data Hold Skew Factor		-	0.5	ns	11
tDQSS	WRITE command to first DQS latching transition		0.75	1.25	tCK	
tDQSH	DQS input high pulse width		0.4	-	tCK	
tDQSL	DQS input low pulse width		0.4	-	tCK	
tDSS	DQS falling edge to CK setup time		0.2	-	tCK	
tDSH	DQS falling edge hold time from CK		0.2	-	tCK	
tMRD	Load MODE Register command cycle time		2	-	tCK	
tWPRES	DQS write preamble setup time		0	-	ns	21
tWPST	DQS write postamble		0.4	0.6	tCK	22
tWPRE	DQS write preamble		0.25	-	tCK	
tRPRE	DQS read preamble	CL=3	0.9	1.1	tCK	23
		CL=2(optional)	0.5	1.1	tCK	23
tRPST	DQS read postamble		0.4	0.6	tCK	
tRAS	ACTIVE to PRECHARGE command		40	70,000	ns	
tRC	ACTIVE to ACTIVE / ACTIVE to AUTO REFRESH command period		55	-	ns	
tRFC	Auto Refresh command period		110	-	ns	
tRCD	ACTIVE to READ or WRITE delay		15	-	ns	24
tRP	PRECHARGE command period		15	-	ns	24
tRRD	ACTIVE *bank-a* to ACTIVE *bank-b* command		10	-	ns	
tWR	Write recovery time		15	-	ns	
tDAL	Auto precharge write recovery + precharge time		-	-	-	26
tWTR	Internal WRITE to READ command delay		2	-	tCK	
tXSR	Exit SELF REFRESH to first valid command		200	-	ns	27
tXP	Exit power-down mode to first valid command		25	-	ns	28
tCKE	CKE min. pulse width (high and low pulse width)		2	-	tCK	

Symbol	Parameter	LPDDR400		Unit	Notes
		Min	Max		
tREF	Refresh period	-	64	ms	
tREFI	Average periodic refresh interval	-	7.8	us	29, 30
tSRR	SRR-to-READ	2	-	tCK	
tSRC	Read of SRR to next valid command	CL+1	-	tCK	
tTQ	Internal temperature sensor valid temperature output enable	2	-	ms	31

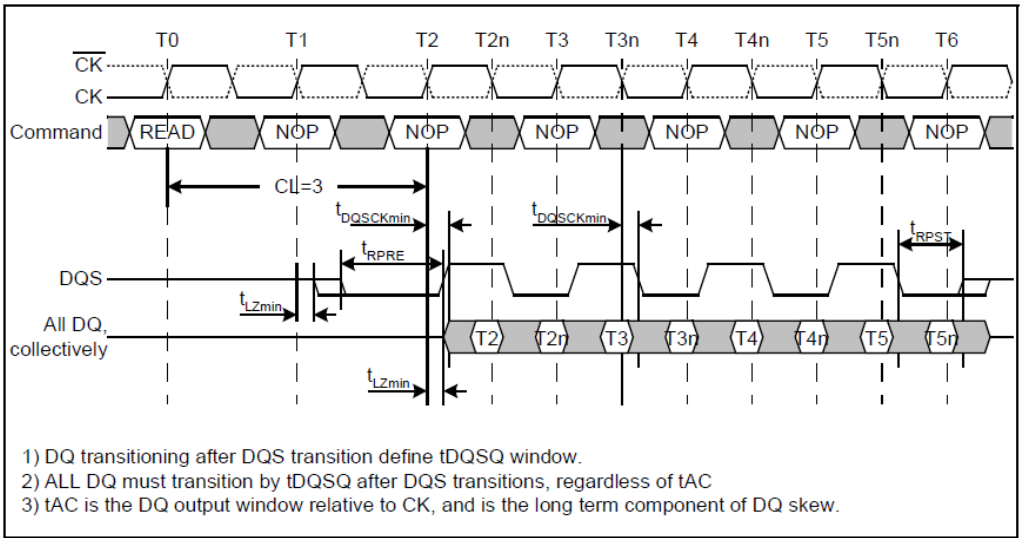
Notes:

1. All voltages referenced to Vss.
2. All parameters assume proper device initialization.
3. Tests for AC timing, and electrical AC and DC characteristics may be conducted at nominal supply voltage levels, but the related specifications and device operation are guaranteed for the full voltage range specified.
4. The circuit shown below represents the timing reference load used in defining the relevant timing parameters of the device. It is not intended to be either a precise representation of the typical system environment or a depiction of the actual load presented by a production tester. System designers will use IBIS or other simulation tools to correlate the timing reference load to system environment. Specifications are correlated to production test conditions (generally a coaxial transmission line terminated at the tester electronics). For the half-strength driver with a nominal 10pF load, parameters ^{t}AC and ^{t}QH are expected to be in the same range. However, these parameters are not subject to production test but are estimated by design/characterization. Use of IBIS or other simulation tools for system design validation is suggested.



5. The CK, $\overline{CK}$ input reference voltage level (for timing referenced to CK, $\overline{CK}$) is the point at which CK and $\overline{CK}$ cross; the input reference voltage level for signals other than CK, $\overline{CK}$ is $V_{DDQ}/2$.
6. The timing reference voltage level is VDDQ/2.
7. AC and DC input and output voltage levels are defined in the section for Electrical Characteristics and AC/DC operating conditions.
8. A CK/$\overline{CK}$ differential slew rate of 2.0 V/ns is assumed for all parameters.

9. CAS latency definition: with CL = 3 the first data element is valid at (2 * tCK + tAC) after the clock at which the READ command was registered (see figure); with CL = 2 the first data element is valid at (tCK + tAC) after the clock at which the READ command was registered; with CL = 4 the first data element is valid at (3 * tCK + tAC) after the clock at which the READ command was registered.



10. Min (tCL, tCH) refers to the smaller of the actual clock low time and the actual clock high time as provided to the device (i.e. this value can be greater than the minimum specification limits for tCL and tCH)

11. tQH = tHP - tQHS, where tHP = minimum half clock period for any given cycle and is defined by clock high or clock low (tCL, tCH). tQHS accounts for 1) the pulse duration distortion of on-chip clock circuits; and 2) the worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are, separately, due to data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers.

12. The only time that the clock frequency is allowed to change is during clock stop, power-down or self-refresh modes.

13. The transition time for DQ, DM and DQS inputs is measured between VIL(DC) to VIH(AC) for rising input signals, and VIH(DC) to VIL(AC) for falling input signals.

14. DQS, DM and DQ input slew rate is specified to prevent double clocking of data and preserve setup and hold times. Signal transitions through the DC region must be monotonic.

15. Input slew rate ≥ 1.0 V/ns.

16. Input slew rate ≥ 0.5 V/ns and < 1.0 V/ns.

17. These parameters guarantee device timing but they are not necessarily tested on each device.

18. The transition time for address and command inputs is measured between VIH and VIL.

19. tHZ and tLZ transitions occur in the same access time windows as valid data transitions. These parameters are not referred to a specific voltage level, but specify when the device is no longer driving (HZ), or begins driving (LZ).

20. tDQSQ consists of data pin skew and output pattern effects, and p-channel to n-channel variation of the output drivers for any given cycle.

21. The specific requirement is that DQS be valid (HIGH, LOW, or some point on a valid transition) on or before the corresponding CK edge. A valid transition is defined as monotonic and meeting the input slew rate specifications of the device. When no writes were previously in progress on the bus, DQS will be transitioning from Hi-Z to logic LOW. If a previous write was in progress, DQS could be HIGH, LOW, or transitioning from HIGH to LOW at this time, depending on tDQSS.

22. The maximum limit for this parameter is not a device limit. The device operates with a greater value for this parameter, but system performance (bus turnaround) will degrade accordingly.
23. A low level on DQS may be maintained during High-Z states (DQS drivers disabled) by adding a weak pull-down element in the system. It is recommended to turn off the weak pull-down element during read and write bursts (DQS drivers enabled).
24. Speed bin (CL - tRCD - tRP) = 3 - 3 - 3
25. Speed bin (CL - tRCD - tRP) = 3 - 4 - 4 (all speed bins except LPDDR200)
26. tDAL = (tWR/tCK) + (tRP/tCK): for each of the terms, if not already an integer, round to the next higher integer.
27. There must be at least two clock pulses during the tXSR period.
28. There must be at least one clock pulse during the tXP period.
29. tREFI values are dependent on density and bus width.
30. A maximum of 8 Refresh commands can be posted to any given LPDDR, meaning that the maximum absolute interval between any Refresh command and the next Refresh command is 8*tREFI.
31. It's not supported for package level.

OUTPUT SLEW RATE CHARACTERISTICS

PARAMETER	MIN	MAX	UNIT	NOTES
Pull-up and Pull-Down Slew Rate for Full Strength Driver	0.7	2.5	V/ns	1,2
Pull-up and Pull-Down Slew Rate for Three-Quarters Strength Driver	0.5	1.75	V/ns	1,2
Pull-up and Pull-Down Slew Rate for Half Strength Driver	0.3	1.0	V/ns	1,2
Output Slew rate Matching ratio (Pull-up to Pull-down)	0.7	1.4	-	3

NOTES:

1. Measured with a test load of 20 pF connected to VSSQ.

2. Output slew rate for rising edge is measured between VILD(DC) to VIHD(AC) and for falling edge between VIHD(DC) to VILD(AC).

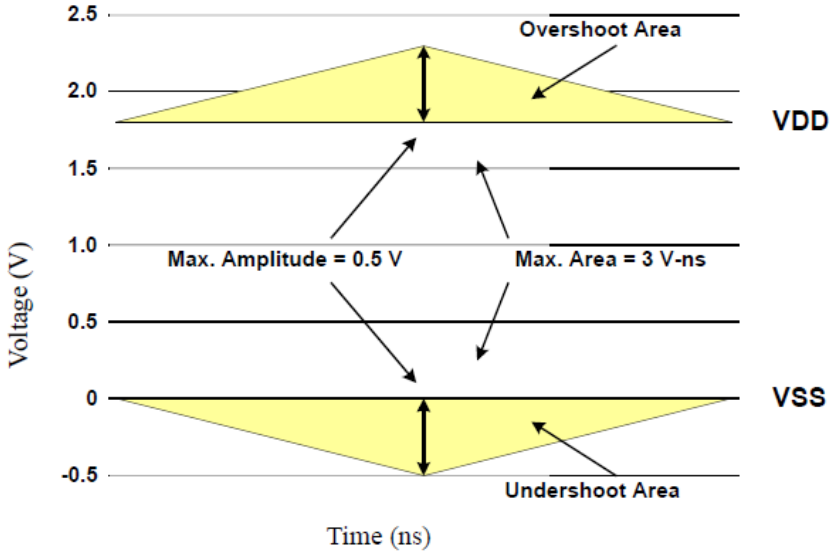
3. The ratio of pull-up slew rate to pull-down slew rate is specified for the same temperature and voltage, over the entire temperature and voltage range. For a given output, it represents the maximum difference between pull-up and pull-down drivers due to process variation.

AC Overshoot/Undershoot Specification

PARAMETER	SPECIFICATION
Maximum peak amplitude allowed for overshoot	0.5 V
Maximum peak amplitude allowed for undershoot	0.5 V
The area between overshoot signal and VDD must be less than or equal to	3 V-ns
The area between undershoot signal and GND must be less than or equal to	3 V-ns

NOTES:
1. This specification is intended for devices with no clamp protection and is guaranteed by design.

AC Overshoot and Undershoot Definition



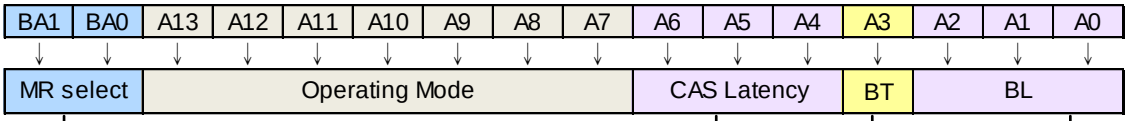
OUTPUT DRIVE STRENGTH CHARACTERISTICS

VOLTAGE [V]	FULL DRIVE STRENGTH				HALF DRIVE STRENGTH				THREE-QUARTERS DRIVE STRENGTH			
	PULL-DOWN CURRENT [mA]		PULL-UP CURRENT [mA]		PULL-DOWN CURRENT [mA]		PULL-UP CURRENT [mA]		PULL-DOWN CURRENT [mA]		PULL-UP CURRENT [mA]	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
0.00	0	0	0	0	0	0	0	0	0	0	0	0
0.10	2.8	18.53	-2.8	-18.53	1.27	8.42	-1.27	-8.42	1.96	12.97	-1.96	-12.97
0.20	5.6	26.8	-5.6	-26.8	2.55	12.3	-2.55	-12.3	3.92	18.76	-3.92	-18.76
0.30	8.4	32.8	-8.4	-32.8	3.82	14.95	-3.82	-14.95	5.88	22.96	-5.88	-22.96
0.40	11.2	37.05	-11.2	-37.05	5.09	16.84	-5.09	-16.84	7.84	25.94	-7.84	-25.94
0.50	14	40	-14	-40	6.36	18.2	-6.36	-18.2	9.8	28	-9.8	-28
0.60	16.8	42.5	-16.8	-42.5	7.64	19.3	-7.64	-19.3	11.76	29.75	-11.76	-29.75
0.70	19.6	44.57	-19.6	-44.57	8.91	20.3	-8.91	-20.3	13.72	31.2	-13.72	-31.2
0.80	22.4	46.5	-22.4	-46.5	10.16	21.2	-10.16	-21.2	15.68	32.55	-15.68	-32.55
0.85	23.8	47.48	-23.8	-47.48	10.8	21.6	-10.8	-21.6	16.66	33.24	-16.66	-33.24
0.90	23.8	48.5	-23.8	-48.5	10.8	22	-10.8	-22	16.66	33.95	-16.66	-33.95
0.95	23.8	49.4	-23.8	-49.4	10.8	22.45	-10.8	-22.45	16.66	34.58	-16.66	-34.58
1.00	23.8	50.05	-23.8	-50.05	10.8	22.73	-10.8	-22.73	16.66	35.04	-16.66	-35.04
1.10	23.8	51.35	-23.8	-51.35	10.8	23.21	-10.8	-23.21	16.66	35.95	-16.66	-35.95
1.20	23.8	52.65	-23.8	-52.65	10.8	23.67	-10.8	-23.67	16.66	36.86	-16.66	-36.86
1.30	23.8	53.95	-23.8	-53.95	10.8	24.14	-10.8	-24.14	16.66	37.77	-16.66	-37.77
1.40	23.8	55.25	-23.8	-55.25	10.8	24.61	-10.8	-24.61	16.66	38.68	-16.66	-38.68
1.50	23.8	56.55	-23.8	-56.55	10.8	25.08	-10.8	-25.08	16.66	39.59	-16.66	-39.59
1.60	23.8	57.85	-23.8	-57.85	10.8	25.54	-10.8	-25.54	16.66	40.5	-16.66	-40.5
1.70	23.8	59.15	-23.8	-59.15	10.8	26.01	-10.8	-26.01	16.66	41.41	-16.66	-41.41
1.80	—	60.45	—	-60.45	—	26.48	—	-26.48	—	42.32	—	-42.32
1.90	—	61.75	—	-61.75	—	26.95	—	-26.95	—	43.23	—	-43.23

NOTES:

1. Based on nominal impedance of 25 Ohms (Full Drive), 55 Ohms (Half Drive) and 36 Ohms(Three-Quarters) at VDDQ/2
2. The full variation in driver current from minimum to maximum due to process, temperature and voltage will lie within the outer bounding lines of the I-V curve.
3. The I-V current for the optional quarter drive strength is approximately 50% of the half drive strength.
4. The IV current for the Three-Quarters Strength Driver is approximately 70% of the full drive strength current.
5. Implementation and availability of Three-Quarters Strength Driver is optional for speed bins LPDDR333 and below.

Standard Mode Register definition



BA1	BA0	MR select
0	0	Standard MR
0	1	Status Register
1	0	Extended MR
1	1	Reserved

A3	Burst Type
0	Sequential
1	Interleaved

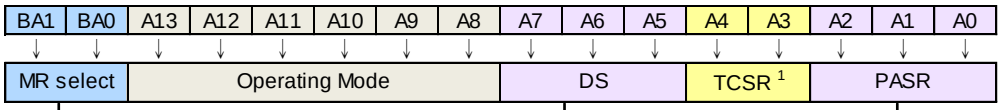
A6	A5	A4	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	BL
0	0	0	Reserved
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A13-A9	A8	A7	Operating Mode
0	0	0	Normal Operation
-	-	-	All other states reserved

NOTE 1: A logic 0 should be programmed to all unused / undefined address bits to ensure future compatibility.

Extended Mode Register Definition



BA1	BA0	MR select
0	0	Standard MR
0	1	Status Register
1	0	Extended MR
1	1	Reserved

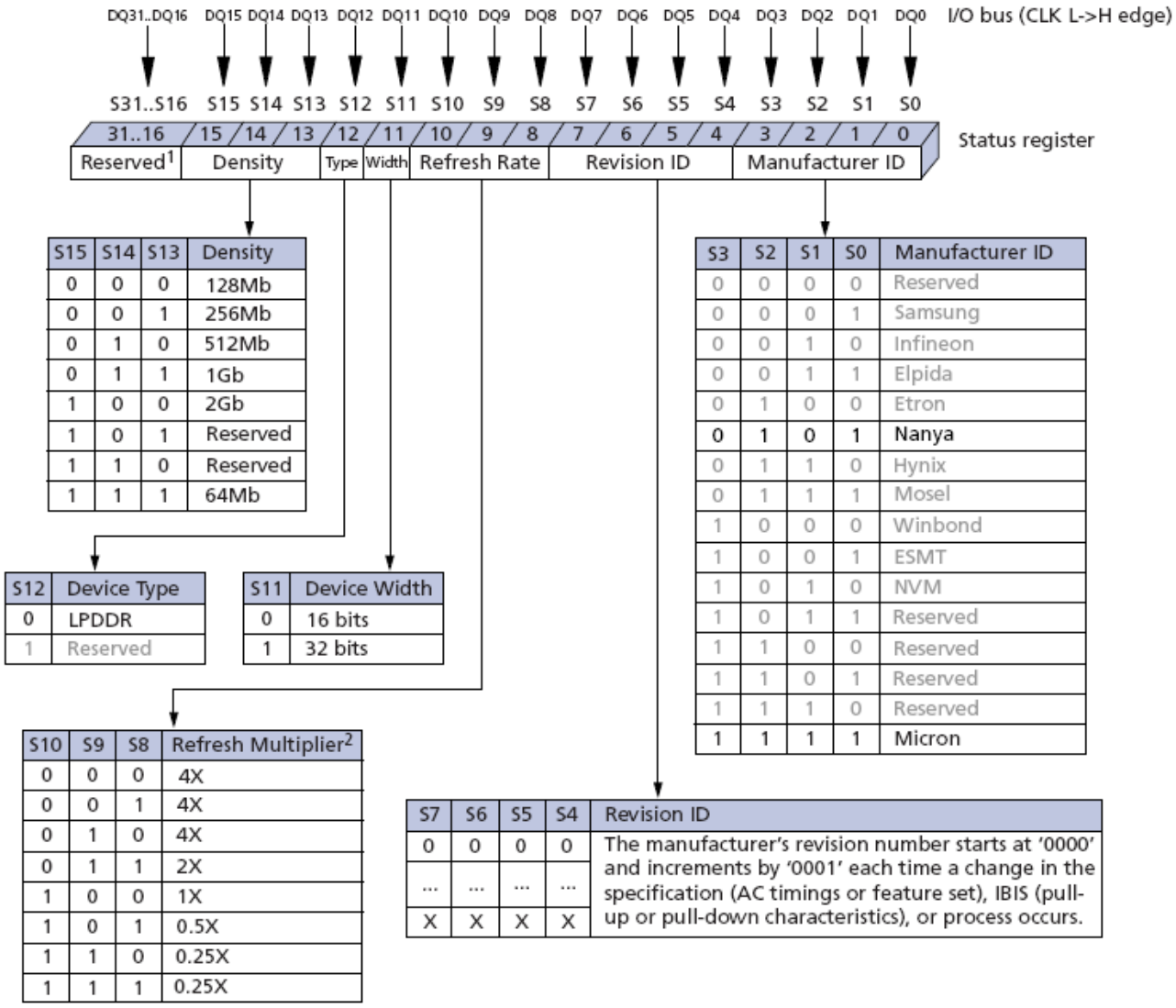
A7	A6	A5	Driver Strength
0	0	0	Full
0	0	1	Half
0	1	0	Quarter
0	1	1	Three-Quarters
1	0	0	Three-Quarters
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

A2	A1	A0	PASR
0	0	0	All banks
0	0	1	Half array(BA1=0)
0	1	0	1/4 array(BA1=BA0=0)
0	1	1	Reserved
1	0	0	Reserved
1	0	1	1/8 array (BA1=BA0=Row Addr MSB=0)
1	1	0	1/16 array (BA1=BA0=Row Addr 2 MSB=0)
1	1	1	Reserved

A13-A9	A8	Operating Mode
0	0	Normal Operation
-	-	All other states reserved

NOTE 1: On-die temperature sensor is used in place of TCSR. Setting these bits will have no effect.
NOTE 2: A logic 0 should be programmed to all unused / undefined address bits to ensure future compatibility.
NOTE 3: Implementation and availability of Three-Quarters Strength Driver is optional for speed bins LPDDR333 and below.

Status Read Register (SRR)



S15	S14	S13	Density
0	0	0	128Mb
0	0	1	256Mb
0	1	0	512Mb
0	1	1	1Gb
1	0	0	2Gb
1	0	1	Reserved
1	1	0	Reserved
1	1	1	64Mb

S3	S2	S1	S0	Manufacturer ID
0	0	0	0	Reserved
0	0	0	1	Samsung
0	0	1	0	Infineon
0	0	1	1	Elpida
0	1	0	0	Etron
0	1	0	1	Nanya
0	1	1	0	Hynix
0	1	1	1	Mosel
1	0	0	0	Winbond
1	0	0	1	ESMT
1	0	1	0	NVM
1	0	1	1	Reserved
1	1	0	0	Reserved
1	1	0	1	Reserved
1	1	1	0	Reserved
1	1	1	1	Micron

S12	Device Type
0	LPDDR
1	Reserved

S11	Device Width
0	16 bits
1	32 bits

S10	S9	S8	Refresh Multiplier[2]
0	0	0	4X
0	0	1	4X
0	1	0	4X
0	1	1	2X
1	0	0	1X
1	0	1	0.5X
1	1	0	0.25X
1	1	1	0.25X

S7	S6	S5	S4	Revision ID
0	0	0	0	The manufacturer's revision number starts at '0000' and increments by '0001' each time a change in the specification (AC timings or feature set), IBIS (pull-up or pull-down characteristics), or process occurs.
...	...	...	...	
X	X	X	X	

Status Register Definition

NOTES:

1. Reserved bits should be set to zero for future compatibility.
2. Refresh multiplier is based on the memory device's on-board temperature sensor. Required average periodic refresh interval = tREFI x multiplier.

Revision History

Rev	Page	Modified	Description	Released
1.0	-	-	Preliminary Release	07/2014
1.1	P3	Part numbering Guide	Renew NAND speed:300μs (was:250μs)	10/2014
	P4	Features	Add ECC.	
	P20	-	Modified ECC : 8 bit (was: TBD bit)	
1.2	P24-38	Power-on/off sequence & Timing Diagrams	New	04/2016
1.3	-	-	Official Release	09/2016

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