

Normally – OFF Silicon Carbide Junction Transistor

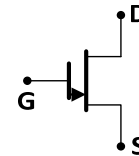
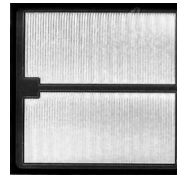
V_{DS}	=	600 V
$R_{DS(ON)}$	=	25 mΩ
I_D ($T_c = 25^\circ\text{C}$)	=	100 A
h_{FE} ($T_c = 25^\circ\text{C}$)	=	105

Features

- 250°C maximum operating temperature
- Gate Oxide Free SiC switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Co-efficient of $R_{DS,ON}$
- Suitable for connecting an anti-parallel diode

Advantages

- Compatible with Si MOSFET/IGBT gate-drivers
- > 20 μs Short-Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth



Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Values	Unit
Drain – Source Voltage	V_{DS}	$V_{GS} = 0\text{ V}$	600	V
Continuous Drain Current	I_D	$T_{VJ} < 250^\circ\text{C}$	50	A
Gate Peak Current	I_{GM}		10	A
Turn-Off Safe Operating Area	RBSOA	$T_{VJ} = 250^\circ\text{C}$, $I_G = 1\text{ A}$, Clamped Inductive Load	$I_{D,max} = 50$ @ $V_{DS} \leq V_{DSmax}$	A
Short Circuit Safe Operating Area	SCSOA	$T_{VJ} = 250^\circ\text{C}$, $I_G = 1\text{ A}$, $V_{DS} = 400\text{ V}$, Non Repetitive	20	μs
Reverse Gate – Source Voltage	V_{GS}		30	V
Reverse Drain – Source Voltage	V_{DS}		25	V
Operating and Storage Temperature	T_j, T_{stg}		-55 to 250	°C

Electrical Characteristics

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

On Characteristics

Drain – Source On Resistance	$R_{DS(ON)}$	$I_D = 50\text{ A}$, $I_G = 1000\text{ mA}$, $T_j = 25^\circ\text{C}$	25	mΩ
		$I_D = 50\text{ A}$, $I_G = 1000\text{ mA}$, $T_j = 125^\circ\text{C}$	39	
		$I_D = 50\text{ A}$, $I_G = 2000\text{ mA}$, $T_j = 175^\circ\text{C}$	43	
		$I_D = 50\text{ A}$, $I_G = 2000\text{ mA}$, $T_j = 250^\circ\text{C}$	62	
Gate Forward Voltage	$V_{GS(FWD)}$	$I_G = 1000\text{ mA}$, $T_j = 25^\circ\text{C}$	2.9	V
		$I_G = 1000\text{ mA}$, $T_j = 250^\circ\text{C}$	2.6	
DC Current Gain	β	$V_{DS} = 5\text{ V}$, $I_D = 50\text{ A}$, $T_j = 25^\circ\text{C}$	105	
		$V_{DS} = 5\text{ V}$, $I_D = 50\text{ A}$, $T_j = 125^\circ\text{C}$	77	
		$V_{DS} = 5\text{ V}$, $I_D = 50\text{ A}$, $T_j = 175^\circ\text{C}$	71	
		$V_{DS} = 5\text{ V}$, $I_D = 50\text{ A}$, $T_j = 250^\circ\text{C}$	69	

Off Characteristics

Drain Leakage Current	I_{DSS}	$V_R = 600\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 25^\circ\text{C}$	10	μA
		$V_R = 600\text{ V}$, $V_{GS} = 0\text{ V}$, $T_j = 250^\circ\text{C}$	100	
Gate – Source Leakage Current	I_{GSS}	$V_{GS} = -20\text{ V}$, $T_j = 25^\circ\text{C}$	20	nA

Capacitance Characteristics

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}$, $V_D = 100\text{ V}$, $f = 1\text{ MHz}$	6440	pF
Reverse Transfer/Output Capacitance	C_{rss}/C_{oss}	$V_D = 100\text{ V}$, $f = 1\text{ MHz}$	420	pF

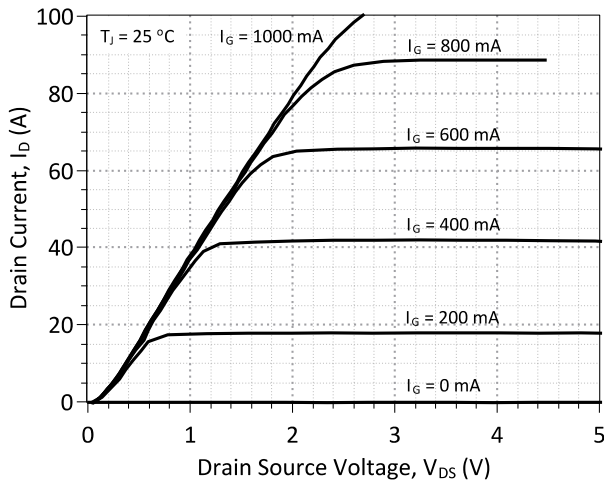


Figure 1: Typical Output Characteristics at 25 °C

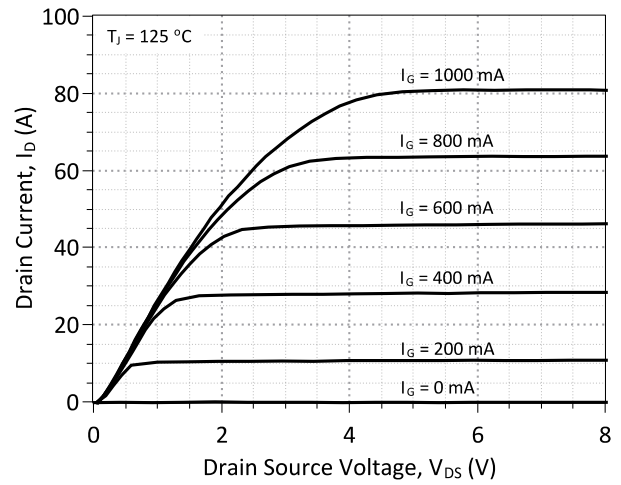


Figure 2: Typical Output Characteristics at 125 °C

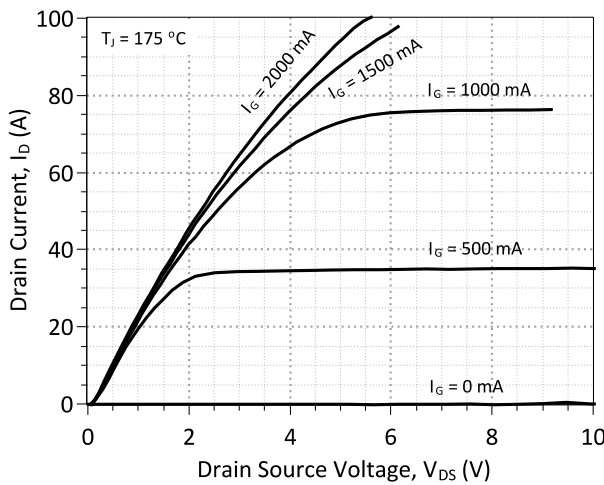


Figure 3: Typical Output Characteristics at 175 °C

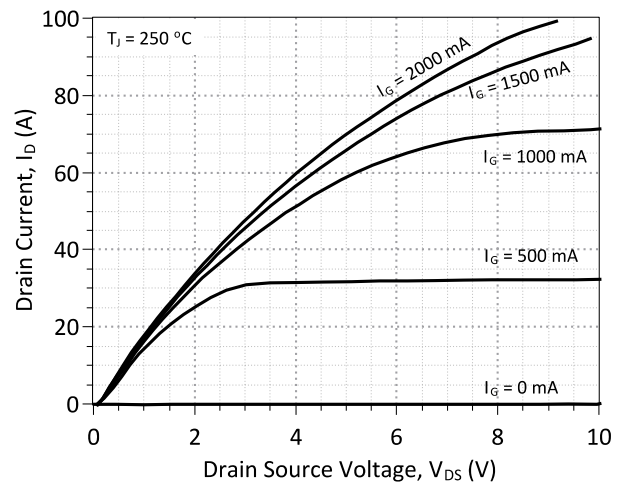


Figure 4: Typical Output Characteristics at 250 °C

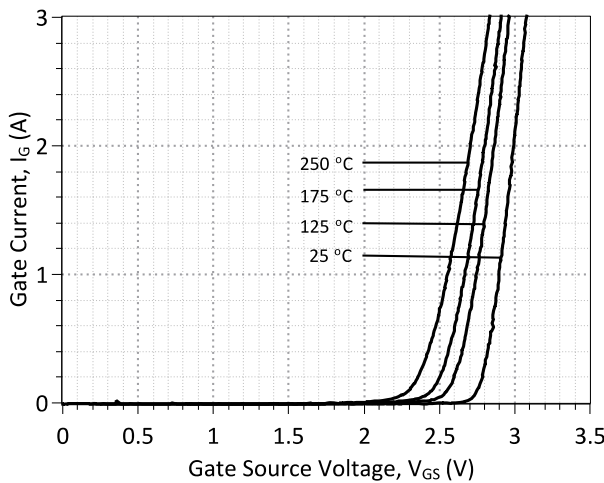


Figure 5: Typical Gate Source I-V Characteristics vs. Temperature

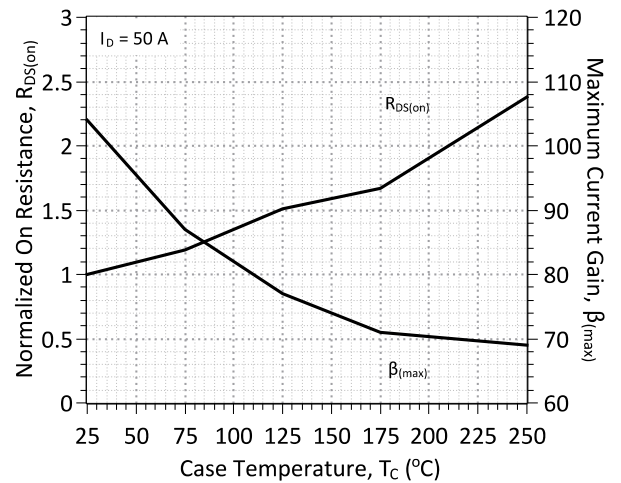


Figure 6: Normalized On-Resistance and Current Gain vs. Temperature

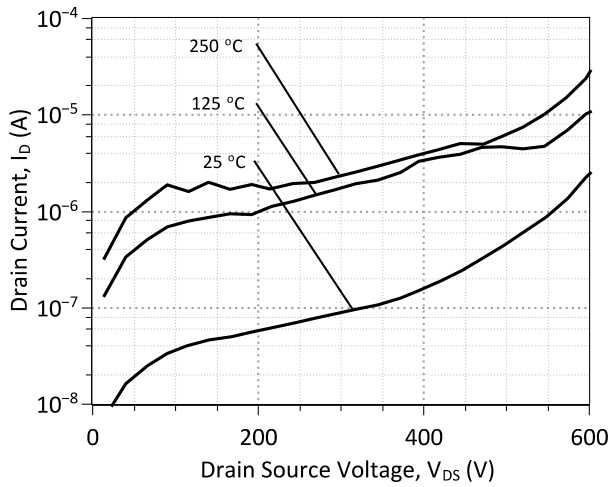


Figure 7: Typical Blocking Characteristics

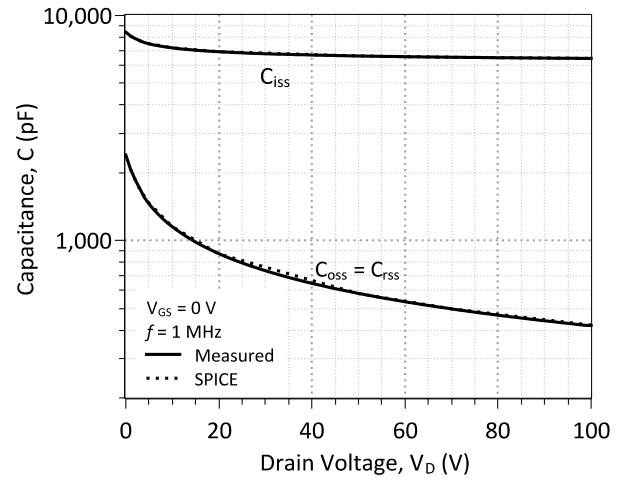


Figure 8: Capacitance Characteristics

Gate Drive Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 9.

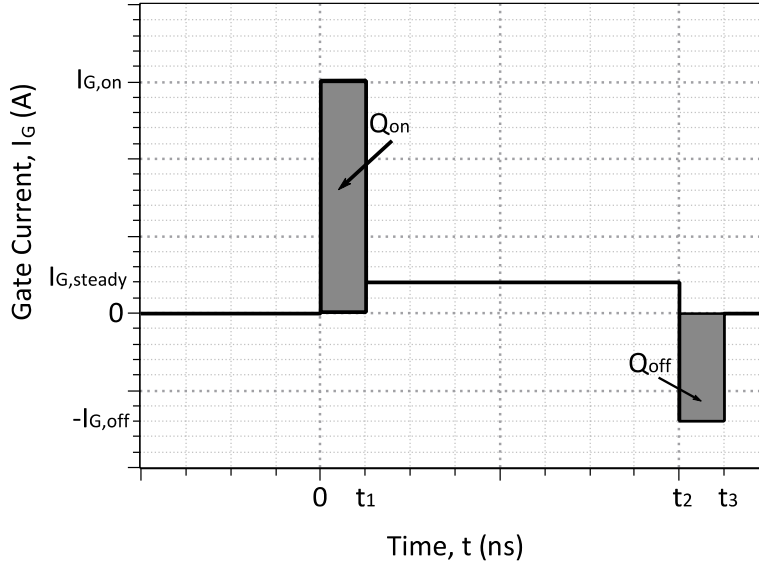


Figure 9: Idealized Gate Current Waveform

Gate Currents, $I_{G,pk}/-I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G , for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS} , and gate-drain capacitance, C_{GD} , are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

The $I_{G,on}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s , can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

A high negative peak current, $-I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with $V_{GS} = 0$ V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

Steady On-State

After the device is turned on, I_G may be advantageously lowered to $I_{G,steady}$ for reducing unnecessary gate drive losses. The $I_{G,steady}$ is determined by noting the DC current gain, h_{FE} , of the device

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D , DC current gain h_{FE} , and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

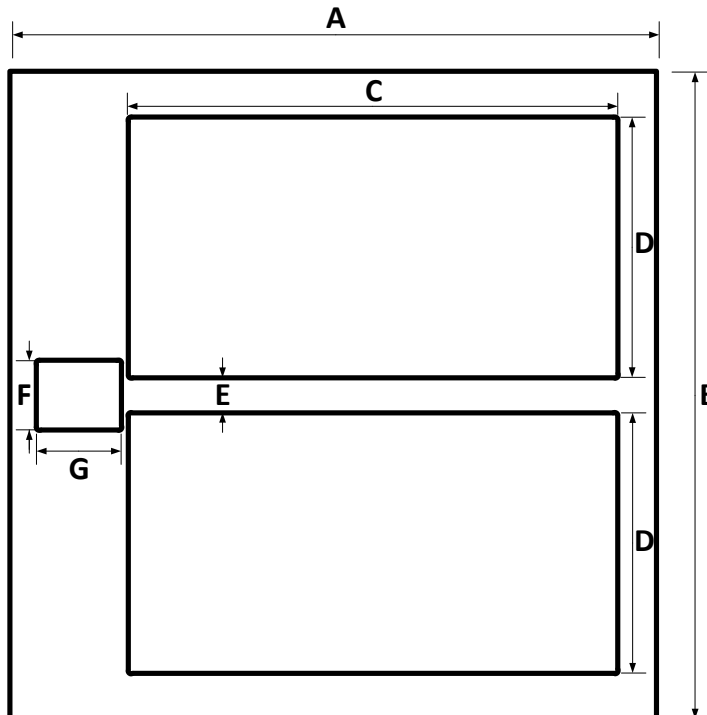
$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

Mechanical Specifications

Mechanical Parameters

Raster Size	4.35 x 4.35	mm ²	171 x 171	mil ²
Area total / active	18.92/16.56	mm ²	29330/25677	mil ²
Thickness	360	μm	14	mil
Wafer Size	100	mm	3937	mil
Flat Position	0	deg	0	deg
Passivation frontside	Polyimide			
Pad Metal (Anode)	4000 nm Al			
Backside Metal (Cathode)	400 nm Ni + 200 nm Au -system			
Die Bond	Electrically conductive glue or solder			
Wire Bond	Al ≤ 10 mil (Source) Al ≤ 3 mil (Gate)			
Reject ink dot size	Φ ≥ 0.3 mm			
Recommended storage environment	Store in original container, in dry nitrogen, < 6 months at an ambient temperature of 23 °C			

Chip Dimensions:



		mm	mil
DIE	A	4.35	171
	B	4.35	171
SOURCE WIREBONDABLE	C	3.30	130
	D	1.75	69
	E	0.24	9
GATE WIREBONDABLE	F	0.46	18
	G	0.57	22

Revision History

Date	Revision	Comments	Supersedes
2014/08/26	2	Updated Electrical Characteristics	
2014/03/03	1	Updated Electrical Characteristics	
2013/12/04	0	Initial release	

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SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/hit_sic/baredie/sjt/GA50JT06-CAL_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA50JT06-CAL.

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*      MODEL OF GeneSiC Semiconductor Inc.
*
*      $Revision:   1.1           $
*      $Date:      03-Mar-2014   $
*
*      GeneSiC Semiconductor Inc.
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*      Models accurate up to 2 times rated drain current.
*
.model GA50JT06 NPN
+ IS      5.00E-47
+ ISE     1.26E-28
+ EG      3.23
+ BF      106
+ BR      0.55
+ IKF     9000
+ NF      1
+ NE      2
+ RB      0.26
+ RE      0.01
+ RC      0.013
+ CJC     2.3989E-9
+ VJC     2.8346223
+ MJC     0.4846
+ CJE     6.026E-09
+ VJE     3.17915435
+ MJE     0.52951635
+ XTI     3
+ XTB     -1.2
+ TRC1    7.00E-3
+ VCEO    600
+ ICRATING 50
+ MFG     GeneSiC_Semiconductor
*
*      End of GA50JT06-CAL SPICE Model
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