N-Channel Enhancement Mode Power MOSFET

MTN2N65CFP

BV_{DSS}	**650V**
I_D @V_{GS}=10V, T_C=25°C	**2A**
I_D @V_{GS}=10V, T_C=100°C	**1.3A**
$R_{DS(ON)}$@V_{GS}=10V, I_D=1A	**4.5Ω(typ)**

Description

The MTN2N65CFP is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.
The TO-220FP package is universally preferred for all commercial-industrial applications

Features

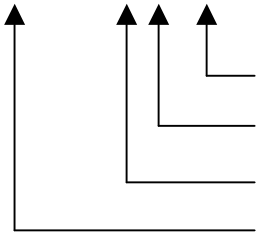
- Low On Resistance
- Simple Drive Requirement
- Fast Switching Characteristic
- Insulating package, front/back side insulating voltage=2500V(AC)
- RoHS compliant package

Applications

- Adapter
- Switching Mode Power Supply

Ordering Information

Device	Package	Shipping
MTN2N65CFP-0-UB-S	TO-220FP (RoHS compliant package)	50 pcs/tube, 20 tubes/box, 4 boxes / carton



Environment friendly grade : S for RoHS compliant products, G for RoHS compliant and green compound products

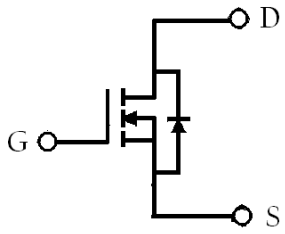
Packing spec, UB : 50 pcs / tube, 20 tubes/box

Product rank, zero for no rank products

Product name

Symbol

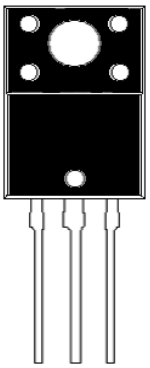
MTN2N65CFP



G：Gate
D：Drain
S：Source

Outline

TO-220FP



G D S

Absolute Maximum Ratings (Tc=25°C)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DS}	650	V
Gate-Source Voltage	V_{GS}	±30	
Continuous Drain Current @T_C=25°C, V_{GS}=10V	I_D	2*	A
Continuous Drain Current @T_C=100°C, V_{GS}=10V		1.3*	
Pulsed Drain Current (Note 1)	I_{DM}	8*	
Avalanche Current (Note 1)	I_{AS}	2	
Single Pulse Avalanche Energy @L=2mH, V_{GS}=10V, V_{DD}= 50V (Note 2)	E_{AS}	4	mJ
Repetitive Avalanche Energy (Note 1)	E_{AR}	2	
Maximum Temperature for Soldering @ Lead at 0.125 in(0.318mm) from case for 10 seconds	T_L	300	°C
Total Power Dissipation (T_C=25℃)	P_D	23	W
Linear Derating Factor		0.18	W/°C
Operating Junction and Storage Temperature	Tj, Tstg	-55~+150	°C

*Drain current limited by maximum junction temperature

Note : 1.Pulse width limited by maximum junction temperature.
2. 100% testsed by conditions of I_{AS}=1A, V_{DD}=50V, L=2mH, V_{GS}=10V, starting T_J=+25℃.

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-case, max	$R_{\theta JC}$	5.5	°C/W
Thermal Resistance, Junction-to-ambient, max	$R_{\theta JA}$	62.5	

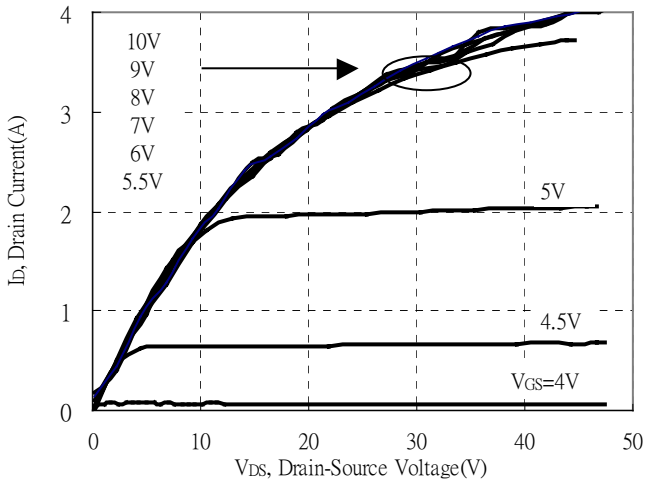
Characteristics (Tj=25°C, unless otherwise specified)

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static					
BV_{DSS}	650	-	-	V	V_{GS}=0V, I_D=250μA, Tj=25℃
$\Delta BV_{DSS}/\Delta Tj$	-	0.7	-	V/°C	Reference to 25°C, I_D=250μA
$V_{GS(th)}$	2.0	-	4.0	V	V_{DS} = V_{GS}, I_D=250μA
*G_{FS}	-	2.3	-	S	V_{DS} =15V, I_D=1A
I_{GSS}	-	-	±100	nA	V_{GS}=±30V
I_{DSS}	-	-	1	μA	V_{DS} =650V, V_{GS} =0V
	-	-	10		V_{DS} =520V, V_{GS} =0V, T_C=125°C
*$R_{DS(ON)}$	-	4.5	5.8	Ω	V_{GS} =10V, I_D=1A
Dynamic					
*Qg	-	7.8	11.7	nC	I_D=2A, V_{DD}=520V, V_{GS}=10V
*Qgs	-	2.3	-		
*Qgd	-	2.4	-		
*$t_{d(ON)}$	-	5.4	10.8	ns	V_{DD}=325V, I_D=1.8A, V_{GS}=10V, R_G=25Ω
*tr	-	3.2	6.4		
*$t_{d(OFF)}$	-	8.6	17.2		
*t_f	-	5.6	11.2		
Ciss	-	268	402	pF	V_{GS}=0V, V_{DS}=25V, f=1MHz
Coss	-	32	48		
Crss	-	11	16		
Rg	-	3.7	-	Ω	f=1MHz
Source-Drain Diode					
*I_S	-	-	2	A	
*I_{SM}	-	-	8		
*V_{SD}	-	0.8	1.5	V	I_S=1A, V_{GS}=0V
*trr	-	286	-	ns	V_{GS}=0V, I_F=1.8A, dI_F/dt=100A/μs
*Qrr	-	760	-	nC	

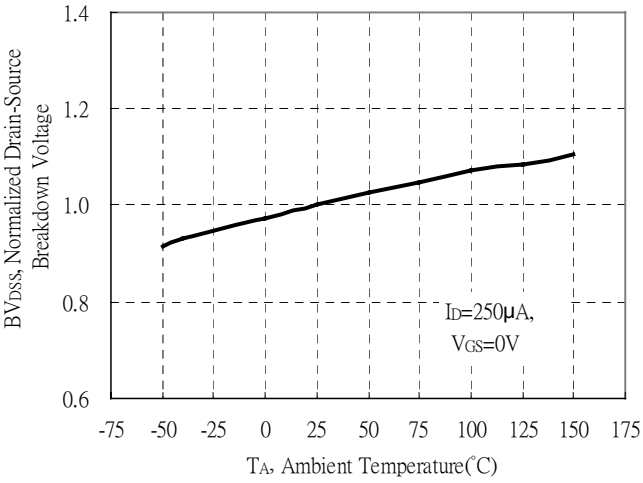
*Pulse Test : Pulse Width ≤300μs, Duty Cycle≤2%

Typical Characteristics

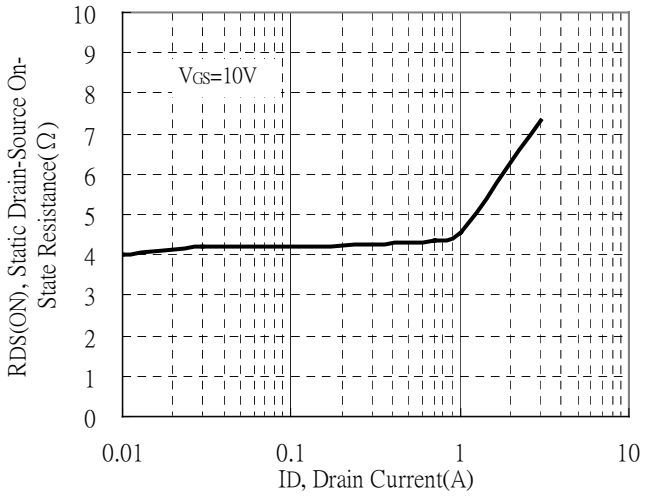
Typical Output Characteristics



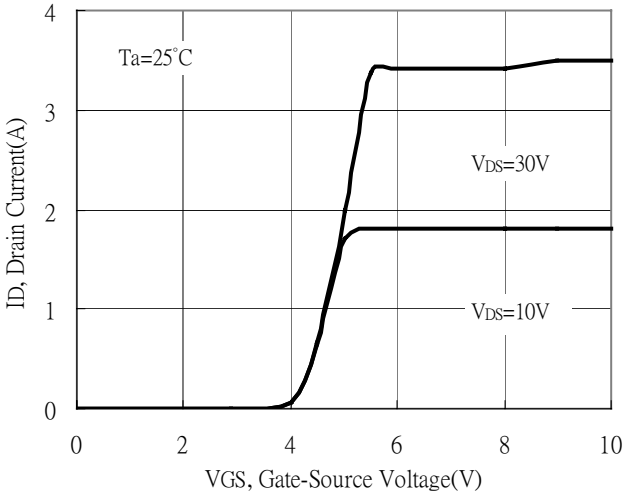
Brekdown Voltage vs Ambient Temperature



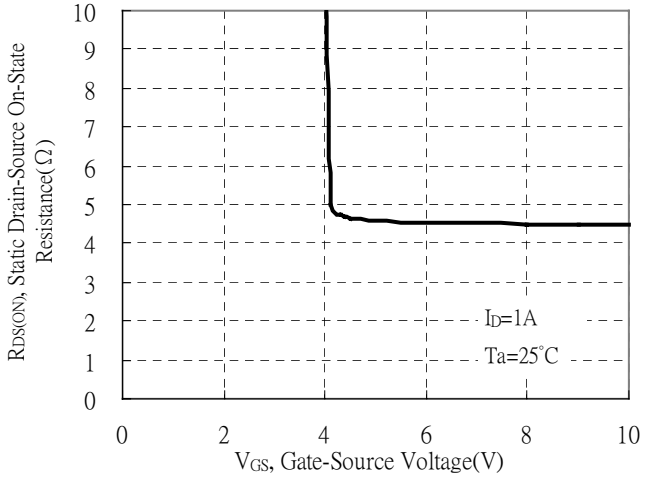
Static Drain-Source On-State resistance vs Drain Current



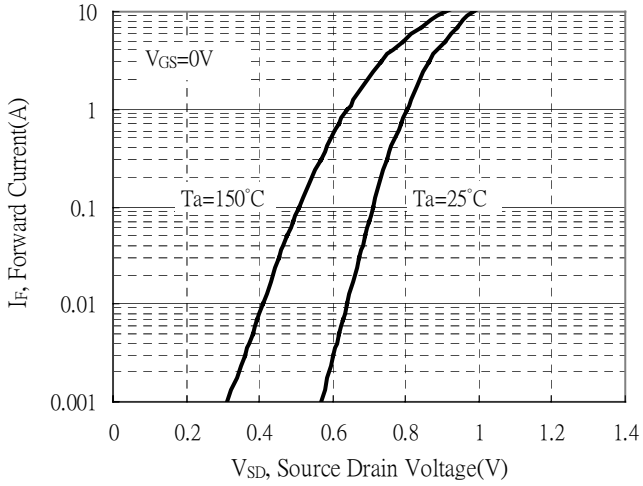
Drain Current vs Gate-Source Voltage



Static Drain-Source On-State Resistance vs Gate-Source Voltage

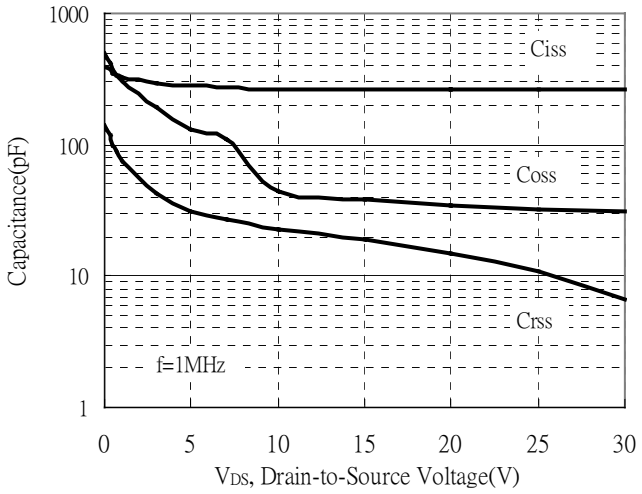


Forward Drain Current vs Source-Drain Voltage

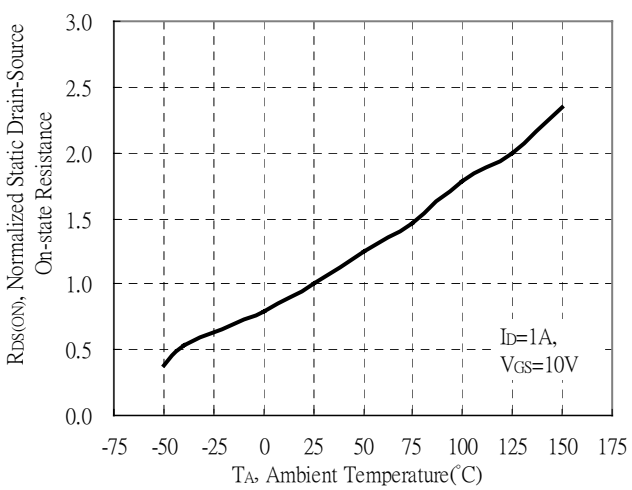


Typical Characteristics(Cont.)

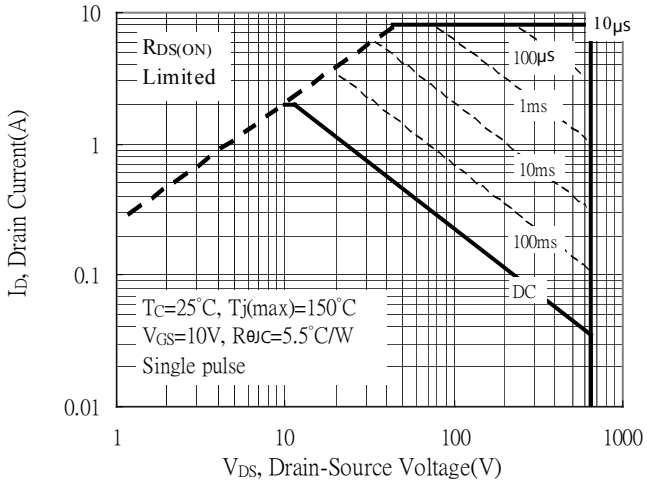
Capacitance vs Reverse Voltage



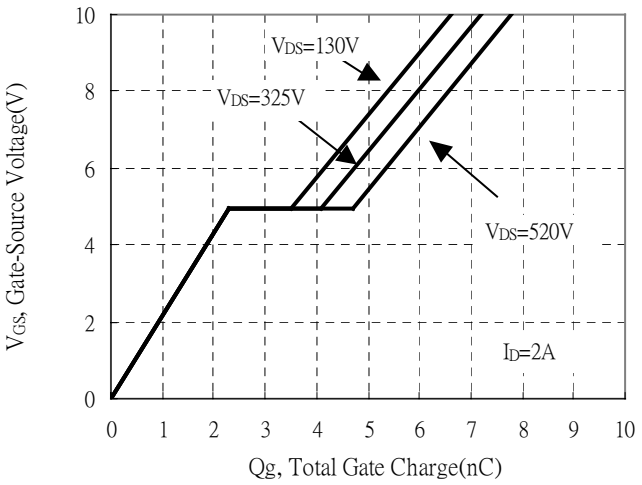
Static Drain-Source On-resistance vs Ambient Temperature



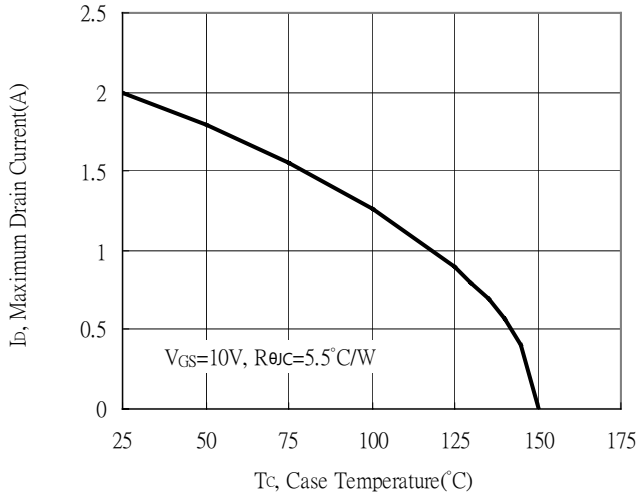
Maximum Safe Operating Area



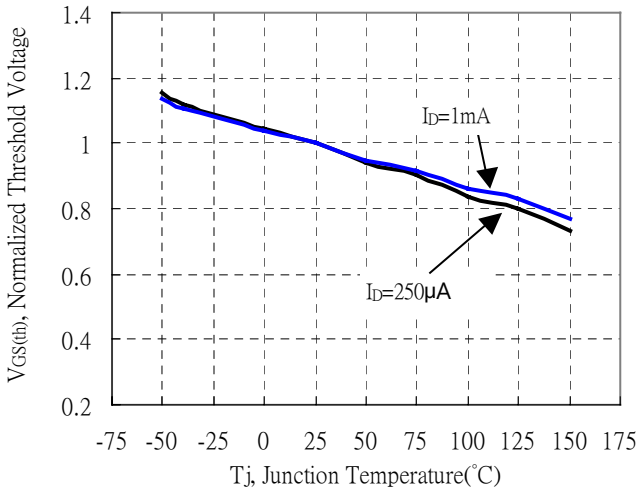
Gate Charge Characteristics



Maximum Drain Current vs Case Temperature

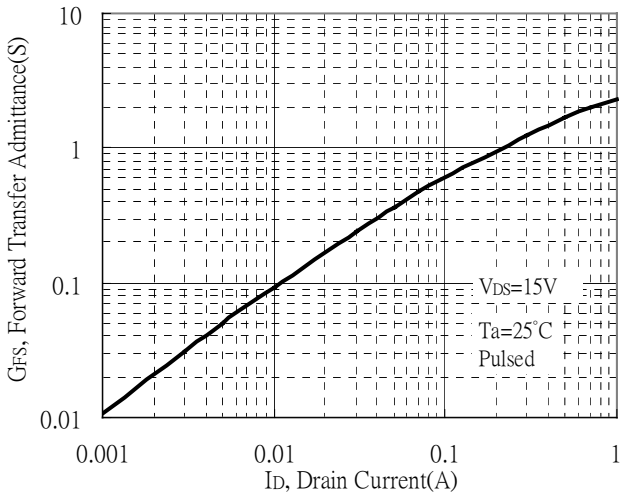


Threshold Voltage vs Junction Tempearture

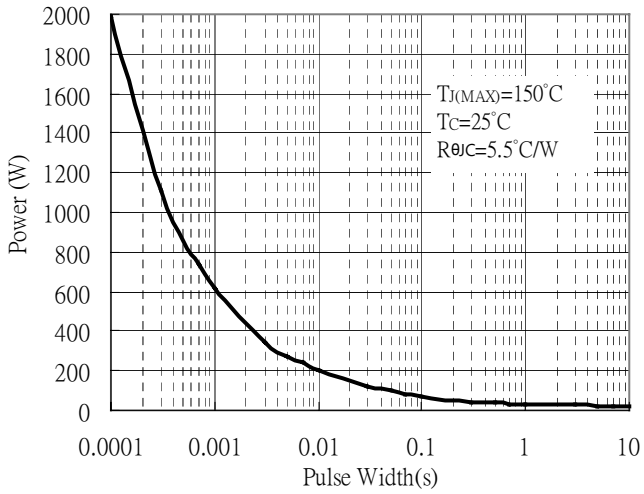


Typical Characteristics(Cont.)

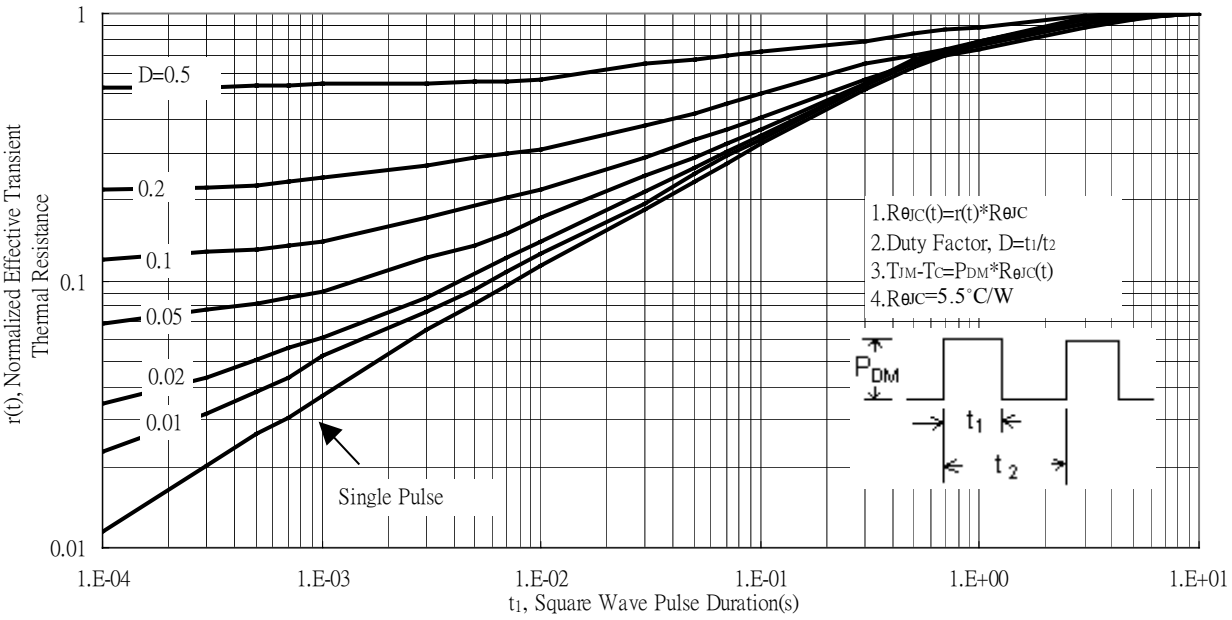
Forward Transfer Admittance vs Drain Current



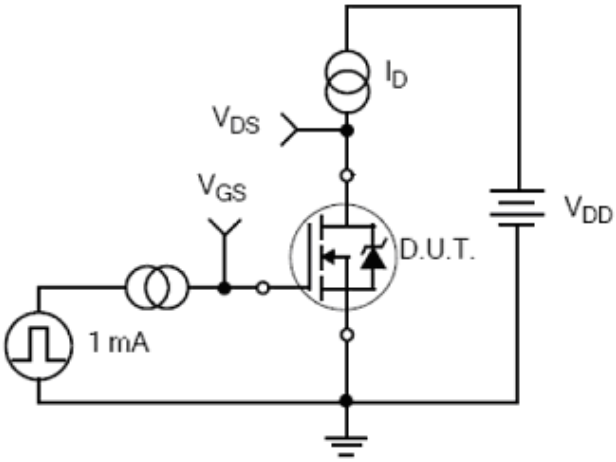
Single Pulse Power Rating, Junction to Case



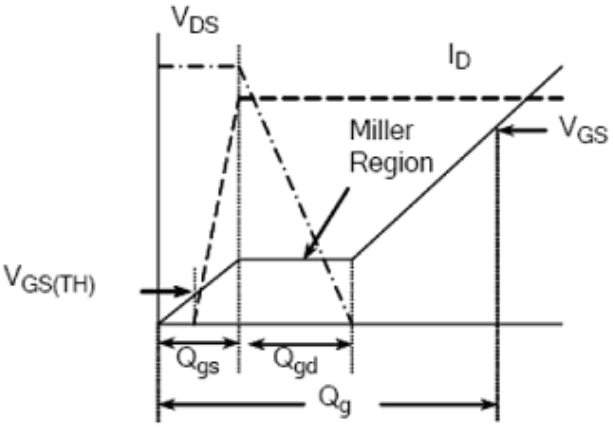
Transient Thermal Response Curves



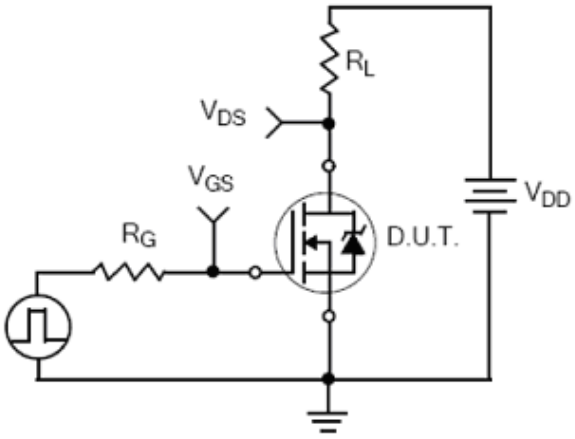
Test Circuit and Waveforms



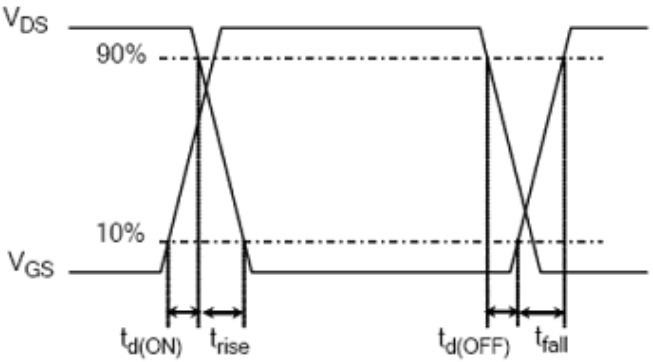
Gate Charge Test Circuit



Gate Charge Waveform

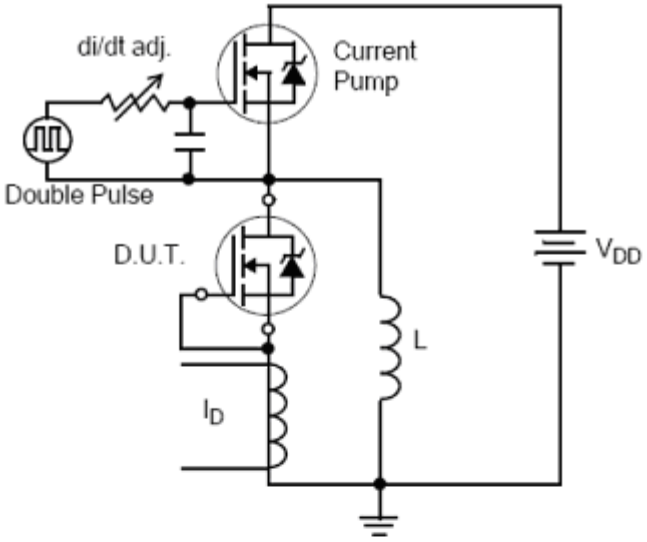


Resistive Switching Test Circuit

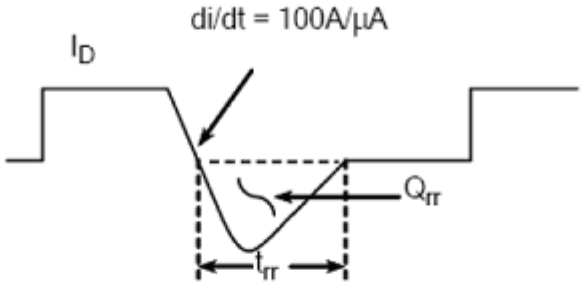


Resistive Switching Waveforms

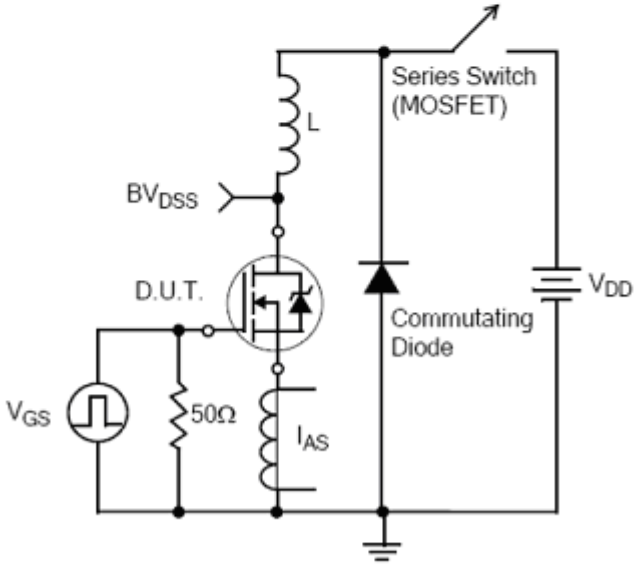
Test Circuit and Waveforms(Cont.)



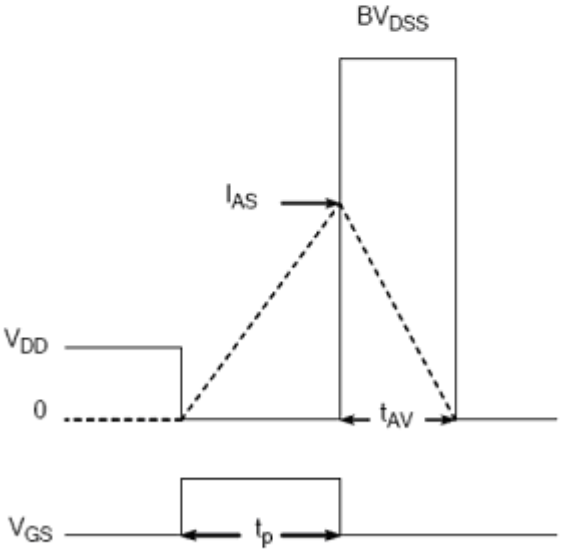
Diode Reverse Recovery Test Circuit



Diode Reverse Recovery Waveform



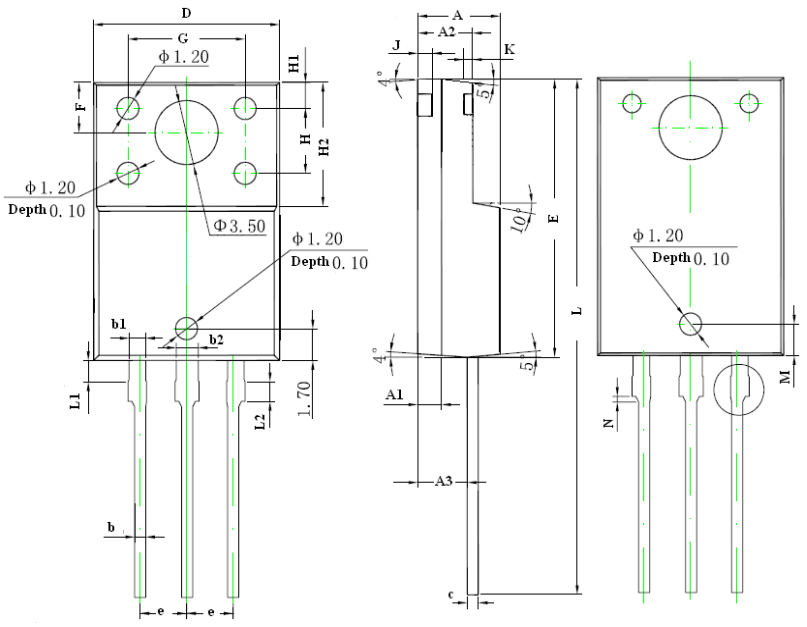
Unclamped Inductive Switching Test Circuit



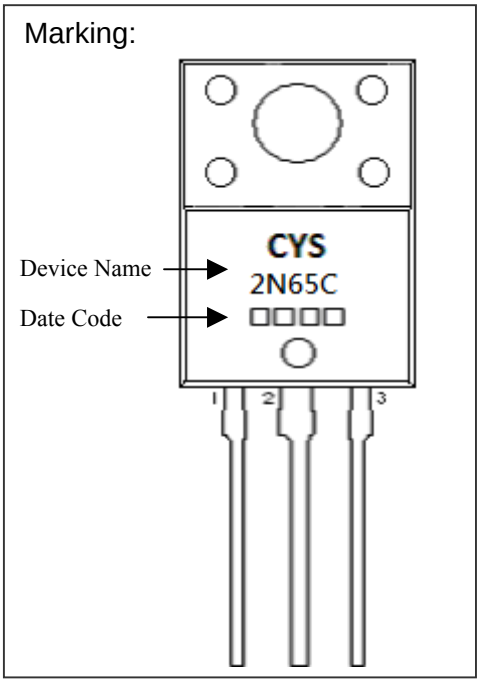
$$E_{AS} = \frac{I_{AS}^2 L}{2}$$

Unclamped Inductive Switching Waveforms

TO-220FP Dimension



3-Lead TO-220FP Plastic Package
CYStek Package Code: FP



Style: Pin 1.Gate 2.Drain 3.Source

*Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.171	0.183	4.35	4.65	G	0.246	0.258	6.25	6.55
A1	0.051 REF		1.300 REF		H	0.138 REF		3.50 REF	
A2	0.112	0.124	2.85	3.15	H1	0.055 REF		1.40 REF	
A3	0.102	0.110	2.60	2.80	H2	0.256	0.272	6.50	6.90
b	0.020	0.030	0.50	0.75	J	0.031 REF		0.80 REF	
b1	0.031	0.041	0.80	1.05	K	0.020		0.50 REF	
b2	0.047 REF		1.20 REF		L	1.102	1.118	28.00	28.40
c	0.020	0.030	0.500	0.750	L1	0.043	0.051	1.10	1.30
D	0.396	0.404	10.06	10.26	L2	0.036	0.043	0.92	1.08
E	0.583	0.598	14.80	15.20	M	0.067 REF		1.70 REF	
e	0.100 *		2.54*		N	0.012 REF		0.30 REF	
F	0.106 REF		2.70 REF						

Notes: 1.Controlling dimension: millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

Important Notice:

- All rights are reserved. Reproduction in whole or in part is prohibited without the prior written approval of CYStek.
- CYStek reserves the right to make changes to its products without notice.
- CYStek ***semiconductor products are not warranted to be suitable for use in Life-Support Applications, or systems.***
- CYStek assumes no liability for any consequence of customer product design, infringement of patents, or application assistance.