

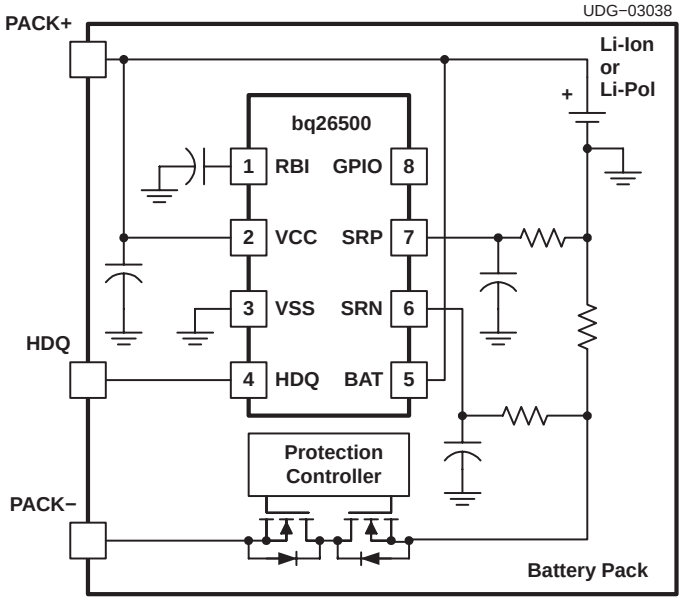
SLUS567A − JUNE, 2003 − REVISED OCTOBER 2003

SINGLE-CELL LI-ION AND LI-POL BATTERY GAS GAUGE IC FOR HANDHELD APPLICATIONS (bqJUNIOR™ FAMILY)

FEATURES

- **Reports Accurate *State-of-Charge* in Li-Ion and Li-Pol Cells, No System Processor Calculations Needed**
- **Reports Cell Temperature and Voltage**
- **High-Accuracy Coulometric Charge and Discharge Current Integration with Automatic Offset Cancellation**
- **Requires No Offset Calibration**
- **Programmable Input/Output Port**
- **Internal Time-Base Eliminates External Crystal Oscillator**
- **Four Automatic Low-Power Operating Modes**
  - **Active: < 100 μA**
  - **Sleep: < 2.5 μA**
  - **Ship: < 1.7 μA**
  - **Hibernate: < 1.5 μA**
- **Small 8-Pin TSSOP Package**

SIMPLIFIED APPLICATION



APPLICATIONS

- **PDAs**
- **Smart Phones**
- **MP3 Players**
- **Digital Cameras**
- **Internet Appliances**
- **Handheld Devices**

DESCRIPTION

The bq26500, the first in the bqJUNIOR™ family of advanced gas gauge device for handhald applications, is a highly accurate standalone single-cell Li-Ion and Li-Pol battery capacity monitoring and reporting device targeted at space limited portable applications. The device monitors a voltage drop across a small current sense resistor connected in series with the battery to determine charge and discharge activity of the battery. Compensations for battery temperature, self-discharge, and rate of discharge are applied to the charge counter to provide available capacity across a wide range of operating conditions. Battery capacity is automatically recalibrated, or learned, in the course of a discharge cycle from full to empty. Internal registers include available capacity, cell temperature and voltage, state-of-charge, and status and control registers.

The bq26500 can operate directly from single-cell Li-Ion and Li-Pol batteries and communicates to the system over a simple one-wire bi-directional serial interface. The 5-kbits/s HDQ bus interface reduces communication overhead in the external microcontroller.

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ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

		bq26500	UNIT
Supply voltage range, V_{CC} (all with respect to V_{SS})		−0.3 to 7.0	V
Input voltage range at SRP, SRN, RBI, and BAT (all with respect to V_{SS})		−0.3 to V_{CC} + 0.3 V	V
Input voltage	HDQ, GPIO (with respect to V_{SS})	−0.3 to 7.0	V
Input voltage	GPIO (with respect to V_{SS}) during EEPROM programming only	−0.3 to 22.0	V
Output sink current at GPIO, HDQ		5	mA
Operating free-air temperature range, T_A		−20 to 70	°C
Storage temperature range, T_{stg}		65°C to 150°C	°C
Junction temperature range, T_J		−40°C to 125°C	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.6		4.5	V
Operating free-air temperature, T_J	−20		70	°C
Input voltage range at SRP and SRN, (with respect to V_{SS})	−100		100	mV

ELECTRICAL CHARACTERISTICS

T_J = −20°C to 70°C, T_J = T_A, 2.6 V ≤ V_{CC} ≤ 4.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
$I_{CC(ACT)}$	Active current	V_{CC} > $V_{CC(min)}$		60	100	µA
$I_{CC(SLP)}$	Sleep current			1.2	2.5	µA
$I_{CC(SHP)}$	Ship current			0.9	1.7	µA
$I_{CC(POR)}$	Hibernate current	0 V < V_{CC} < $V_{(POR)}$		0.6	1.5	µA
	RBI current	RBI pin only, V_{CC} < $V_{(POR)}$			20	nA
$V_{(POR)}$	POR threshold		2.05		2.55	V
	POR threshold hysteresis			100		mV
	Input impedance on BAT pin		10			MΩ
	Input impedance on SRP, SRN pins		10			MΩ
VOLTAGE MEASUREMENT						
	Measurement range	V_{CC} = $V_{I(BAT)}$	2.6		4.5	V
	Reported voltage resolution			1		mV
	Reported accuracy		−20		20	mV
	Voltage update time			2		s
TEMPERATURE MEASUREMENT						
	Reported temperature resolution			0.25		°K
	Reported temperature accuracy		−3		3	°K
	Temperature update time			2		s

ELECTRICAL CHARACTERISTICS(continued)

T_J = −20°C to 70°C, $T_J = T_A$, 2.6 V ≤ V_{CC} ≤ 4.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TIME MEASUREMENT						
f_{OSC}	Internal oscillator frequency		−3.5%	+1.0%	+2.5%	
f_{OSC}	Internal oscillator frequency	T_A = 0°C to 50°C	−2.5%	+1.0%	+2.5%	
CAPACITY MEASUREMENT						
	Voltage-to-frequency converter offset				15	µV
	Voltage-to-frequency converter gain variabilty(3)				1%	
	Voltage-to-frequency input (V_{SRP} − V_{SRN})		−100		100	mV
EEPROM PROGRAMMING (V_{CC} ≥ 3.0 V, 20°C ≤ T_A ≤ 35°C)(1)						
t_{RISE}	Programming voltage rise time			1		ms
t_{PROG}	Programming voltage high time	V_{PROG} = 21 V	20		100	
t_{FALL}	Programming voltage fall time			1		
V_{PROG}	Programming voltage	Applied to GPIO pin	20		22	V
I_{PROG}	EEPROM programming current	Current into GPIO pin			3	mA
IO PORT (GPIO) AND SERIAL INTERFACE (HDQ)						
V_{IH}	High-level input voltage		1.9			V
V_{IL}	Low-level input voltage				0.7	
V_{OL}	GPIO low-level output voltage	I_{OL} = 0.3 mA			0.4	
V_{OL}	HDQ low-level output voltage	I_{OL} = 2 mA			0.4	
I_{HDQPD}	HDQ internal pull-down current				3	µA
STANDARD SERIAL COMMUNICATION (HDQ) TIMING(2)						
$t_{(B)}$	Break timing		190			µs
$t_{(BR)}$	Break recovery time		40			
$t_{(CYCH)}$	Host bit window timing		190			
$t_{(HW1)}$	Host sends 1 time		17		50	
$t_{(HW0)}$	Host sends 0 time		100		145	
$t_{(RSPS)}$	bq26500 to host response time		190		320	
$t_{(CYCD)}$	bq26500 bit window timing		190		260	
$t_{(DW1)}$	bq26500 sends 1 time		32		50	
$t_{(DW0)}$	bq26500 sends 0 time		80		145	

(1) Maximum number of programming cycles on the EEPROM is 10 and data retention time is 10 years at T_A=85°C
(2) See Figure 1.
(3) Not a production tested parameter.

The following timing diagrams describe break and break recovery timing (a), host transmitted bit timing (b), bq26500 transmitted bit timing (c), and bq26500 to host response timing (d).

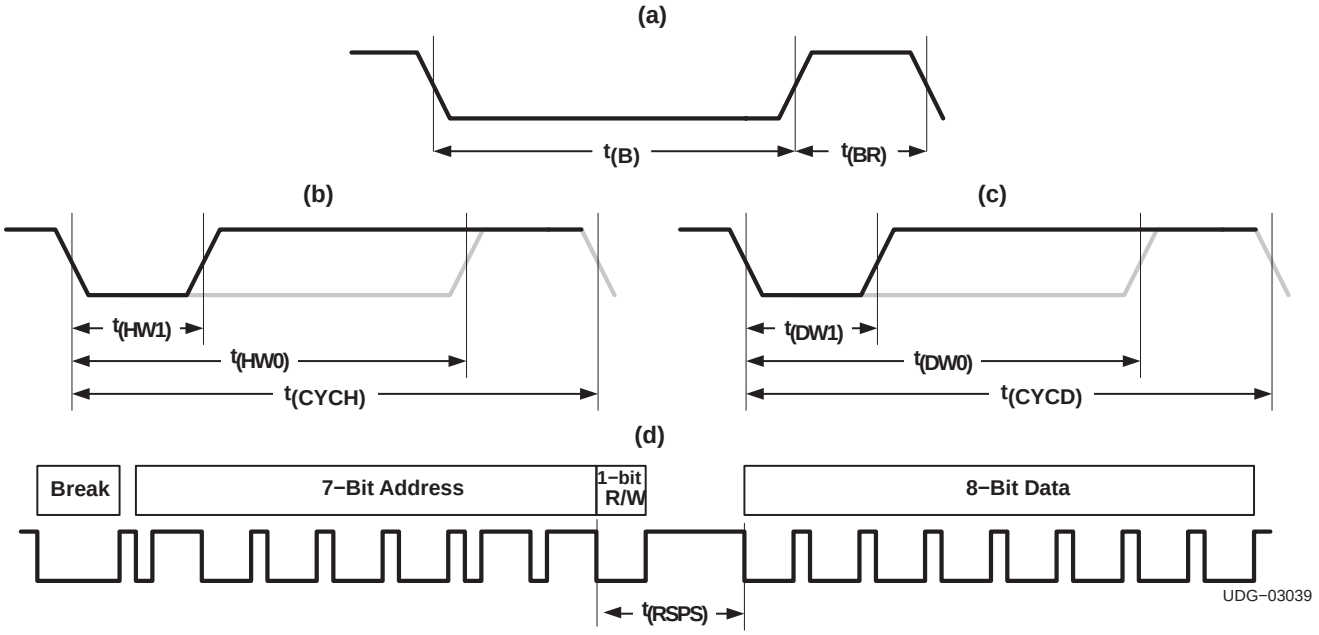


Figure 1. HDQ Bit Timing Diagrams

PIN ASSIGNMENTS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BAT	5	I	Battery voltage sense input
GPIO	8	I/O	General-purpose input/output port
HDQ	4	I/O	Single-wire HDQ serial interface
RBI	1	I	Register back-up input
SRN	6	I	Current sense input (negative)
SRP	7	I	Current sense input (positive)
VCC	2	I	V_{CC} supply input
VSS	3	I	Ground input

PW PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A	PACKAGED DEVICES(1)	MARKINGS
−20°C to 70°C	bq26500PW	26500

(1) The PW package is available taped and reeled. Add R suffix to device type (e.g. bq26500PWR) to order quantities of 2,000 devices per reel.

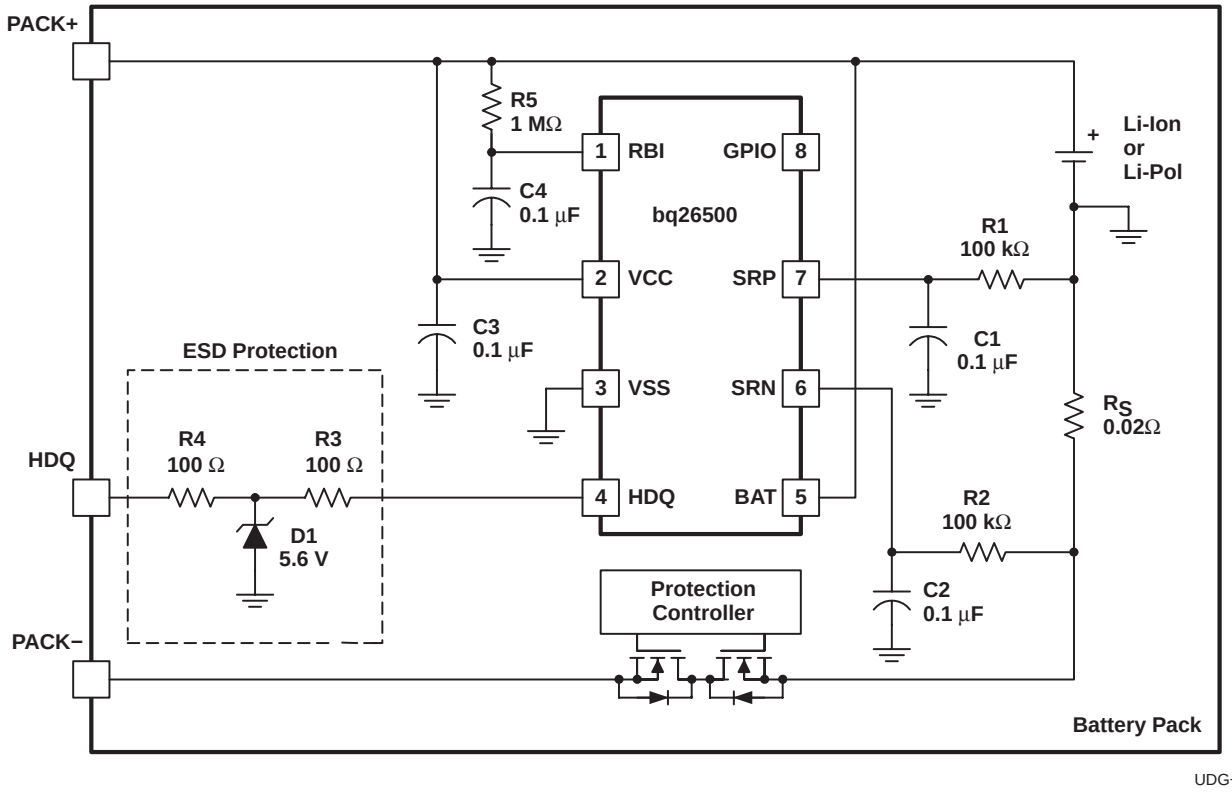


Figure 2. Typical Application Circuit

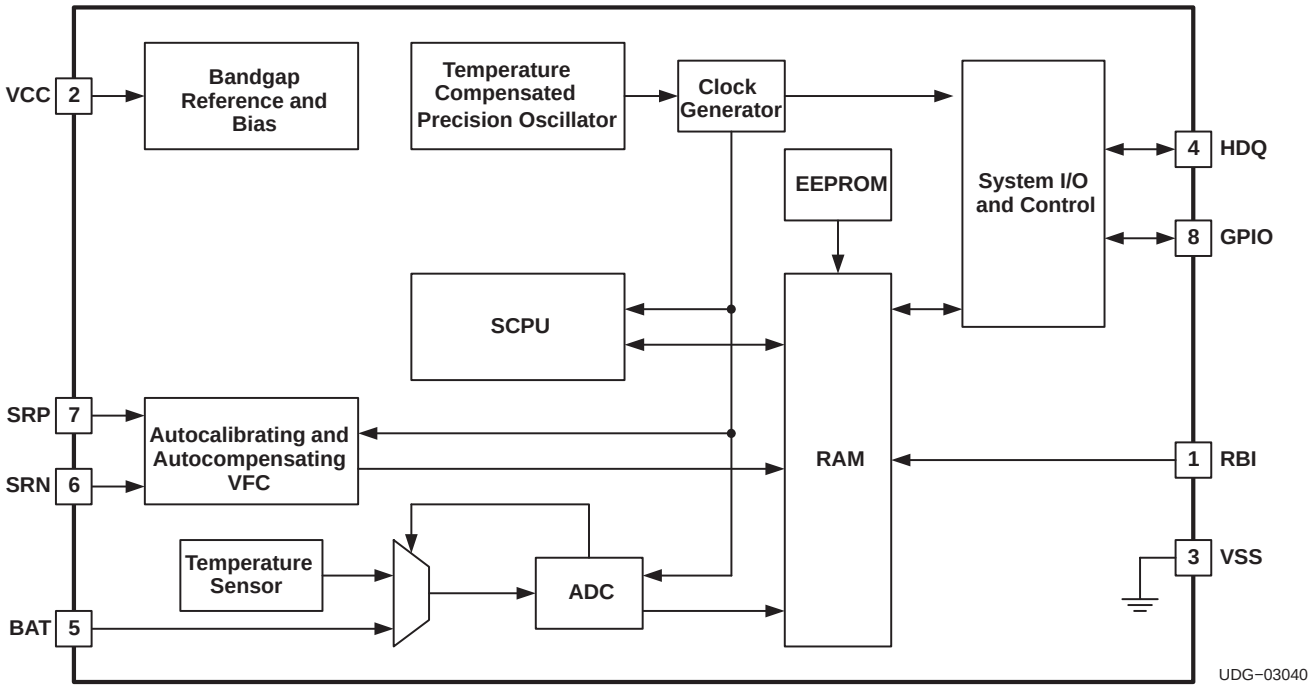


Figure 3. Functional Block Diagram

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The bq26500 determines battery capacity by monitoring the amount of charge input to or removed from a Li-Ion or Li-Pol battery. The bq26500 measures discharge and charge currents, monitors the battery for low voltage thresholds, and compensates for temperature and self-discharge rate. Current is measured across a small value series resistor between the negative terminal of the battery and the pack ground (see R_S in Figure 2). Available capacity is reported with a resolution of $0.003/R_S$(mAh). Time-to-empty (TTE) reporting in minutes at host-provided at-rate currents allow the requirements for host based calculations to be greatly reduced or eliminated; reading a single register pair provides useful and meaningful information to the application's end user.

Figure 2 shows a typical application circuit. Differential sense of the voltage across the current sense resistor, R_S, improves device performance, leading to an improvement in reported time-to-empty accuracy. In the typical application, the GPIO pin can be used as a general-purpose programmable I/O port. An internal pull-down on the HDQ line ensures that the device detects a logic "0" on the HDQ line and automatically enters the low power sleep mode when the system power is switched off or the pack is removed. A 100-kΩ pull-up to V_{CC} can be added to the HDQ line to disable this feature. The bq26500 can operate directly from a single Li-Ion or Li-Pol cell.

Measurements

As shown in the Figure 3, the bq26500 uses a fully differential, dynamically balanced voltage-to-frequency converter (VFC) for charge and discharge counting and an analog-to-digital converter (ADC) for battery voltage and temperature measurement. Both VFC and ADC are automatically compensated for offset. No user calibration or compensation is required.

Charge and Discharge Counting

The bq26500 uses a voltage-to-frequency converter (VFC) to perform a continuous integration of the voltage waveform across a small value sense resistor in the negative lead of the battery, as shown in Figure 2. The integration of the voltage across the sense resistor is the charge added or removed from the battery. Since the VFC directly integrates the waveform, the shape of the current waveform through the sense resistor has no effect on the measurement accuracy. The low-pass filter that feeds the sense resistor voltage to the bq26500 SRP and SRN inputs serves to filter out system noise and does not affect the measurement accuracy, since the low-pass filter does not change the integrated value of the waveform.

Offset Calibration

The offset voltage of the VFC measurement must be very low to be able to measure small signal levels accurately. The bq26500 provides an auto-compensation feature to cancel the internal voltage offset error across SRP and SRN for maximum charge measurement accuracy.

> **NOTE:NO CALIBRATION IS REQUIRED**. See the *Layout Considerations* section for details on minimizing PCB induced offset across the SRP and SRN pins.

APPLICATION INFORMATION

Digital Magnitude Filter

The digital magnitude filter (DMF) threshold can be set in EEPROM to indicate a threshold below which any charge or discharge accumulation is ignored. This allows setting a threshold above the maximum VFC offset expected from the device and PCB combination. This ensures that when no charge or discharge current is present, the measured capacity change by the bq26500 is zero. Note that even a small PCB offset can add up to a large error over a long period. In addition to setting the threshold above the largest offset expected, the DMF should be set below the minimum signal level to be measured. Since the measured signal can only be measured as accurately as the VFC offset induced from the PCB, the sense resistor value should be large enough to allow the minimum current level to provide a signal level substantially higher than the maximum offset voltage. Conversely, the sense resistor must be small enough to meet the system requirement for insertion loss as well as keep the maximum voltage across the sense resistor below the ±100-mV maximum that the VFC can accurately measure.

The DMF threshold is programmed in EEPROM in increments of 6 μV. Programming a zero in the DMF value disables the DMF function and no VFC counts are ignored.

Voltage

The bq26500 monitors the battery voltage through the BAT pin and reports an offset corrected value through the internal registers. The bq26500 also monitors the voltage for the end-of-discharge voltage (EDV) thresholds. The EDV threshold levels are used to determine when the battery has reached an empty state.

Temperature

The bq26500 uses an integrated temperature sensor to monitor the pack temperature. The temperature measurements reported through the internal registers are used to adjust charge and discharge rate compensations, and self-discharge capacity loss estimation.

RBI Input

The register back-up input pin, RBI, is used with an external capacitor to provide backup potential to the internal registers when V_{CC} drops below the power-on-reset voltage $V_{(POR)}$. V_{CC} is output on RBI when V_{CC} is above $V_{(POR)}$, charging the capacitor. Figure 2 shows an optional 1-MΩ resistor from RBI pin to VCC. This allows the device to maintain RAM register data when the battery voltage is below $V_{(POR)}$ and above 1.3 V. The bq26500 checks for RAM corruption by storing redundant copies of the high bytes of NAC and LMD. After a reset, the bq26500 compares the redundant NAC and LMD values and verifies the accuracy of 2 checkbyte values. If the redundant copies match and the checkbytes are correct, NAC and LMD are retained and the CI bit in FLAGS is left unchanged. If these checks are not correct, NAC is cleared, LMD is initialized from EEPROM, and the CI bit in FLAGS is set to “1”. All other RAM is initialized on all resets.

Layout Considerations

The auto-compensating VFC approach effectively cancels the internal offset voltage within the bq26500, but any external offset caused by PCB layout is not cancelled. This makes it critical to pay special attention to the PCB layout. To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the filter capacitors from SRP and SRN to V_{SS} should be placed as closely as possible to the bq26500, with short trace runs to both signal and VSS pins. All low-current V_{SS} connections should be kept separate from the high-current discharge path from the battery and should tie into the high current trace at a point directly next to the sense resistor. This should be a trace connection to the edge or inside of the sense resistor connection, so that no part of the V_{SS} interconnections carry any load current and no portion of the high-current PCB trace is included in the effective sense resistor (i.e. *Kelvin* connection).

APPLICATION INFORMATION

Gas Gauge Operation

Figure 4 illustrates an operational overview of the gas gauge function.

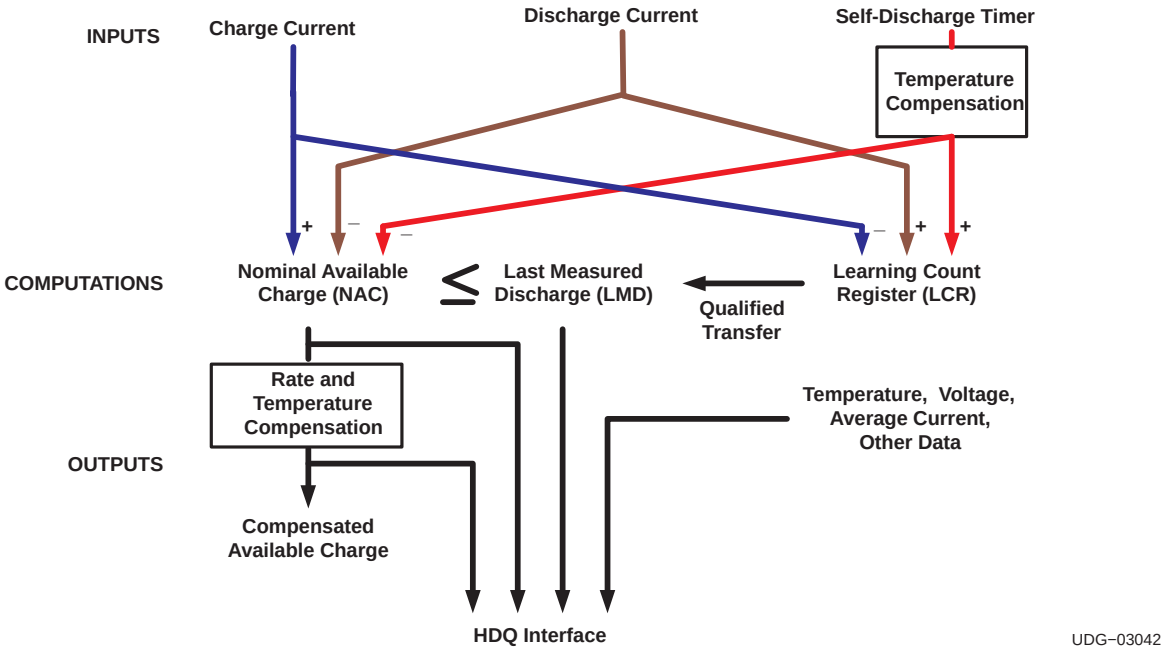


Figure 4. Operational Overview

The bq26500 measures the capacity of the battery during actual use conditions and updates the last measured discharge (LMD) register with the latest measured value. The bq26500 retains the learned LMD value unless a full reset occurs. By measuring the capacity that the battery delivers as it is discharged from full to the EDV1 threshold without any disqualifying events, the bq26500 learns the capacity of the battery. During normal use conditions, the bq26500 should learn a new capacity only after a full discharge. Learning cycles are disqualified by several abnormal conditions (see list at end of section). In the event that a learning cycle occurs with a significant reduction in learned capacity, the new LMD value is restricted to a maximum LMD reduction during any single learning discharge of LMD/8. The capacity inaccurate (CI) bit in FLAGS is cleared after the first learning cycle. This bit remains cleared unless a full reset occurs.

The battery-full condition is defined as nominal available capacity (NAC) = LMD. The valid discharge flag (VDQ) in the FLAGS register is set when this condition occurs and remains set until the learning discharge cycle completes or an event occurs that disqualifies the learning cycle.

The learning discharge cycle completes when the battery is discharged to the condition where VOLT ≤ EDV1 threshold. The EDV1 threshold should be set at a voltage that guarantees at least 6.25% of battery capacity below that threshold. The EDVF threshold should be set at a voltage that the system sees as the zero capacity battery voltage.

The bq26500 does not learn the capacity between EDV1 and EDVF thresholds, but assumes that the capacity is 6.25% of LMD, so care should be taken to set EDV1 based on the characteristics of the battery. The measured LMD value is determined by measuring the capacity delivered from the battery from NAC=LMD until VOLT ≤ EDV1, plus LMD/16 to account for the 6.25% capacity remaining below the EDV1 threshold.

APPLICATION INFORMATION

VDQ is cleared and a capacity learning cycle is disqualified by any of the following conditions:

1. Cold temperature: Temperature less than or equal to the TOFF value programmed in the TCOMP register when the EDV1 threshold voltage is reached.
2. Light load: Average current is less than or equal to 2 times the initial standby load (ISLC) when the EDV1 threshold voltage is reached.
3. Fast voltage drop: VOLT ≤ (EDV1 − 256 mV) when EDV1 is set.
4. Excessive charging: Cumulative charge added is greater than 255 mAh during a learning discharge cycle (alternating discharge-charge-discharge before EDV1 is set).
5. Reset: VDQ is cleared on reset.
6. Excessive self-discharge: NAC reduction from self−discharge estimate exceeds 12.48%.
7. Self-discharge at termination of learning cycle. If self-discharge estimate reduces NAC until NAC ≤ LMD/16.

APPLICATION INFORMATION

Register Interface for bq26500

The bq26500 stores all calculated information in RAM, which is backed up by the voltage present on the RBI pin. EEPROM registers store permanent user data. The memory map for bq26500 is shown in Table 1.

Table 1. bq26500 Memory Map

HDQ ADDRESS	NAME	FUNCTION (256 x High Byte + Low Byte)	LSB VALUE
EEPROM Registers			
0x7F	TCOMP	Temperature compensation constants, ***OR***, ID#1	
0x7E	DCOMP	Discharge rate compensation constants, ***OR***, ID#2	
0x7D	ID3	ID#3	
0x7C	PKCFG	Pack configuration values	
0x7B	TAPER	Charge termination taper current	192 μV(1)
0x7A	DMFSD	Digital magnitude filter and self-discharge rate constants	
0x79	ISLC	Initial standby load current	6 μV(1)
0x78	SEDV1	Scaled EDV1 threshold	
0x77	SEDVF	Scaled EDVF threshold	
0x76	ILMD	Initial last measured discharge high byte	768 μVh(1)
RAM Registers			
0x6F − 0x75	−	*RESERVED*	
0x6E	EE_EN	EEPROM program enable	
0x14 − 0x6D	−	*RESERVED*	
0x13 − 0x12	LMD	Last measured discharge high − low byte	3 μVh(1)
0x11 − 0x10	CACT	Temperature compensated CACD high – low byte	3 μVh(1)
0x0F − 0x0E	CACD	Discharge compensated NAC high − low byte	3 μVh(1)
0x0D − 0x0C	NAC	Nominal available capacity high − low byte	3 μVh(1)
0x0B	RSOC	Relative state of charge	1%
0x0A	FLAGS	Status flags	
0x09 − 0x08	VOLT	Reported voltage high − low byte	1 mV
0x07 − 0x06	TEMP	Reported temperature high − low byte	0.25°K
0x05 − 0x04	ARTTE	At rate time-to-empty high − low byte	1 minute
0x03 − 0x02	AR	At rate high − low byte	3 μV(1)
0x01	MODE	Device mode register	
0x00	CTRL	Device control register	

(1) Divide by $R_S(m\Omega)$ to convert μV to mA or μVh to mAh.

APPLICATION INFORMATION

REGISTER DESCRIPTIONS

Device Control Register (CTRL) − Address 0x00

The device control register is used by the host system to request special operations by the bq26500. The highest priority command set in the MODE register performs when the host writes data 0xA9 to the control register. The CTRL register is cleared when the action is complete. Note that writing any value other than 0xA9 has no effect.

Mode Register (MODE) − Address 0x01

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GPIEN	GPSTAT	WRTNAC	DONE	PRST	POR	FRST	SHIP

MODE REGISTER	DESCRIPTION
GPIEN	GPIEN sets the state of the GPIO pin. A “1” configures the GPIO pin as input, while a “0” configures the GPIO pin as an open-drain output. This bit is initialized to the value of bit 7 of the PKCFG register in the EEPROM
GPSTAT	GPSTAT sets the state of the open drain output of the GPIO pin (GPIEN = 0). A “1” turns off the open drain output while a “0” turns the output on. This bit is set to 1 on POR. When the GPIO pin is an input (GPIEN=1), this bit returns the logic state of the GPIO pin.
WRTNAC	WRTNAC is used to transfer data from the AR registers to the NAC registers. Other registers are updated as appropriate. This command is useful during the pack manufacture and test to initialize the gauge to match the estimated battery capacity. This bit is cleared on all resets.
DONE	DONE is used to write NAC to LMD. Useful if the host uses a charge termination method that does not allow the monitor to detect the taper current. The host system could use this command when the charging is complete to force update of internal registers to a full battery condition. This bit is cleared on all resets.
PRST	Partial reset. This command requests a full reset, except that the NAC, LMD, and the CI bit in FLAGS should not be restored to their initial values. This command is intended for manufacturing use. This bit is cleared on all resets.
POR	The POR status bit is set to “1” by the bq26500 following a power-on-reset (POR). This is a flag to the host that V_{CC} was less than $V_{(POR)}$ and caused a reset. The bit is cleared to “0” by the bq26500 when a full charge condition is reached or it may be cleared by the host. The host may set this bit, but it has no effect on the bq26500 operation.
FRST	Full reset. This command bit requests a full reset. A full reset re-initializes all RAM registers, including the NAC, LMD, and FLAGS registers. This command is intended for manufacturing use. This bit is cleared on all resets.
SHIP	This command bit requests that the device should be put in ship mode. See the *Power Modes* section for a description of the ship mode. This command is intended for manufacturing use. This bit is cleared on all resets.

WRTNAC, DONE, PRST, FRST, and SHIP commands are prioritized in bit order. This means that WRTNAC (bit 5) has higher priority than DONE (bit 4); PRST (bit 3) has higher priority than FRST (bit 1), and so on. Only the highest priority mode set is enabled each time the CTRL register is written with data 0xA9, and the firmware clears all other mode bits and the CTRL register when that action is complete. The host system must make two writes for every mode to be enabled, one write to the mode register to set the appropriate bit and a second write to the CTRL register to signal that the mode should be enabled.

APPLICATION INFORMATION

At Rate Registers (ARH/ARL) − Address 0x02/0x03

For the bq26500, the host writes the current value to this register for predictive calculation of time-to-empty. The device uses this value to predict the time-to-empty at any desired current. The current value written into this register pair is always assumed to be a discharge current. The value written to AR should be the predicted voltage across the sense resistor expressed in units of 3 μV per count.

This register is also used during pack manufacturing to input a nominal available charge (NAC) value to set the NAC registers to the approximate initial pack capacity value.

At Rate Time to Empty Registers (ARTTEL/ARTTEH) − Address 0x04/0x05

Predicted time-to-empty, in minutes, at user entered discharge rate. The discharge current used in the calculation is entered by the host system in the at-rate (AR) registers. The at-rate capacitance (ARCAP) value used may be larger or smaller than CACT. It is computed using the same formulas as CACT, except the discharge compensation is computed using AR, instead of average discharge current (AI), for the discharge rate. The equation used to predict at rate time-to-empty is:

$$ARTTE = 60 \times \frac{ARCAP}{AR} \quad (1)$$

The host system has read only access to this register pair.

Reported Temperature Registers (TEMPL/TEMPH) − Address 0x06/0x07

The TEMPH and the TEMPL registers contain the reported die temperature. The temperature is expressed in units of 0.25°K per count and updated every 2 seconds. The equation to calculate reported pack temperature is:

$$T_{PACK} = 0.25 \times (256 \times TEMPH + TEMPL) \quad (2)$$

The host system has read-only access to this register pair.

Reported Battery Voltage Registers (VOLTL/VOLTH) − Address 0x08/0x09

The VOLTH and the VOLTL low-byte registers contain the reported battery voltage measured on the BAT pin. Voltage is expressed in mV and is updated every two seconds. Reported voltage cannot exceed 5000 mV. The host system has read only access to this register pair.

APPLICATION INFORMATION

Status Flag Register (FLAGS) − Address 0x0A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	CHGS	NOACT	IMIN	CI	RSVD	VDQ	EDV1	EDVF
POR STATUS	0	0	0	1	0	0	0	0

MODE REGISTER	DESCRIPTION
CHGS	Charge-state flag. A “1” in the CHGS indicates a charge current (VSRP > VSRN). A “0” indicates a lack of charge activity. This bit should be read when the host system reads the average current register pair to determine the sign of the average current magnitude. This bit is cleared to “0” on all resets.
NOACT	No-activity flag. A “1” indicates that the voltage across R_S is less than the digital magnitude filter. See the *Digital Magnitude Filter* section for more information. This bit is cleared to ”0” on all resets.
IMIN	Li-ion taper current detection flag. A “1” indicates that the charge current has tapered to less than the taper value set in EEPROM and that the battery voltage is greater than or equal to the value selected by the QV0 and QV1 bits in the PKCFG register (see *EEPROM Data Registers* description for more details). This bit is cleared to “0” on all resets.
CI	Capacity Inaccurate flag. A ”1” indicates that the firmware has not been through a valid learning cycle and is basing all calculations on design values programmed into EEPROM. This bit will be set on a full reset and will only be cleared on a LMD update following a learning cycle.
RSVD	Reserved bit.
VDQ	Valid-discharge flag. A “1” indicates that the bq26500 has met all necessary requirements for a capacity learning discharge cycle. This bit clears to “0” on a LMD update or condition that disqualifies a learning cycle. This bit is cleared to “0” on all resets.
EDV1	End-of-discharge-voltage-1 flag. A “1” indicates that voltage on the BAT pin is less than or equal to the EDV1 voltage programmed in EEPROM and the battery has less than or equal to 6.25% of LMD capacity remaining. LMD updates immediately if the VDQ bit is set when this bit transitions from 0 to 1. This bit is cleared to ”0” on all resets or when charging.
EDVF	End-of-discharge-voltage-final flag. A “1” indicates that the battery has discharged fully based on design capacity programmed in EEPROM. Used to define the empty capacity threshold. This bit is cleared to ”0” on all resets or when charging.

The host system has read-only access to this register.

APPLICATION INFORMATION

Relative State of Charge (RSOC) – Address 0x0B

RSOC reports the battery charge as a percentage of the last measured discharge value (LMD). This value should be used if the end equipment reports percentage rather than time-to-empty. The equation is:

$$RSOC(\%) = 100 \times \frac{NAC}{LMD} \quad (3)$$

The host system has read-only access to this register.

Nominal Available Capacity Registers (NACL/NACH) – Address 0x0C/0x0D

Uncompensated available capacity in the battery. NAC is reported in counts of 3 μVh. This register pair increments during charge ($V_{SRP} > V_{SRN}$) and decrements during discharge ($V_{SRP} < V_{SRN}$). The NAC registers are cleared when the BAT voltage is less than or equal to EDVF while discharging. The NAC registers are cleared during reset or power-on-reset (POR), if RAM corruption is detected. The register value is retained after a reset if RAM corruption is not detected. The host system has read only access to this register pair.

Discharge Rate Compensated Available Capacity Registers (CACDL/CACDH) – Address 0x0E/0x0F

Available capacity in the battery, compensated for discharge rate. CACD is reported in counts of 3 μVh. This register pair follows NAC during charge and discharge by an amount computed from the measured discharge rate and the discharge rate compensation value programmed into EEPROM. CACD is not allowed to increase while discharging, so that if the discharge rate decreases, the available capacity does not increase. CACD equals NAC if the CHGS bit is **“1”**. If CHGS is **“0”**, CACD is the smaller of the previous and new computed values. The host system has read-only access to this register pair.

Temperature Compensated CACD Registers (CACTL/CACTH) – Address 0x10/0x11

Available capacity in the battery, compensated for discharge rate and temperature. CACT is reported in counts of 3 μVh. This register pair follows CACD during both charge and discharge unless the temperature is less than the threshold programmed into EEPROM. Once the temperature falls below the programmed threshold, the CACT value is reduced from CACD by an amount computed from ILMD and the temperature compensation constants programmed into EEPROM. The host system has read only access to this register pair.

Last Measured Discharge Registers (LMDL/LMDH) – Address 0x12/0x13

Last measured discharge, used as a measured full reference, is based on the measured discharge capacity of the battery from full to empty. LMD is reported in counts of 3 μVh.The firmware updates LMD on a valid capacity learning cycle, which is defined as the battery reaching the EDV1 level while the VDQ bit is set. Used with NAC register values to calculate relative state of charge (RSOC). The host system has read only access to this register pair.

APPLICATION INFORMATION

Reserved Registers

The addresses 0x14 – 0x6D and addresses 0x6F – 0x75 are reserved and cannot be written by the host.

EEPROM Enable Register (EE_EN) – Address 0x6E

Register used to enable host writes to EEPROM data locations (addresses 0x76 – 0x7F). Host must write data 0xDD to this register to enable EEPROM programming. See the *Programming the EEPROM* section for further information on programming the EEPROM bytes.

EEPROM Data Registers (EE_DATA) – Address 0x76 – 0x7F

The EEPROM data registers contain information vital to the performance of the device. These registers are to be programmed during pack manufacturing to allow flexibility in the design values of the battery to be monitored. The EEPROM data registers are listed in Table 2. Detailed descriptions of what should be programmed follows. See *Programming the EEPROM* for detailed information on writing the values to EEPROM.

Table 2. bq26500 EEPROM Memory Map

ADDRESS	NAME	FUNCTION
0x7F	TCOMP	Temperature compensation constants, ***OR***, ID#1
0x7E	DCOMP	Discharge rate compensation constants, ***OR***, ID#2
0x7D	ID3	ID#3
0x7C	PKCFG	Pack configuration values
0x7B	TAPER	Charge termination taper current
0x7A	DMFSD	Digital magnitude filter and self-discharge rate constants
0x79	ISLC	Initial standby load current
0x78	SEDV1	Scaled EDV1 threshold
0x77	SEDVF	Scaled EDVF threshold
0x76	ILMD	Initial last measured discharge high byte

APPLICATION INFORMATION

Initial Last Measured Discharge High Byte (ILMD) – Address 0x76

This register contains the scaled design capacity of the battery to be monitored. The equation to calculate the initial LMD is:

$$\text{ILMD} = \frac{\text{Design Capacity (mAh)} \times R_S(\text{m}\Omega)}{(256 \times 3\ \mu\text{Vh})} \quad (4)$$

where R_S is the value of the sense resistor used in the system. This value is used as the high byte for the initial LMD values. The initial low byte value is "**0**".

Scaled EDVF Threshold (SEDVF) – Address 0x77

This register contains the scaled value of the threshold for zero battery capacity. To calculate the value to program, use the following equation:

$$\text{SEDVF} = \frac{\text{Design EDVF (mV)}}{8} - 256 \quad (5)$$

Scaled EDV1 Threshold (SEDV1) – Address 0x78

This register contains the scaled value of the voltage when the battery has 6.25% remaining capacity. When the battery reaches this threshold during a valid discharge, the device learns the full battery capacity, including the remaining 6.25%. To calculate the value to program, use the following equation:

$$\text{SEDV1} = \frac{\text{Design EDV1 (mV)}}{8} - 256 \quad (6)$$

Initial Standby Load Current (ISLC) – Address 0x79

This register contains the scaled end equipment design standby current. A capacity learning cycle is disqualified if average current is less than or equal to two times the initial standby load when the EDV1 threshold voltage is reached. The equation for programming this value is:

$$\text{ISLC} = \frac{\text{Design Standby Current (mA)} \times R_S\ (\text{m}\Omega)}{6\ (\mu\text{V})} \quad (7)$$

where R_S is the value of the sense resistor used in the system.

APPLICATION INFORMATION

Digital Magnitude Filter and Self-Discharge Values (DMFSD) – Address 0x7A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DMF[3]	DMF[2]	DMF[1]	DMF[0]	SD[3]	SD[2]	SD[1]	SD[0]

MODE REGISTER	DESCRIPTION
DMF[3]	Sets the digital magnitude filter (DMF) threshold. See *Digital Magnitude Filter* section for more information on the function of the DMF. The value to be programmed is: $DMF[3:0] = \frac{\text{Design Threshold}}{6}, \ \mu V$
DMF[2]	
DMF[1]	
DMF[0]	
SD[3]	Sets the self-discharge rate %/day value at 25°C. NAC is reduced with an estimated self-discharge correction to adjust for the expected self-discharge of the battery. This estimation is only performed when the battery is not being charged. The rate programmed in EEPROM for DMFSD determines the self-discharge when 20°C ≤ TEMP < 30°C. The self-discharge estimation is doubled for each 10°C decade hotter than the 20°C−30°C decade, up to a maximum of 16 times the programmed rate for TEMP ≥ 60°C and is halved for each 10°C decade colder than the 20°C−30°C decade, down to a minimum of one-quarter the programmed rate for TEMP < 0°C. The self-discharge estimation is performed by reducing NAC by NAC/512 at a time interval that achieves the desired estimation. If DMFSD is programmed with 12 decimal, the self-discharge rate is 0.195% per day in the 20°C−30°C decade. This is accomplished by reducing NAC by NAC/512 (100/512 = 0.195%) a single time every 24 hours. If temperature rises by 10°C, the 0.195% NAC reduction is made every 12 hours. The value to be programmed is: $SD[3:0] = \frac{2.34}{\text{Design SD}}$, %/day
SD[2]	
SD[1]	
SD[0]	

Taper Current (TAPER) − Address 0x7B

This register contains the scaled end equipment design charge taper current. This value, in addition to battery voltage, is used to determine when the battery has reached a full charge state. The equation for programming this value is:

$$TAPER = \frac{I_{TAPER}\,(mA) \times R_S\,(m\Omega)}{192\,(\mu V)} \quad (8)$$

where R_S is the value of the sense resistor used in the system.

APPLICATION INFORMATION

Pack Configuration (PKCFG) − Address 0x7C

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GPIEN	QV1	QV0	RSVD	RSVD	RSVD	DCFIX	TCFIX

PKCFG REGISTER	DESCRIPTION
GPIEN	Allows the pack manufacturer to set the state of the GPIO pin on initial power up. If the bit is “0”, the GPIEN bit is cleared on reset and the GPIO pin acts as a high impedance output. If the bit is “1”, the GPIEN bit is set on reset and the GPIO pin acts as an input. The state of the GPIO pin can then be read through the GPSTAT bit in the MODE register.
QV1	These bits set the end voltage for charge termination. The terminating voltage is set as shown in Table 3.
QV2	
RSVD	No function.
DCFIX	Fixed discharge compensation. Normal discharge rate compensation (DCOMP register) is used if this bit is set to “0”. If this bit is set to “1”, the device assumes a fixed value of 0x42 for DCOMP, giving a discharge rate compensation gain of 6.25% with a compensation threshold of C/4. Setting the bit to “1” frees the EEPROM location of 0x7E for use as a programmable identification byte.
TCFIX	Fixed temperature compensation. Normal temperature compensation (TCOMP register) is used if this bit is set to “0”. If this bit is set to “1”, the device assumes a fixed value of 0x7C for TCOMP, giving a temperature compensation gain of 0.68% of Design Capacity/°C with an offset of 12°C. Setting this bit to “1” frees the EEPROM location of 0x7F for use as a programmable identification byte.

Table 3. Charge Termination Voltage Settings

QV1	QV2	VOLTAGE (mV)
0	0	3968
0	1	4016
1	0	4064
1	1	4112

APPLICATION INFORMATION

Identification Byte #3 (ID3) − Address 0x7D

This register may be programmed to any desired value.The contents do not affect the operation of the bq26500.

Discharge Rate Compensation Constants (DCOMP) or ID2 − Address 0x7E

This register is used to set the compensation coefficients for discharge rate. These coefficients are applied to the nominal available charge (NAC) to more accurately predict capacity at high discharge rates.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DCGN[5]	DCGN[4]	DCGN[3]	DCGN[2]	DCGN[1]	DCGN[0]	DCOFF[1]	DCOFF[0]

MODE REGISTER	DESCRIPTION
DCGN[5]	Discharge rate compensation gain. Used to set the slope of the discharge capacity compensation as a percentage of discharge current. The gain factor adjustment is in increments of 0.39% of discharge current in excess of the DCOFF value. The equation for programming the value is: DCGN[5:0] = 2.56 × design discharge compensation gain %
DCGN[4]	
DCGN[3]	
DCGN[2]	
DCGN[1]	
DCGN[0]	
DCOFF[1]	These bits set the discharge threshold of compensating the nominal available charge for discharge rate. The threshold is set as shown in Table 4.
DCOFF[0]	

Table 4. Discharge Rate Compensation Thresholds

DCOFF[1]	DCOFF[0]	DCOFF THRESHOLD
0	0	0
0	1	LMD/2
1	0	LMD/4
1	1	LMD/8

Discharge compensation, DCMP, is computed from these coefficients as follows:

$$DCMP = \frac{DCGN \times (AI - DCOFF)}{256} \quad (9)$$

where DCMP is restricted to ≥ 0. AI is the average discharge current. The CACD register then takes on the value:

$$CACD = NAC - (DCMP - DCMPADJ), \text{ if } DCMP > DCMPADJ \text{ or} \quad (10)$$

$$CACD = NAC, \text{ if } DCMP \leq DCMPADJ \quad (11)$$

where DCMPADJ is the value of DCMP at a previous EDV1 detection. This allows the compensation for CACD to adapt as the LMD value is learned.

If PKCFG[1]=1, the device assumes a fixed value of 0x42 for DCOMP, giving a discharge rate compensation gain of 6.25% with a compensation threshold of C/4. This frees the EEPROM location of 0x7E for a user-defined identification byte, ID2.

APPLICATION INFORMATION

Temperature Compensation Constants (TCOMP) or ID1 – Address 0x7F

This register is used to set the compensation coefficients for temperature. These coefficients are applied to the discharge rate compensated available charge (CACD) to more accurately predict capacity available at cold temperature.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	TCGN[3]	TCGN[2]	TCGN[1]	TCGN[0]	TOFF[3]	TOFF[2]	TOFF[1]	TOFF[0]

MODE REGISTER	DESCRIPTION
TCGN[3]	Temperature compensation gain. Used to set the slope of the compensation as a percentage of design capacity (DC) decrease per °C. The equation for programming the value is: TCGN[3:0] = 10.24 × design temp compensation gain % DC/°C
TCGN[2]	
TCGN[1]	
TCGN[0]	
TOFF[3]	Temperature compensation offset. Used to set the offset of the compensation. The temperature threshold is also used as the cold temperature disqualification for learning cycle even if TCGN=0. The equation for programming the value is: TOFF[3:0] = design temp compensation offset (°K) − 273
TOFF[2]	
TOFF[1]	
TOFF[0]	

Temperature compensation, TCMP, is computed from these coefficients as follows:

$$TCMP = TCGN \times \frac{ILMD \times (273 + TOFF - T)}{4} \quad (12)$$

where T is the temperature in °K and T < 273 + TOFF. TCMP = 0 if T ≥ 273 + TOFF. CACT is then computed as follows:

$$CACT = CACD - (TCMP - TCMPADJ) \quad (13)$$

where TEMPADJ is the value of TCMP at EDV1 or is equal to zero, depending on whether the EDV1 condition or full condition respectively, occurred last.

If PKCFG[0]=1, the device assumes a fixed value of 0x7C for TCOMP, giving a temperature compensation gain of 0.68% DC/°C with an offset of 12°C. This frees the EEPROM location of 0x7F for a user-defined identification byte, ID1.

APPLICATION INFORMATION

POWER MODES

The bq26500 has four power modes: active, sleep, ship, and hibernate. Figure 5 shows the flow that moves the device between the active, sleep, and ship modes. Hibernate is a special mode not included in the flow. Detailed explanations of each mode follow the diagram.

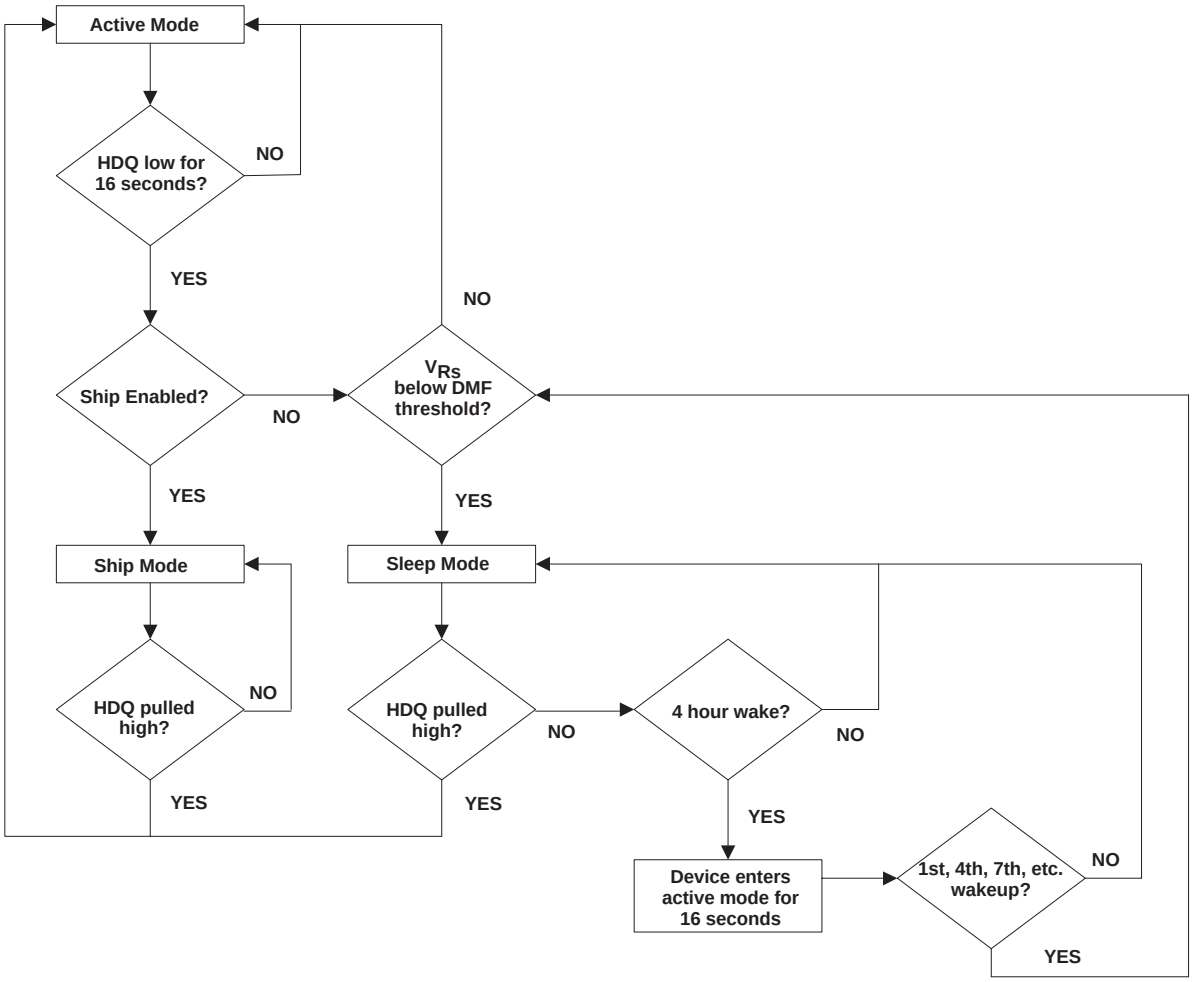


Figure 5. Power Mode Flow Chart

APPLICATION INFORMATION

Active Mode

During normal operation, the device is in active mode, which corresponds to the highest power consumption. Normal gas gauging is performed in this mode. If system requirements mandate that bq26500 should not enter sleep or ship modes then an external pull-up resistor between V_{CC} and HDQ is required on the bq26500 side of the system. The resistor value chosen should be small enough to force a logic “1” on HDQ even with the HDQ internal pull-down current and any external ESD protection circuitry loading.

Sleep Mode

This low power mode is entered when the HDQ line is pulled low for at least 16 seconds and the charge or discharge activity is below the digital magnitude filter. It may take up to 30 minutes to determine the no-activity condition after charge or discharge current is removed. Normal gas gauging ceases, but battery self-discharge, based on the temperature when the device entered sleep mode, is maintained internally. The device wakes every 4 hours to perform a temperature conversion and will go back to sleep after 16 seconds if the HDQ line is still low. bq26500 has an internal pull-down device that sinks less than I_{HDQPD}, allowing the device to enter sleep mode if the battery pack is pulled from the system and there is not a pull-up mechanism present.

When the device wakes the first time to perform a temperature update, it stays in active mode long enough to confirm that the charge or discharge activity is still below the digital magnitude filter threshold. This is meant to minimize possible error if the battery pack is removed from the end equipment and is later re-inserted without a transition on the HDQ line. This is only an issue if the system has some current drain from the battery even though HDQ is pulled low. The activity check will take 15 minutes to complete. The device reenters sleep mode if the activity is below the digital magnitude filter threshold. The device repeats the activity check every 3 wakeups (12 hours).

When the HDQ line is pulled high, the device leaves the sleep mode. The device enters the sleep mode again only after the HDQ line is pulled low for at least 16 seconds and the charge/discharge activity is below the digital magnitude filter threshold. If the DMF threshold is set to zero and HDQ line is pulled low, the device enters sleep mode if the VFC activity is less than 2 counts in 15 minutes. This is equivalent to approximately 24 μV across the current-sense resistor.

A 100-kΩ pull-up resistor from HDQ to V_{CC} can be added in the battery pack to disable the sleep function.

Ship Mode

This low power mode is to be used when the pack manufacturer has completed assembly and test of the pack. The ship mode is enabled by setting the SHIP bit in the MODE register and issuing the control command (data 0xA9 to register 0x00). Ship mode is entered only after the ship mode is enabled and the HDQ line has been pulled low for 16 seconds. This allows the pack manufacturer to enable the ship mode and pull the pack from the test equipment without any additional overhead. After the ship mode has been enabled but before the device has entered ship mode, transients on the HDQ line do not cause the device to stay in active mode.

All device functionality stops in ship mode and it does not start again until the HDQ line is pulled high (by plugging it into the end equipment) or the battery voltage drops below and then rises above the $V_{(POR)}$ threshold. Care should be taken to ensure that there are no glitches on the HDQ line after the device enters ship mode or else the device enters the active mode. It enters sleep if HDQ remains low, but does not re-enter ship mode unless another ship mode command is sent.

APPLICATION INFORMATION

Hibernate Mode

The device enters hibernate mode when V_{CC} drops below $V_{(POR)}$ and there is a voltage source connected to the RBI pin. V_{CC} must be raised above $V_{(POR)}$ in order to exit the hibernate mode. This mode retains RAM integrity and allows retention of remaining capacity, learned LMD, and the CI flag.

PROGRAMMING THE EEPROM

The bq26500 has 10 bytes of EEPROM that are used for firmware control and application data (see the *Register Descriptions* section for more information). Programming the EEPROM through the HDQ pin should take place during pack manufacturing, as a 21-V pulse is needed on the GPIO pin. The programming mode must be enabled prior to writing any values to the EEPROM locations. The programming mode is enabled by writing to the EE_EN register (address 0x6E) with data 0xDD. Once the programming mode is enabled, the desired data can be written to the appropriate address. Figure 6 shows the method for programming all locations.

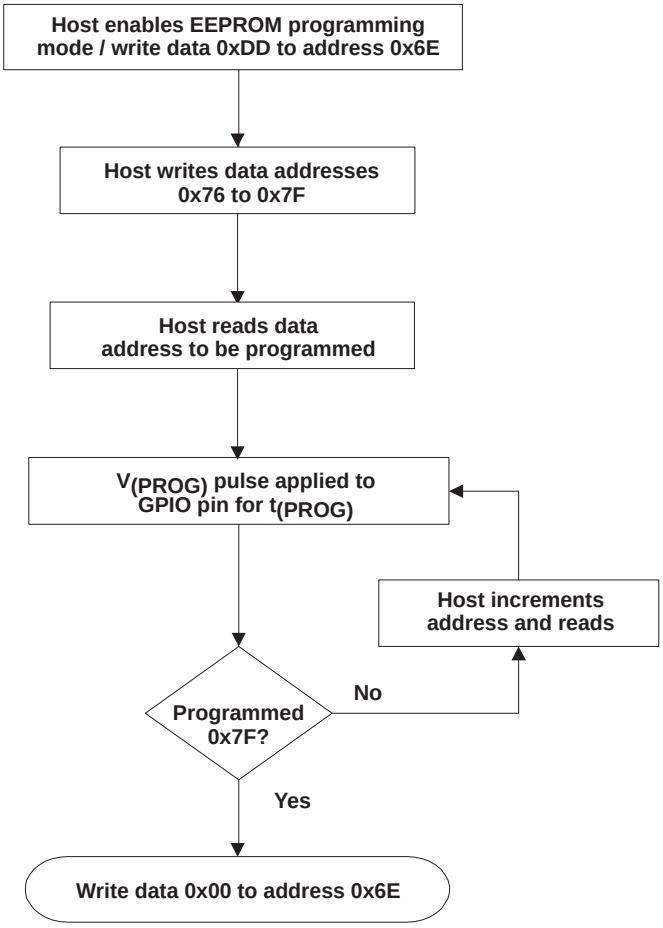


Figure 6. EEPROM Programming Flow Chart

It is not required that addresses 0x76 − 0x7F be programmed at the same time or in any particular order. The programming method illustrated in Figure 6 can be used to program any of the bytes as long as the sequence of enable, write, read, apply programming pulse, and disable is followed.

APPLICATION INFORMATION

COMMUNICATING WITH THE bq26500

The bq26500 includes a single-wire HDQ serial data interface. Host processors, configured for either polled or interrupt processing, can use the interface to access various bq26500 registers. The HDQ pin is an open drain device, which requires an external pull-up resistor. The interface uses a command-based protocol, where the host processor sends a command byte to the bq26500. The command directs the bq26500 to either store the next eight bits of data received to a register specified by the command byte, or to output the eight bits of data from a register specified by the command byte.

The communication protocol is asynchronous return-to-one and is referenced to V_{SS}. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5 Kbits/s. The least-significant bit of a command or data byte is transmitted first. Data input from the bq26500 may be sampled using the pulse-width capture timers available on some microcontrollers. A UART can also be configured to communicate with the bq26500.

If a communication time-out occurs (for example, if the host waits longer than $t_{(RSPS)}$ for the bq26500 to respond) or if this is the first access command, then a BREAK should be sent by the host. The host may then resend the command. The bq26500 detects a BREAK when the HDQ pin is driven to a logic-low state for a time $t_{(B)}$ or greater when the bus is free. If the host sends a BREAK when the bq26500 is transmitting a bit, it is possible that the BREAK would be ignored. Best practice is to hold all BREAK transmissions for twice the minimum time listed in the HDQ specification table. The HDQ pin then returns to its normal ready-high logic state for a time $t_{(BR)}$.The bq26500 is then ready for a command from the host processor.

The return-to-one data-bit frame consists of three distinct sections:

1. The first section starts the transmission by either the host or the bq26500 taking the HDQ pin to a logic-low state for a period equal to $t_{(HW1)}$ or $t_{(DW1)}$.
2. The next section is the actual data transmission, where the data should be valid for $t_{(HW0)} - t_{(HW1)}$ or $t_{(DW0)} - t_{(DW1)}$.
3. The final section stops the transmission by returning the HDQ pin to a logic-high state and holding it high until the time from bit start to bit end is equal to $t_{(CYCH)}$ or $t_{(CYCD)}$.

The HDQ line may remain high for an indefinite period of time between each bit of address or between each bit of data on a write cycle. After the last bit of address is sent on a read cycle, the bq26500 starts outputting the data after $t_{(RSPS)}$ with timing as specified. The serial communication timing specification and illustration sections give the timings for data and break communication. Communication with the bq26500 always occurs with the least-significant bit being transmitted first.

Plugging in the battery pack may be seen as the start of a communication due to contact bounce. It is recommended that each communication or string of communications be preceded by a break to reset the HDQ engine.

APPLICATION INFORMATION

Command Byte

The command byte of the bq26500 consists of eight contiguous valid command bits. The command byte contains two fields: W/R command and address. The command byte values are shown in the following table:

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	W/R	AD6	AD5	AD4	AD3	AD2	AD1	AD0

MODE REGISTER	DESCRIPTION
W/R	W/R indicates whether the command bytes is a read or write command. A “1” indicates a write command and that the following eight bits should be written to the register specified by the address field of the command byte, while a “0” indicates that the command is a read. On a read command, the bq26500 outputs the requested register contents specified by the address field portion of the command Byte.
AD[6]	The seven bits labeled AD6 through AD0 containing the address portion of the register to be accessed
AD[5]	
AD[4]	
AD[3]	
AD[2]	
AD[1]	
AD[0]	

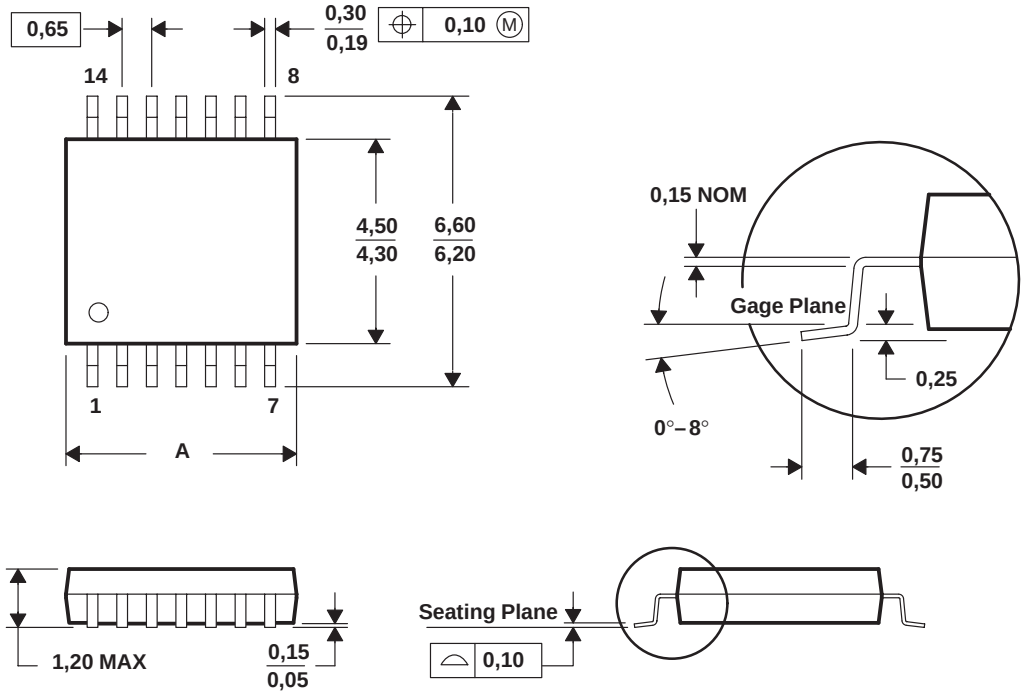
Reading 16 bit Registers

Since 16-bit values are only read 8 bits at a time with the HDQ interface, it is possible that the device may update the register value between the time the host reads the first and second bytes. To prevent any system issues, any 16-bit values read by the host should be read using the following protocol. The entire read sequence should complete in less than 0.8 s, the fastest rate at which any register pair is updated.

1. Read high byte (H0)
2. Read low byte (L0)
3. Read high byte (H1)
4. If H1 = H0, then valid result is H0, L0
5. Otherwise, read low byte (L1) and valid result is H1, L1.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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