4 Mbit / 8 Mbit LPC Serial Flash

SST49LF004C / SST49LF008C

Advance Information

FEATURES:

- **Organized as 512K x8 / 1M x8**
- **Conforms to Intel® LPC Interface Specification v1.1**
  - Support Multi-Byte Firmware Memory Read/ Write Cycles
- **Single 3.0-3.6V Read and Write Operations**
- **LPC Mode**
  - 5-signal LPC bus interface for both in-system and factory programming using programmer equipment
  - Multi-Byte Read capability allowing 15.6 MB/s data transfer rate @ 33 MHz PCI clock
    - Firmware Memory Read cycle supporting 1, 2, 4, 16, and 128 Byte Read
    - Firmware Memory Write cycle supporting 1, 2, and 4 Byte Write
  - 33 MHz clock frequency operation
  - WP#/AAI and TBL# pins provide hardware Write protect for entire chip and/or top Boot Block
  - Block Locking Registers for individual block Read-Lock, Write-Lock, and Lock-Down protection
  - 5 GPI pins for system design flexibility
  - 4 ID pins for multi-chip selection
  - Multi-Byte capability registers (read-only registers)
  - Status register for End-of-Write detection
  - Program-/Erase-Suspend Read or Write to other blocks during Program-/Erase-Suspend
- **Two-cycle Command Set**
- **Security ID Feature**
  - 256-bit Secure ID space
    - 64-bit Unique Factory Pre-programmed Device Identifier
    - 192-bit User-Programmable OTP
- **Low Power Consumption**
  - Active Read Current: 12 mA (typical)
    - Standby Current: 10 µA (typical)
- **Protected Data Area**
  - 12-KByte Protected Data Area space
  - Three 4-KByte User-Programmable flash memory sectors
  - Read-lock, write-lock and lock-down protection for each sector
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Uniform 4 KByte sectors**
  - SST49LF004C: 11 Overlay Blocks:
    - one 16-KByte Boot Block
    - two 8-KByte Parameter Blocks
    - one 32-Kbyte Parameter Block
    - seven 64-KByte Main Blocks
  - SST49LF008C: 19 Overlay Blocks:
    - one 16-KByte Boot Block
    - two 8-KByte Parameter Blocks
    - one 32-Kbyte Parameter Block
    - 15 64-KByte Main Blocks
- **Fast Sector-Erase/Program Operation**
  - Sector-Erase Time: 18 ms (typical)
  - Block-Erase Time: 18 ms (typical)
  - Program Time: 7 µs (typical)
- **Auto Address Increment (AAI) for Rapid Factory Programming (High Voltage Enabled)**
  - RY/BY# pin for End-of-Write detection
  - Multi-Byte Program
  - Chip Rewrite Time: (typical)
    - SST49LF004C: 1 seconds
    - SST49LF008C: 2 seconds
- **Packages Available**
  - 32-lead PLCC
  - 32-lead TSOP (8mm x 14mm)
- **All non-Pb (lead-free) devices are RoHS compliant**

PRODUCT DESCRIPTION

The SST49LF00xC flash memory devices are designed to interface with host controllers (chipsets) that support a low-pin-count (LPC) interface for system firmware applications. The SST49LF00xC device complies with Intel's LPC Interface Specification 1.1, supporting a Burst-Read (up to 128 bytes in a single operation) which enables a 15.6 MByte per second data transfer. The LPC interface operates with 5 signal pins versus 28 pins of a 8-bit parallel flash memory. This frees up pins on the ASIC host controller resulting in lower ASIC costs and a reduction in overall system costs due to simplified signal routing.

The SST49LF00xC use a 5-signal LPC interface to support both in-system and rapid factory programming using programmer equipment. A high voltage pin (WP#/AAI) is used to enable Auto Address Increment (AAI) mode. The SST49LF00xC offers hardware block protection in addition to individual block protection via software registers for critical system code and data. A 256-bit Security ID space with a 64-bit factory pre-programmed unique number and a 192-bit user programmable OTP area as well as 12-KByte Protected Data Area (PDA) enhances the user's ability to implement new security techniques and data protection

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scheme. The PDA can be also used to store system configuration data (EEPROM replacement). The SST49LF00xC also provides general purpose inputs (GPI) for system design flexibility.

The SST49LF00xC flash memory device is manufactured with SST's proprietary, high-performance SuperFlash technology. The split-gate cell design and thick-oxide tunneling injector attain greater reliability and manufacturability compared with alternative technology approaches. The SST49LF00xC device significantly improves performance and reliability, while lowering power consumption. The SST49LF00xC device writes (Program or Erase) in-system with a single 3.0-3.6V power supply. It uses less energy during Erase and Program than alternative flash memory technologies.

The total energy consumed is a function of the applied voltage, current and time of application. Since for any given voltage range, the SuperFlash technology uses less current to program and has a shorter erase time, the total energy consumed during any Erase or Program operation is less than alternative flash memory technologies.

The SuperFlash technology provides fixed Erase and Program time, independent of the number of Erase/Program cycles that have performed. Therefore the system software or hardware does not have to be calibrated or correlated to the cumulative number of erase cycles as is necessary with alternative flash memory technologies, whose Erase and Program time increase with accumulated Erase/Program cycles. To protect against inadvertent write, the SST49LF00xC device has on-chip hardware and software write protection schemes. It is offered with a typical endurance of 100,000 cycles. Data retention is rated at greater than 100 years.

The SST49LF00xC product provides a maximum program time of 10 µs per byte with a single-byte Program operation; effectively 5 µs per byte with a dual-byte Program operation and 2.5 µs per byte with a quad-byte Program operation. End-of-Write can be detected by the RY/BY# pin output in AAI mode and by reading the software status register during an in-system Program or Erase operation.

The SST49LF00xC is offered in 32-PLCC, and 32-TSOP packages. In addition, the SST49LF00xC devices are offered in lead-free (non-Pb) package options to address the growing need for non-Pb solutions in electronic components. Non-Pb package versions can be obtained by ordering products with a package code suffix of "E" as the environmental attribute in the product part number. See Figures 3 and 4 for pin assignments and Table 1 for pin descriptions.

TABLE OF CONTENTS

PRODUCT DESCRIPTION 1

LIST OF FIGURES 5

LIST OF TABLES 6

FUNCTIONAL BLOCKS 7

DEVICE MEMORY MAPS 8

PIN ASSIGNMENTS 9

PIN DESCRIPTIONS 10

- Clock 11
- Input/Output Communications 11
- Input Communication Frame 11
- Reset 11
- Identification Inputs 11
- General Purpose Inputs 11
- Write Protect / Top Block Lock 11
- AAI Enable 11
- Ready/Busy 12
- Load Enable 12
- No Connection (NC) 12

DESIGN CONSIDERATIONS 12

MODE SELECTION 12

LPC MODE 12

- Device Operation 12

FIRMWARE MEMORY CYCLES 13

- Firmware Memory Read Cycle 13
- Firmware Memory Write Cycle 14
- Abort Mechanism 15
- Response to Invalid Fields for Firmware Memory Cycle 15
- Multiple Device Selection 16

Advance Information

DEVICE COMMANDS 17
Read-Array Command 18
Read-Software-ID Command 18
Read-Status-Register Command 18
Clear-Status-Register Command 18
Sector-/Block-Erase Command 19
Program Command. 19
Program-/Erase-Suspend or Program-/Erase-Resume Operations 19
Erase-Suspend/Erase-Resume Commands. 19
Program-Suspend/Program-Resume Command 20
Security ID Commands 20
REGISTERS 21
Multi-Byte Read/Write Configuration Registers (Firmware Memory Cycle) 21
General Purpose Inputs Register 21
Block and PDA Sector Locking Registers. 22
Security ID Registers 24
JEDEC ID Registers 24
AUTO-ADDRESS INCREMENT (AAI) MODE 25
AAI Mode with Multi-byte Programming 25
AAI Data Load Protocol 26
ELECTRICAL SPECIFICATIONS 27
DC Characteristics 28
AC Characteristics 31
PRODUCT ORDERING INFORMATION. 34
PACKAGING DIAGRAMS 35

LIST OF FIGURES

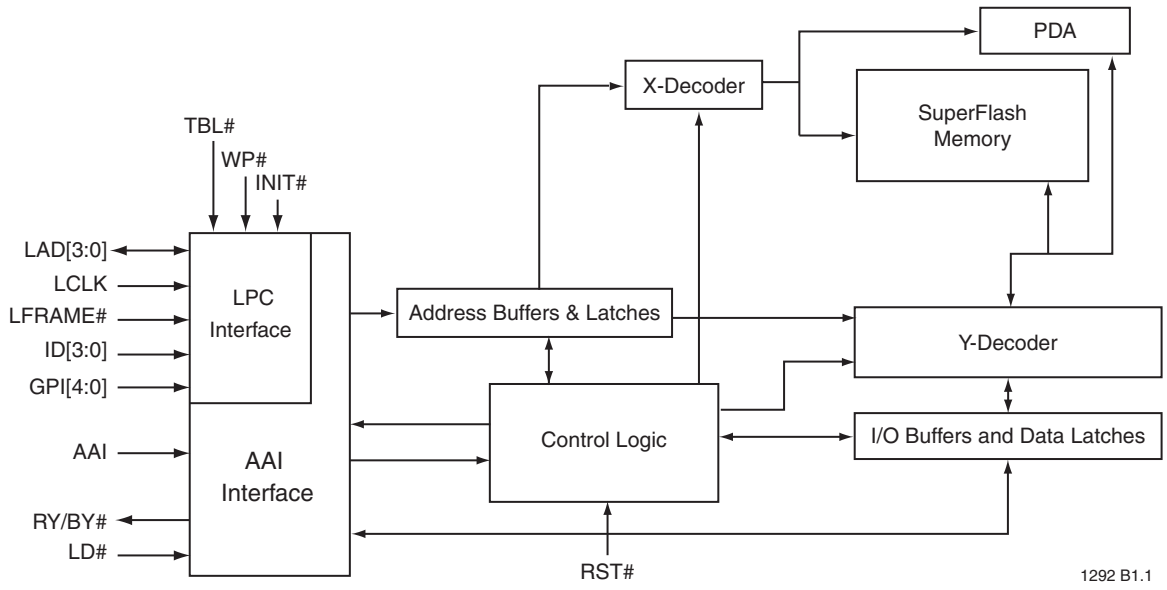
FIGURE 1: Device Memory Map for SST49LF004C 8
FIGURE 2: Device Memory Map for SST49LF008C 8
FIGURE 3: Pin Assignments for 32-lead PLCC 9
FIGURE 4: Pin Assignments for 32-lead TSOP 9
FIGURE 5: Firmware Memory Read Cycle Waveform 13
FIGURE 6: Firmware Memory Write Cycle Waveform 14
FIGURE 7: Erase-Suspend Flow Chart 20
FIGURE 8: AAI Load Protocol Waveform. 26
FIGURE 9: LCLK Waveform (LPC Mode) 29
FIGURE 10: Reset Timing Diagram (LPC MODE) 30
FIGURE 11: Output Timing parameters (LPC Mode) 32
FIGURE 12: Input Timing Parameters (LPC Mode) 32
FIGURE 13: Input Timing Parameters (AAI Mode) 33
FIGURE 14: A Test Load Example. 33

LIST OF TABLES

TABLE 1: Pin Description 10
TABLE 2: Transfer Size Supported 12
TABLE 3: Firmware Memory Cycles START Field Definition 12
TABLE 4: Firmware Memory Read Cycle Field Definitions 13
TABLE 5: Firmware Memory Write Cycle 14
TABLE 6: Valid MSIZE field Values for Firmware Memory Cycles 15
TABLE 7: Firmware Memory Multiple Device Selection Configuration 16
TABLE 8: Software Command Sequence 17
TABLE 9: Product Identification 18
TABLE 10: Software Status Register 18
TABLE 11: Security ID Addresses 20
TABLE 12: General Purpose Register 21
TABLE 13: Multi-byte Read/Write Configuration Registers 21
TABLE 14: Block Locking Registers 22
TABLE 15: Protected Data Area Sector Locking Registers 22
TABLE 16: Block/PDA Sector Locking Register Bits 23
TABLE 17: Security ID Registers 24
TABLE 18: JEDEC ID Registers 24
TABLE 19: LD# Input and RY/BY# Status inAAI Mode 25
TABLE 20: AAI Programming Cycle (initiated with WP#/AAI at V_H ONLY) 26
TABLE 21: DC Operating Characteristics (All Interfaces) 28
TABLE 22: Recommended System Power-up Timings 28
TABLE 23: Pin Capacitance 28
TABLE 25: Clock Timing Parameters (LPC Mode) 29
TABLE 24: Reliability Characteristics 29
TABLE 26: Reset Timing Parameters (LPC Mode) 30
TABLE 27: Read/Write Cycle Timing Parameters (LPC Mode) 31
TABLE 28: AC Input/Output Specifications (LPC Mode) 31
TABLE 29: Interface Measurement Condition Parameters (LPC Mode) 32
TABLE 30: Input Cycle Timing Parameters (AAI Mode) 33
TABLE 31: Revision History 36

FUNCTIONAL BLOCKS

FUNCTIONAL BLOCK DIAGRAM



Advance Information

DEVICE MEMORY MAPS

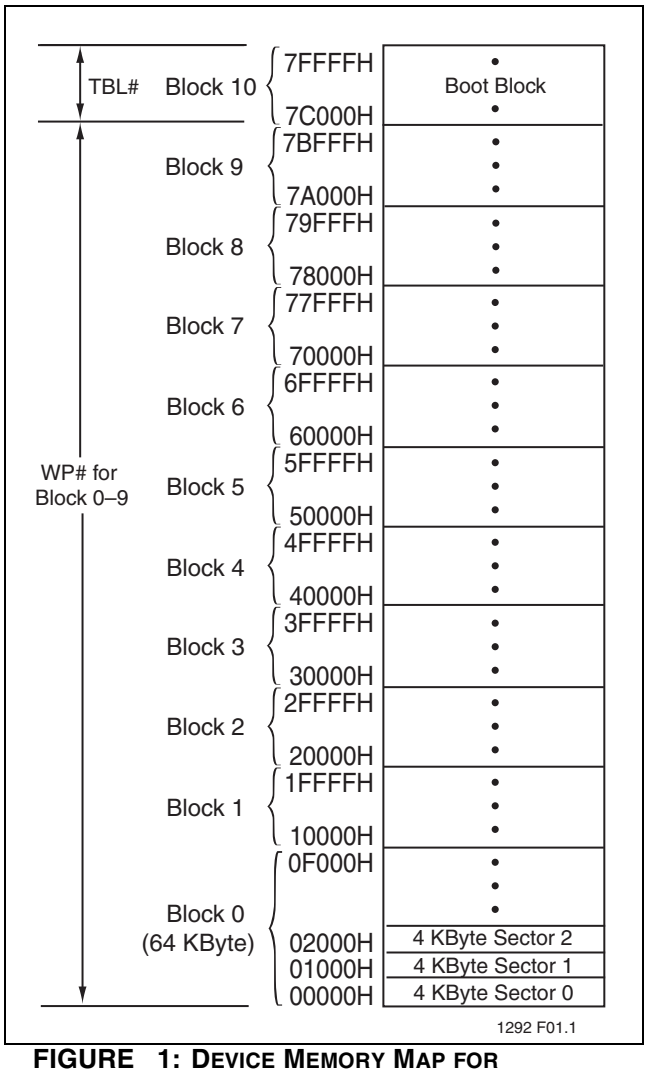


FIGURE 1: DEVICE MEMORY MAP FOR SST49LF004C

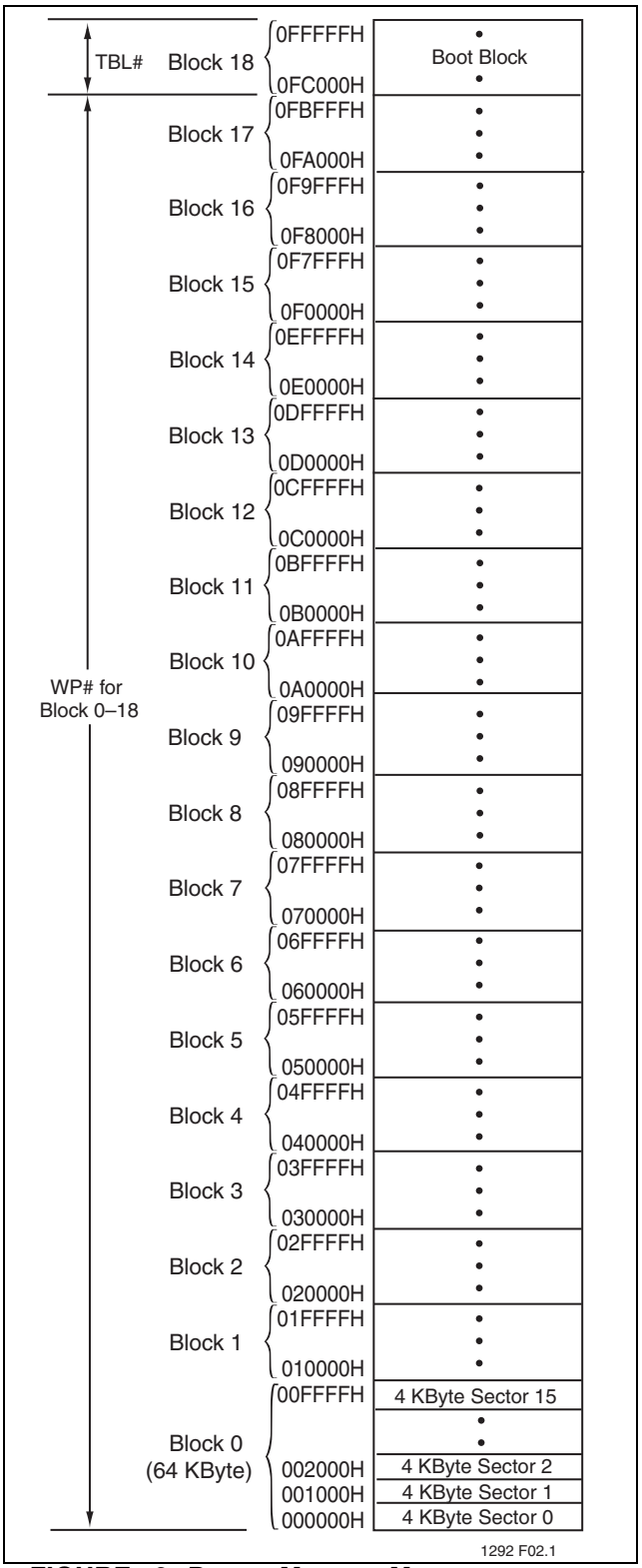


FIGURE 2: DEVICE MEMORY MAP FOR SST49LF008C

PIN ASSIGNMENTS

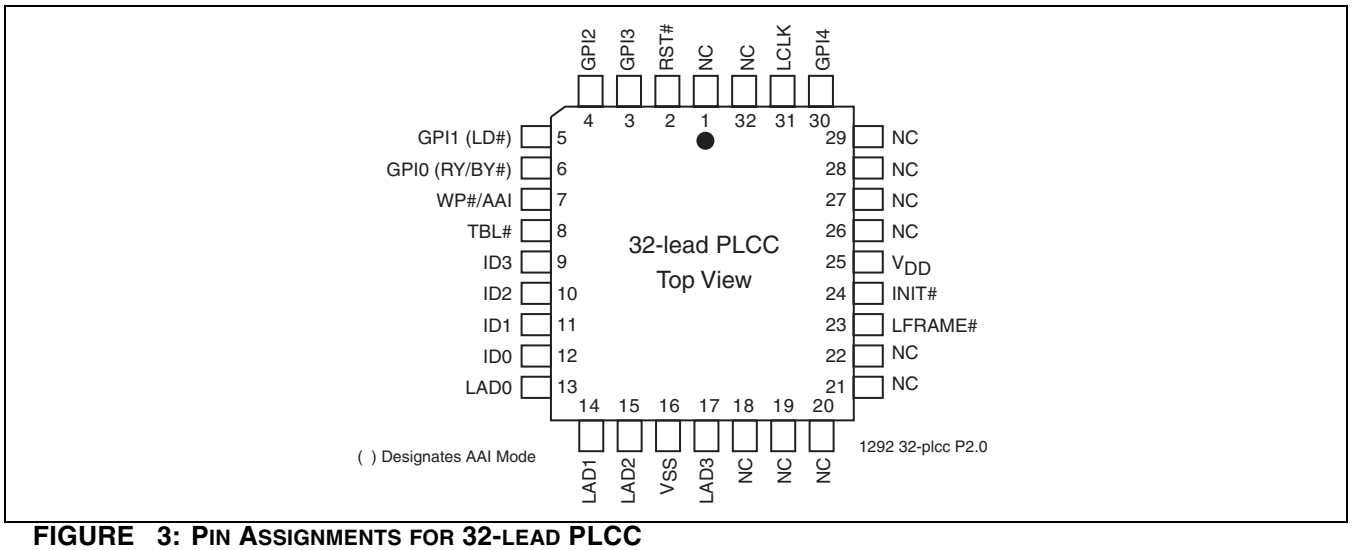


FIGURE 3: PIN ASSIGNMENTS FOR 32-LEAD PLCC

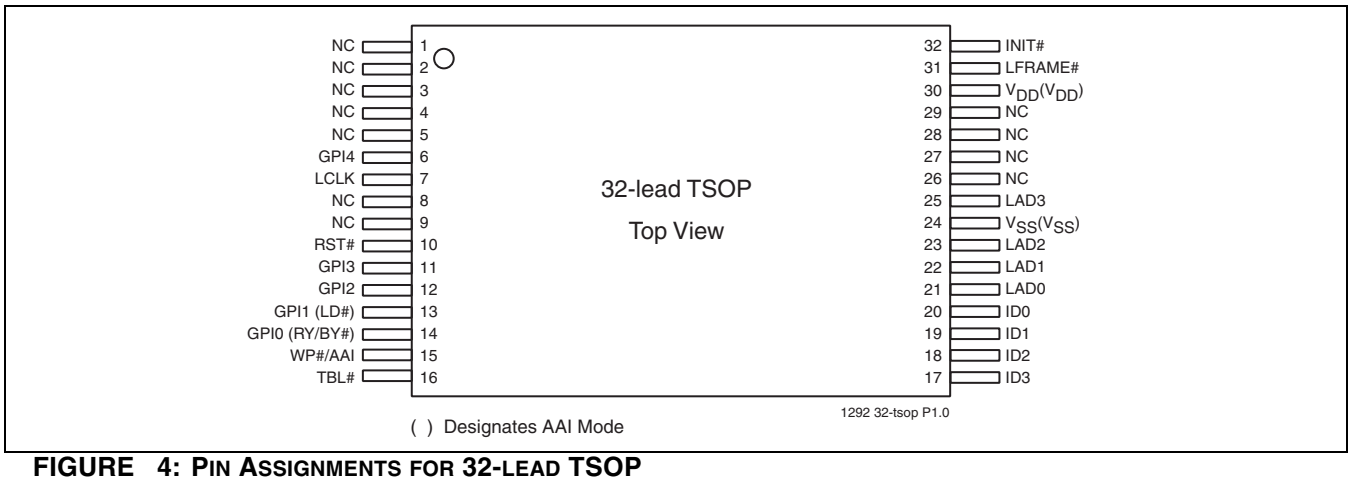


FIGURE 4: PIN ASSIGNMENTS FOR 32-LEAD TSOP

Advance Information

PIN DESCRIPTIONS

TABLE 1: PIN DESCRIPTION

Symbol	Pin Name	Type[1]	Interface		Functions
			AAI	LPC	
LCLK	Clock	I	X	X	To accept a clock input from the control unit
LAD[3:0]	Address and Data	I/O	X	X	To provide LPC bus information, such as addresses and command Inputs/Outputs data.
LFRAME#	Frame	I	X	X	To indicate the start of a data transfer operation; also used to abort an LPC cycle in progress.
RST#	Reset	I	X	X	To reset the operation of the device
INIT#	Initialize	I	X	X	This is the second reset pin for in-system use. This pin is internally combined with the RST# pin. If this pin or RST# pin is driven low, identical operation is exhibited.
ID[3:0]	Identification Inputs	I	X	X	These four pins are part of the mechanism that allows multiple parts to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:0]=0000, all subsequent devices should use sequential up-count strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ. When in AAI mode, these pins operate identically as in Firmware Memory cycles.
GPI[4:0]	General Purpose Inputs	I		X	These individual inputs can be used for additional board flexibility. The state of these pins can be read through LPC registers. These inputs should be at their desired state before the start of the LPC clock cycle during which the read is attempted, and should remain in place until the end of the Read cycle. Unused GPI pins must not be floated. GPI[2:4] are ignored when in AAI mode.
TBL#	Top Block Lock	I		X	When low, prevents programming to the boot block sectors at top of device memory. When TBL# is high it disables hardware write protection for the top block sectors. This pin cannot be left unconnected. TBL# setting is ignored when in AAI mode.
WP#/AAI	Write Protect	I		X	When low, prevents programming to all but the highest addressable block (Boot Block). When WP# is high it disables hardware write protection for these blocks. This pin cannot be left unconnected.
WP#/AAI	AAI Enable	I	X		When set to the Supervoltage V_H = 9V, configures the device to program multiple bytes in AAI mode. When brought to V_{IL}/V_{IH}, returns device to LPC mode.
RY/BY#	Ready/Busy#	O	X		Open drain output that indicates the device is ready to accept data in an AAI mode, or that the internal cycle is complete. Used in conjunction with LD# pin to switch between these two flag states.
LD#	Load-Enable#	I	X		Input pin which when low, indicates the host is loading data in an AAI programming cycle. If LD# is high, the host signals the AAI interface that it is terminating a command. LD# low/high switches the RY/BY# output from a “buffer free” flag to a “programming complete” flag.
V_{DD}	Power Supply	PWR	X	X	To provide power supply (3.0-3.6V)
V_{SS}	Ground	PWR	X	X	Circuit ground (0V reference)
NC	No Connection		N/A	N/A	Unconnected pins.

T1.0 1292

1. I=Input, O=Output

Clock

The LCLK pin accepts a clock input from the host controller.

Input/Output Communications

The LAD[3:0] pins are used to serially communicate cycle information such as cycle type, cycle direction, ID selection, address, data, and sync fields.

Input Communication Frame

The LFRAME# pin is used to indicate start of a LPC bus cycle. The pin is also used to abort an LPC bus cycle in progress.

Reset

A V_{IL} on INIT# or RST# pin initiates a device reset. INIT# and RST# pins have the same function internally. It is required to drive INIT# or RST# pins low during a system reset to ensure proper CPU initialization. During a Read operation, driving INIT# or RST# pins low deselects the device and places the output drivers, LAD[3:0], in a high impedance state. The reset signal must be held low for a minimum of time T_{RSTP}. A reset latency occurs if a reset procedure is performed during a Program or Erase operation. See Table 26, Reset Timing Parameters, for more information. A device reset during an active Program or Erase operation will abort the operation and memory contents may become invalid due to data being altered or corrupted from an incomplete Erase or Program operation.

Identification Inputs

These pins are part of a mechanism that allows multiple devices to be attached to the same bus. The strapping of these pins is used to identify the component. The boot device must have ID[3:0] = 0; all subsequent devices should use sequential count-up strapping. These pins are internally pulled-down with a resistor between 20-100 KΩ

General Purpose Inputs

The General Purpose Inputs (GPI[4:0]) can be used as digital inputs for the CPU to read. The GPI register holds the values on these pins. The data on the GPI pins must be stable before the start of a GPI register Read and remain stable until the Read cycle is complete. The pins must be driven low, V_{IL}, or high, V_{IH} but not left unconnected (float).

Write Protect / Top Block Lock

The Top Boot Lock (TBL#) and Write Protect (WP#/AAI) pins are provided for hardware write protection of device memory in the SST49LF00xC. The TBL# pin is used to write protect 16 KByte at the highest memory address range for the SST49LF00xC. WP#/AAI pin write protects the remaining sectors in the flash memory. An active low signal at the TBL# pin prevents Program and Erase operations of the top Boot Block. When TBL# pin is held high, write protection of the top Boot Block is then determined by the Boot Block Locking registers. The WP#/AAI pin serves the same function for the remaining sectors of the device memory. The TBL# and WP#/AAI pins write protection functions operate independently of one another. Both TBL# and WP#/AAI pins must be set to their required protection states prior to starting a Program or Erase operation. A logic level change occurring at the TBL# or WP#/AAI pin during a Program or Erase operation could cause unpredictable results. TBL# and WP#/AAI pins cannot be left unconnected.

TBL# is internally OR'ed with the top Boot Block Locking register. When TBL# is low, the top Boot Block is hardware write protected regardless of the state of the Write-Lock bit for the Boot Block Locking register. Clearing the Write-Protect bit in the register when TBL# is low will have no functional effect, even though the register may indicate that the block is no longer locked.

WP#/AAI is internally OR'ed with the Block Locking register. When WP#/AAI is low, the blocks are hardware write protected regardless of the state of the Write-Lock bit for the corresponding Block Locking registers. Clearing the Write-Protect bit in any register when WP#/AAI is low will have no functional effect, even though the register may indicate that the block is no longer locked.

The TBL# pin and WP# pin do not affect the protection of the Protected Data Area. The PDA protection status is only determined by the value of the PDA Sector Locking Registers. (See "Block and PDA Sector Locking Registers" on page 22.)

AAI Enable

The AAI Enable pin (WP#/AAI) is used to enable the Auto Address Increment (AAI) mode. When the WP#/AAI pin is set to the Supervoltage V_H (9±0.5V), the device is in AAI mode with Multi-Byte programming. When the WP#/AAI pin is brought to V_{IL}/V_{IH} levels, the device returns to LPC mode.

Advance Information

Ready/Busy

The Ready/Busy pin (RY/BY#), is an open drain output which indicates the device is ready to accept data in an AAI mode, or that the internal programming cycle is complete. The pin is used in conjunction with the LD# pin to switch between these two flag states (see Table 19).

Load Enable

The Load Enable pin (LD#), is an input pin which when low, indicates the host is loading data in an AAI programming cycle. Data is loaded in the SST49LF00xC at the rising edge of the clock. If LD# is high, it signals the AAI interface that the host is terminating the command. LD# low/high switches the RY/BY# output from buffer free flag to programming complete flag (see Table 19).

No Connection (NC)

These pins are not connected internally.

DESIGN CONSIDERATIONS

SST recommends a high frequency 0.1 µF ceramic capacitor to be placed as close as possible between V_{DD} and V_{SS} less than 1 cm away from the V_{DD} pin of the device. Additionally, a low frequency 4.7 µF electrolytic capacitor from V_{DD} to V_{SS} should be placed within 1 cm of the V_{DD} pin. If you use a socket for programming purposes add an additional 1-10 µF next to each socket. The RST# pin must remain stable at V_{IH} for the entire duration of an Erase operation. WP#/AAI must remain stable at V_{IH} for the entire duration of the Erase and Program operations for non-Boot Block sectors. To write data to the top Boot Block sectors, the TBL# pin must also remain stable at V_{IH} for the entire duration of the Erase and Program operations.

MODE SELECTION

The SST49LF00xC flash memory device operates in two distinct interface modes: the LPC mode and the Auto Address Increment (AAI) mode. The WP#/AAI pin is used to set the interface mode selection. The device is in AAI mode when the WP#/AAI pin is set to the Supervoltage V_H (9±0.5V), and in the LPC mode when the WP#/AAI is set to V_{IL}/V_{IH}. The mode selection must be configured prior to device operation.

LPC MODE

Device Operation

The SST49LF00xC supports Multi-Byte Firmware Memory Read and Write cycle types as defined in Intel Low Pin Count Interface Specification, Revision 1.1. Table 2 shows the size of transfer supported by the SST49LF00xC.

TABLE 2: TRANSFER SIZE SUPPORTED

Cycle Type	Size of Transfer
Firmware Memory Read	1, 2, 4, 16, 128 Bytes
Firmware Memory Write	1, 2, 4 Bytes

T2.0 1292

The LPC mode uses a 5-signal communication interface: one control line, LFRAME#, which is driven by the host to start or abort a bus cycle, a 4-bit data bus, LAD[3:0], used to communicate cycle type, cycle direction, ID selection, address, data and sync fields. The device enters standby mode when LFRAME# is taken high and no internal operation is in progress.

The host drives LFRAME# signal from low-to-high to capture the start field of a LPC cycle. On the cycle in which LFRAME# goes inactive, the last latched value is taken as the START value. The START value determines whether the SST49LF00xC will respond to a Firmware Memory Read/Write cycle type as defined in Table 3.

TABLE 3: FIRMWARE MEMORY CYCLES START FIELD DEFINITION

START Value	Definition
1101	Start of a Firmware Memory Read cycle
1110	Start of a Firmware Memory Write cycle

T3.0 1292

See following sections on details of Firmware Memory cycle types (Tables 4 and 5). Two-cycle Program and Erase command sequences are used to initiate Firmware Memory Program and Erase operations. See Table 8 for a listing of Program and Erase commands.

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FIRMWARE MEMORY CYCLES

Firmware Memory Read Cycle

TABLE 4: FIRMWARE MEMORY READ CYCLE FIELD DEFINITIONS

Clock Cycle	Field Name	Field Contents LAD[3:0][1]	LAD[3:0] Direction	Comments
1	START	1101	IN	LFRAME# must be active (low) for the part to respond. Only the last start field (before LFRAME# transitions high) will be recognized. The START field contents (1101b) indicate a Firmware Memory Read cycle.
2	IDSEL	0000 to 1111	IN	Indicates which SST49LF00xC device should respond. If the IDSEL (ID select) field matches the value of ID[3:0], then that particular device will respond to the LPC bus cycle.
3-9	MADDR	YYYY	IN	These seven clock cycles make up the 28-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first.
10	MSIZE	KKKK	IN	The MSIZE field indicates how many bytes will be transferred during multi-byte operations. Device will execute multi-byte read of 2^{MSIZE} bytes. SST49LF00xC supports only MSIZE = 0, 1, 2, 4, 7 (1, 2, 4, 16, 128 Bytes), with KKKK=0000b, 0001b, 0010b, 0100b, or 0111b.
11	TAR0	1111	IN, then Float	In this clock cycle, the master (Intel ICH) has driven the bus to all '1's and then floats the bus, prior to the next clock cycle. This is the first part of the bus "turnaround cycle."
12	TAR1	1111 (float)	Float, then OUT	The SST49LF00xC takes control of the bus during this cycle.
13	RSYNC	0000 (READY)	OUT	During this clock cycle, the device generates a "ready sync" (RSYNC) indicating that the device has received the input data. The least-significant nibble of the least-significant byte will be available during the next clock cycle.
14-A	DATA	ZZZZ	OUT	A=(13+2^{n+1}); n = MSIZE Least significant nibbles outputs first.
(A+1)	TAR0	1111	OUT, then Float	In this clock cycle, the SST49LF00xC drives the bus to all ones and then floats the bus prior to the next clock cycle. This is the first part of the bus "turnaround cycle." A=(13+2^{n+1}); n = MSIZE
(A+2)	TAR1	1111 (float)	Float, then IN	The host resumes control of the bus during this cycle. A=(13+2^{n+1}); n = MSIZE

T4.0 1292

1. Field contents are valid on the rising edge of the present clock cycle.

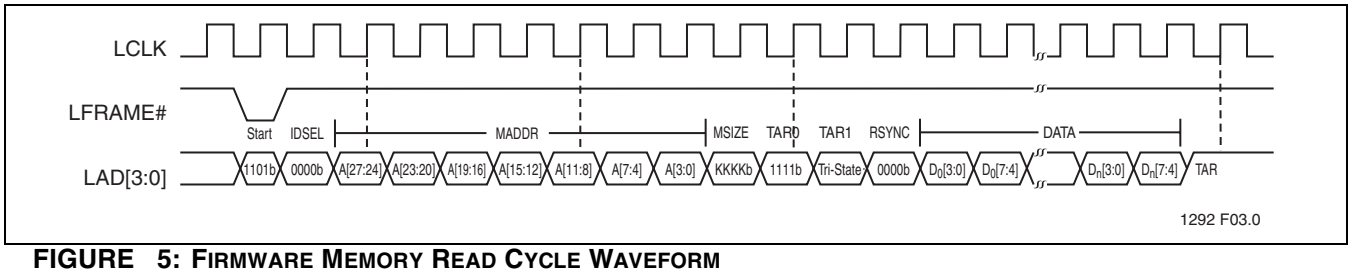


FIGURE 5: FIRMWARE MEMORY READ CYCLE WAVEFORM

Firmware Memory Write Cycle

TABLE 5: FIRMWARE MEMORY WRITE CYCLE

Clock Cycle	Field Name	Field Contents LAD[3:0][1]	LAD[3:0] Direction	Comments
1	START	1110	IN	LFRAME# must be active (low) for the part to respond. Only the last start field (before LFRAME# transitions high) will be recognized. The START field contents (1110b) indicate a Firmware Memory Write cycle.
2	IDSEL	0000 to 1111	IN	Indicates which SST49LF00xC device should respond. If the IDSEL (ID select) field matches the value of ID[3:0], then that particular device will respond to the whole bus cycle.
3-9	MADDR	YYYY	IN	These seven clock cycles make up the 28-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first.
10	MSIZE	KKKK	IN	The MSIZE field indicates how many bytes will be transferred during multi-byte operations. Device supports 1, 2, and 4 Bytes write with MSIZE = 0, 1, or 2, and KKKK=0000b, 0001b, or 0010b.
11-A	DATA	ZZZZ	IN	A=(10+2^{n+1}); n = MSIZE Least significant nibble entered first.
(A+1)	TAR0	1111	IN then Float	In this clock cycle, the master (Intel ICH) has driven the bus to all '1's and then floats the bus prior to the next clock cycle. This is the first part of the bus "turnaround cycle." A=(10+2^{n+1}); n = MSIZE
(A+2)	TAR1	1111 (float)	Float then OUT	The SST49LF00xC takes control of the bus during this cycle. A=(10+2^{n+1}); n = MSIZE
(A+3)	RSYNC	0000	OUT	During this clock cycle, the SST49LF00xC generates a "ready sync" (RSYNC) and outputs the values 0000, indicating that it has received data or a flash command. A=(10+2^{n+1}); n = MSIZE
(A+4)	TAR0	1111	OUT then Float	In this clock cycle, the SST49LF00xC drives the bus to all '1's and then floats the bus prior to the next clock cycle. This is the first part of the bus "turnaround cycle". A=(10+2^{n+1}); n = MSIZE
(A+5)	TAR1	1111 (float)	Float then IN	The host resumes control of the bus during this cycle. A=(10+2^{n+1}); n = MSIZE

T5.0 1292

1. Field contents are valid on the rising edge of the present clock cycle.

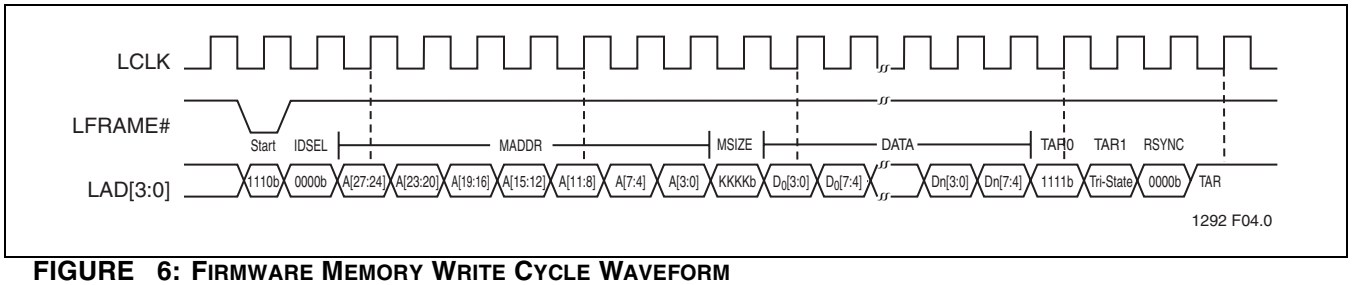


FIGURE 6: FIRMWARE MEMORY WRITE CYCLE WAVEFORM

Abort Mechanism

If LFRAME# is driven low for one or more clock cycles after the start of a bus cycle, the cycle will be terminated. The host may drive the LAD[3:0] with '1111b' (ABORT nibble) to return the interface to ready mode. The ABORT only affects the current bus cycle. For a multi-cycle command sequence, such as the Erase or Program commands, ABORT doesn't interrupt the entire command sequence, only the current bus cycle of the command sequence. The host can re-send the bus cycle for the aborted command and continue the command sequence after the device is ready again.

Response to Invalid Fields for Firmware Memory Cycle

During an on-going Firmware Memory bus cycle, the SST49LF00xC will not explicitly indicate that it has received invalid field sequences. The response to specific invalid fields or sequences is described as follows:

ID mismatch: If the IDSEL field does not match ID[3:0], the device will ignore the cycle. See "Multiple Device Selection for Firmware Memory Cycle" on page 16 for details.

Address out of range: The address sequence is 7 fields long (28 bits) with Firmware Memory bus cycles. Only some of the address fields bits are decoded by the SST49LF00xC devices. SST49LF004c decodes A_0 through A_{18} and $A_{22,}$ and SST49LF008C decodes A_0 through A_{19} and A_{22}. Address A_{22} has the special function of directing reads and writes to the flash core (A_{22}=1) or to the register space (A_{22}=0).

Invalid MSIZE field: If the SST49LF00xC receives an invalid size field during a Firmware Memory Read or Write operation, the device will reset and no operation will be attempted. The device will not generate any kind of response in this situation. The SST49LF00xC will only respond to values listed in Table 6.

TABLE 6: VALID MSIZE FIELD VALUES FOR FIRMWARE MEMORY CYCLES

MSIZE	Direction	Size of Transfer
0000	R/W	1 Byte
0001	R/W	2 Byte
0010	R/W	4 Byte
0100	R	16 Byte
0111	R	128 Byte

T6.0 1292

Once valid START, IDSEL, and MSIZE are received, the SST49LF00xC will always complete the bus cycle. However, if the device is busy performing a flash Erase or Program operation, no new internal memory Write will be executed. As long as the states of LAD[3:0] and LFRAME# are known, the response of the ST49LF00xC to signals received during the cycle is predictable.

Non-boundary-aligned address: The SST49LF00xC accepts multi-byte transfers for both Read and Write operations. The device address space is divided into uniform page sizes 2, 4, 16, or 128 bytes wide, according to the MSIZE value (see Table 6). The host issues only one address in the MADDR field of the Firmware Memory Cycle, but multiple bytes are read from or written to the device. For this reason the MADDR address should be page boundary-aligned. This means the address should be aligned to a Word boundary (A_0 = 0) for a 2-byte transfer, a double Word boundary (e.g. A_0 = 0, A_1 = 0) for a 4-byte transfer, and so on. If the address supplied by the host is not page boundary-aligned, the SST49LF00xC will force a boundary alignment, starting the multi-byte Read or Write operation from the lower byte of the addressed page.

Advance Information

Multiple Device Selection

Multiple LPC firmware flash devices may be strapped to increase memory densities in a system. The four ID pins, ID[3:0], allow up to 16 devices to be attached to the same bus by using different ID strapping in a system. BIOS support, bus loading, or the attaching bridge may limit this number. The boot device must have an ID of 0000b (determined by ID[3:0]); subsequent devices use incremental numbering. Equal density must be used with multiple devices.

Multiple Device Selection for Firmware Memory Cycle

For Firmware Memory Read/Write cycles, hardware strapping values on ID[3:0] must match the values in IDSEL field. The SST49LF00xC will compare these bits with ID[3:0]'s strapping values. If there is a mismatch, the device will ignore the remainder of the cycle. See Table 7 for Multiple Device Selection Configuration.

TABLE 7: FIRMWARE MEMORY MULTIPLE DEVICE SELECTION CONFIGURATION

Device #	ID[3:0]	IDSEL
0 (Boot device)	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
6	0110	0110
7	0111	0111
8	1000	1000
9	1001	1001
10	1010	1010
11	1011	1011
12	1100	1100
13	1101	1101
14	1110	1110
15	1111	1111

T7.0 1292

DEVICE COMMANDS

Device operation is controlled by commands written to the Command User Interface (CUI). Execution of a specific command is handled by internal functions after a CUI receives and processes the command. After power-up or a Reset operation the device enters Read mode. Commands consist of one or two sequential Bus-Write operations. The commands are summarized in Table 8, "Software Command Sequence".

TABLE 8: SOFTWARE COMMAND SEQUENCE

Command	Bus Cycles Required	First Bus Cycle			Second Bus Cycle		
		Oper	Addr[1]	Data	Oper	Addr[1]	Data
Read-Array/Reset	1	Write	X	FFH			
Read-Software-ID/ Read-Security-ID[2,3,4]	≥ 2	Write	X	90H	Read	IA[5]	ID[6]
Read-Status-Register[3,4]	2	Write	X	70H	Read	X	SRD[7]
Clear-Status-Register	1	Write	X	50H			
Sector-Erase[8]	2	Write	X	30H	Write	SAx[9]	D0H
Block-Erase[8]	2	Write	X	20H	Write	BAx	D0H
Program[8,10]	2	Write	X	40H or 10H	Write	WA[11]	WD[12]
Program-/Erase-Suspend	1	Write	X	B0H			
Program-/Erase-Resume	1	Write	X	D0H			
User-Security-ID-Program[13]	2	Write	X	A5H	Write	WA[11]	Data
User-Security-ID-Program-Lockout	2	Write	X	85H	Write	X	00H
Protected-Area-Sector-Erase[8,14]	2	Write	X	32H	Write	SA	D0H
Program-Protected-Area[8,14]	2	Write	X	42H	Write	WA	Data
Open-Protected-Area[15]	1	Write	X	62H			
Hide-Protected-Area[15]	1	Write	X	6DH			

T8.0 1292

1. This value must be a valid address within the device Memory Address Space. X can be V_{IH} or $V_{IL,}$ but no other value.
2. SST Manufacturer's ID = BFH, is read with A_{19}-A_0 = 0.
   SST49LF004C/008C Device ID = 54H/59H, is read with A_{19}-A_1 = 0, A_0 = 1.
   Following the Read-Software-ID/Read-Security-ID command,
   Read operations access Manufacturer's ID and Device ID or Security ID.
3. Read-Software-ID/Read Security ID and Read Status Register will return ID/Register data until another valid command is written.
4. Following the Read-Software-ID/Read-Security-ID command, Read operations access manufacturer's ID and Device ID or Security ID. Read-Software-ID/Read-Security-ID and Read-Status-Register will return register data until another valid command is written.
5. IA = Device Identification Address/Security ID Address.
6. ID = Data read from identifier codes/Data read from Security ID
7. SRD = Data read from Status register
8. The sector or block must not be write-locked when attempting Erase or Program operations.
   Attempts to issue an Erase or Program command to a write-locked sector/block will fail.
9. SA_X for Sector-Erase Address
   BA_X for Block-Erase Address
10. The Program Command can operate on multiple bytes.
11. WA = Address of memory location to be written
12. WD = Data to be written at location WA
13. Valid addresses for the User Security ID space are from FFFC 0188H to FFFC 019FH.
14. Valid address WA of Protected Data Area location is from FFFC 8000H to FFFC AFFFH. For Sector Erase Command any address within the sector in the Protected Data Area being erased can be used: PDA Sector 0 - SA+ FFC 8000H to FFFC 8FFFH. PDA Sector 1 - SA = FFFC 9000H to FFFC 9FFFH. PDA Sector 2 - SA = FFFC A000H to FFFC AFFFH.
15. After Open Protected Area command is executed the contents of the area can be read at addresses FFBC 8000H to FFBC AFFFH if it is not read-locked. After Hide Protected Area command is executed the contents of the area is not accessible regardless of read-lock status. By default (after Power On or reset) Protected Data Area is hidden.

Advance Information

Read-Array Command

Upon initial device power-up and after exit from reset, the device defaults to the Read Array mode. This operation can also be initiated by writing the Read-Array command. (See Table 8.) The device remains available for array reads until another command is written. Once an internal Program/Erase operation starts, the device will not recognize the Read-Array command until the operation is completed, unless the operation is suspended via a Program-/Erase-Suspend command.

Read-Software-ID Command

The Read-Software-ID operation is initiated by writing the Read-Software-ID command. Following the command, the device will output the manufacturer's ID and device ID from the addresses shown in Table 9. Any other valid command will terminate the Read-Software-ID operation.

The Read-Software-ID command is the same as the Read-Security-ID command. See "Security ID Commands" on page 20.

TABLE 9: PRODUCT IDENTIFICATION

	Address[1]	Data
Manufacturer's ID	FFFC 0000H	BFH
Device ID		
SST49LF004C	FFFC 0001H	54H
SST49LF008C	FFFC 0001H	59H

T9.0 1292

1. Address shown in this column is for boot device only. Address locations should appear elsewhere in the 4 GByte system memory map depending on ID strapping values on ID[3:0] pins when multiple LPC memory devices are used in a system.

Read-Status-Register Command

The Status register may be read to determine when a Sector-/Block-Erase or Program completes, and whether the operation completed successfully. The Status register may be read at any time by writing the Read-Status-Register command. After writing this command, all subsequent Read operations will return data from the Status register until another valid command is written.

The default value of the Status register after device power-up or reset is 80H.

Clear-Status-Register Command

The user can reset the Status register's Block Protect Status (BPS) bit to 0 by issuing a Clear-Status-Register command. Device power-up and hardware reset will also reset BPS to 0.

TABLE 10: SOFTWARE STATUS REGISTER

Bit	Name	Function
0	RES	Reserved for future use
1	BPS	Block Protect Status The Block Write-Lock bit should be interrogated only after Erase or Program command is issued. It informs the system whether or not the selected block is locked. BPS does not provide a continuous indication of Write-Lock bit value. 0: Block Unlocked 1: Operation Aborted, Block Write-Lock bit set.
2:5	RES	Reserved for future use
6	ESS	Erase Suspend Status 0: Erase in progress/completed 1: Erase suspended
7	WSMS	Write State Machine Status Check WSMS to determine erase or program completion. 0: Busy 1: Ready

T10.0 1292

Sector-/Block-Erase Command

The Erase Command operates on one sector or block at a time. This command requires an (arbitrary) address within the sector or block to be erased. Note that a Sector/Block Erase operation changes all Sector/Block byte data to FFh. If a Read operation is performed after issuing the erase command, the device will automatically output Status Register data. The system can poll the Status Register in order to verify the completion of the Sector/Block Erase operation (please refer to Table 10, Status Register Definition). If a Sector/Block Erase is attempted on a locked block, the operation will fail and the data in the Sector/Block will not be changed. In this case, the Status Register will report the error (BPS=1).

Program Command

The Program command operates on multiple bytes as shown in Table 5. This command specifies the address and data to be programmed. During the Program operation the device automatically outputs the Status Register data when read. The system can poll the Status Register in order to verify the completion of the Program operation (refer to Table 10, “Software Status Register”). If a Program operation is attempted on a locked block, the operation will fail and the data in the addressed byte will not be changed. In this case, the Status Register will report the error (BPS=1).

Program-/Erase-Suspend or Program-/Erase-Resume Operations

The Program-Suspend and Erase-Suspend operations share the same software command sequence (B0H). The Program-Resume and Erase-Resume operations share the same software command sequence (D0H). See Table 8, “Software Command Sequence” on page 17.

Erase-Suspend/ Erase-Resume Commands

The Erase Suspend command allows Sector-Erase or Block-Erase interruption in order to read or program data in another block of memory. Once the Erase-Suspend command is executed, the device will suspend any ongoing Erase operation within time T_{ES} (10 µs). The device outputs status register data when read after the Erase-Suspend command is written. The system is able to determine when the Erase operation has been completed (WSMS=1) by polling the status register. After an Erase-Suspend, the device will set the status register ESS bit (ESS=1) if the Erase has been successfully suspended (refer to Table 10, “Software Status Register”). The Erase-Resume command resumes the Erase operation that had been previously suspended.

After a successful Erase-Suspend, a Read-Array command may be written to read data from a Sector/Block other than the suspended Sector/Block. A Program command sequence may also be issued during Erase Suspend to program data in memory locations other than the Sector/Block currently in the Erase-Suspend mode. If a Read-Array command is written to an address within the suspended Sector/Block this may result in reading invalid data. If a Program command is written to an address within the suspended Sector/Block the command is acknowledged but rejected. Other valid commands while erase is suspended include Read-Status-Register, Read-Device-ID, and Erase-Resume.

The Erase-Resume command resumes the Erase process in the suspended sector or block. After the Erase-Resume command is written, the device will continue the Erase process. Erase cannot resume until any Program operation initiated during Erase-Suspend has completed. Suspended operations cannot be nested: the system needs to complete or resume any previously suspended operation before a new operation can be suspended. See Figure 7 for flowchart.

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Program-Suspend/ Program-Resume Command

The Program-Suspend and Program-Resume commands have no influence on the device. Since the device requires a maximum of T_{BP} (10 µs) in order to program a byte (see Table 27), when a Program-Suspend command is written, the suspended Byte Program operation will always be successfully completed within the suspend latency time (T_{ES} = T_{BP} = 10 µs).

Security ID Commands

The SST49LF00xC device offers a 256-bit Security ID space. The Security ID space is divided into two parts. One 64-bit segment is programmed at SST with a unique 64-bit number: this number cannot be changed by the user. The other segment is 192-bit wide and is left blank: this space is available for customers and can be programmed as desired.

The User-Security-ID-Program command is shown in Table 8, "Software Command Sequence". Use the memory addresses specified in Table 11 for Security ID programming. Once the customer segment is programmed, it can be locked to prevent any alteration. The User-Security-ID-Program-Lockout command is shown in Table 8, "Software Command Sequence".

In order to read the Security ID information, the user can issue a Read Security ID Command (90H) to the device. At this point the device enters the Read-Software-ID/Read-Security-ID mode. The Security ID information can be read at the memory addresses in Table 11.

A Read-Array/Reset command (FFH) must then be issued to the device in order to exit the Read-Software-ID/Read-Security-ID mode and return to Read-Array mode.

An alternate method to read the Security ID information is to read the Security ID registers located into the register space as described in the "Security ID Registers" section.

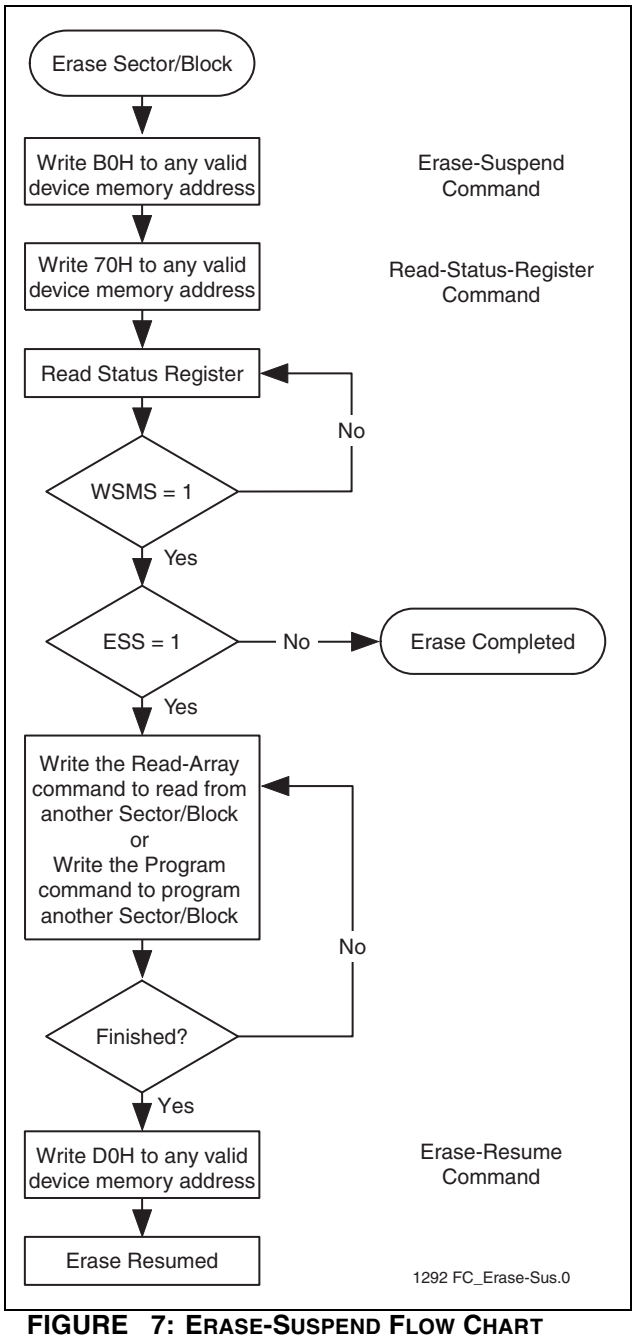


FIGURE 7: ERASE-SUSPEND FLOW CHART

TABLE 11: SECURITY ID ADDRESSES

Address Range[1]	Security ID Segment	Size
FFFC 0180 to FFFC 0187	Factory-Programmed	8 bytes – 64 bit
FFFC 0188 to FFFC 019F	User-Programmed	24 bytes – 192 bit

T11.0 1292

1. Address shown is for boot device only. Address locations should appear elsewhere in the 4 GByte system memory map depending on ID strapping values on ID[3:0} pins according with multiple device selection mechanism.

REGISTERS

There are five types of registers available on the SST49LF00xC, the multi-byte Read/Write configuration registers, General Purpose Inputs registers, Block Locking registers, Security ID register, and the JEDEC ID registers. These registers appear at their respective address location in the 4 GByte system memory map. Unused register locations will read as 00H. Any attempt to read or write any register during an internal Write operation will be ignored.

Read or write access to the register during an internal Program/Erase operation will be completed as follows:

- Multi-byte Read/Write Configuration registers, General Purpose Inputs register, and Block Locking registers can be accessed normally
- Security ID register and the JEDEC ID registers can not be accessed (reading these registers will return unused register data 00H).

Multi-Byte Read/Write Configuration Registers (Firmware Memory Cycle)

The multi-byte read/write configuration (MBR) registers are four 8-bit read-only registers located at addresses FFBC0005-FFBC0008 for boot configured device (see Table 13). These registers are accessible using Firmware Memory Read cycle only. These registers contain information about multi-byte read and write access sizes that will be accepted for Firmware Memory multi-byte Read commands. The registers are not available in AAI mode.

In case of multi-byte Firmware Memory register reads, the device will return register data for the addressed register until the command finishes, or is aborted.

General Purpose Inputs Register

The General Purpose Inputs register (GPI_REG) passes the state of GPI[4:0] pins on the SST49LF00xC. It is recommended that the GPI[4:0] pins be in the desired state before LFRAME# is brought low for the beginning of the bus cycle, and remain in that state until the end of the cycle. There is no default value since this is a pass-through register. The GPI_REG register for the boot device appears at FFBC0100H in the 4 GByte system memory map, and will appear elsewhere if the device is not the boot device (see Table 12). This register is not available to be read when the device is in an Erase/Program operation. In case of multi-byte Firmware Memory cycle register reads, the device will return register data for the addressed register until the command finishes, or is aborted.

TABLE 12: GENERAL PURPOSE REGISTER

Register	Register Address[1]	Default Value	Access
GPI_REG	FFBC 0100H	N/A	R

T12.0 1292

1. Address shown in this column is for boot device only. Address locations should appear elsewhere in the 4 GByte system memory map depending on ID strapping values on ID[3:0] pins according with multiple device selection mechanism.

TABLE 13: MULTI-BYTE READ/WRITE CONFIGURATION REGISTERS

Register	Register Address[1]	Data	Access	Description
MULTI_BYTE_READ_L	FFBC 0005H	0100 1011b	R	Device supports 1,2,4, 16, 128 Byte reads
MULTI_BYTE_READ_H	FFBC 0006H	0000 0000b	R	Future Expansion for Read
MULTI_BYTE_WRITE_L	FFBC 0007H	0000 0011b	R	Device supports 1, 2, 4 Byte Write
MULTI_BYTE_WRITE_H	FFBC 0008H	0000 0000b	R	Future Expansion for Write

T13.0 1292

1. Address shown in this column is for boot device only. Address locations should appear elsewhere in the 4 GByte system memory map depending on ID strapping values on ID[3:0] pins when multiple LPC memory devices are used in a system.

Block and PDA Sector Locking Registers

SST49LF00xC provides software controlled lock protection through a set of Block Locking registers. The Block Locking registers are read/write registers and they are accessible through standard addressable memory locations specified in Table 14. Unused register locations will return 00H if read.

In case of multi-byte register reads with Firmware Memory cycle, the device will return register data for the addressed register until the command finishes, or is aborted.

SST49LF00xC also provides PDA Sector Locking Registers at addresses shown in Table 15. These locking registers can be accessed only after Open Protected Area command is executed. After Hide Protected Area command, as well as after Power On and Reset, read from addresses specified in Table 15 returns unused register space data 00H, and write to these addresses is ignored.

In case of multi-byte read of any locking register, the device will return register data for the addressed register until the command finishes, or is aborted.

TABLE 14: BLOCK LOCKING REGISTERS

Register	Block Size	Protected Memory Address[1] Range		Memory Map Register Address[1]
		SST49LF004C	SST49LF008C	
T_BLOCK_LK	16K	07FFFFH-07C000H	0FFFFFH-0FC000H	FFBFC002H
T_MINUS01_LK	8K	07BFFFH-07A000H	0FBFFFH-0FA000H	FFBFA002H
T_MINUS02_LK	8K	079FFFH-078000H	0F9FFFH-0F8000H	FFBF8002H
T_MINUS03_LK	32K	077FFFH-070000H	0F7FFFH-0F0000H	FFBF0002H
T_MINUS04_LK	64K	06FFFFH-060000H	0EFFFFH-0E0000H	FFBE0002H
T_MINUS05_LK	64K	05FFFFH-050000H	0DFFFFH-0D0000H	FFBD0002H
T_MINUS06_LK	64K	04FFFFH-040000H	0CFFFFH-0C0000H	FFBC0002H
T_MINUS07_LK	64K	03FFFFH-030000H	0BFFFFH-0B0000H	FFBB0002H
T_MINUS08_LK	64K	02FFFFH-020000H	0AFFFFH-0A0000H	FFBA0002H
T_MINUS09_LK	64K	01FFFFH-010000H	09FFFFH-090000H	FFB90002H
T_MINUS10_LK	64K	00FFFFH-000000H	08FFFFH-080000H	FFB80002H
T_MINUS11_LK	64K		07FFFFH-070000H	FFB70002H
T_MINUS12_LK	64K		06FFFFH-060000H	FFB60002H
T_MINUS13_LK	64K		05FFFFH-050000H	FFB50002H
T_MINUS14_LK	64K		04FFFFH-040000H	FFB40002H
T_MINUS15_LK	64K		03FFFFH-030000H	FFB30002H
T_MINUS16_LK	64K		02FFFFH-020000H	FFB20002H
T_MINUS17_LK	64K		01FFFFH-010000H	FFB10002H
T_MINUS18_LK	64K		00FFFFH-000000H	FFB00002H

T14.0 1292

1. Address shown in this column is for boot device only. Address locations should appear elsewhere in the 4 GByte system memory map depending on ID strapping values on ID[3:0] pins when multiple LPC memory devices are used in a system.

TABLE 15: PROTECTED DATA AREA SECTOR LOCKING REGISTERS

Register	Sector Size	SST49LF00xC PDA Protected Addresses[1]		Memory Map Register Address[1]
		For Write Access	For Read Access	
T_PDA2_LK	4K	FFFC A000H–FFFC AFFFH	FFBC A000H–FFBC AFFFH	FFBC 2202H
T_PDA1_LK	4K	FFFC 9000H–FFFC 9FFFH	FFBC 9000H–FFBC 9FFFH	FFBC 1202H
T_PDA0_LK	4K	FFFC 8000H–FFFC 8FFFH	FFBC 8000H–FFBC 8FFFH	FFBC 0202H

T15.0 1292

1. Address shown in this column is for boot device only. Address locations should appear elsewhere in the 4 GByte system memory map depending on ID strapping values on ID[3:0] pins when multiple LPC memory devices are used in a system.

TABLE 16: BLOCK/PDA SECTOR LOCKING REGISTER BITS

Reserved Bit [7:3]	Read-Lock Bit [2]	Lock-Down Bit [1]	Write-Lock Bit [0]	Lock Status
00000	0	0	0	Full Access
00000	0	0	1	Write Locked (Default State at Power-Up)
00000	0	1	0	Locked Open (Full Access Locked Down)
00000	0	1	1	Write Locked Down
00000	1	0	0	Block Read Locked (Registers alterable)
00000	1	0	1	Block Read & Write Lock (Registers alterable)
00000	1	1	0	Block Read Locked Down (Registers not alterable)
00000	1	1	1	Block Read & Write lock Down (Registers not alterable)

T16.0 1292

Write-Lock Bit

The Write-Lock bit, bit 0, controls the lock state described in Table 16. The default Write status of all blocks after power up is write locked. When bit 0 of the Block Locking register is set, Program and Erase operations for the corresponding block are prevented. Clearing the Write-Lock bit will unprotect the block. The Write-Lock bit must be cleared prior to starting a Program or Erase operation since it is sampled at the beginning of the operation. The Write-Lock bit functions in conjunction with the hardware Write Lock pin TBL# for the top Boot Block. When TBL# is low, it overrides the software locking scheme. The top Boot Block Locking register does not indicate the state of the TBL# pin. The Write-Lock bit functions in conjunction with the hardware WP#/AAI pin for the remaining blocks (Blocks 0 to 17 for 49LF008C and Blocks 0 to 9 for 49LF004C). When WP#/AAI is low, it overrides the software locking scheme. The Block Locking register does not indicate the state of the WP#/AAI pin.

Lock-Down Bit

The Lock-Down bit, bit 1, controls the Block Locking register as described in Table 16. When in LPC interface mode, the default Lock Down status of all blocks upon power-up is not locked down. Once the Lock-Down bit is set, any future attempted changes to that Block Locking register will be ignored. The Lock-Down bit is only cleared upon a device reset with RST# or INIT# or power down. Current Lock Down status of a particular block can be determined by reading the corresponding Lock-Down bit. Once a block's Lock-Down bit is set, the Read-Lock and Write-Lock bits for that block can no longer be modified: the block is locked down in its current state of read/write accessibility.

Read-Lock Bit

The default read status of all blocks upon power-up is read-unlocked. When a block's read lock bit is set, data cannot be read from that block. An attempted read from a read-locked block will result in the data 00h. The read lock status can be unlocked by clearing the read lock bit: this can only be done provided that the block is not locked down. The current read lock status of a particular block can be determined by reading the corresponding read-lock bit.

Security ID Registers

The SST49LF0xxC devices offer a 256-bit Security ID register space. The Security ID space is divided into two segments - one (64 bits) factory programmed segment and one (192 bits) user programmed segment. The first segment is programmed and locked at SST with a unique 64-bit number. The user segment (192-bits) is left blank (FFH) for the customer to be programmed as desired. The user can use standard Register read cycles to read the Security ID space, or use the Security ID Program command to program the space. Refer to Table 8, "Software Command Sequence" for more details.

The Security ID Information and its Write Lock/Unlock status can be Read in the Register Access Space for Execute-In-Place (XIP) type of applications. (See Table 17.)

The Write Lock-out status of the Security ID space can be read from the SEC_ID_WRITE_LOCK register (see Table 17). The SEC_ID_WRITE_LOCK register is a "read only" register that is accessible at the address location specified in Table 14. In the case of multi-byte register reads with Firmware Memory cycle, for SEC_ID_WRITE_LOCK register, the device will return register data for the addressed register until the command finishes, or is aborted.

In the case of multi-byte register reads with Firmware Memory cycle, for the all the SEC_ID_BYTE registers, the device will return page-aligned sequential register data with wrap-around until the command finishes, or is aborted.

TABLE 17: SECURITY ID REGISTERS

Register	Register Address[1]	Value	Access	Description
SEC_ID__WRITE_LOCK	FFBC0102H	0000 0000b 0000 0001b	R	Write Unlocked Write Locked
SEC_ID_BYTE_0	FFBC0180H		R	Factory Programmed
SEC_ID_BYTE_1	FFBC0181H		R	Factory Programmed
SEC_ID_BYTE_2	FFBC0182H		R	Factory Programmed
SEC_ID_BYTE_3	FFBC0183H		R	Factory Programmed
…	…		…	…
SEC_ID_BYTE_7	FFBC0187H		R	Factory Programmed
SEC_ID_BYTE_8	FFBC0188H		R	User Programmed
SEC_ID_BYTE_9	FFBC0189H		R	User Programmed
…	…		…	…
SEC_ID_BYTE_30	FFBC019EH		R	User Programmed
SEC_ID_BYTE_31	FFBC019FH		R	User Programmed

T17.0 1292

1. Address shown in this column is for boot device only. Address locations should appear elsewhere in the 4GByte system memory map depending on ID strapping values on ID[3:0] pins according with multiple device selection mechanism.

JEDEC ID Registers

The JEDEC ID registers for the boot device appear at FFBC0000H and FFBC0001H in the 4 GByte system memory map, and will appear elsewhere if the device is not the boot device. This register is not available to be read when the device is in Erase/Program operation. Unused register location will read as 00H. See Table 18 for the JEDEC device ID code. In case of multi-byte register reads with Firmware Memory cycle, the device will return register data for the addressed register until the command finishes, or is aborted.

TABLE 18: JEDEC ID REGISTERS

Register	Register Address[1]	Default Value	Access
MANUF_REG	FFBC 0000H	BFH	R
DEV_REG			
SST49LF004C	FFBC 0001H	54H	R
SST49LF008C	FFBC 0001H	59H	

T18.0 1292

1. Address shown in this column is for boot device only. Address locations should appear elsewhere in the 4 GByte system memory map depending on ID strapping values on ID[3:0] pins when multiple LPC memory devices are used in a system.

AUTO-ADDRESS INCREMENT (AAI) MODE

AAI Mode with Multi-byte Programming

AAI mode with multi-byte programming is provided for high-speed production programming. Auto-Address Increment mode requires only one address load for each 128-byte page of data. The Multi-Byte Programming feature allows simultaneous multi-byte programming. Note: The Security ID area and the Protected Data Area cannot be programmed using AAI mode.

Taking the WP#/AAI pin to the Supervoltage V_H enables the AAI mode. The AAI command is started as a normal Firmware Memory cycle. LD# should be low (V_{IL}) as long as data is being loaded into the device. In the MADDR field, the host may input any address within the 128-byte page to be programmed. The least significant seven bits of the address field will be ignored and the device will begin programming at the beginning of the 128-byte page (i.e., the address will be page-aligned). The device Ready/Busy status is output on the RY/BY# pin.

Data is accepted until the internal buffer is full. At that point RY/BY# goes low (busy) to indicate that the internal buffer is full and cannot accept any more data. When the device is ready, RY/BY# pin goes high and indicates to the host that more data (the next group of bytes) can be accepted by the internal data buffer (see Table 19 and Figure 8).

LD# is taken high by the host after loading the final byte(s) of the 128-byte page. the RY/BY# signal remains low until the completion of internal programming. After the completion of programming, the part will go into idle mode and the RY/BY# will go high indicating that the AAI command has been completed (see Table 19). A subsequent AAI command may be initiated to begin programming the next 128-byte page.

Data will be accepted by the device as long as LD# is low and RY/BY# is high (until the last byte of the 128-byte page has been entered). For partial data-loads (i.e., less than 128 Bytes), LD# may be taken high (V_{IH}) to end the data loading. If LD# goes high before the full 128-byte page has been entered, the device will program the data which has been entered to that point, and then terminate the AAI page programming command. Any incompletely loaded data byte (nibble) will not be programmed. The device will signify completion of the command by driving RY/BY# high. Once RY/BY# goes high, LD# can be taken low to begin a new AAI programming operation at a different address location.

The RY/BY# pin will stay low while internal programming completes. When the entire 128-byte page has been programmed, the device will return to the idle mode and the RY/BY# pin will go high (V_{IH}) to indicate the AAI command has been completed.

TABLE 19: LD# INPUT AND RY/BY# STATUS IN AAI MODE

LD# state	RY/BY# status	RY/BY# Flag indication
L	H	Device is Ready, can accept more data until the last (128^{th}) byte.
L	L	Device is Busy, cannot accept more data
L	H	Device is Ready for next operation if previous data is the last (128^{th}) byte.
H	H	Device is Ready for next operation
H	L	Device is Busy programming

T19.0 1292

The user may terminate AAI programming by dropping the WP#/AAI pin to TTL levels (V_{IH}/V_{IL}) as long as LD# is high and RY/BY# returns to high indicating the completion of the AAI cycle. Software block-locking will be disabled in AAI mode (all blocks will be write-unlocked). If AAI drops below the Supervoltage V_H before RY/BY# returns to high (and LD# high), the contents of the page may be indeterminate.

AAI Data Load Protocol

TABLE 20: AAI PROGRAMMING CYCLE (INITIATED WITH WP#/AAI AT V_H ONLY)

Clock Cycle	Field Name	Field Contents	LAD[3:0]	Comments
1	START	1110	IN	LFRAME# must be active (low) for the part to respond. Only the last start field (before LFRAME# transitions high) should be recognized. The START field contents indicate a Firmware Memory Write cycle. (1110b)
2	IDSEL	0000b to 1111b	IN	ID works identically to Firmware Memory cycle. This field indicates which SST49LF00xC device should respond. If the IDSEL (ID select) field matches the value of ID[3:0], then that particular device will respond to the whole bus cycle.
3-9	MADDR	YYYY	IN	These seven clock cycles make up the 28-bit memory address. YYYY is one nibble of the entire address. Addresses are transferred most-significant nibble first. Only bits [19:7] for 8M, [18.7] for 4M of the total address [27:0] are used for AAI mode. The rest are “don’t care”.
10	MSIZE	KKKK	IN	MSIZE field is don’t care when in AAI mode
11-266	DATA	ZZZZ	IN	Data is transmitted to the device least significant nibble first, from byte 0 to byte 127 as long as the RY/BY# is high and LD# low. The host will pause the clock and data stream when RY/BY# goes low until it returns high, signifying that the chip is ready for more data

T20.0 1292

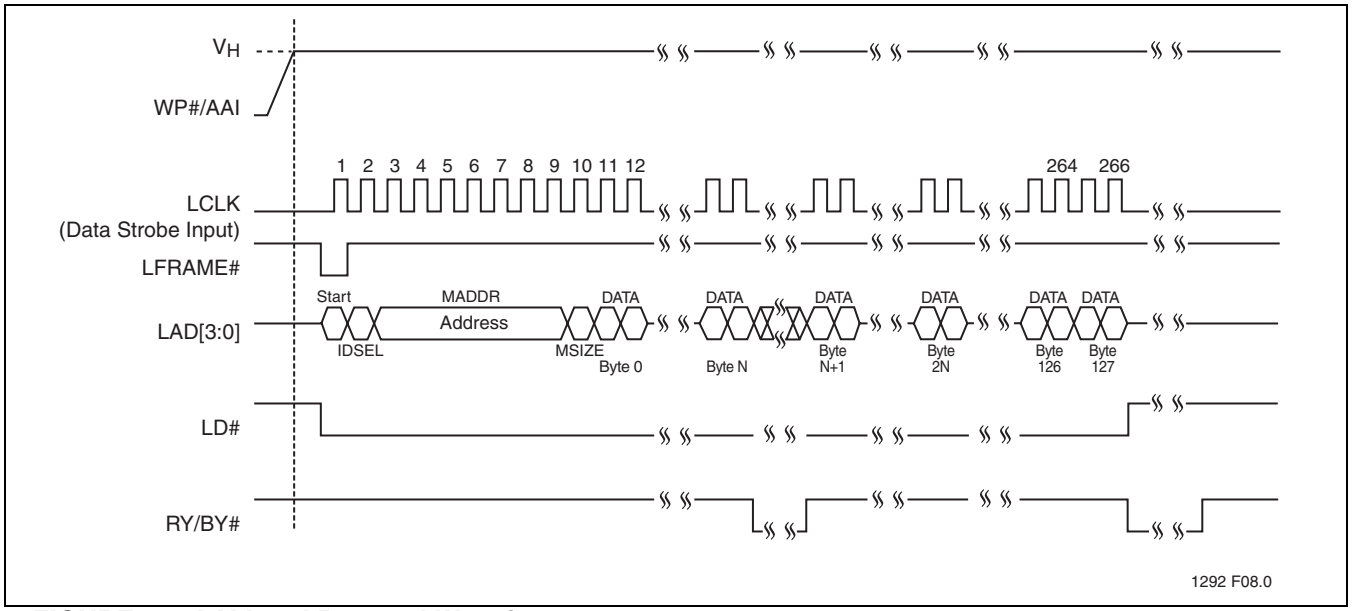


FIGURE 8: AAI Load Protocol Waveform

ELECTRICAL SPECIFICATIONS

The AC and DC specifications for the LPC interface signals (LAD[3:0], LFRAME#, LCLCK and RST#) as defined in Section 4.2.2.4 of the PCI local Bus specification, Rev. 2.1. Refer to Table 21 for the DC voltage and current specifications. Refer to Table 25 through Table 27 for the AC timing specifications for Clock, Read, Write, and Reset operations.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Temperature Under Bias . . . . . -55°C to +125°C
Storage Temperature . . . . . -65°C to +150°C
D.C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}+0.5V
Transient Voltage (<20 ns) on Any Pin (except WP#/AAI) to Ground Potential[1] . . . . . -2.0V to V_{DD}+2.0V
Voltage on WP#/AAI Pin to Ground Potential[2] . . . . . -0.5V to 11.0V
Package Power Dissipation Capability (T_A=25°C) 1.0W
Surface Mount Solder Reflow Temperature[3] . . . . . 260°C for 10 seconds
Output Short Circuit Current[4] . . . . . 50 mA

1. Do not violate processor or chipset specification regarding INIT# voltage.
2. The maximum DC voltage on WP#/AAI pin may reach 11V for periods <20ns.
3. Excluding certain with-Pb 32-PLCC units, all packages are 260°C capable in both non-Pb and with-Pb solder versions. Certain with-Pb 32-PLCC package types are capable of 240°C for 10 seconds; please consult the factory for the latest information.
4. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +85°C	3.0-3.6V

AC CONDITIONS OF TEST

Input Rise/Fall Time . . . . . 3 ns
Output Load . . . . . C_L = 30 pF
See Figure 14

Advance Information

DC Characteristics

TABLE 21: DC OPERATING CHARACTERISTICS (ALL INTERFACES)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}[1]	Active V_{DD} Current				LCLK (LPC mode)=V_{ILT}/V_{IHT} at f=33 MHz All other inputs=V_{IL} or V_{IH}
	Read		18	mA	All outputs = open, V_{DD}=V_{DD} Max
	Single-/Dual-Byte Program, Erase		40	mA	f=33 MHz
	Quad-Byte Program		60	mA	f=33 MHz
I_{SB}	Standby V_{DD} Current (LPC Interface)		100	µA	LCLK (LPC mode)=V_{ILT}/V_{IHT} at f=33 MHz LFRAME#=.9V_{DD}, f=33 MHz, V_{DD}=V_{DD} Max All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_{RY}[2]	Ready Mode V_{DD} Current		10	mA	LCLK (LPC mode)=V_{ILT}/V_{IHT} at f=33 MHz LFRAME#=V_{IL}, f=33 MHz, V_{DD}=V_{DD} Max All other inputs ≥ 0.9 V_{DD} or ≤ 0.1 V_{DD}
I_I	Input Leakage Current for ID[3:0] pins		200	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_{LO}	Output Leakage Current		1	µA	V_{OUT}=GND to V_{DD}, V_{DD}=V_{DD} Max
I_H	Supervoltage Current for WP#/AAI		200	µA	
V_H	Supervoltage for WP#/AAI	8.5	9.5	V	
V_{IHI}[3]	INIT# Input High Voltage	1.1	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{ILI}[3]	INIT# Input Low Voltage	-0.5	0.4	V	V_{DD}=V_{DD} Min
V_{IL}	Input Low Voltage	-0.5	0.3 V_{DD}	V	V_{DD}=V_{DD} Min
V_{IH}	Input High Voltage	0.5 V_{DD}	V_{DD}+0.5	V	V_{DD}=V_{DD} Max
V_{OL}	Output Low Voltage		0.1 V_{DD}	V	I_{OL}=1500 µA, V_{DD}=V_{DD} Min
V_{OH}	Output High Voltage	0.9 V_{DD}		V	I_{OH}=-500 µA, V_{DD}=V_{DD} Min

T21.0 1292

1. I_{DD} active while a Read or Write (Program or Erase) operation is in progress.
2. The device is in Ready mode when no activity is on the LPC bus.
3. Do not violate processor or chipset specification regarding INIT# voltage.

TABLE 22: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T22.0 1292

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter

TABLE 23: PIN CAPACITANCE (V_{DD}=3.3V, T_A=25 °C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$=0V	12 pF
C_{IN}[1]	Input Capacitance	V_{IN}=0V	12 pF
L_{PIN}[2]	Pin Inductance		20 nH

T23.0 1292

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.
2. Refer to PCI spec.

TABLE 24: RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T24.0 1292

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 25: CLOCK TIMING PARAMETERS (LPC MODE)

Symbol	Parameter	Min	Max	Units
T_{CYC}	Cycle Time	30		ns
T_{HIGH}	LCLK High Time	11		ns
T_{LOW}	LCLK Low Time	11		ns
-	LCLK Slew Rate (peak-to-peak)	1	4	V/ns
-	RST# or INIT# Slew Rate	50		mV/ns

T25.0 1292

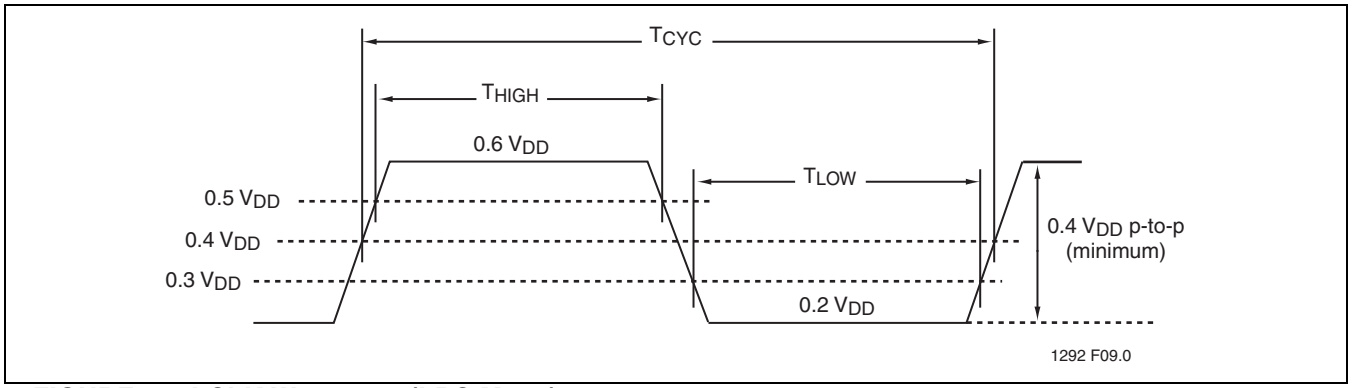


FIGURE 9: LCLK WAVEFORM (LPC MODE)

Advance Information

TABLE 26: RESET TIMING PARAMETERS, V_{DD}=3.0-3.6V (LPC MODE)

Symbol	Parameter	Min	Max	Units
T_{PRST}	V_{DD} stable to Reset High	100		µs
T_{RSTP}	RST# Pulse Width	100		ns
T_{RSTF}	RST# Low to Output Float		48	ns
T_{RST}[1]	RST# High to LFRAME# Low	5		LCLK cycles
T_{RSTE}	RST# Low to reset during Sector-/Block-Erase or Program		10	µs

T26.0 1292

1. There will be a latency due to T_{RSTE} if a reset procedure is performed during a Program or Erase operation,

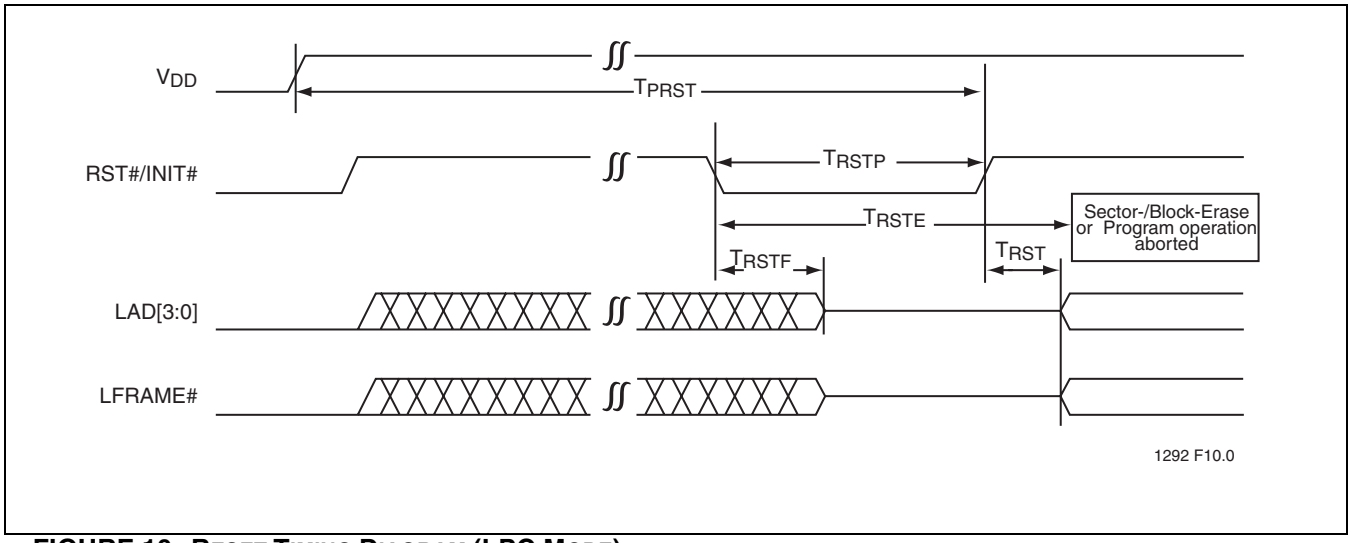


FIGURE 10: RESET TIMING DIAGRAM (LPC MODE)

AC Characteristics

TABLE 27: READ/WRITE CYCLE TIMING PARAMETERS, V_{DD}=3.0-3.6V (LPC MODE)

Symbol	Parameter	Min	Max	Units
T_{CYC}	Clock Cycle Time	30		ns
T_{SU}	Data Set Up Time to Clock Rising	7		ns
T_{DH}	Clock Rising to Data Hold Time	0		ns
T_{VAL}[1]	Clock Rising to Data Valid	2	11	ns
T_{BP}	Byte Programming Time		10	µs
T_{SE}	Sector-Erase Time		25	ms
T_{BE}	Block-Erase Time		25	ms
T_{ES}	Program/Erase-Suspend Latency		10	µs
T_{ON}	Clock Rising to Active (Float to Active Delay)	2		ns
T_{OFF}	Clock Rising to Inactive (Active to Float Delay)		28	ns

T27.0 1292

1. Minimum and maximum times have different loads. See PCI spec

TABLE 28: AC INPUT/OUTPUT SPECIFICATIONS (LPC MODE)

Symbol	Parameter	Min	Max	Units	Conditions
I_{OH}(AC)	Switching Current High	-12 V_{DD}		mA	$0 < V_{OUT} \leq 0.3V_{DD}$
		-17.1(V_{DD}-V_{OUT})		mA	$0.3V_{DD} < V_{OUT} < 0.9V_{DD}$
			Equation C[1]		$0.7V_{DD} < V_{OUT} < V_{DD}$
	(Test Point)		-32 V_{DD}	mA	$V_{OUT} = 0.7V_{DD}$
I_{OL}(AC)	Switching Current Low	16 V_{DD}	Equation D[1]	mA	$V_{DD} > V_{OUT} \geq 0.6V_{DD}$
		26.7 V_{OUT}		mA	$0.6V_{DD} > V_{OUT} > 0.1V_{DD}$
					$0.18V_{DD} > V_{OUT} > 0$
	(Test Point)		38 V_{DD}	mA	$V_{OUT} = 0.18V_{DD}$
I_{CL}	Low Clamp Current	-25+(V_{IN}+1)/0.015		mA	$-3 < V_{IN} \leq -1$
I_{CH}	High Clamp Current	25+(V_{IN}-V_{DD}-1)/0.015		mA	$V_{DD}+4 > V_{IN} \geq V_{DD}+1$
slewr[2]	Output Rise Slew Rate	1	4	V/ns	$0.2V_{DD}$-$0.6V_{DD}$ load
slewf[2]	Output Fall Slew Rate	1	4	V/ns	$0.6V_{DD}$-$0.2V_{DD}$ load

T28.0 1292

1. See PCI spec.
2. PCI specification output load is used.

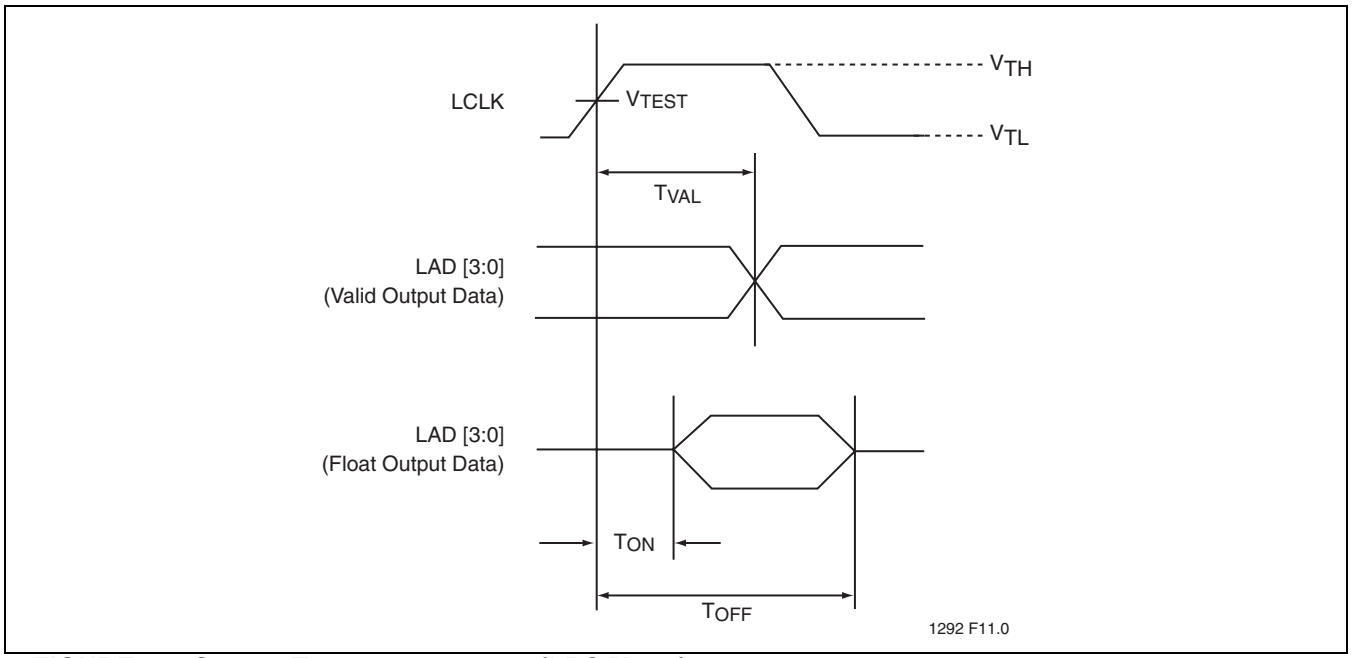


FIGURE 11: OUTPUT TIMING PARAMETERS (LPC MODE)

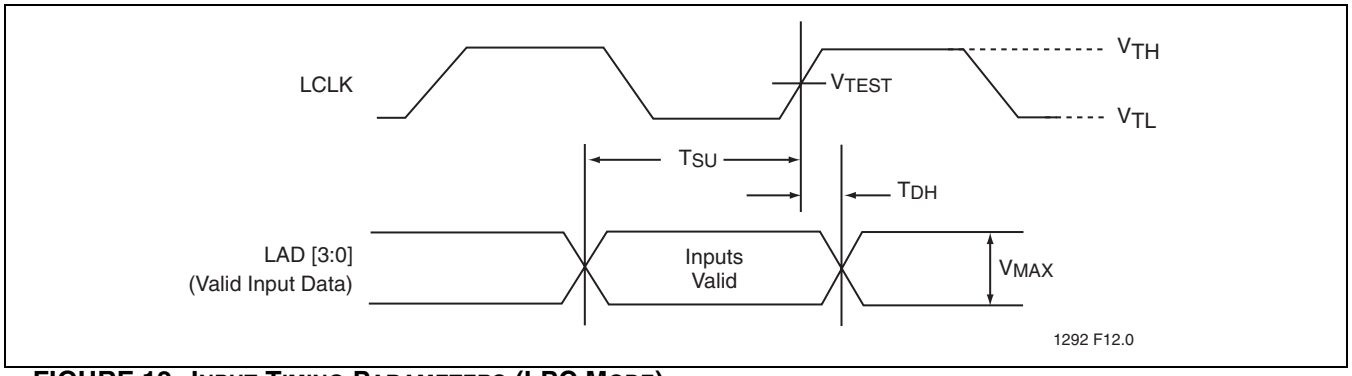


FIGURE 12: INPUT TIMING PARAMETERS (LPC MODE)

TABLE 29: INTERFACE MEASUREMENT CONDITION PARAMETERS (LPC MODE)

Symbol	Value	Units
V_{TH}[1,2]	0.6 V_{DD}	V
V_{TL}[1,2]	0.2 V_{DD}	V
V_{TEST}	0.4 V_{DD}	V
V_{MAX}[1,2]	0.4 V_{DD}	V
Input Signal Edge Rate	1	V/ns

T29.0 1292

1. The input test environment is done with 0.1 V_{DD} of overdrive over V_{IH} and V_{IL}. Timing parameters must be met with no more overdrive than this. V_{MAX} specifies the maximum peak-to-peak waveform allowed for measuring input timing. Production testing may use different voltage values, but must correlate results back to these parameters.
2. In the case of multi-byte read, V_{TL} = 0.1 V_{DD} and V_{TH} = 0.9V_{DD}

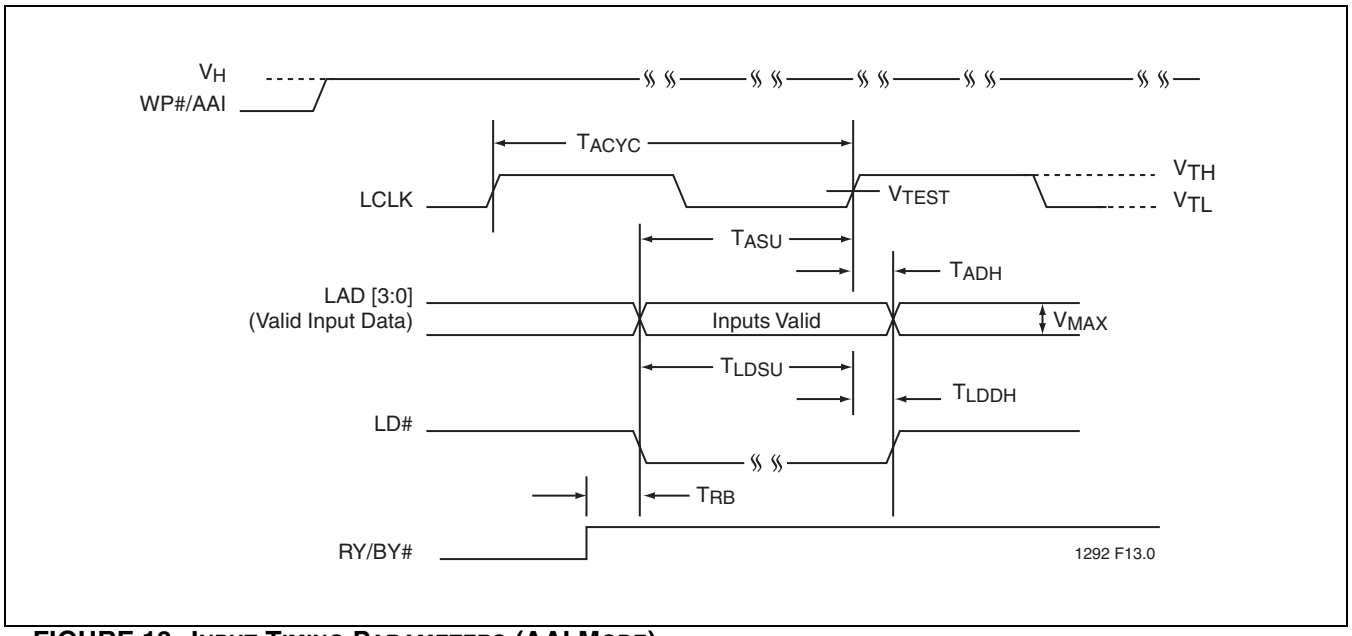


FIGURE 13: INPUT TIMING PARAMETERS (AAI MODE)

TABLE 30: INPUT CYCLE TIMING PARAMETERS, V_{DD}=3.0-3.6V (AAI MODE)

Symbol	Parameter	Min	Max	Units
T_{ACYC}	Clock Cycle Time	135		ns
T_{ASU}	Data Set Up Time to Clock Rising	25		ns
T_{ADH}	Clock Rising to Data Hold Time	25		ns
T_{RB}	RY/BY# LD# Falling	25		ns
T_{LDSU}	LD# Set Up Time	25		ns
T_{LDDH}	LD# Hold Time	25		ns

T30.0 1292

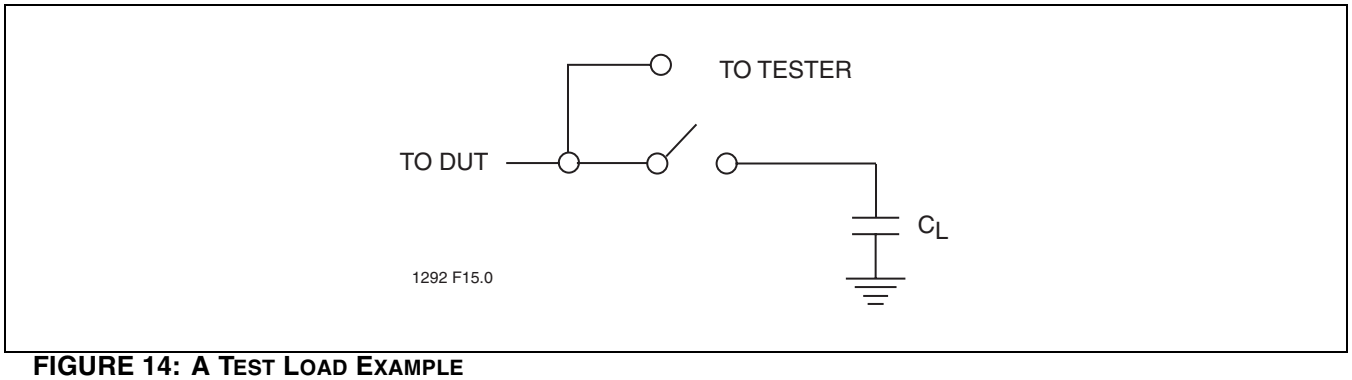
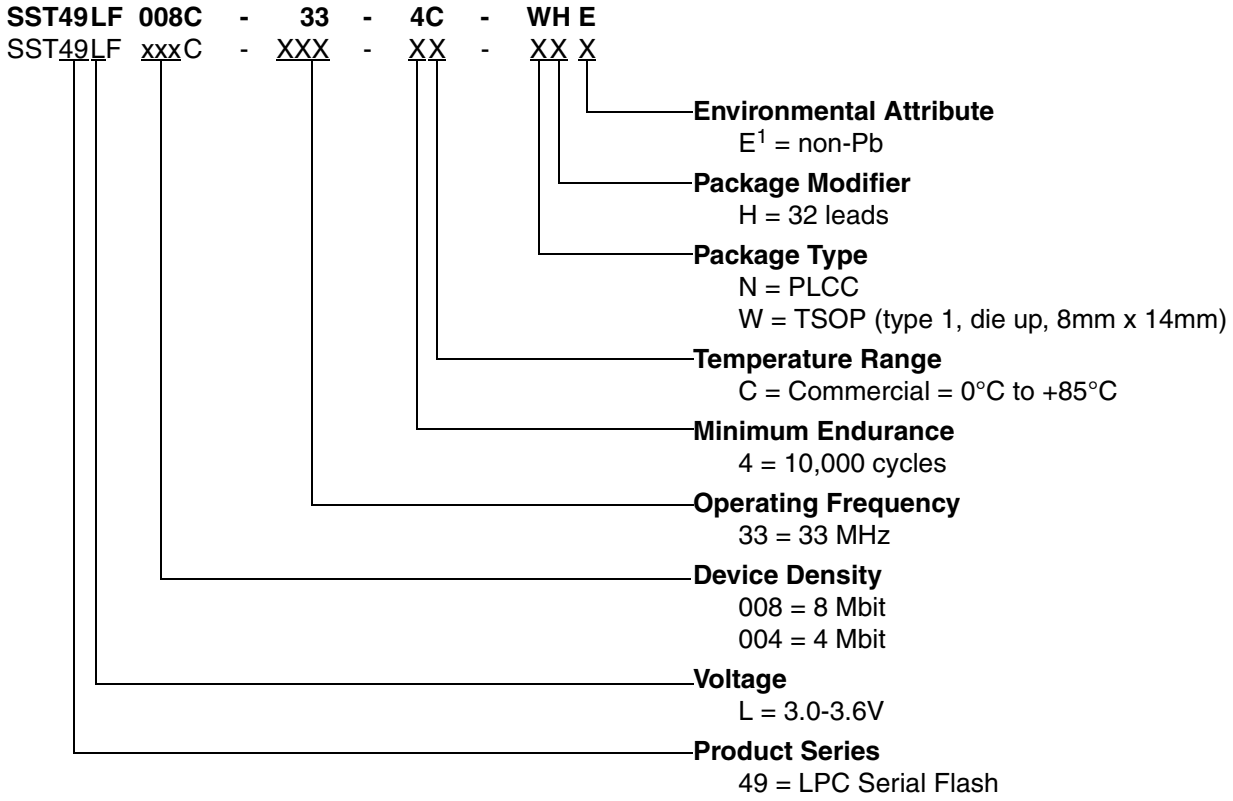


FIGURE 14: A TEST LOAD EXAMPLE

Advance Information

PRODUCT ORDERING INFORMATION



1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST49LF004C

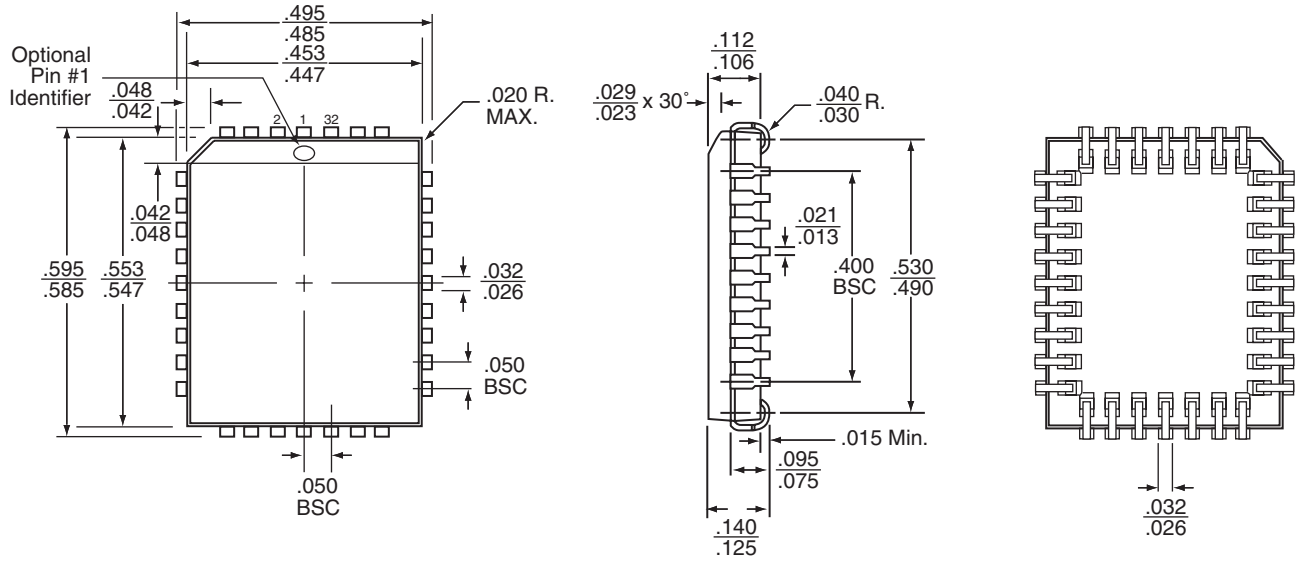
SST49LF004C-33-4C-NHE SST49LF004C-33-4C-WHE

Valid combinations for SST49LF008C

SST49LF008C-33-4C-NHE SST49LF008C-33-4C-WHE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

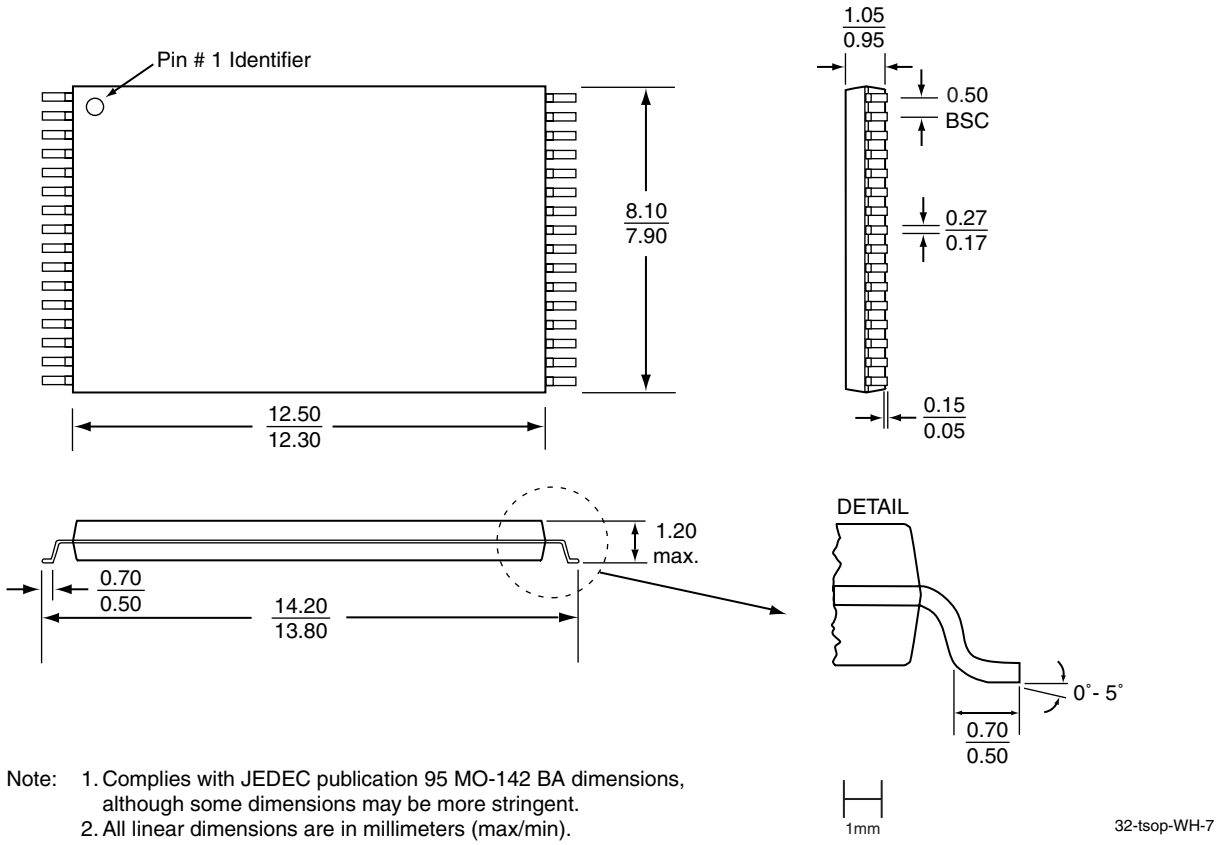
PACKAGING DIAGRAMS



Note: 1. Complies with JEDEC publication 95 MS-016 AE dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in inches (max/min).
3. Dimensions do not include mold flash. Maximum allowable mold flash is .008 inches.
4. Coplanarity: 4 mils.

32-plcc-NH-3

32-LEAD PLASTIC LEAD CHIP CARRIER (PLCC)
SST PACKAGE CODE: NH



Note: 1. Complies with JEDEC publication 95 MO-142 BA dimensions, although some dimensions may be more stringent.
2. All linear dimensions are in millimeters (max/min).
3. Coplanarity: 0.1 mm
4. Maximum allowable mold flash is 0.15 mm at the package ends, and 0.25 mm between leads.

32-LEAD THIN SMALL OUTLINE PACKAGE (TSOP) 8MM X 14MM
SST PACKAGE CODE: WH

TABLE 31: REVISION HISTORY

Revision	Description	Date
00	• Initial release of data sheet	Jan 2006

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