MAS6180

AM Receiver IC

- **Single Band Receiver IC**
- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**
- **Fast Startup Feature**

DESCRIPTION

The MAS6180 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiver. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary.

MAS6180 has options for compensating shunt capacitances of different crystals (See ordering information on page 9).

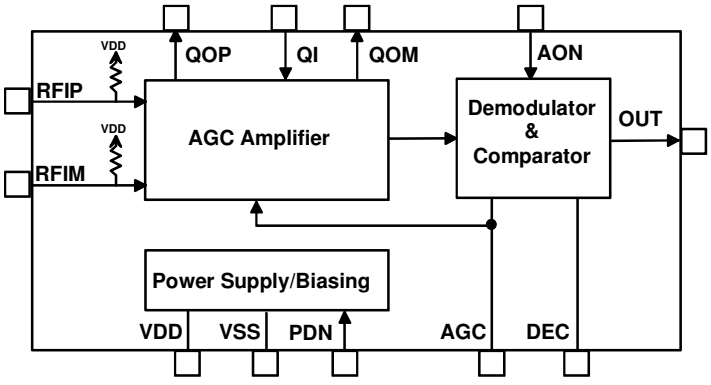
FEATURES

- Single Band Receiver IC
- Highly Sensitive AM Receiver, 0.4 μV_{RMS} typ.
- Wide Supply Voltage Range from 1.1 V to 3.6 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter
- Crystal Compensation Capacitance Options
- Differential Input

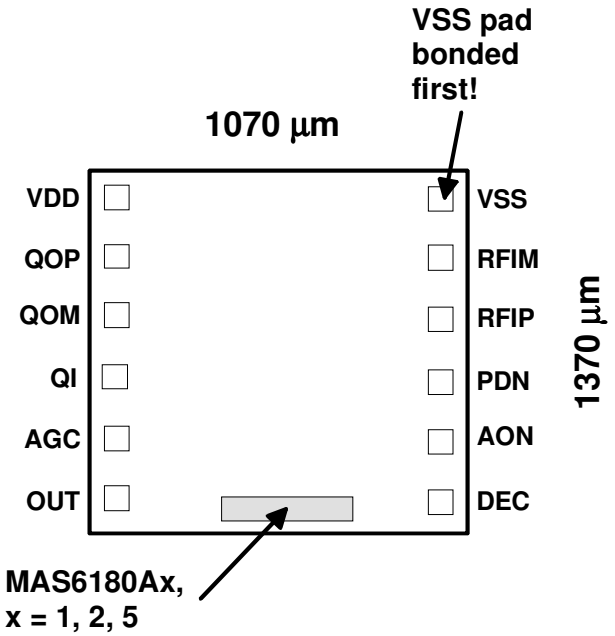
APPLICATIONS

- Single Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK), HGB (Switzerland) and BPC (China)

BLOCK DIAGRAM



MAS6180 PAD LAYOUT



DIE size = 1.07 mm x 1.37 mm; PAD size = 80 µm x 80 µm

Note: Because the substrate of the die is internally connected to VSS, the die has to be connected to VSS or left floating. Please make sure that VSS is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	152 µm	1137 µm	
Positive Quartz Filter Output for Crystal	QOP	152 µm	1002 µm	
Negative Quartz Filter Output for Crystal	QOM	152 µm	815 µm	1
Quartz Filter Input for Crystal and External Compensation Capacitor	QI	152 µm	629 µm	
AGC Capacitor	AGC	152 µm	443 µm	
Receiver Output	OUT	152 µm	257 µm	2
Demodulator Capacitor	DEC	915 µm	265 µm	
AGC On Control	AON	915 µm	451 µm	3
Power Down	PDN	915 µm	636 µm	4
Positive Receiver Input	RFIP	915 µm	824 µm	5
Negative Receiver Input	RFIM	915 µm	1010 µm	5
Power Supply Ground	VSS	915 µm	1158 µm	

Notes:
1) External crystal compensation capacitor pin QOM is connected only in MAS6180A5 version. It is left unconnected in MAS6180A1 and A2 versions which have internal compensation capacitor.
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5$ µA
   - at power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
4) PDN = VSS means receiver on; PDN = VDD means receiver off
   Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
5) Receiver inputs RFIP and RFIM have both 600 kΩ biasing resistors towards VDD

ABSOLUTE MAXIMUM RATINGS

All Voltages with Respect to Ground

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}-V_{SS}		- 0.3	5.5	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
ESD Rating	V_{ESD}	For all pins, Human Body Model (HBM), ESD Association Standard Test Method ESD-STM5.1-1998, C_{ESD} = 100 pF, Rs = 1500 Ω),	±2		kV
Latchup Current Limit	I_{LUT}	For all pins, test according to Micro Analog Systems specification ESQ0141. See note below.	±100		mA
Operating Temperature	T_{OP}		-40	+85	℃
Storage Temperature	T_{ST}		- 55	+150	℃

Stresses beyond those listed may cause permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.

Note: In latchup testing the supply voltages are connected normally to the tested device. Then pulsed test current is fed to each input separately and device current consumption is observed. If the device current consumption increases suddenly due to test current pulses and the abnormally high current consumption continues after test current pulses are cut off then the device has gone to latch up. Current pulse is turned on for 10 ms and off for 20 ms.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 1.5V, Temperature = 25℃, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10		3.6	V
Current Consumption	I_{DD}	VDD=1.5 V, Vin=0 µVrms VDD=1.5 V, Vin=20 mVrms VDD=3.6 V, Vin=0 µVrms VDD=3.6 V, Vin=20 mVrms	40 24	55 40 58 43	80 65	µA
Stand-By Current	I_{DDoff}	See note below.			0.1	µA
Input Frequency Range	f_{IN}		40		100	kHz
Minimum Input Voltage	$V_{IN\ min}$			0.4	1	µVrms
Maximum Input Voltage	$V_{IN\ max}$		20			mVrms
Receiver Input Resistance Receiver Input Capacitance	R_{RFI} C_{RFI}	Differential Input, f=40 kHz..77.5 kHz		600 0.5		kΩ pF
Input Levels $\|I_{IN}\|$<0.5 µA	V_{IL} V_{IH}		 V_{DD}-0.35		0.35	V
Output Current V_{OL}<0.2 V_{DD};V_{OH} >0.8 V_{DD}	$\|I_{OUT}\|$		5			µA
Output Pulse	T_{100ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	50		140	ms
	T_{200ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	150		230	ms
	T_{500ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	400	500	600	ms
	T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms	700	800	900	ms
Startup Time	T_{Start}	Fast Start-up, Vin=0.4 µVrms Fast Start-up, Vin=20 mVrms		1.3 3.5		s
Output Delay Time	T_{Delay}			50	100	ms

Note: Stand-by current consumption may increase if V_{IH} and V_{IL} differ from VDD and 0 respectively.

TYPICAL APPLICATION

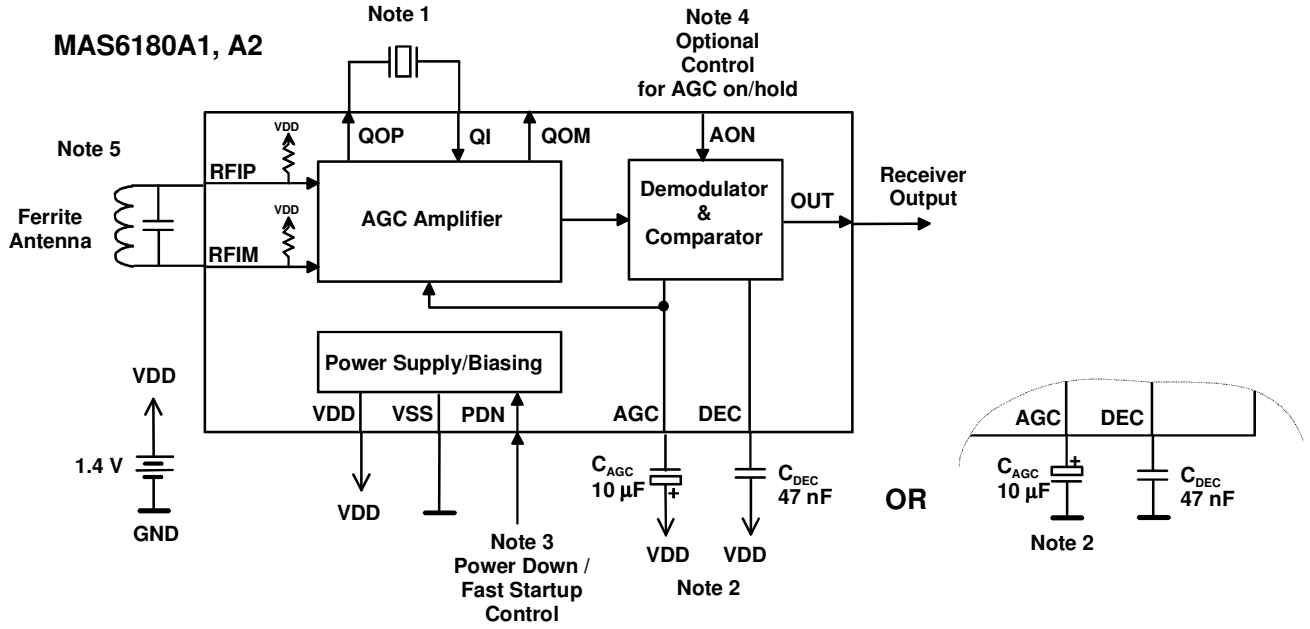


Figure 1. Application circuit of internal compensation capacitance option version MAS6180A1 and A2.

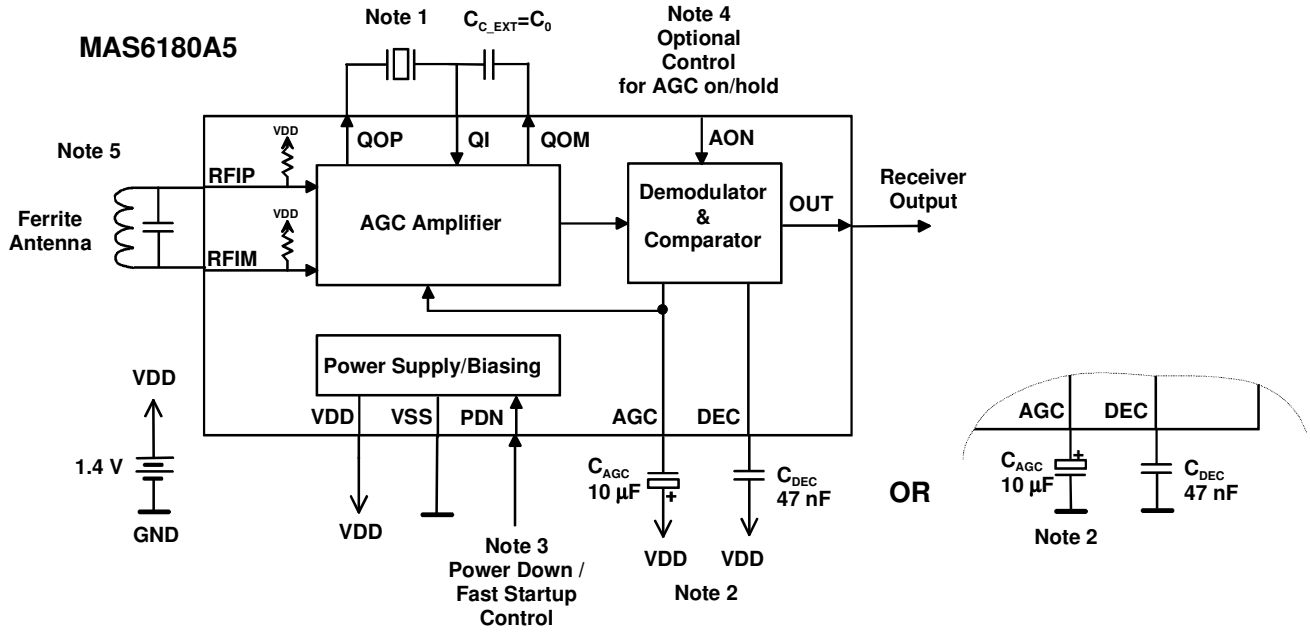


Figure 2. Application circuit of external compensation capacitance option version MAS6180A5.

TYPICAL APPLICATION (Continued)

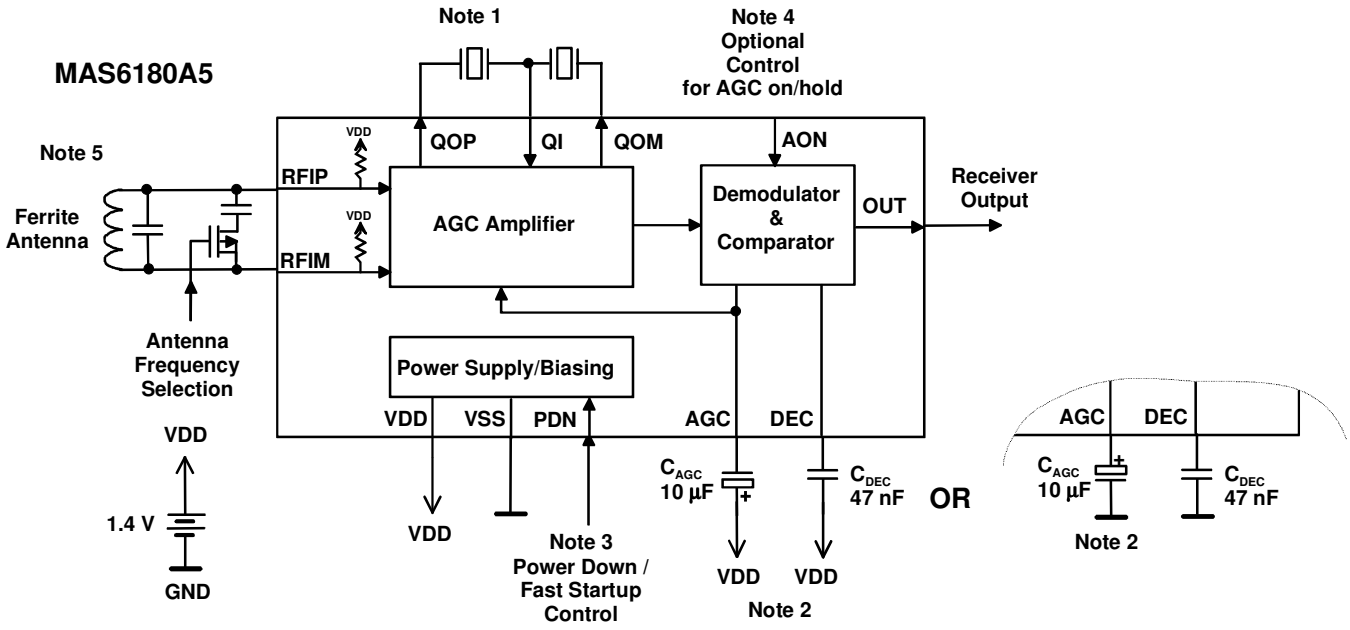


Figure 3. Dual band application circuit of external compensation capacitance option version MAS6180A5. PMOS switch transistor is used since RFIM input is biased close to VDD voltage.

TYPICAL APPLICATION (Continued)

Note 1: Crystals
The crystal as well as ferrite antenna frequencies are chosen according to the time-signal system (Table 1). The crystal shunt capacitance C_0 should be matched as well as possible with the internal shunt capacitance compensation capacitor C_C of MAS6180. MAS6180A5 is option for external crystal compensation capacitor. The external compensation capacitor should be matched similarly as well as possible with crystal's shunt capacitance. See Compensation Capacitance Options on table 2.

Table 1. Time-Signal System Frequencies

Time-Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 kHz
HGB	Switzerland	75 kHz	75.003 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz
BPC	China	68.5 kHz	68.505 kHz

Table 2. Compensation Capacitance Options

Device	C_C	Crystal Description
MAS6180A1	0.75 pF	For low C_0 crystals
MAS6180A2	1.3 pF	For high C_0 crystals
MAS6180A5	C_{C_EXT}	For any crystals, external compensation capacitor

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example crystal with 1 pF floating package shunt capacitance can have 0.85 pF grounded package shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

In dual band receiver configuration the crystals can be connected in parallel thus external compensation capacitor value C_{C_EXT} must be sum of two crystals' shunt capacitances. Instead of parallel crystal connection it is also possible to connect other crystal from QOP pin and the other crystal from QOM pin to common QI pin (figure 3). In this circuit configuration no external compensation capacitor is required since the crystals compensate each other. The sensitivity of dual band receiver configuration will be lower than that of single band receiver configuration since the noise band width of crystal filter with two parallel crystals is double.

Table 3 below presents some crystal manufacturers having suitable crystals for timesignal receiver application.

Table 3. Crystal Manufacturers and Crystal Types in Alphaphetical Order for Timesignal Receiver Application

Manufacturer	Crystal Type	Dimensions	Web Link
Citizen	CFV-206	ø 2.0 x 6.0	http://www.citizen.co.jp/tokuhan/quartz/
Epson Toyocom	C-2-Type C-4-Type	ø 1.5 x 5.0 ø 2.0 x 6.0	http://www.epsontoyocom.co.jp/english/
KDS Daishinku	DT-261	ø 2.0 x 6.0	http://www.kds.info/index_en.htm
Microcrystal	MX1V-L2N MX1V-T1K	ø 2.0 x 6.0 ø 2.0 x 8.1	http://www.microcrystal.com/
Seiko Instruments	VTC-120	ø 1.2 x 4.7	http://www.sii-crystal.com

TYPICAL APPLICATION (Continued)

Note 2: AGC Capacitor
The AGC and DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum 100 MΩ. Also probes with at least few 100 MΩ impedance should be used for voltage probing of the AGC and DEC pins. Electrolytic AGC capacitor should have voltage rating at least 25 V for low enough leakage. DEC capacitor can be low leakage chip capacitor.
Both the AGC and DEC capacitors can be connected either to VDD or to VSS. To minimize leakage currents during power down the AGC and DEC capacitors are best to be connected to VDD since in power down the AGC and DEC pins go to VDD voltage potential. In this case the positive polarity pin of electrolyte capacitor should be connected to VDD. If the capacitors are connected to VSS then the negative polarity pin of electrolyte capacitor should be connected to VSS.

Note 3: Power Down / Fast Startup Control
Both power down and fast startup are controlled using the PDN pin. The device is in power down (turned off) if PDN = VDD and in power up (turned on) if PDN = VSS. Fast startup is triggered automatically by the falling edge of PDN signal, i.e., controlling device from power down to power up. The VDD must be high before falling edge of PDN to guarantee proper operation of fast startup circuitry. Before power up the device should have been kept in power down state at least 50ms. This guarantees that the AGC capacitor voltage has been completely pulled to VDD during power down. The startup time without proper fast startup control can be several minutes but with fast startup it is shortened typically to few seconds.

Note 4: Optional Control for AGC On/Hold
AON control pin has internal pull up which turns AGC circuit on all the time if AON pin is left unconnected. Optionally AON control can be used to hold and release AGC circuit. Stepper motor drive of analog clock or watch can produce disturbing amount of noise which can shift the input amplifier gain to unoptimal level. This can be avoided by controlling AGC hold (AON=VSS) during stepper motor drive periods and releasing AGC (AON=VDD) when motors are not driven. The AGC should be in hold only during disturbances and kept on other time released since due to leakage the AGC can change slowly when in hold.

Note 5: Ferrite Antenna
The ferrite antenna converts the transmitted radio wave into a voltage signal. It has an important role in determining receiver performance. Recommended antenna impedance at resonance is around 150 kΩ.
Low antenna impedance corresponds to low noise but often also to small signal amplitude. On the other hand high antenna impedance corresponds to high noise but also large signal. The optimum performance where signal-to-noise ratio is at maximum is achieved in between.
The antenna should have also some selectivity for rejecting near signal band disturbances. This is determined by the antenna quality factor which should be approximately 100. Much higher quality factor antennas suffer from extensive tuning accuracy requirements and possible tuning drifts by the temperature.

Antenna impedance can be calculated using equation 1 where f_0, L, Q_{ant} and C are resonance frequency, coil inductance, antenna quality factor and antenna tuning capacitor respectively. Antenna quality factor Q_{ant} is defined by ratio of resonance frequency f_0 and antenna bandwidth B (equation 2).

$$R_{antenna} = 2\pi \cdot f_0 \cdot L \cdot Q_{antenna} = \frac{Q_{antenna}}{2\pi \cdot f_0 \cdot C} = \frac{1}{2\pi \cdot B \cdot C} \qquad \textbf{Equation 1.}$$

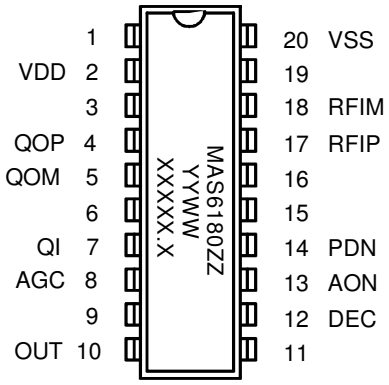
$$Q_{antenna} = \frac{f_0}{B} \qquad \textbf{Equation 2.}$$

Table 4 below presents some antenna manufacturers for time signal application.

Table 4. Antenna Manufacturers and Antenna Types in Alphaphetical Order for Time Signal Application

Manufacturer	Antenna Type	Dimensions	Web Link
HR Electronic GmbH	60716 (60kHz) 60708 (77.5kHz)	ø 10 x 60 mm	http://www.hrelectronic.com/
Sumida	ACL80A/B (40kHz, 60kHz) ACL27 (40kHz, 60kHz)	ø 14 x 83 mm 6 x 7.3 x 28 mm	www.sumida.co.jp/jeita/XJA021.pdf

MAS6180 SAMPLES IN SBDIL 20 PACKAGE



Top Marking Definitions:
YYWW = Year Week
XXXXX.X = Lot Number
ZZ =Sample Version

PIN DESCRIPTION

Pin Name	Pin	Type	Function	Note
	1	NC		
VDD	2	P	Positive Power Supply	
	3	NC		
QOP	4	AO	Positive Quartz Filter Output for Crystal	
QOM	5	NC	Negative Quartz Filter Output for External Compensation Capacitor or Second Crystal	1
	6	NC		2
QI	7	AI	Quartz Filter Input for Crystal and External Compensation Capacitor	
AGC	8	AO	AGC Capacitor	
	9	NC		
OUT	10	DO	Receiver Output	3
	11	NC		
DEC	12	AO	Demodulator Capacitor	
AON	13	DI	AGC On Control	4
PDN	14	DI	Power Down Input	5
	15	NC		
	16	NC		
RFIP	17	AI	Positive Receiver Input	6
RFIM	18	AI	Negative Receiver Input	6
	19	NC		
VSS	20	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:

1) External crystal compensation capacitor pin QOM is connected only in MAS6180A5 version. It is left unconnected in MAS6180A1 and A2 versions which have internal compensation capacitor.
2) Pin 6 between QOM and QI must be connected to VSS to eliminate DIL package lead frame parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) type pins are also recommended to be connected to VSS to minimize noise coupling.
3) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - the output is a current source/sink with $|I_{OUT}| > 5\ \mu A$
   - at power down the output is pulled to VSS (pull down switch)
4) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (working)
   - Internal pull-up with current < 1 µA which is switched off at power down
5) PDN = VSS means receiver on; PDN = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down (PDN=VDD) controlled to power up (PDN=VSS) i.e. at the falling edge of PDN signal.
6) Receiver inputs RFIP and RFIM have both 600 kΩ biasing resistors towards VDD

ORDERING INFORMATION

Product Code	Product	Description	Capacitance Option
MAS6180A1TC00	Single Band AM-Receiver IC with Differential Input	EWS-tested wafer, diameter 150 mm, thickness 400 µm.	C_C = 0.75 pF
MAS6180A2TC00	Single Band AM-Receiver IC with Differential Input	EWS-tested wafer, diameter 150 mm, thickness 400 µm.	C_C = 1.3 pF
MAS6180A5TC00	Single Band AM-Receiver IC with Differential Input	EWS-tested wafer, diameter 150 mm, thickness 400 µm.	External compensation capacitor

Contact Micro Analog Systems Oy for other wafer thickness options.

◆ **The formation of product code**

An example for MAS6180A1TC00:

MAS6180	**A**	**1**	**TC**	**00**
Product name	Design version	Capacitance option: C_C = 0.75 pF	Package type: TC = 400 µm thick EWS tested wafer	Delivery format: 00 = bare wafer 05 = dies on tray

LOCAL DISTRIBUTOR

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