RNA53A30F

System Organizer IC for Dedicate Microcomputer

R03DS0034EJ0400
Rev.4.00
Jun 26, 2013

Description

RNA53A30F is reset function and reference voltage output for microcontroller has been installed.

Provide support for Renesas MCU operation.

Features

- Reset detection voltage: 3.05 V ± 1%
- Standard voltage: 3.050 V ± 0.8%
- Delay time: 50,100 ms (fine regulation by resistance is possible)
- Corresponds to manual reset
- Sleep mode is installed

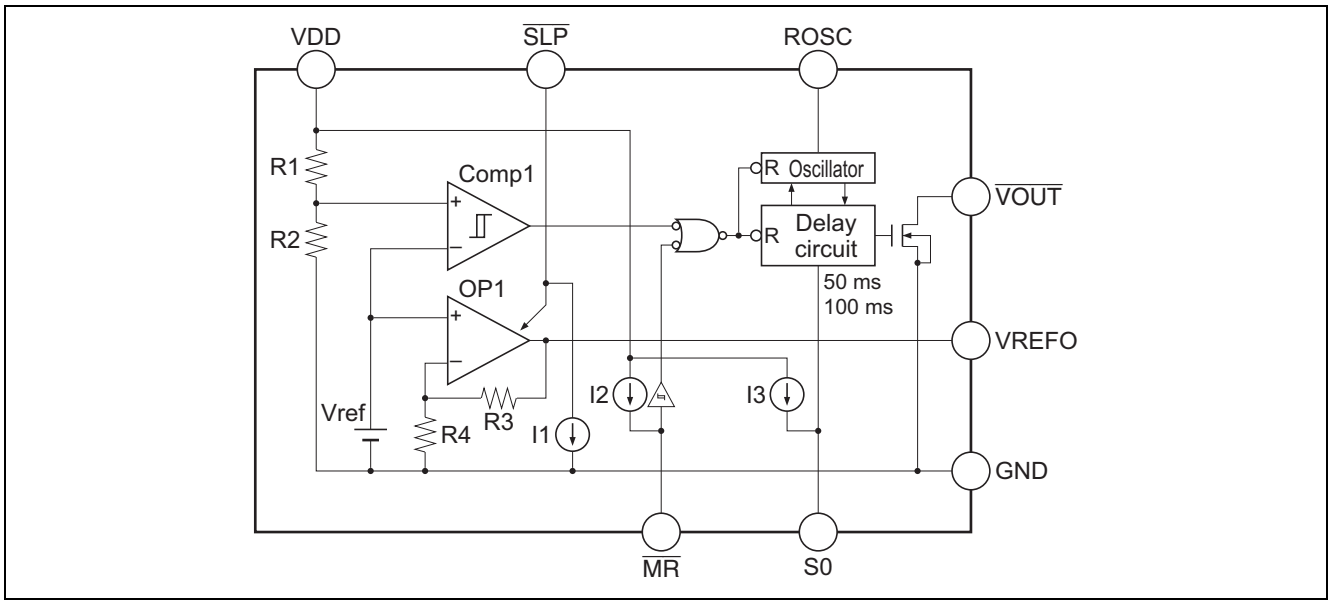
Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RNA53A30FUSH1	SSOP-8	PVSP0008KA-A	US	H (3,000 pcs/reel)	1 (Sn/Bi)

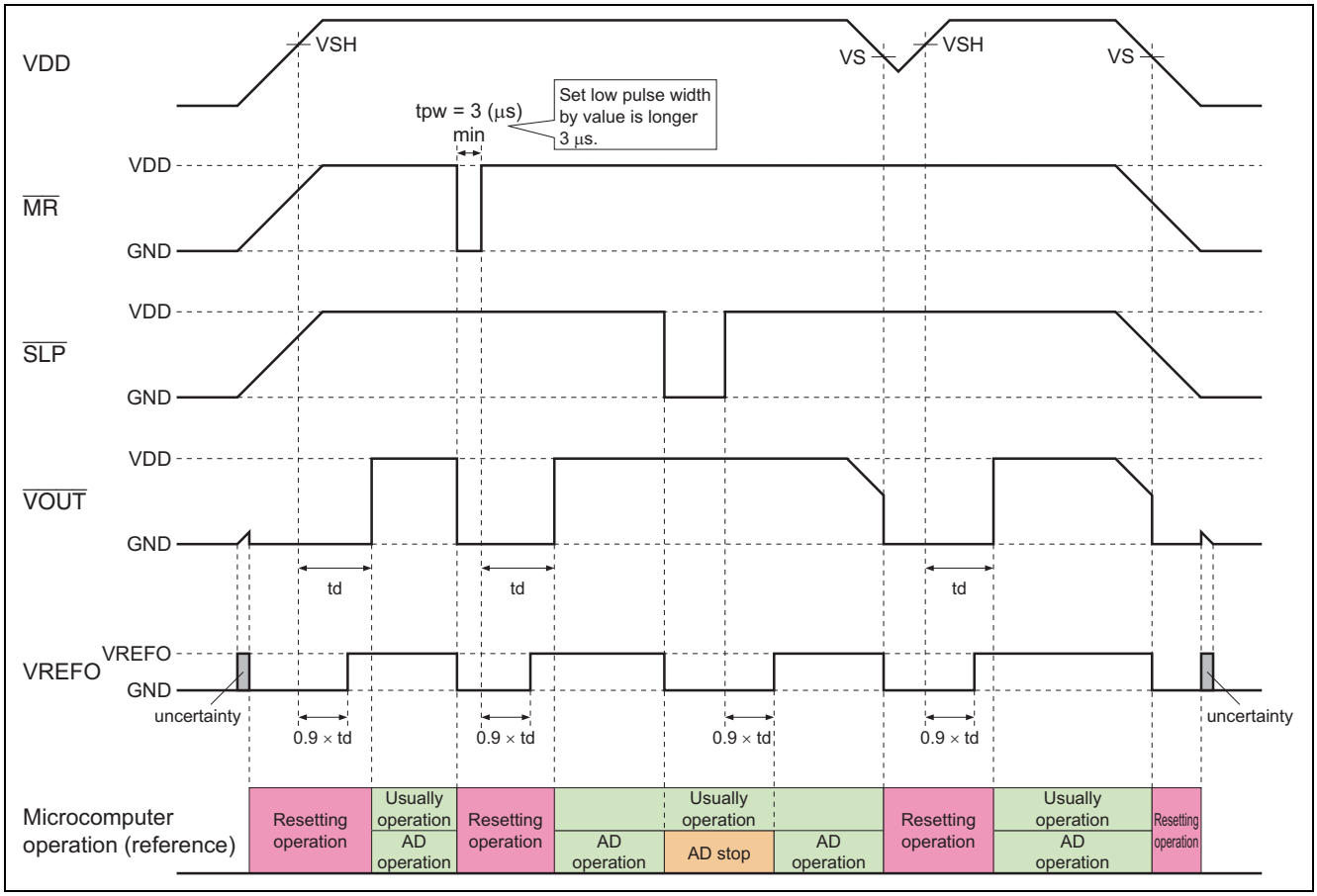
Application

- Power supply voltage monitoring for microprocessors
- Computers and notebook computers
- Digital still camera, digital video camera, and PDA

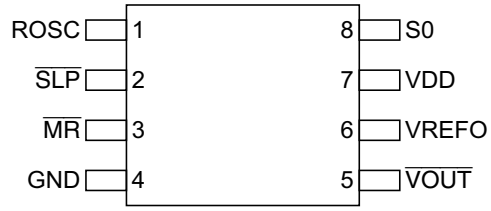
Block Diagram



Timing Chart

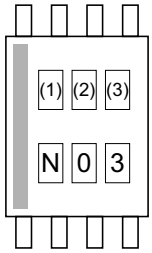


Pin Arrangement



(Top view)

Mark Indication



(1)	Year code	The last digit of year
(2)	Month code	Starting in January "A", "B", "C", "D", "E", "F", "G", "H", "J", "K", "L", "M"
(3)	Week code	View week of month, 1 week → "1"

Pin Description

Pin No.	Terminal Marking	Terminal Name	I/O	Function
1	ROSC	Oscillation control resistance installation terminal	—	• 1.1 MΩ is installed between GND usually. • Delay adjustment range of resistance: 650(kΩ) to 1.35(MΩ)
2	$\overline{\text{SLP}}$	Sleep mode control	I	• L: Sleep mode (Power-supply current becomes several μA) • H: Usually mode • Terminal is open, Pull-down in GND
3	$\overline{\text{MR}}$	Manual reset input	I	• Low is input, 5pin($\overline{\text{VOUT}}$) output the low level Set the low pulse width by value is longer 3 μs • Terminal open, pull-up in VDD
4	GND	GND	—	• Sorcing 0 V.
5	$\overline{\text{VOUT}}$	Reset output	O	• Power-supply voltage reaches the value below the detection voltage, low is output • Low level is input to $\overline{\text{MR}}$ terminal, low is output • Open drain output • Range pull-up resistance: 10(kΩ) to 100(kΩ)
6	VREFO	Standard voltage output	O	• Standard voltage (3.05 V typ) for AD/DA is output • Outside puts capacity (0.1 μF) by pursuant for microcomputer
7	VDD	Power-supply terminal	—	• Sorcing power-supply voltage.
8	S0	Delay time switch	I	• Delay time is switched. Low: 50 (ms), High: 100 (ms) • Terminal is open, pull-up in Vdd

Absolute Maximum Ratings

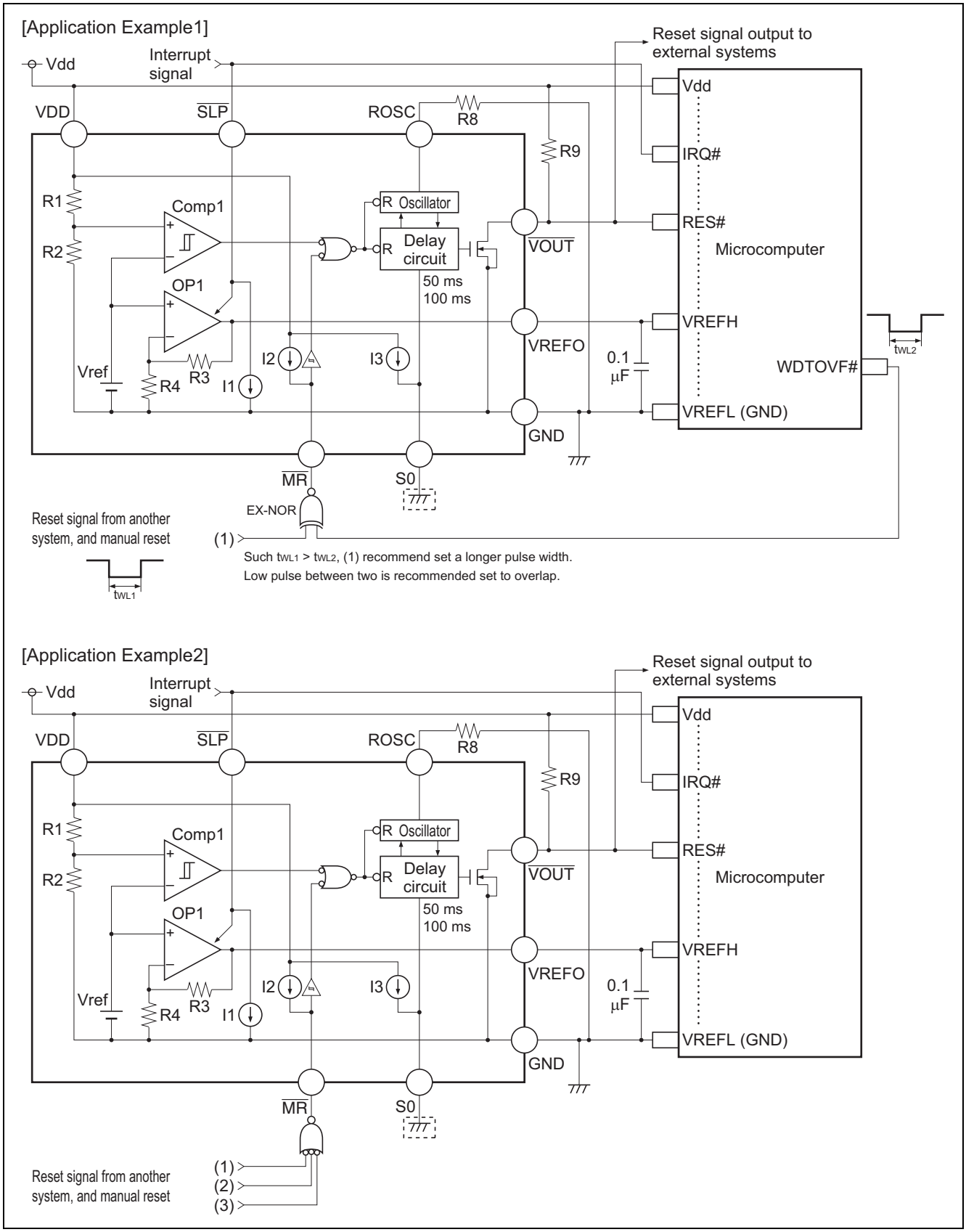
Item	Symbol	Ratings	Unit
Supply voltage	VDD	6.5	V
Output voltage (open-drain type)	Vout	–0.3 to +6.5	V
Input voltage	Vin	–0.3 to VDD	V
Output current	Iout	10	mA
Standard voltage terminal source current	IREF	5	mA
Continuous power dissipation	Pd	160 (Ta = 25°C)	mW
Operating temperature	Topr	–40 to +85	°C
Storage temperature	Tstg	–55 to +125	°C

Electrical Characteristics

(Vdd = 3.3 V, Ta = 25°C, unless otherwise noted)

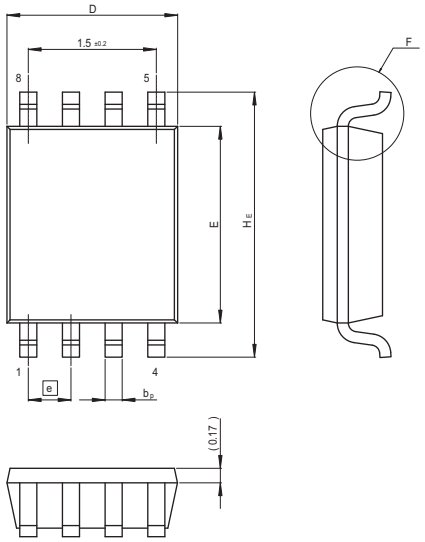
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output fixation voltage	VOUL	—	—	0.9	V	$\overline{\text{VOUT}}$ terminal, RL = 10 (kΩ)
Operating limit voltage	VOPM	2.7	—	—	V	
Current consumption	Idd	—	100	200	µA	Vdd = 3.3 V, $\overline{\text{SLP}}$ = Hi (Vdd)
Standing circuit current	IddSLP	—	2.8	5.6	µA	$\overline{\text{SLP}}$ = Low (GND), $\overline{\text{MR}}$ = Hi (Vdd), $\overline{\text{S0}}$ = Hi (Vdd)
Detecting voltage	VS	3.019	3.049	3.079	V	
Detecting voltage temperature coefficient	Vs/ΔT	—	±100	—	ppm/°C	
Hysteresis voltage	VHYS	VS×0.01	VS×0.02	VS×0.03	V	
Standard voltage	VREF	3.026	3.050	3.074	V	Vdd ≥ 3.3 V, Isource = 0 to 3 mA, CL = 0.1 µF
Standard voltage temperature coefficient	VREF/ ΔT	—	±100	—	ppm/°C	
Standard voltage return time	VRCV	—	—	0.9×td	ms	
Output low voltage	VOL	—	0.3	0.54	V	$\overline{\text{VOUT}}$, Isink = 4 mA, Vdd = 2.6 (V)
Output leakage current	ILK	—	—	100	nA	$\overline{\text{VOUT}}$, Vdd = 3.6 V
Minimum pulse width	tpw	3	—	—	µs	MR terminal input
Delay time	td	35	50	65	ms	S0 = Low
		70	100	130	ms	S0 = High
Reactive time	tPHL	—	6	—	µs	VDD drop to time until outputting $\overline{\text{VOUT}}$ $\overline{\text{MR}}$ input to time until outputting $\overline{\text{VOUT}}$
High input voltage	VIH	Vdd×0.8	—	Vdd	V	$\overline{\text{MR}}$ terminal, $\overline{\text{SLP}}$ terminal, S0 terminal, Vdd = 3.0 V to 3.6 V
Low input voltage	VIL	0	—	Vdd×0.2	V	$\overline{\text{MR}}$ terminal, $\overline{\text{SLP}}$ terminal, S0 terminal, Vdd = 3.0 V to 3.6 V
S0 terminal pull-up current	IPUS0	—	—	0.5	µA	S0 terminal
$\overline{\text{MR}}$ terminal pull-up current	IPUMR	1.5	3	6	µA	$\overline{\text{MR}}$ terminal
$\overline{\text{SLP}}$ terminal pull-down current	IPDSLP	—	—	0.5	µA	$\overline{\text{SLP}}$ terminal

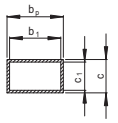
Example of Application Circuit



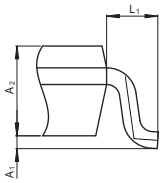
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VSSOP8-2.3x2-0.50	PVSP0008KA-A	TTP-8DB/TTP-8DBV	0.010g





Terminal cross section



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	1.8	2.0	2.2
E	2.2	2.3	2.4
A_2	0.6	0.7	0.8
A_1	0	—	0.1
A	—	—	—
b_p	0.15	0.22	0.3
b_1	—	0.20	—
c	0.08	0.13	0.23
c_1	—	0.11	—
θ	—	—	—
H_E	2.8	3.1	3.4
e	—	(0.5)	—
x	—	—	—
y	—	—	—
Z	—	—	—
L	—	—	—
L_1	—	(0.4)	—

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

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