M68AR024D

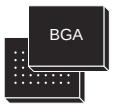
16 Mbit (1M x16) 1.8V Asynchronous SRAM

PRELIMINARY DATA

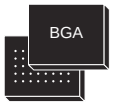
FEATURES SUMMARY

- SUPPLY VOLTAGE: 1.65 to 1.95V
- I/O SUPPLY VOLTAGE: 1.5 to 1.95V
- 1M WORDS x 16 bits LOW POWER SRAM
- EQUAL CYCLE and ACCESS TIME: 70ns
- LOW V_{CC} DATA RETENTION: 1.0V
- LOW STANDBY CURRENT
- TRI-STATE COMMON I/O
- SINGLE BYTE READ/WRITE
- AUTOMATIC POWER DOWN

Figure 1. Packages



TFBGA48 (ZH)
8 x 10 mm
(for Engineering Samples only)



TFBGA48 (ZB)
6.5 x 10 mm

This is preliminary information on a new product now in development or undergoing evaluation. Details are subject to change without notice.

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SUMMARY DESCRIPTION

The M68AR024D is a 16 Mbit (16,777,216 bit) Low Power SRAM fabricated in STMicroelectronics advanced CMOS technology, organized as 1,048,576 words by 16 bits. The device exhibits fully static operation requiring no external clocks or timing strobes.

It needs 1.65 to 1.95V supply voltage. By using the V_{CCQ} pin all the outputs can be powered independently from the core supply voltage allowing to drive the I/O pins down to 1.5V. V_{CCQ} pin can be tied to Vcc if the feature is not required.

This device has a standard Asynchronous SRAM Interface. Read and Write cycles can be performed on a single byte by using $\overline{UB}$/$\overline{LB}$ signals.

The device can be put into standby mode by using $\overline{E1}$/E2 pins. The same pins can be used to cascade more devices in order to achieve deep memory expansion.

Standby mode allows a low current consumption, up to 99%, by reducing internal activities.

The M68AR024D is available in TFBGA48 (0.75 mm pitch) package with industrial standard footprint.

Figure 2. Logic Diagram

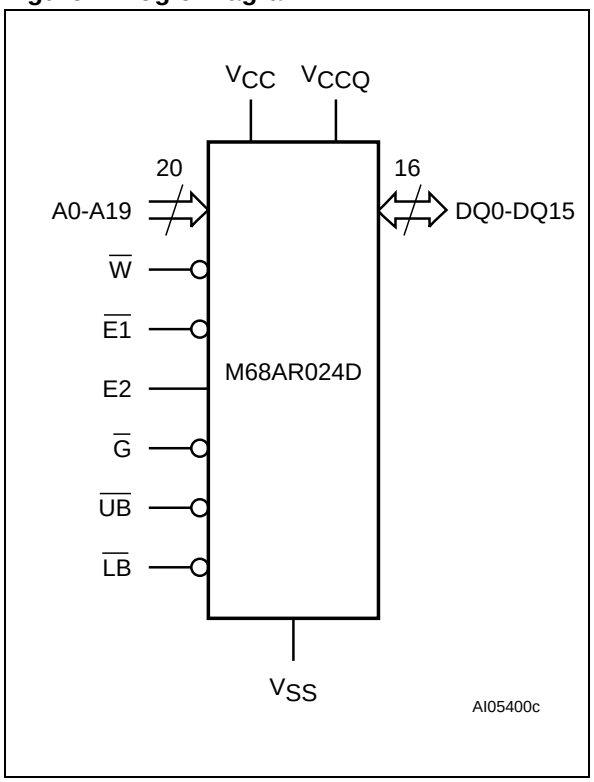


Table 1. Signal Names

A0-A19	Address Inputs
DQ0-DQ15	Data Input/Output
$\overline{E1}$, E2	Chip Enables
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
$\overline{UB}$	Upper Byte Enable Input
$\overline{LB}$	Lower Byte Enable Input
V_{CC}	Supply Voltage
V_{CCQ}	I/O Supply Voltage
V_{SS}	Ground
NC	Not Connected Internally
DU	Don't Use as Internally Connected

Figure 3. TFBGA Connections (Top view through package)

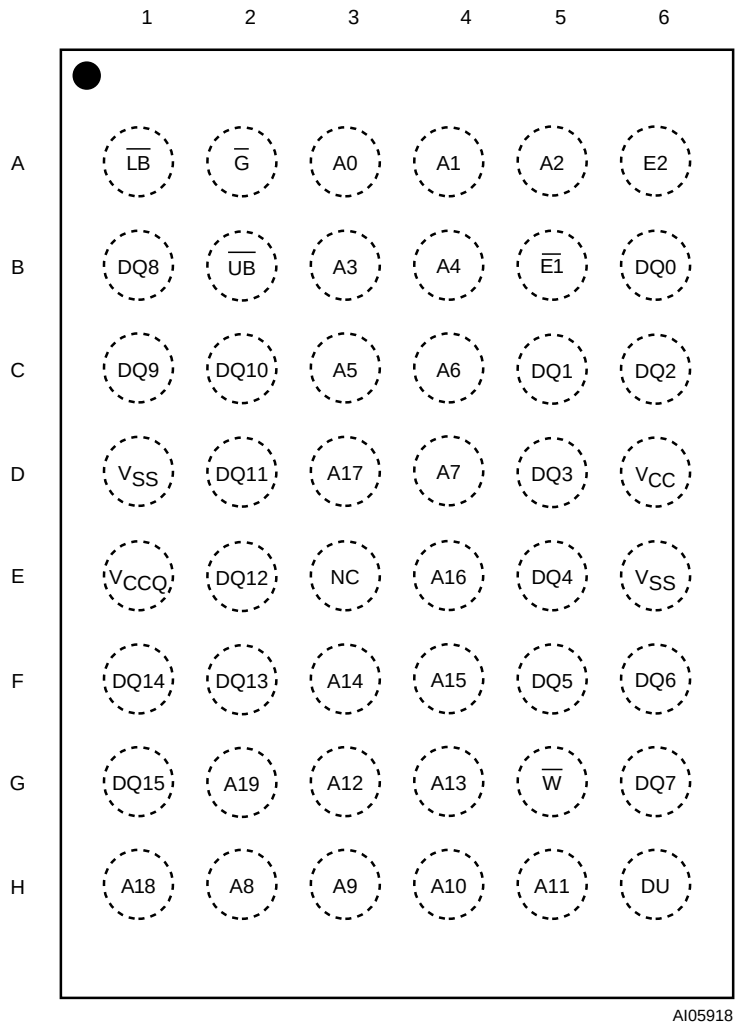
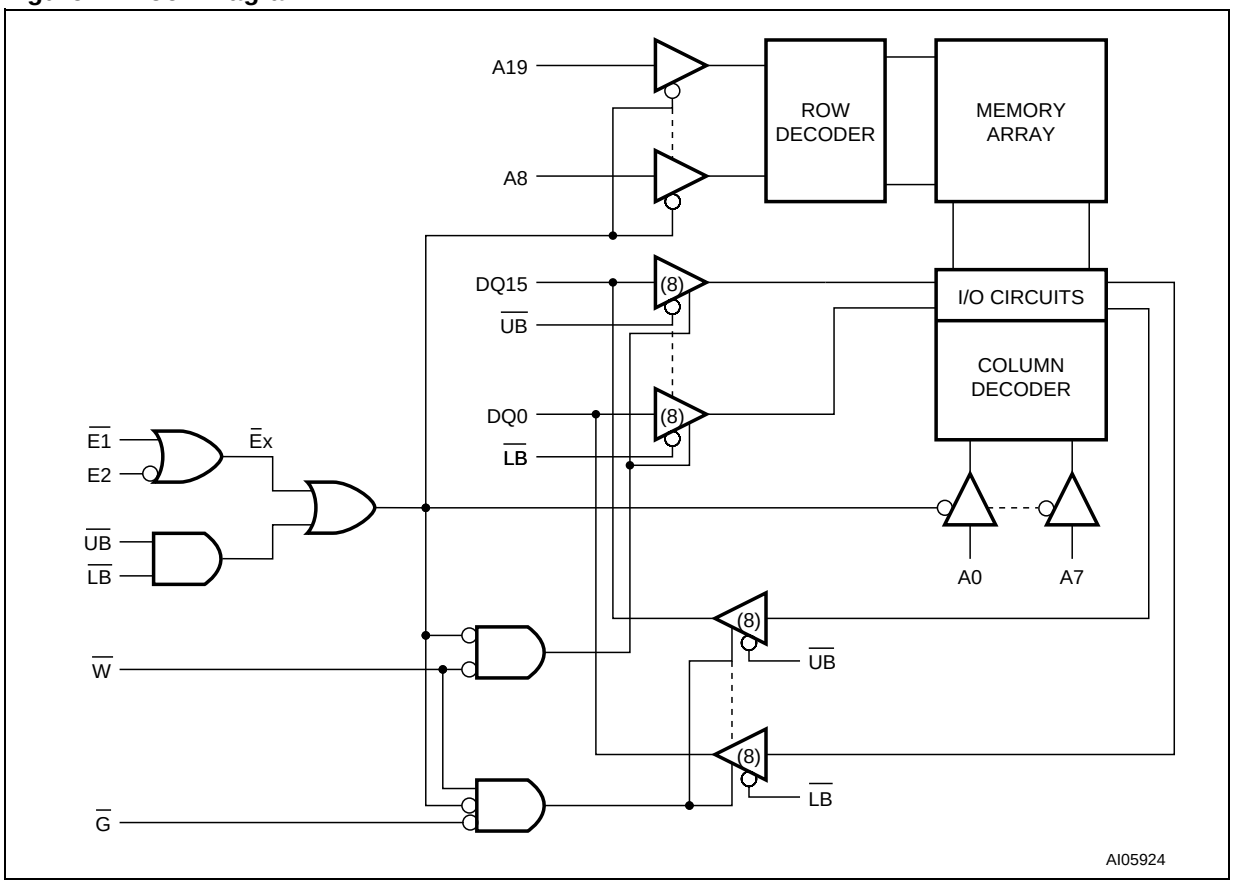


Figure 4. Block Diagram



MAXIMUM RATING

Stressing the device above the rating listed in the Absolute Maximum Ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for periods greater than 1 sec may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 2. Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
I_O (1)	Output Current	20	mA
P_D	Power Dissipation	1	W
T_A	Ambient Operating Temperature	–55 to 125	°C
T_{STG}	Storage Temperature	–65 to 150	°C
V_{CC}	Supply Voltage	–0.5 to 2.5	V
V_{CCQ}	I/O Supply Voltage	–0.5 to 2.5	V
V_{IO} (2)	Input or Output Voltage	–0.5 to V_{CCQ} +0.5	V

Note: 1. One output at time not to exceed 1 second duration.
2. Up to a maximum operating V_{CC} or V_{CCQ} of 1.95V only.

DC AND AC PARAMETERS

This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC Characteristic tables are derived from tests performed under the Measurement Conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 3. Operating and AC Measurement Conditions

Parameter		M68AR024D
V_{CC} Supply Voltage		1.65 to 1.95V
V_{CCQ} I/O Supply Voltage ($V_{CCQ} \le V_{CC}$)		1.5 to 1.95V
Ambient Operating Temperature	Range 1	0 to 70°C
	Range 6	–40 to 85°C
Load Capacitance (C_L)		30pF
Output Circuit Protection Resistance (R_1)		15.3kΩ
Load Resistance (R_2)		11.3kΩ
Input Rise and Fall Times		≤ 1ns/V
Input Pulse Voltages		0 to V_{CCQ}
Input and Output Timing Ref. Voltages		$V_{CCQ}/2$
Output Transition Timing Ref. Voltages		$V_{RL} = 0.3V_{CCQ}$; $V_{RH} = 0.7V_{CCQ}$

Figure 5. AC Measurement I/O Waveform

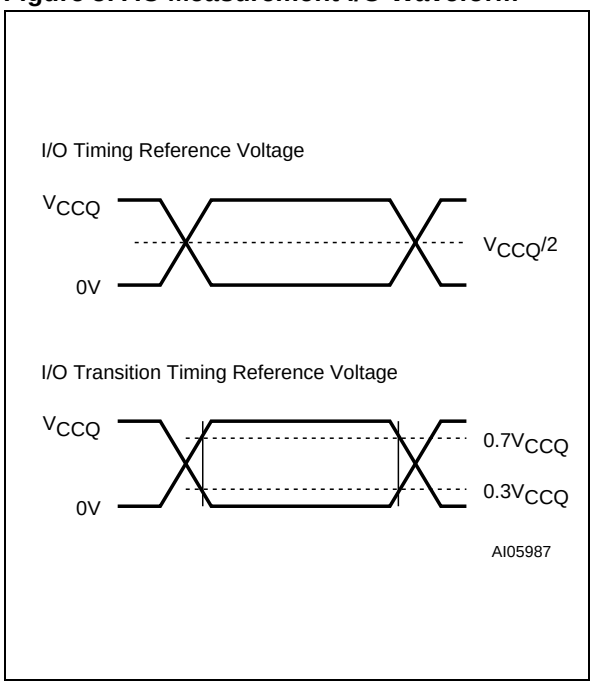


Figure 6. AC Measurement Load Circuit

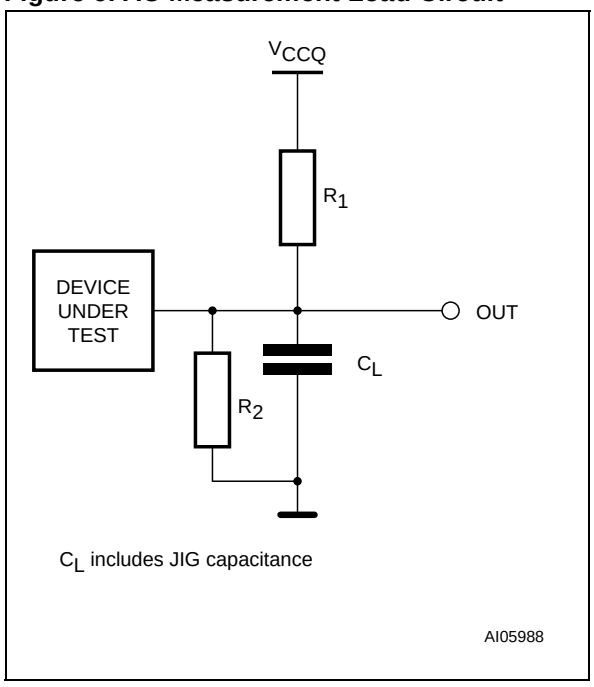


Table 4. Capacitance

Symbol	Parameter (1,2)	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance on all pins (except DQ)	V_{IN} = 0V		6	pF
C_{OUT} (3)	Output Capacitance	V_{OUT} = 0V		8	pF

Note: 1. Sampled only, not 100% tested.
2. At T_A = 25°C, f = 1MHz, V_{CC} = 1.8V.
3. Outputs deselected.

Table 5. DC Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{CC1} (1,2)	Operating Supply Current	V_{CC} = 1.95V, f = $1/t_{AVAV}$, I_{OUT} = 0mA		5	25	mA
I_{CC2} (3)	Operating Supply Current	V_{CC} = 1.95V, f = 1MHz, I_{OUT} = 0mA			3	mA
I_{LI}	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}	–1		1	µA
I_{LO} (4)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}	–1		1	µA
I_{SB}	Standby Supply Current CMOS	V_{CC} = 1.95V, $\overline{E1}$ ≥ V_{CCQ} –0.2V OR E2 ≤ 0.2V OR $\overline{UB}$, $\overline{LB}$ ≥ V_{CCQ} –0.2V, f = 0		1	15	µA
V_{IH}	Input High Voltage		V_{CCQ} – 0.4		V_{CCQ} + 0.3	V
V_{IL}	Input Low Voltage		–0.3		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –100µA	V_{CCQ} – 0.2			V
V_{OL}	Output Low Voltage	I_{OL} = 100µA			0.2	V

Note: 1. Average AC current, cycling at t_{AVAV} minimum.
2. $\overline{E1}$ = V_{IL}, E2 = V_{IH}, $\overline{UB}$ OR/AND $\overline{LB}$ = V_{IL}, V_{IN} = V_{IH} OR V_{IL}.
3. $\overline{E1}$ ≤ 0.2V or E2 ≥ V_{CCQ} –0.2V, $\overline{UB}$ OR/AND $\overline{LB}$ ≤ 0.2V, V_{IN} ≤ 0.2V or V_{IN} ≥ V_{CCQ} –0.2V.
4. Output disabled.

OPERATION

The M68AR024D has a Chip Enable power down feature which invokes an automatic standby mode whenever Chip Enable is de-asserted ($\overline{E1}$ = High) or Chip Select is asserted (E2 = Low), or $\overline{UB}$/$\overline{LB}$ are de-asserted ($\overline{UB}$/$\overline{LB}$ = High). An Output Enable ($\overline{G}$) signal provides a high speed tri-state control, allowing fast read/write cycles to be achieved with the common I/O data bus. Operational modes are determined by device control inputs $\overline{W}$, $\overline{E1}$, $\overline{LB}$ and $\overline{UB}$ as summarized in the Operating Modes table (see Table 6).

Table 6. Operating Modes

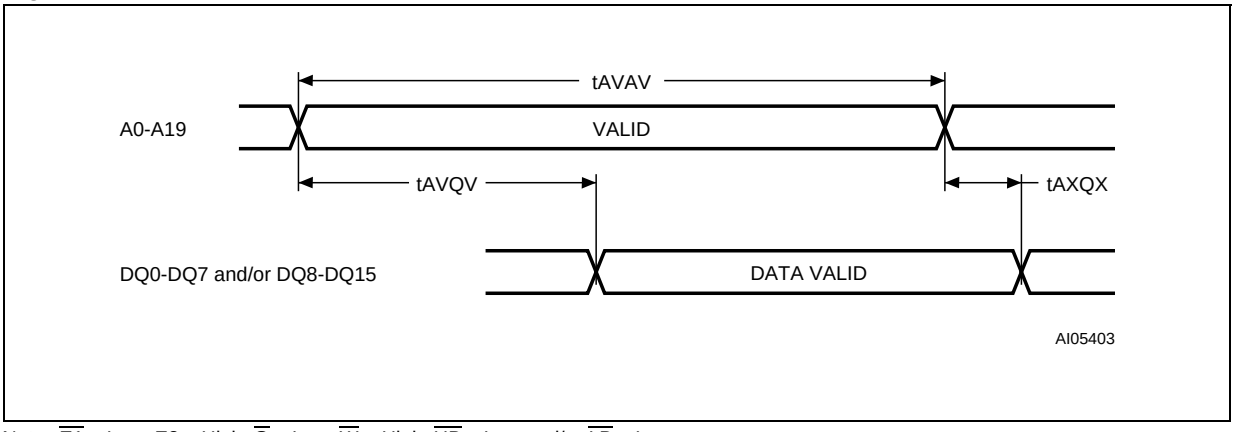
Operation	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$	$\overline{LB}$	$\overline{UB}$	DQ0-DQ7	DQ8-DQ15	Power
Deselected/Standby	V_{IH}	X	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
Deselected/Standby	X	V_{IL}	X	X	X	X	Hi-Z	Hi-Z	Standby (I_{SB})
Deselected/Standby	X	X	X	X	V_{IH}	V_{IH}	Hi-Z	Hi-Z	Standby (I_{SB})
Lower Byte Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IH}	Data Output	Hi-Z	Active (I_{CC})
Lower Byte Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IL}	V_{IH}	Data Input	Hi-Z	Active (I_{CC})
Output Disabled	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	Hi-Z	Hi-Z	Active (I_{CC})
Upper Byte Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IH}	V_{IL}	Hi-Z	Data Output	Active (I_{CC})
Upper Byte Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IH}	V_{IL}	Hi-Z	Data Input	Active (I_{CC})
Word Read	V_{IL}	V_{IH}	V_{IH}	V_{IL}	V_{IL}	V_{IL}	Data Output	Data Output	Active (I_{CC})
Word Write	V_{IL}	V_{IH}	V_{IL}	X	V_{IL}	V_{IL}	Data Input	Data Input	Active (I_{CC})

Note: 1. X = V_{IH} or V_{IL}.

Read Mode

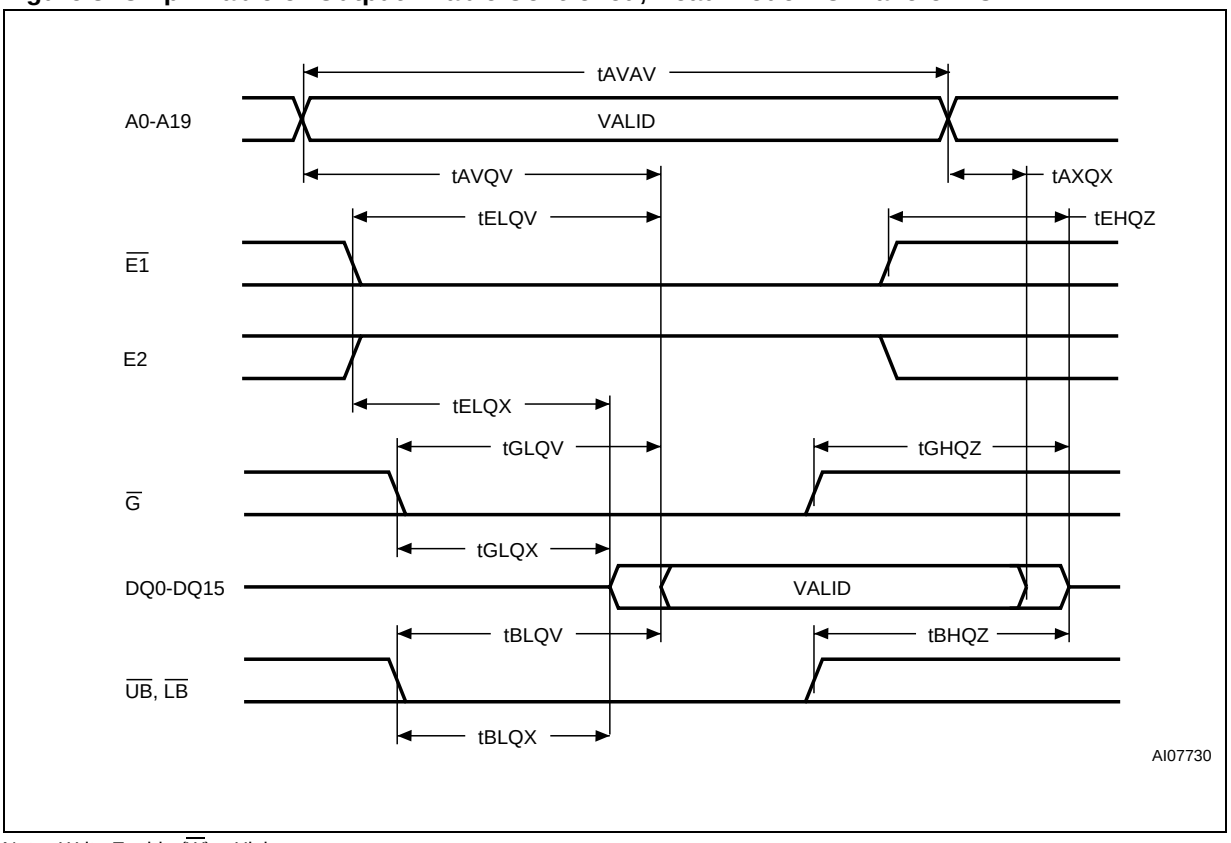
The M68AR024D, when Chip Select (E2) is High, is in the read mode whenever Write Enable ($\overline{W}$) is High with Output Enable ($\overline{G}$) Low, and Chip Enable ($\overline{E1}$) is asserted. This provides access to data from eight or sixteen, depending on the status of the signal $\overline{UB}$ and $\overline{LB}$, of the 16,777,216 locations in the static memory array, specified by the 20 address inputs. Valid data will be available at the eight or sixteen output pins within t_{AVQV} after the last stable address, providing $\overline{G}$ is Low and $\overline{E1}$ is Low. If Chip Enable or Output Enable access times are not met, data access will be measured from the limiting parameter (t_{ELQV}, t_{GLQV} or t_{BLQV}) rather than the address. Data out may be indeterminate at t_{ELQX}, t_{GLQX} and t_{BLQX}, but data lines will always be valid at t_{AVQV}

Figure 7. Address Controlled, Read Mode AC Waveforms



Note: $\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{W}$ = High, $\overline{UB}$ = Low and/or $\overline{LB}$ = Low.

Figure 8. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms



Note: Write Enable ($\overline{W}$) = High

Figure 9. Chip Enable or $\overline{UB}$/$\overline{LB}$ Controlled, Standby Mode AC Waveforms

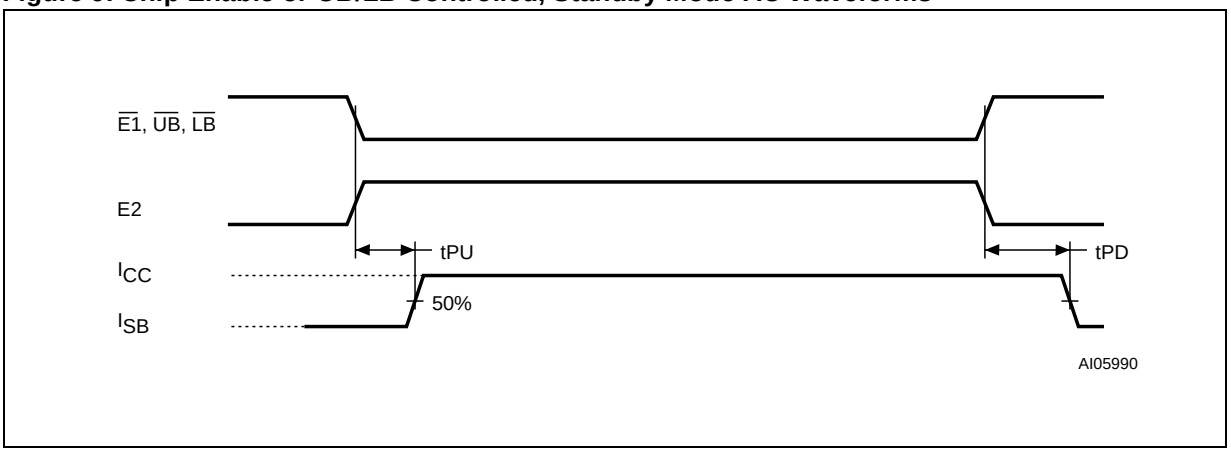


Table 7. Read and Standby Mode AC Characteristics

Symbol	Parameter	M68AR024D		Unit
			70	
t_{AVAV}	Read Cycle Time	Min	70	ns
t_{AVQV}	Address Valid to Output Valid	Max	70	ns
t_{AXQX} (1)	Data hold from address change	Min	5	ns
t_{BHQZ} (2, 3)	Upper/Lower Byte Enable High to Output Hi-Z	Max	25	ns
t_{BLQV}	Upper/Lower Byte Enable Low to Output Valid	Max	70	ns
t_{BLQX} (1)	Upper/Lower Byte Enable Low to Output Transition	Min	5	ns
t_{EHQZ} (2, 3)	Chip Enable High to Output Hi-Z	Max	25	ns
t_{ELQV}	Chip Enable Low to Output Valid	Max	70	ns
t_{ELQX} (1)	Chip Enable Low to Output Transition	Min	5	ns
t_{GHQZ} (2, 3)	Output Enable High to Output Hi-Z	Max	25	ns
t_{GLQV}	Output Enable Low to Output Valid	Max	35	ns
t_{GLQX} (1)	Output Enable Low to Output Transition	Min	5	ns
t_{PD} (4)	Chip Enable High to Power Down	Max	0	ns
t_{PU} (4)	Chip Enable Low to Power Up	Min	70	ns

Note: 1. Test conditions assume transition timing reference level = $0.3V_{CCQ}$ to $0.7V_{CCQ}$.
2. At any given temperature and voltage condition, t_{GHQZ} is less than t_{GLQX}, t_{BHQZ} is less than t_{BLQX} and t_{EHQZ} is less than t_{ELQX} for any given device.
3. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
4. Tested initially and after any design or process changes that may affect these parameters.

Write Mode

The M68AR024D, when Chip Select (E2) is High, is in the Write Mode whenever the $\overline{W}$ and $\overline{E1}$ are Low. Either the Chip Enable Input ($\overline{E1}$) or the Write Enable input ($\overline{W}$) must be de-asserted during Address transitions for subsequent write cycles. When $\overline{E1}$ or $\overline{W}$ is Low, and $\overline{UB}$ or $\overline{LB}$ is Low, write cycle begins on the $\overline{W}$ or $\overline{E1}$ falling edge. When $\overline{E1}$ and $\overline{W}$ are Low, and $\overline{UB}$ = $\overline{LB}$ = High, write cycle begins on the first falling edge of $\overline{UB}$ or $\overline{LB}$. Therefore, address setup time is referenced to Write Enable, Chip Enables and $\overline{UB}$/$\overline{LB}$ as t_{AVWL}, t_{AVEL} and t_{AVBL} respectively, and is determined by the latter occurring falling edge.

The Write cycle can be terminated by the earlier rising edge of $\overline{E1}$, $\overline{W}$, $\overline{UB}$ and $\overline{LB}$.

If the Output is enabled ($\overline{E1}$ = Low, E2 = High, $\overline{G}$ = Low, $\overline{LB}$ or $\overline{UB}$ = Low), then $\overline{W}$ will return the outputs to high impedance within t_{WLQZ} of its falling edge. Care must be taken to avoid bus contention in this type of operation. Data input must be valid for t_{DVWH} before the rising edge of Write Enable, or for t_{DVEH} before the rising edge of $\overline{E1}$ or for t_{DVBH} before the rising edge of $\overline{UB}$/$\overline{LB}$, whichever occurs first, and remain valid for t_{WHDX}, t_{EHDX} and t_{BHDX} respectively.

Figure 10. Write Enable Controlled, Write AC Waveforms

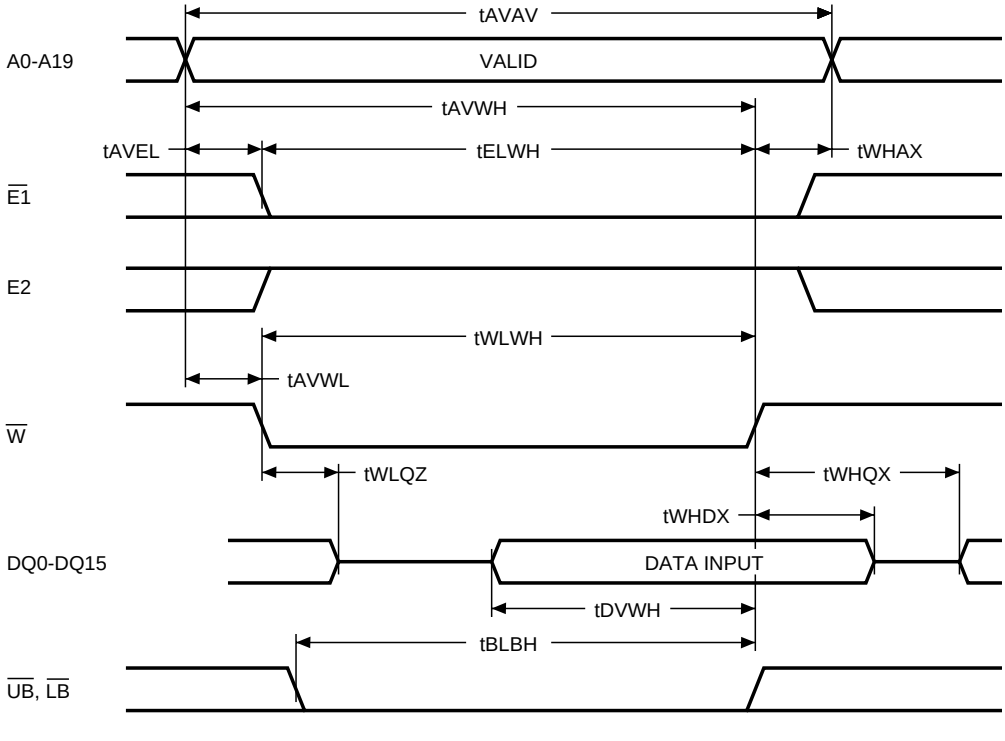


Figure 11. Chip Enable $\overline{E1}$ Controlled, Write AC Waveforms

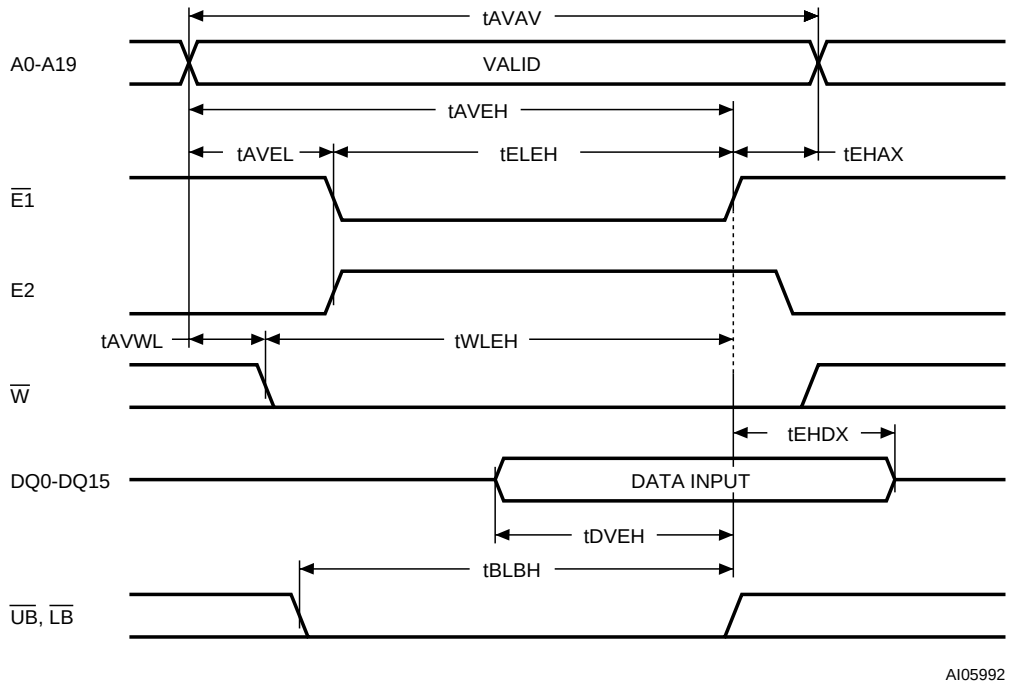
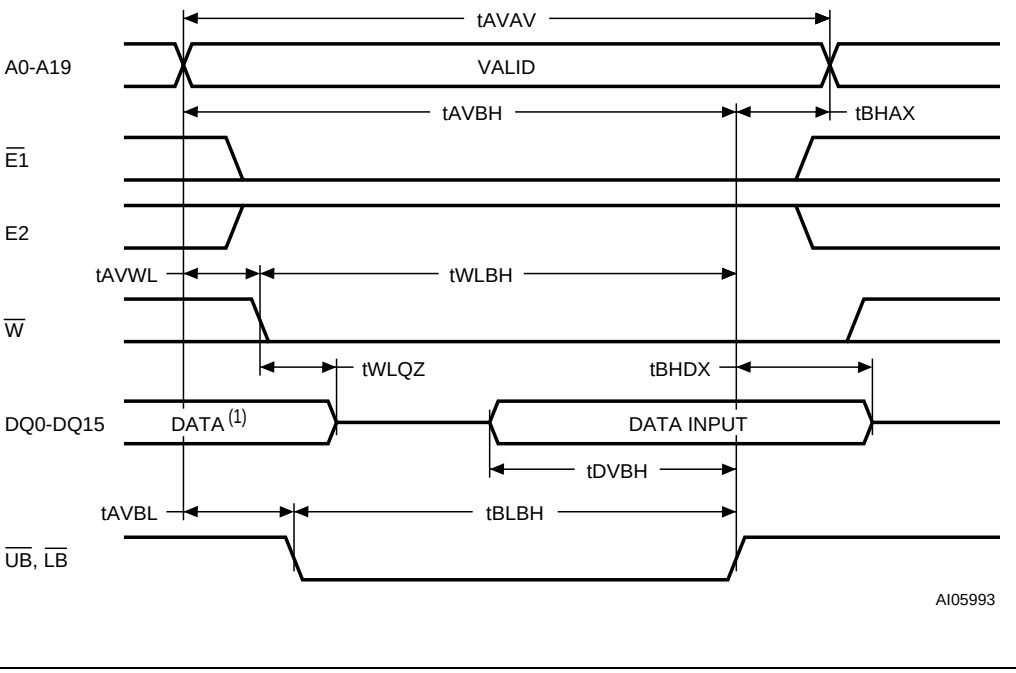


Figure 12. $\overline{UB}$/$\overline{LB}$ Controlled, Write AC Waveforms



Note: 1. During this period DQ0-DQ15 are in output state and input signals should not be applied.

Table 8. Write Mode AC Characteristics

Symbol	Parameter	M68AR024D		Unit
			70	
t_{AVAV}	Write Cycle Time	Min	70	ns
t_{AVBH}	Address Valid to $\overline{LB}$, $\overline{UB}$ High	Min	60	ns
t_{AVBL}	Addess Valid to $\overline{LB}$, $\overline{UB}$ Low	Min	0	ns
t_{AVEH}	Address Valid to Chip Enable High	Min	60	ns
t_{AVEL}	Address valid to Chip Enable Low	Min	0	ns
t_{AVWH}	Address Valid to Write Enable High	Min	60	ns
t_{AVWL}	Address Valid to Write Enable Low	Min	0	ns
t_{BHAX}	$\overline{LB}$, $\overline{UB}$ High to Address Transition	Min	0	ns
t_{BHDX}	$\overline{LB}$, $\overline{UB}$ High to Input Transition	Min	0	ns
t_{BLBH}	$\overline{LB}$, $\overline{UB}$ Low to $\overline{LB}$, $\overline{UB}$ High	Min	60	ns
t_{BLEH}	$\overline{LB}$, $\overline{UB}$ Low to Chip Enable High	Min	60	ns
t_{BLWH}	$\overline{LB}$, $\overline{UB}$ Low to Write Enable High	Min	60	ns
t_{DVBH}	Input Valid to $\overline{LB}$, $\overline{UB}$ High	Min	30	ns
t_{DVEH}	Input Valid to Chip Enable High	Min	30	ns
t_{DVWH}	Input Valid to Write Enable High	Min	30	ns
t_{EHAX}	Chip Enable High to Address Transition	Min	0	ns
t_{EHDX}	Chip enable High to Input Transition	Min	0	ns
t_{ELBH}	Chip Enable Low to $\overline{LB}$, $\overline{UB}$ High	Min	60	ns
t_{ELEH}	Chip Enable Low to Chip Enable High	Min	60	ns
t_{ELWH}	Chip Enable Low to Write Enable High	Min	60	ns
t_{WHAX}	Write Enable High to Address Transition	Min	0	ns
t_{WHDX}	Write Enable High to Input Transition	Min	0	ns
t_{WHQX} (1)	Write Enable High to Output Transition	Min	5	ns
t_{WLBH}	Write Enable Low to $\overline{LB}$, $\overline{UB}$ High	Min	60	ns
t_{WLEH}	Write Enable Low to Chip Enable High	Min	60	ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z	Max	20	ns
t_{WLWH}	Write Enable Low to Write Enable High	Min	50	ns

Note: 1. At any given temperature and voltage condition, t_{WHQZ} is less than t_{WLQX} for any given device.
2. These parameters are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.

Figure 13. $\overline{E1}$ Controlled, Low V_{CC} Data Retention AC Waveforms

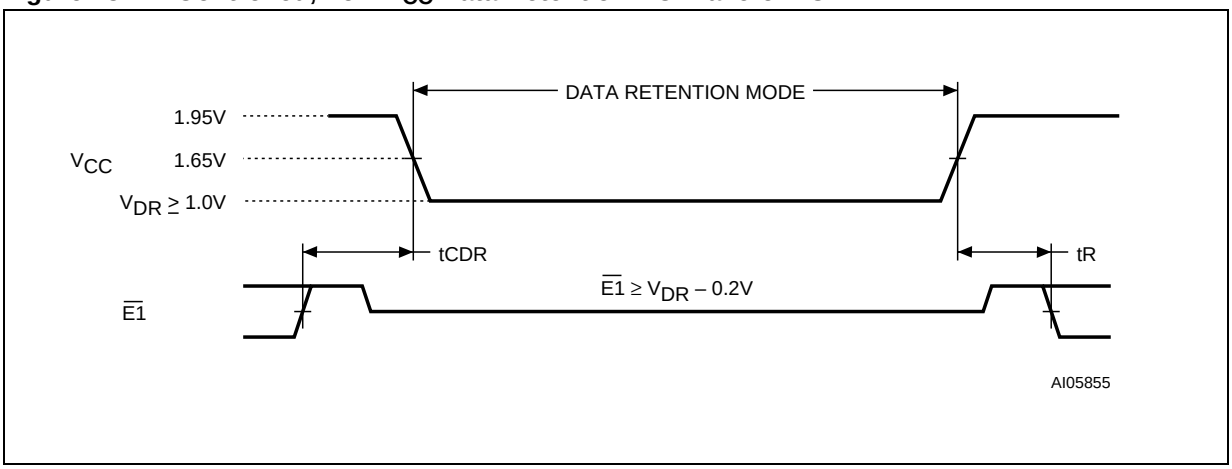


Figure 14. E2 Controlled, Low V_{CC} Data Retention AC Waveforms

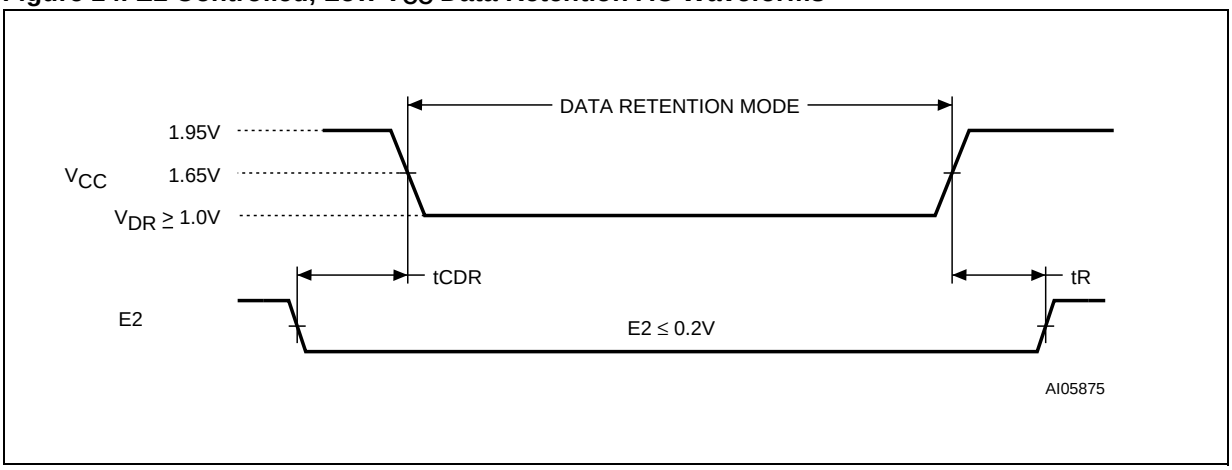


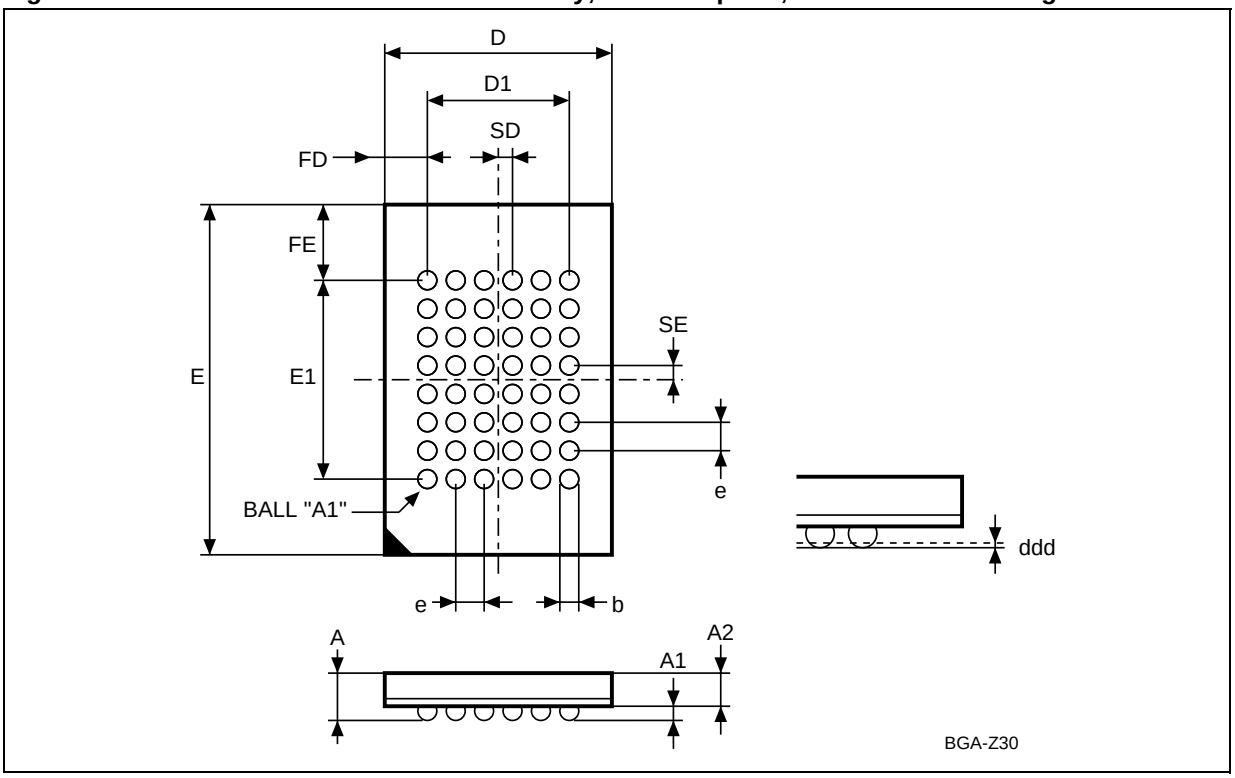
Table 9. Low V_{CC} Data Retention Characteristics

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
I_{CCDR} (1)	Supply Current (Data Retention)	V_{CC} = 1.0V, $\overline{E1} \geq V_{CCQ}$ –0.2V OR $E2 \leq 0.2V$ OR $\overline{UB}, \overline{LB} \geq V_{CCQ}$ –0.2V, f = 0		0.5	5	µA
t_{CDR} (2)	Chip deselected to Data Retention Time		0			ns
t_R (2)	Operation Recovery Time		t_{AVAV}			ns
V_{DR} (1)	Supply Voltage (Data Retention)	$\overline{E1} \geq V_{CCQ}$ –0.2V OR $E2 \leq 0.2V$ OR $\overline{UB}, \overline{LB} \geq V_{CCQ}$ –0.2V, f = 0	1.0			V

Note: 1. All other Inputs at $V_{IH} \geq V_{CCQ}$ –0.2V or $V_{IL} \leq 0.2V$.
2. Tested initially and after any design or process changes that may affect these parameters. t_{AVAV} is Read cycle time.
3. No input may exceed V_{CC} +0.2V.

PACKAGE MECHANICAL

Figure 15. TFBGA48 6.5x10mm - 6x8 ball array, 0.75 mm pitch, Bottom View Package Outline

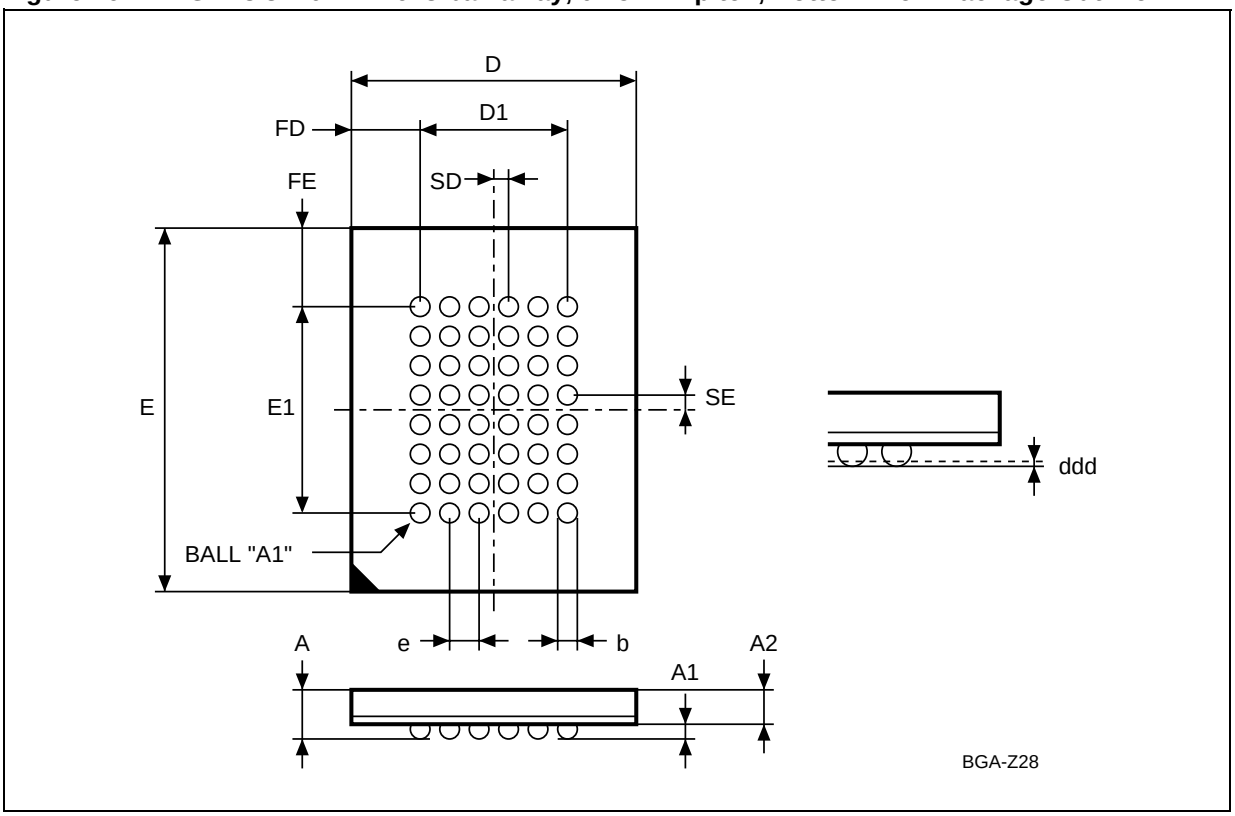


Note: Drawing is not to scale.

Table 10. TFBGA48 6.5x10mm - 6x8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.300	0.400		0.0118	0.0157
A2	0.790			0.0311		
b		0.350	0.450		0.0138	0.0177
D	6.500	6.400	6.600	0.2559	0.2520	0.2598
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	0.875	–	–	0.0344	–	–
FE	3.125	–	–	0.1230	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

Figure 16. TFBGA48 8x10mm - 6x8 ball array, 0.75 mm pitch, Bottom View Package Outline



Note: Drawing is not to scale.

Table 11. TFBGA48 8x10mm - 6x8 ball array, 0.75 mm pitch, Package Mechanical Data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.200			0.0472
A1		0.260			0.0102	
A2			0.900			0.0354
b		0.350	0.450		0.0138	0.0177
D	8.000	7.900	8.100	0.3150	0.3110	0.3189
D1	3.750	–	–	0.1476	–	–
ddd			0.100			0.0039
E	10.000	9.900	10.100	0.3937	0.3898	0.3976
E1	5.250	–	–	0.2067	–	–
e	0.750	–	–	0.0295	–	–
FD	2.125	–	–	0.0837	–	–
FE	2.375	–	–	0.0935	–	–
SD	0.375	–	–	0.0148	–	–
SE	0.375	–	–	0.0148	–	–

PART NUMBERING

Table 12. Ordering Information Scheme

Example: M68AR016 D N 70 ZB 6 T

Device Type
M68

Mode
A = Asynchronous

Operating Voltage
R = 1.65 to 1.95V

Array Organization
024 = 16 Mbit (1M x16)

Option 1
D = 2 Chip Enable; Write and Standby from $\overline{UB}$ and $\overline{LB}$

Option 2
N = N-Die

Speed Class
70 = 70 ns

Package
ZH = TFBGA48: 0.75 mm pitch (8x10mm) (1)
ZB = TFBGA48: 0.75 mm pitch (6.5x10mm)

Operative Temperature
1 = 0 to 70°C
6 = –40 to 85 °C

Shipping
T = Tape & Reel Packing

Note: 1. This package is available for Engineering Samples only.

REVISION HISTORY

Table 13. Document Revision History

Date	Version	Revision Details
July 2001	-01	First Issue
24-Oct-2001	-02	Table of Contents added Block Diagram added, Data Retention AC Waveforms clarified Package Mechanical Data and Drawing added
07-Nov-2001	-03	Voltage range extended up to 2.2V
19-Feb-2002	-04	Document totally revised
12-Mar-2002	-05	Features Summary clarified Tables 2, 3, 4, 5, 6, 7, 8 and 9 clarified Figures 8, 10, 11 and 12 clarified
20-Mar-2002	-06	TFBGA 6.5x10 package added
19-Apr-2002	-07	Chip Enable Controlled, Low V_{CC} Data Retention AC Waveforms clarified (Figures 13 and 14)
02-Oct-2002	7.1	Revision numbering modified: a minor revision will be indicated by incrementing the digit after the dot, and a major revision, by incrementing the digit before the dot (revision version 07 equals 7.0). Part number changed.
04-Oct-2002	7.2	Document status changed from Target Specification to Preliminary Data.
09-Oct-2002	7.3	Part number modified.

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