# iC-JX

16-FOLD 24 V HIGH-SIDE DRIVER WITH µC INTERFACE



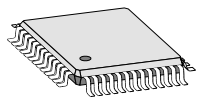
## FEATURES

- 16 bidirectional input/output stages at 24 V
- Input/output mode programmable in 4-channel blocks
- Short-circuit-proof high-side drivers with diagnosis function
- 500 mA pulse and 150 mA permanent load driving capability
- Active flyback circuit
- Load diagnosis for driver current, output voltage and impedance (cable fractures, resistance and short circuits)
- 10-bit A/D converter for the generation of diagnosis measurement values
- Safety devices (voltage monitor, temperature sensor with warning and shutdown features, power output enable pin)
- Programmable interrupt generation with an events storage facility
- Variable digital filters for the debouncing of I/O signals
- Fast 8-bit parallel or serial SPI™-compatible µC interface permits use in buses
- Logic supply from 3 V upwards

## APPLICATIONS

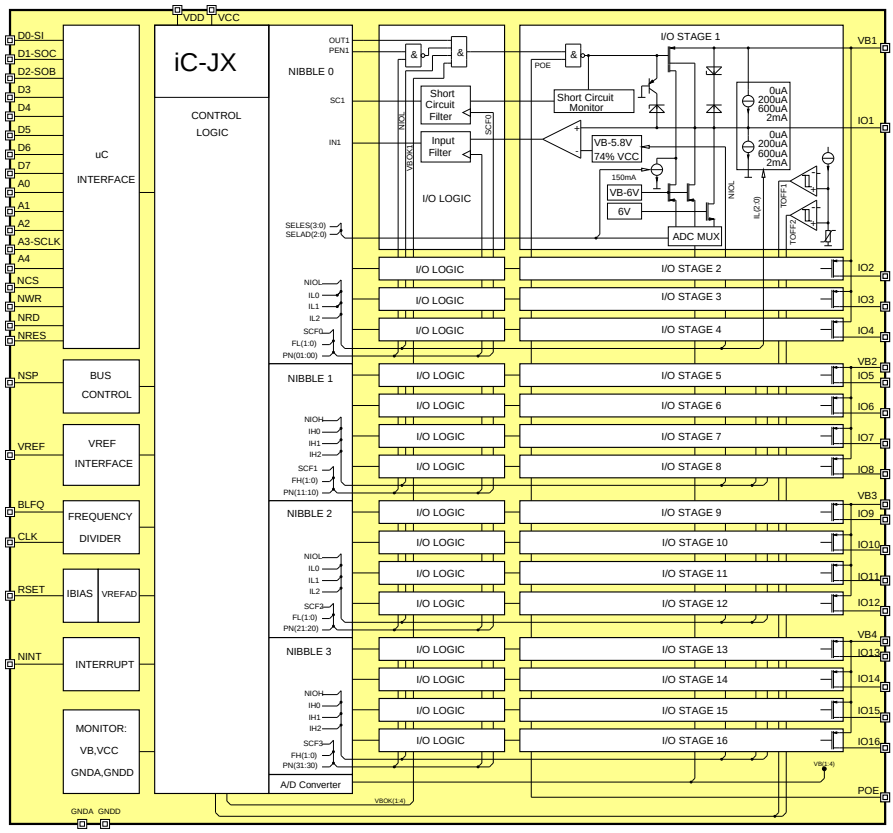
- Industrial 24 V applications
- Lamp switches with diagnostic features
- Inductive load driver circuits for relays and valves etc.

## PACKAGES



MQFP52

## BLOCK DIAGRAM



## DESCRIPTION

iC-JX is a bidirectional I/O device with 4x4 high-side driver stages. The input or output function can be separately selected for blocks or nibbles of four I/O stages.

Each block can also be individually programmed with various filtering options for the debouncing of I/O pin signals or overcurrent messages, with current sources for the defining of levels at the inputs (low-side sources) or for load diagnosis at the outputs (high-side sources) and also with a flash pulse function.

To enable communication with the controller the device includes a parallel interface (with eight data, five address and three control pins) and also an SPI-compatible serial interface (with one pin for the clock, chip selection, data input and data output respectively). The type of interface is selected via pin NSP.

I/O stages with an input function can record logic levels at 24 V where a programmable pull-down current source (of up to 2 mA) either defines the level for open inputs or supplies a bias current for external switch contacts. Connecting safety circuits with integrated serial/parallel resistors to the device also enables leakage currents and short circuits to be pinpointed. The contact status can be read out using the microcontroller interface.

I/O stages with an output function drive various loads (such as lamps, cables or relays, for example) to a common ground with 150 mA of permanent current or 500 mA in pulse operation. Spikes and flyback currents are discharged by the integrated flyback circuits.

For synchronous flash display, as used for indicator lamps in plugboards, for example, a flash pulse enable can be individually set for each output to offload the controller. A common inhibiting input (POE) permits the global shutdown of all outputs and can be operated by an autonomous watchdog circuit.

All output stages are short-circuit-proof and protected against thermal destruction in the event of extreme power dissipation. Each stage has its own temperature sensor which is evaluated in two stages and generates interrupt messages for the controller. The latter is warned before the device is forcibly shutdown. A short circuit also triggers an interrupt message; the current status here can be read out by the controller.

For the purpose of load diagnosis a programmable pull-up current source (of up to 2 mA) can be used to determine an initial load breakage or open loop (caused by a fractured cable, for example) before an output is switched on. The I/O pin status can always be read back via comparators. A load current measurement circuit then permits the load to be assessed; failed valves and faulty or wrongly implemented indicator lamps can be verified in this way. In addition, the analog measurement of voltage at the I/O pins allows safety switches to be analyzed with reference to ground, here without the driver function.

All analog measurements for the load current (per stage), for the I/O pin voltage (per stage, either referenced to Ground or VB), for the driver supply (all VB pins) , for the internal voltage reference (VBG) and for the chip temperature are made available to the microcontroller as digital measurements by an integrated A/D converter which has 10 bits of resolution.

An interrupt pipeline which limits the loss of interrupts allows reliable processing of interrupts by the microcontroller. Registers provide information as to current events; messages can be individually enabled for all available interrupt sources.

iC-JX monitors all supply voltages and also the GNDD-GNDA connection to ground.

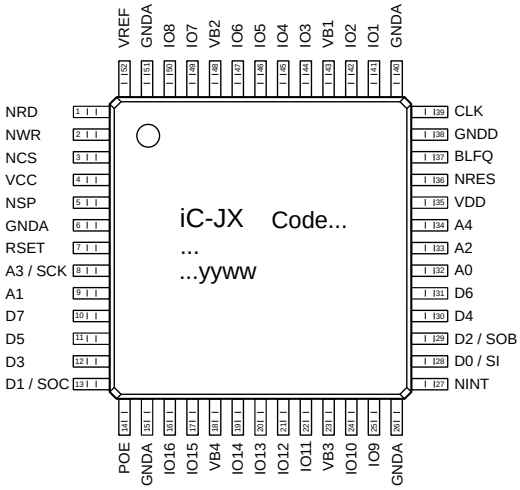
Monitored separately, undervoltage in the range of 2.5V at analog supply VCC or even short disruption of digital supply VDD causes all registers to be reset and the output stages to be shutdown.
Undervoltage at 24 V driver supply VB triggers a shutdown of the output stages without deleting the contents of the registers.

Diodes protect all inputs and outputs against destruction by ESD. iC-JX is also immune to burst transients according to IEC 1000-4-4 (4 kV; previously IEC 801-4).

## PACKAGES MQFP52 to JEDEC Standard

### PIN CONFIGURATION
**MQFP52, pitch 0.65 mm**

Orientation of the package label (*JX code...*) is subject to change.




### PIN FUNCTIONS

| No. | Name | Function |
|---|---|---|
| 1 | NRD | Not Read Enable |
| 2 | NWR | Not Write Enable |
| 3 | NCS | Not Chip Select |
| 4 | VCC | Supply Voltage (analog, 3...5.5 V) |
| 5 | NSP | Not Serial / Parallel (Mode) |
| 6 | GNDA | Ground (analog) |
| 7 | RSET | Resistor Setting (10 kΩ optional) |
| 8 | A3 | Adress Bus |
| 9 | A1 | Adress Bus |
| 10 | D7 | Data Bus |
| 11 | D5 | Data Bus |
| 12 | D3 | Data Bus |
| 13 | D1 | Data Bus |
| 14 | POE | Power Output Enable |
| 15 | GNDA | Ground (analog) |
| 16 | IO16 | I/O Stage |
| 17 | IO15 | I/O Stage |
| 18 | VB4 | Supply Voltage for I/O Stages 13...16 |
| 19 | IO14 | I/O Stage |
| 20 | IO13 | I/O Stage |
| 21 | IO12 | I/O Stage |

### PIN FUNCTIONS

| No. | Name | Function |
|---|---|---|
| 22 | IO11 | I/O Stage |
| 23 | VB3 | Supply Voltage for I/O Stages 9...12 |
| 24 | IO10 | I/O Stage |
| 25 | IO9 | I/O Stage |
| 26 | GNDA | Ground (analog) |
| 27 | NINT | Not Interrupt |
| 28 | D0 | Data Bus |
| 29 | D2 | Data Bus |
| 30 | D4 | Data Bus |
| 31 | D6 | Data Bus |
| 32 | A0 | Adress Bus |
| 33 | A2 | Adress Bus |
| 34 | A4 | Adress Bus |
| 35 | VDD | Supply Voltage (logic, 3...5.5 V) |
| 36 | NRES | Not Reset |
| 37 | BLFQ | Blink Frequency |
| 38 | GNDD | Ground (logic) |
| 39 | CLK | Clock (optional) |
| 40 | GNDA | Ground (analog) |
| 41 | IO1 | I/O Stage |
| 42 | IO2 | I/O Stage |
| 43 | VB1 | Supply Voltage for I/O Stages 1...4 |
| 44 | IO3 | I/O Stage |
| 45 | IO4 | I/O Stage |
| 46 | IO5 | I/O Stage |
| 47 | IO6 | I/O Stage |
| 48 | VB2 | Supply Voltage for I/O Stages 5...8 |
| 49 | IO7 | I/O Stage |
| 50 | IO8 | I/O Stage |
| 51 | GNDA | Ground (analog) |
| 52 | VREF | External Voltage Reference (optional) |

*Additional Pin Function in SPI Mode (NSP = low)*

| | | |
|---|---|---|
| 3 | NCS | Not Chip Select |
| 8 | SCK | Serial Clock |
| 9 | A1 | Device ID Bit 1 |
| 13 | SOC | Serial Out Chain |
| 28 | SI | Serial In |
| 29 | SOB | Serias Out Bus |
| 32 | A0 | Device ID Bit 0 |
| 33 | A2 | Select Chain / Bus |
| 34 | A4 | Enable Interrupt Report SOC/SOB |

Separate supply voltages at VB1..4 are possible. All GNDA pins must be connected up externally. GNDA must be connected to GNDD externally when just one voltage supply is available. VCC and VDD can be powered either mutually or separately.

## ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed. Absolute Maximum Ratings are no Operating Conditions. Integrated circuits with system interfaces, e.g. via cable accessible pins (I/O pins, line drivers) are per principle endangered by injected interferences, which may compromise the function or durability. The robustness of the devices has to be verified by the user during system development with regards to applying standards and ensured where necessary by additional protective circuitry. By the manufacturer suggested protective circuitry is for information only and given without responsibility and has to be verified within the actual system with respect to actual interferences.
(Legend: x = 1..16, y = 1..4)

| Item No. | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| G001 | VCC, VDD | Supply Voltage | | -0.3 | 6 | V |
| G002 | VBy | Driver Supply Voltage | | -0.3 | 40 | V |
| G003 | V(IOx) | Voltages at IO1...16 | IOx = off; see additional remark [1] | -10 | 40 | V |
| G004 | Idc(IOx) | Current in IO1...16 | see Figure 1 | -500 | 150 | mA |
| G005 | Ipk(IOx) | Pulse current in IO1...16 | IOx = hi, $\tau$ = 2 ms, T $\leq$ 2 s<br>see Figure 2 | -1.0 | | A |
| G006 | Imax() | Current in VCC, VDD | | -100 | 100 | mA |
| G007 | Imax(VBy) | Current in VB1...4 | | -8 | 8 | A |
| G008 | Ic() | Current in NCS, NWR, NRD, A0...4, D0...7, NRES, CLK, BLFQ, POE, NSP, RSET, VREF | D0...7 with input function | -20 | 20 | mA |
| G009 | I() | Current in D0...7, NINT, | D0...7 with output function | -25 | 25 | mA |
| G010 | Ilu() | Pulse current in NCS, NWR, NRD, A0...4, D0...7, NRES, CLK, BLFQ, NINT, NSP, POE, IO1...16, RSET, VREF (latch up test) | Pulse width < 10 µs,<br>all inputs / outputs open | -100 | 100 | mA |
| G011 | Vd() | ESD-voltage, all pins | HBM 100 pF discharged over 1.5 kΩ | | 2 | kV |
| G012 | Vb() | Burst transients at IO1...16 | after IEC 1000-4-4 | | 4 | kV |
| G013 | Tj | Chip temperature | | -40 | 150 | °C |
| G014 | Ts | Storage temperature | | -40 | 150 | °C |

[1] If the voltage supplies can not be guaranteed to be present at the time signals appear at the pins IO1..IO16, additional diodes or sufficient current limiting ohmic resistors have to be connected in series to the IO-pins to prevent reverse back biasing of the device.

## THERMAL DATA

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, all inputs on defined logic states (high or low)

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| T01 | Ta | Ambient temperature | extended temperature range on request | -40 | | 85 | °C |
| T02 | Rthja | Thermal resistance chip/ambient | package mounted on PCB | | 55 | | K/W |

All voltages are referenced to ground unless otherwise stated.
All currents flowing into the device pins are positive; all currents flowing out of the device pins are negative.

## ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **General** | | | | | | | |
| 001 | VCC | Permissible Supply Voltage VCC | | 3 | | 5.5 | V |
| 002 | I(VCC) | Supply Current in VCC | | | 10 | 20 | mA |
| 003 | I(VCC) | Supply Current in VCC | no supply voltage VBy | | | 30 | mA |
| 004 | VDD | Permissible Supply Voltage VDD | | 3 | | 5.5 | V |
| 005 | I(VDD) | Supply Current in VDD (static) | all logic inputs lo = 0 V or hi=VDD | | 3 | 6 | mA |
| 006 | I(VDD) | Supply Current in VDD (dynamic) | continuous reading cycle all 200ns, data word '00' and 'FF' is alternating read, CL(D0... 7) = 200 pF | | | 30 | mA |
| 007 | I(VDD) | Supply Current in VDD | all logic inputs lo=0.8V | | 3 | | mA |
| 008 | I(VDD) | Supply Current in VDD | all logic inputs hi=2.0V | | 5 | | mA |
| 009 | VBy | Permissible Supply Voltage VB1...4 (operating range) | | 12 | | 36 | V |
| 010 | I(VBy) | Supply Current in VB1...4 | POE = hi, IOx = hi, unbelastet | | 7 | 20 | mA |
| 011 | I(VBy) | Supply Current in VB1...4 | IOx = off | | 5 | 10 | mA |
| 012 | Vc()lo | ESD Clamp Voltage lo at VCC, VDD, VB1...4, RSET, VREF | I() = -10 mA | -1.4 | | -0.3 | V |
| 013 | Vc()hi | ESD Clamp Voltage hi at VCC, VDD | I() = 10 mA | 6 | | | V |
| 014 | Vc()hi | ESD Clamp Voltage hi at VB1...4 | I() = 10 mA | 30 | | 55 | V |
| 015 | Vc()lo | ESD Clamp Voltage lo at IO1...16 | I() = 10 mA, IOx = off | -25 | | -19 | V |
| 016 | Vc()lo | ESD Clamp Voltage hi at IO1...16 | I() = 10 mA | 30 | | 55 | V |
| 017 | Vc()hi | ESD Clamp Voltage hi at NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NINT, POE, NSP | Vc()hi = V() - VDD, D0...7 as input, I() = 10 mA | 0.4 | | 1.5 | V |
| 018 | Vc()lo | ESD Clamp Voltage lo at NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NINT, POE, NSP | D0...7 as input, I() = -10 mA | -1.5 | | -0.4 | V |
| 019 | Ifl(IOx) | Leakage Current of I/O Pins (x=1..16) beyond operating conditions | VCC = 0 V and VDD = 0 V, VBy = 2..30 V) | -0.2 | | | mA |
| **I/O Stages: High-Side Driver IO1...16** | | | | | | | |
| 101 | Vs()hi | Saturation Voltage hi | Vs()hi = VBy - V(IOx), I(IOx) = -15 mA; see Fig. 1 | | | 0.2 | V |
| 102 | Vs()hi | Saturation Voltage hi | Vs()hi = VBy - V(IOx), I(IOx) = -150 mA; see Fig. 1 | | | 0.6 | V |
| 103 | Vs()hi | Saturation Voltage hi for pulse load | Vs()hi = VBy -V(IOx), I(IOx)= -500 mA, $\tau$ = 2 ms, T $\leq$ 2 s; see Fig. 2 | | | 2 | V |
| 104 | Isc()hi | Overcurrent Cut-off | V(IOx) = 0 .. VBy - 3 V | -1.6 | | -0.51 | A |
| 105 | It()scs | Threshold Current for Overcurrent Message | | -1.2 | | -0.51 | A |
| 106 | Vc()lo | Free-wheeling Clamp Voltage low | I(IOx) = -150 mA | -18 | | -12 | V |
| 107 | SR()hi | Slew Rate hi | CL = 0 ... 100 pF, I(IOx) = -150mA | 5 | | 17 | V/µs |

## ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| 108 | SR()lo | Slew Rate lo | CL = 0 ... 100 pF, I(IOx) = -150mA | 5 | | 17 | V/µs |
| 109 | tplh() | Propagation Delay until IOx: lo → hi | V(IOx) > V0(IOx) + 1 V | | | 6 | µs |
| 110 | tphl() | Propagation Delay until IOx = off | V(IOx) < 80 % (VBy - Vs(IOx)hi) | | | 6 | µs |
| **I/O Stages: Current Sources at IO1...16** | | | | | | | |
| 201 | Ipd() | Pull-down Current Source (200 µA) | V(IOx) = 3 V .. VBy; | 160 | 200 | 240 | µA |
| 202 | Ipd() | Pull-down Current Source (600 µA) | V(IOx) = 3 V .. VBy; | 510 | 600 | 690 | µA |
| 203 | Ipd() | Pull-down Current Source (2 mA) | V(IOx) = 3 V .. VBy; | 1.6 | 2 | 2.4 | mA |
| 204 | Ipu() | Pull-up Current Source (200 µA) | IOx = off, V(IOx) = 0 V .. VBy - 3 V | 150 | 200 | 250 | µA |
| 205 | Ipu() | Pull-up Current Source (600 µA) | IOx = off, V(IOx) = 0 V .. VBy - 3 V | 510 | 600 | 690 | µA |
| 206 | Ipu() | Pull-up Current Source (2 mA) | IOx = off, V(IOx) = 0 V ..VBy - 3 V | 1.6 | 2 | 2.4 | mA |
| 207 | tp()Ion | Turn-on Time Current Source aktiv | I(IOx) > 90 % Ipd(IOx) resp. I(IOx) > 90 %Ipu(IOx) | | | 5 | µs |
| 208 | tp()Ioff | Turn-off Time Current Source inaktiv | I(IOx) < 10 % Ipd(IOx) resp. I(IOx) < 10 % Ipu(IOx) | | | 5 | µs |
| 209 | Ifu() | Leakage Current | IOx with Input Function or Output Function with IOx = off; VBy = 30 V IL2 = IH2 = IL1 = IH1 = IL0 = IH0 = 0, V(IOx) = 0V .. VBy | -50 | | 70 | µA |
| 210 | Irb() | Leakage Current | Conditions see Item-No. 209; V(IOx) = -10 V .. 0 V, VBy = 30 V | -1.5 | | | mA |
| 211 | Irb() | Leakage Current | Conditions see Item-No. 209; only Input Function V(IOx) = VBy ... VBy + 0.3 V | | | 250 | µA |
| 212 | Irb() | Leakage Current | Conditions see Item-No. 209; only Input Function V(IOx) = VBy + 0.3V ... VBy + 2V | | | 1 | mA |
| 213 | Irb() | Leakage Current | no supply voltages VBy $V(IO)_{max}$ = 36V | | | 5 | mA |
| **I/O Stages: Comparator IO 1..16** | | | | | | | |
| 301 | Vt()hi | Threshold voltage hi | IOx with input function | | | 82 | %VCC |
| 302 | Vt()lo | Threshold voltage lo | IOx with input function | 66 | | | %VCC |
| 303 | Vt()hys | Hysteresis | IOx with input function, Vt()hys = Vt()hi - Vt()lo | 100 | | | mV |
| 304 | Vt()hi | Threshold voltage hi referenced to VBy | IOx with output function, Vt()hi = VBy - V(IOx) | 5.0 | | | V |
| 305 | Vt()lo | Threshold voltage lo referenced to VBy | IOx with output function, Vt()lo = VBy - V(IOx) | | | 6.7 | V |
| 306 | Vt()hys | Hysteresis | IOx with output function, Vt()hys = Vt()lo - Vt()hi | 100 | | | mV |
| 307 | tp(IOx-Dx) | Propagation Delay Input IOx to Data Output Dx | I/O-Filter inaktive | | | 20 | µs |
| **Thermal Shutdown** | | | | | | | |
| 401 | Toff1 | Overtemperatur threshold level 1: warning | | 120 | | 145 | °C |
| 402 | Ton1 | Level 1 Release | | 115 | | 140 | °C |
| 403 | Thys1 | Level 1 Hysteresis | Thys1 = Toff1 - Ton1 | 2 | | 7 | °C |
| 404 | Toff2 | Overtemperatur threshold level 2: shutdown | | 140 | | 165 | °C |
| 405 | Ton2 | Level 2 Release | | 120 | | 145 | °C |
| 406 | Thys2 | Level 2 Hysteresis | Thys2 = Toff2 - Ton2 | 13 | | 35 | °C |
| 407 | ΔT | Temperature Difference Level 2 to Level 1 | ΔT = Toff2 - Toff1 | 13 | | 35 | °C |

## ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| **Bias and Low Voltage Detection** | | | | | | | |
| 501 | VCCon, VDDon | Turn-on Threshold VCC, VDD (Power-on release) | | 2.4 | 2.6 | 2.9 | V |
| 502 | VCCoff, VDDoff | Undervoltage Threshold VCC, VDD (Power-down reset) | | 2.3 | 2.5 | 2.8 | V |
| 503 | VCChys, VDDhys | Hysteresis | VCChys = VCCon - VCCoff,<br>VDDhys = VDDon - VDDoff | 60 | 100 | 140 | mV |
| 504 | tmin()lv | Power Down Time required for low voltage detection | VCC = 0.8 V .. VCCoff,<br>VDD = 0.8 V .. VDDoff | 1 | | | µs |
| 505 | tpoff | Propagation Delay until Reset after Low Voltage at VCC, VDD | | | | 12 | µs |
| 506 | Vrefad | Reference Voltage for A/D-Converter | | 2.6 | 2.75 | 3.0 | V |
| **A/D-Converter** | | | | | | | |
| 701 | VR1 | ADC - Measurement Range 1 | Current and voltage measurement High at IO, SELAD = ’0b001’ resp. ’0b010’, EME = 0 | VBy - 0.6 V | | VBy | V |
| 702 | VR2 | ADC - Measurement Range 2 | Voltage measurement High at IO, SELAD = ’0b010’, EME = 1 | VBy - 5V | | VBy | V |
| 703 | VR3 | ADC - Measurement Range 3 | Voltage measurement Low at IO, SELAD = ’0b100’, EME = 0 | 0 | | 0.6 | V |
| 704 | VR4 | ADC - Measurement Range 4 | Voltage measurement Low at IO SELAD = ’0b100’; VB or VBG measurement SELAD = ’0b101’ or. ’0b110’, EME = 1 | 0 | | 5 | V |
| 705 | VR5 | ADC - Measurement Range 5 | Total voltage measurement range SELAD = ’0b011’ | 0 | | VB | V |
| 706 | VR6 | ADC - Measurement Range 6 | Temperature measurement SELAD = ’0b111’ | -40 | | 125 | °C |
| 707 | Vbitlo | Bit-Equivalent of voltage | EME = 0 | | 0.6 | | mV |
| 708 | Vbithi | Bit-Equivalent of voltage | EME = 1 | | 5.4 | | mV |
| 709 | Dtemp1 | Digital value of temperature measurement 1 | SVREF = 0, TEMP = (774-Dtemp1)/TKtemp1<br>Tj = -40°C<br>Tj = 27°C<br>Tj = 95°C | <br>826<br>670<br>519 | <br>863<br>712<br>563 | <br>900<br>755<br>608 | |
| 710 | TKtemp1 | Temperature coefficient 1 | SVREF = 0 | 2.16 | 2.22 | 2.27 | 1/°C |
| 711 | Dtemp2 | Digital value of temperature measurement 2 | SVREF = 1, V(VREF) = 2.5V ±0.2%<br>TEMP = (861-Dtemp2)/TKtemp2<br>Tj = -40°C<br>Tj = 27°C<br>Tj = 95°C | <br><br>931<br>761<br>585 | <br><br>957<br>800<br>632 | <br><br>984<br>839<br>679 | |
| 712 | TKtemp2 | Temperature coefficient 2 | SVREF = 1, V(VREF) = 2.5V ±0.2% | 2.26 | 2.41 | 2.55 | 1/°C |
| 713 | $f_{ICLK}$ | Internal oscillating frequency | | 0.9 | 1.25 | 1.5 | MHz |
| 714 | $t_{SAR1}$ | Conversion time SAR-converter 1 | Current measurement SELAD = ’0b001’ | | 154 / $f_{ICLK}$ | | µs |
| 715 | $t_{SAR2}$ | Conversion time SAR-converter 2 | Voltage measurement Low resp. High; SELAD = ’0b010’ resp. ’0b100’ | | 90 / $f_{ICLK}$ | | µs |
| 716 | $t_{SAR3}$ | Conversion time SAR-converter 3 | Total voltage measurement SELAD = ’0b011’; VBy voltage measurement SELAD = ’0b101’; VBG voltage measurement SELAD = ’0b110’; temperature measurement SELAD = ’0b111’ | | 26 / $f_{ICLK}$ | | µs |
| 717 | $D_{VBG,1}$ | Digital value of VBG measurement (external reference) | SELAD = ’0b110’, SVREF = 1 | 480 | 520 | 560 | |
| 718 | $D_{VBY,1}$ | Digital value of VBy measurement (external reference) | SVREF = 1, V(VBy) = 36 V, SELAD = ’0b101’ | 940 | 990 | 1022 | |
| 719 | $DR_{VBY,1}$ | Relative value of VBy measurement (external reference) | SVREF = 1; $DR_{VBY,1} = D_{VBY,1}(V) / D_{VBY,1}$<br>V(VBy) = 24 V, SELAD = ’0b101’<br>V(VBy) = 12 V, SELAD = ’0b101’ | <br>64.6<br>31.3 | <br>66.6<br>33.3 | <br>68.6<br>35.2 | <br>%<br>% |

## ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| 720 | $D1_{IO,1}$ | Digital value using VR1 range (external reference) | SELAD = '0b010', EME = '0b0', SVREF = 1, V(IOx) = V(VBy) − 0.6V | 840 | 900 | 1022 | |
| 721 | $DR1_{IO,1}$ | Digital relative value using VR1 range (external reference) | SELAD = '0b010', EME = '0b0', SVREF = 1; $DR1_{IO,1} = D1_{IO,1}(V) / D1_{IO,1}$; V(IOx) = V(VBy) − 0.3 V<br>V(IOx) = V(VBy) − 0.1 V | 46<br>12 | 49<br>15 | 52<br>18 | %<br>% |
| 722 | $D2_{IO,1}$ | Digital absolute value using VR2 range (external reference) | SELAD = '0b010', EME = '0b1', SVREF = 1, V(IOx) = V(VBy) − 5.0 V | 870 | 930 | 1022 | |
| 723 | $DR2_{IO,1}$ | Digital relative value using VR2 range (external reference) | SELAD = '0b010', EME = '0b1', SVREF = 1; $DR2_{IO,1} = D2_{IO,1}(V) / D2_{IO,1}$; V(IOx) = V(VBy) − 2.5 V<br>V(IOx) = V(VBy) − 0.6 V | 48<br>9.5 | 50<br>11.5 | 52<br>14 | %<br>% |
| 724 | $D3_{IO,1}$ | Digital absolute value using VR3 range (external reference) | SELAD = '0b100', EME = '0b0', SVREF = 1, V(IOx) = 0.6 V; | 880 | 940 | 1022 | |
| 725 | $DR3_{IO,1}$ | Digital relative value using VR3 range (external reference) | SELAD = '0b100', EME = '0b0', SVREF = 1; $DR3_{IO,1} = D3_{IO,1}(V) / D3_{IO,1}$; V(IOx) = 0.3 V<br>V(IOx) = 0.1 V | 48<br>14.5 | 50<br>16 | 52<br>18.5 | %<br>% |
| 726 | $D4_{IO,1}$ | Digital absolute value using VR4 range (external reference) | SELAD = '0b100', EME = '0b1', SVREF = 1; V(IOx) = 5.0V | 870 | 930 | 1022 | |
| 727 | $DR4_{IO,1}$ | Digital relative value using VR4 range (external reference) | SELAD = '0b100', EME = '0b1', SVREF = 1; $DR4_{IO,1} = D4_{IO,1}(V) / D4_{IO,1}$<br>V(IOx) = 2.5V<br>V(IOx) = 0.6V | 48<br>9.5 | 50<br>11.5 | 52<br>14 | %<br>% |
| 728 | $D5_{IO,1}$ | Digital absolute value using VR5 range (external reference) | SELAD = '0b011', SVREF = 1, V(IOx) = 36.0V | 930 | 980 | 1022 | |
| 729 | $DR5_{IO,1}$ | Digital relative value using VR5 range (external reference) | SELAD = '0b011', SVREF = 1; $DR5_{IO,1} = D5_{IO,1}(V) / D5_{IO,1}$<br>V(IOx) = 24.0V<br>V(IOx) = 5.0V | 64.6<br>11.8 | 66.6<br>13.8 | 68.6<br>15.8 | %<br>% |
| 730 | $DC_{IO,1}$ | Digital value of current measurement (external reference) | SELAD = '0b001',SVREF = 1, I(IOx) = 150mA | 700 | 800 | 1022 | |
| 731 | $DRC_{IO,1}$ | Relative value of current measurement (external reference) | SELAD = '0b001', SVREF = 1; $DRC_{IO,1} = DC_{IO,1}(I) / DC_{IO,1}$<br>I(IOx) = 75mA<br>I(IOx) = 15mA | 48<br>6.2 | 51<br>9.2 | 54<br>12.2 | %<br>% |
| 732 | $D_{VBg,0}$ | Digital value of VBG measurement (internal reference) | SELAD = '0b110', SVREF = 0 | 435 | 460 | 485 | |
| 733 | $D_{VBY,0}$ | Digital value of VBG measurement (internal reference) | SVREF = 0, V(VBy) = 36V, SELAD = '0b101' | 830 | 880 | 1022 | |
| 734 | $DR_{VBY,0}$ | Relative value using VR1 range (internal reference) | SVREF = 0, SELAD = '0b101; $DR_{VBY,0} = D_{VBY,0}(V) / D_{VBY,0}$<br>V(VBy) = 24V<br>V(VBy) = 12V | 64.6<br>31.3 | 66.6<br>33.3 | 68.6<br>35.3 | %<br>% |
| 735 | $D1_{IO,0}$ | Digital value using VR1 range (internal reference) | SELAD = '0b010', EME = '0b0', SVREF = 0, V(IOx) = V(VBy) - 0.6V | 760 | 820 | 1022 | |
| 736 | $DR1_{IO,0}$ | Relative value using VR1 range (internal reference) | SELAD = '0b010', EME = '0b0', SVREF = 0; $DR1_{IO,0} = D1_{IO,0}(V) / D1_{IO,0}$<br>V(IOx) = V(VBy) - 0.3V<br>V(IOx) = V(VBy) - 0.1V | 46<br>12 | 49<br>15 | 52<br>18 | %<br>% |
| 737 | $D2_{IO,0}$ | Digital value using VR2 range (internal reference) | SELAD = '0b010', EME = '0b1', SVREF = 0, V(IOx) = V(VBy) - 5.0V | 790 | 840 | 1022 | |
| 738 | $DR2_{IO,0}$ | Relative value using VR2 range (internal reference) | SELAD = '0b010', EME = '0b1', SVREF = 0; $DR2_{IO,0} = D2_{IO,0}(V) / D2_{IO,0}$<br>V(IOx) = V(VBy) - 2.5V<br>V(IOx) = V(VBy) - 0.6V | 48<br>9.5 | 50<br>11.5 | 52<br>14 | %<br>% |
| 739 | $D3_{IO,0}$ | Digital value using VR3 range (internal reference) | SELAD = '0b100', EME = '0b0', SVREF = 0, V(IOx) = 0.6V | 790 | 840 | 1022 | |

## ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| 740 | $DR3_{IO,0}$ | Relative value using VR3 range (internal reference) | SELAD = '0b100', EME = '0b0', SVREF = 0; $DR3_{IO,0} = D3_{IO,0}(V) / D3_{IO,0}$<br>V(IOx) = 0.3V<br>V(IOx) = 0.1V | <br>48<br>14.5 | <br>50<br>16 | <br>52<br>18.5 | <br>%<br>% |
| 741 | $D4_{IO,0}$ | Digital value using VR4 range (internal reference) | SELAD = '0b100', EME = '0b1', SVREF = 0,<br>V(IOx) = 5.0V | 790 | 840 | 1022 | |
| 742 | $DR4_{IO,0}$ | Relative value using VR4 range (internal reference) | SELAD = '0b100', EME = '0b1', SVREF = 0; $DR4_{IO,0} = D4_{IO,0}(V) / D4_{IO,0}$<br>V(IOx) = 2.5V<br>V(IOx) = 0.6V | <br>48<br>9.5 | <br>50<br>11.5 | <br>52<br>14 | <br>%<br>% |
| 743 | $D5_{IO,0}$ | Digital value using VR5 range (internal reference) | SELAD = '0b011', SVREF = 0<br>V(IOx) = 36.0V | 810 | 870 | 1022 | |
| 744 | $DR5_{IO,0}$ | Relative value using VR5 range (internal reference) | SELAD = '0b011', SVREF = 0; $DR5_{IO,0} = D5_{IO,0}(V) / D5_{IO,0}$<br>V(IOx) = 24.0V<br>V(IOx) = 5.0V | <br>64.6<br>11.8 | <br>66.6<br>13.8 | <br>68.6<br>15.8 | <br>%<br>% |
| 745 | $DC_{IO,0}$ | Digital value of current measurement (internal reference) | SELAD = '0b001', SVREF = 0, I(IOx) = 150mA | 720 | 820 | 1022 | |
| 746 | $DRC_{IO,0}$ | Digital value of current measurement (internal reference) | SELAD = '0b001', SVREF = 0; $DRC_{IO,0} = DC_{IO,0}(I) / DC_{IO,0}$<br>I(IOx) = 75mA<br>I(IOx) = 15mA | <br>48<br>6.2 | <br>51<br>9.2 | <br>54<br>12.2 | <br>%<br>% |
| **Input RSET** | | | | | | | |
| B01 | V(RSET) | Voltage at RSET | | 1.15 | 1.22 | 1.30 | V |
| B02 | R(RSET) | Range value for RSET | | 9 | 10 | 14 | kΩ |
| **Burst-Indication** | | | | | | | |
| C01 | VSPon | Input On-Threshold for burst recognition | | 1.3 | | 2.9 | V |
| C02 | VSPoff | Input Off-Threshold for Burst-recognition | | 1.4 | | 3 | V |
| C03 | tpoff | Delay time to Reset after spike at VCC, VDD | Spike duration: 10 ns | 2 | | 110 | µs |
| **Pin monitoring GNDA, GNDD** | | | | | | | |
| H01 | Vt()gnd | Threshold voltage for open ciruit detection on pins GNDA, GNDD | | 35 | | 65 | mV |
| H02 | tmin()gnd | Minimum duration for open circuit detection | V(GNDA,GNDD) = 0 V ... Vt()gnd | 1 | | | µs |
| H03 | tpoff | Delay time to reset after open circuit detection at GNDA, GNDD | | | | 15 | µs |
| **Undervoltage detection VB** | | | | | | | |
| I01 | VByon | Undervoltage message VB1...4 on | | 10.6 | 11.2 | 11.8 | V |
| I02 | VByoff | Undervoltage message VB1...4 off | | 10.0 | 10.6 | 11.2 | V |
| I03 | VByhys | Hysteresis | VByhys = VByon - VByoff | 400 | | | mV |
| I04 | tmin()lv | Minimum duration for Power-Down detection | VBy = 0.8 V ... VByoff | 1 | | | µs |
| I05 | tpoff | Delay time for undervoltage message VB1...4 | | | | 6 | µs |
| **µC-Intrface, I/O-Logic, Frequency divider, Interrupt** | | | | | | | |
| K01 | Vt()hi | Threshold voltage High at Schmitt-Trigger-Inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE | D0...7 with input function | | | 2 | V |

## ELECTRICAL CHARACTERISTICS

Operating conditions: VCC = VDD = 3 ... 5.5 V, VBy = 12 ... 36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1% . All inputs on defined logic states (high or low), Tj = -40 ... 125 °C unless otherwise stated. Functionality and parameters beyond operating conditions (for example w.r. to independent voltage supplies) are to be verified within the individual application by FMEA methods.

| Item No. | Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| K02 | Vt()lo | Threshold voltage Low at Schmitt-Trigger-Inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE | D0...7 with input function | 0.8 | | | V |
| K03 | Vt()hys | Schmitt-Trigger-Hysteresis at inputs NCS, NWR, NRD, A0...4, NRES, CLK, BLFQ, D0...7, NSP, POE | Vt()hys = Vt()hi - Vt()lo; D0...7 mit Eingangsfunktion | 150 | | | mV |
| K04 | Vs()hi | Saturation voltage high an NINT, Dx | Vs()hi = VDD - V( ); I( ) = -4 mA | | | 0.8 | V |
| K05 | Vs()lo | Saturation voltage low an NINT, Dx | I( ) = 4 mA | | | 0.49 | V |
| K06 | Ipd() | Pull Down current sources at A0...4, NRES, CLK, BLFQ, D0...7, POE | V() = 1V .. VDD | 2 | | 70 | µA |
| K07 | Ipu() | Pull Up current sources at NSP, NCS, NWR, NRD | V() = 0V .. VDD - 1 V | -70 | | 2 | µA |
| K08 | tp(POE-IOx) | Delay time output enable: POE to IOx disabled | RL = 240 Ω... 1 kΩ, POE: hi → lo to V(IOx) < 80 % (VBy - Vs(IOx)hi) | | | 6 | µs |
| K09 | tw()lo | Permissible pulse width for enable/disable at POE | | 600 | | | ns |
| K10 | tw() | Permissible burst pulse width at POE | | | | 100 | ns |
| K11 | tmin()nres | minimum duration for reset at NRES | | 200 | | | ns |
| **Frequency BLFQ, CLK** | | | | | | | |
| P01 | td() | maximum frequency at CLK | | | | TBD | MHz |
| P02 | td() | maximum frequency at BLFQ | | | | TBD | MHz |

## Characteristics: Diagrams

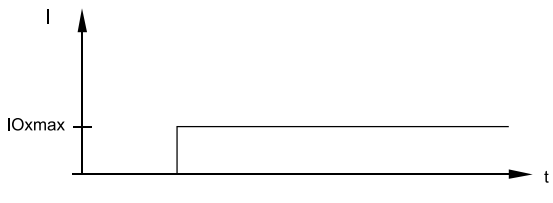



Figure 1: DC load

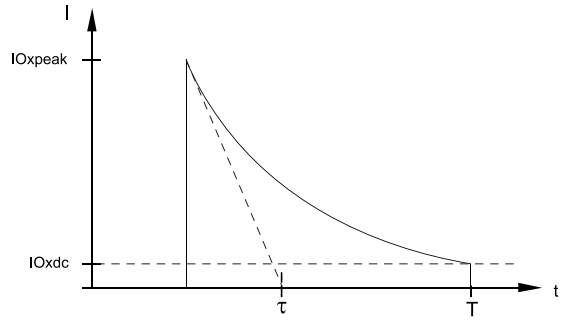



Figure 2: Pulse load

## OPERATING REQUIREMENTS: Parallel µC Interface

Operating Conditions: VCC = VDD = 3...5.5 V, VBy = 12...36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1 %
Ta = 0...70 °C, CL() = 150 pF, input level lo = 0.8 V, hi = 2.2 V, reference levels according to figure 3

| Item No. | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Read Cycle** | | | | | | |
| I001 | $t_{AR1}$, $t_{AR2}$ | Setup Time: NCS, A0...4 set before NRD hi → lo | see Figure 4 | 30 | | ns |
| I002 | $t_{RA}$ | Hold Time: NCS, A0...4 set before NRD lo → hi | see Figure 4 | 0 | | ns |
| I003 | $t_{RD}$ | Wait Time : Data valid after NRD hi → lo | see Figure 4 | | 120 | ns |
| I004 | $t_{DF}$ | Hold Time: Data Bus high impedance after NRD lo → hi | see Figure 4 | | 65 | ns |
| I005 | $t_{RL}$ | Required Read Signal Duration at NRD | | 50 | | ns |
| **Write Cycle** | | | | | | |
| I006 | $t_{AW1}$, $t_{AW2}$ | Setup Time: NCS, A0...4 set before NWR lo → hi | see Figure 4 | 30 | | ns |
| I007 | $t_{DW}$ | Setup time : Data valid before NWR lo → hi | see Figure 4 | 100 | | ns |
| I008 | $t_{WA}$ | Hold time: NCS, A0...4 stable after NWR lo → hi | see Figure 4 | 10 | | ns |
| I009 | $t_{WD}$ | Hold time: Data valid after NWR lo → hi | see Figure 4 | 10 | | ns |
| I010 | $t_{WL}$ | Required Write Signal Duration at NWR | see Figure 4 | 50 | | ns |
| **Read/Write Timing** | | | | | | |
| I011 | $t_{cyc}$ | Recovery Time between cycles: NRD lo → hi to NRD hi → lo, NRD lo → hi to NWR hi → lo, NWR lo → hi to NWR hi → lo, NWR lo → hi to NRD hi → lo | see Figure 4 | 165 | | ns |

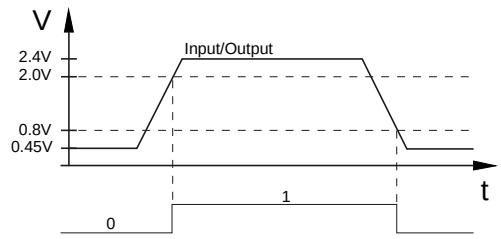



Figure 3: Reference levels for displayed values of time

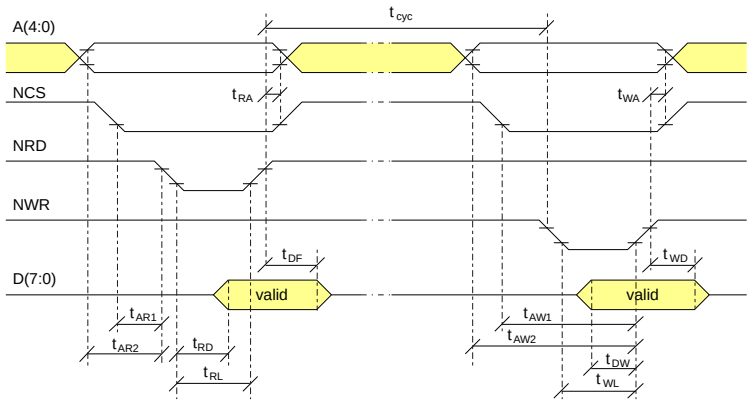



Figure 4: Read and write cycle for the parallel interface

## OPERATING REQUIREMENTS: Serial µC Interface

Operating Conditions: VCC = VDD = 3...5.5 V, VBy = 12...36 V, GNDA = GNDD = 0 V, RSET = 10 kΩ ±1 %
Ta = 0...70 °C, CL() = 150 pF, input level lo = 0.8 V, hi = 2.2 V, reference levels according to figure 3

| Item No. | Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| **Gruppe 2.0 EN** | | | | | | |
| I111 | $t_{sCCL}$ | Setup time:<br>NCS hi → lo to SCK(A3) lo → hi | see Figure 5 | 50 | | ns |
| I112 | $t_{sDCL}$ | Setup time:<br>SI(D0) stabil before SCK(A3) lo → hi | see Figure 5 | 40 | | ns |
| I113 | $t_{hDCL}$ | Hold time:<br>SI(D0) stabil after SCK(A3) lo → hi | see Figure 5 | 30 | | ns |
| I114 | $t_{CLh}$ | Clock duration SCK(A3) hi | see Figure 5 | 100 | | ns |
| I115 | $t_{CLl}$ | Clock duration SCK(A3) lo | see Figure 5 | 100 | | ns |
| I116 | $t_{CSh}$ | Pulse duration NCS hi | see Figure 5 | 100 | | ns |
| I117 | $t_{pCLD}$ | Delay time:<br>SOC(D1) resp. SOB(D2) stable after SCK(A3) hi → lo | see Figure 5 | 0 | 50 | ns |
| I118 | $t_{pCSD}$ | Delay time:<br>SOC(D1) resp. SOB(D2) high impedance after NCS lo → hi | see Figure 5 | 0 | 50 | ns |

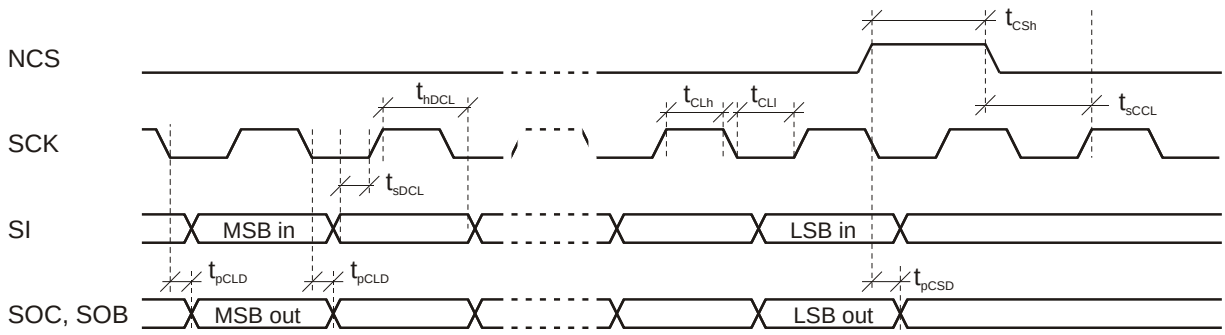



Figure 5: µC interface in SPI mode

## PROGRAMMING

| **Register Overview** | | | | | | | |
|---|---|---|---|---|---|---|---|
| Adress | | | | | | | |
| **A(4...0)** | A4 | A3 | A2 | A1 | A0 | **Write** | **Read** |
| **0x00** | 0 | 0 | 0 | 0 | 0 | - | Input Register A[1,2] |
| **0x01** | 0 | 0 | 0 | 0 | 1 | - | Input Register B[1,2] |
| **0x02** | 0 | 0 | 0 | 1 | 0 | - | Input Change Message A[1,3] |
| **0x03** | 0 | 0 | 0 | 1 | 1 | - | Input Change Message B[1,3] |
| **0x04** | 0 | 0 | 1 | 0 | 0 | - | Interrupt Message Register A |
| **0x05** | 0 | 0 | 1 | 0 | 1 | - | Interrupt Message Register B |
| **0x06** | 0 | 0 | 1 | 1 | 0 | - | Overcurrent Message A[1,4] |
| **0x07** | 0 | 0 | 1 | 1 | 1 | - | Overcurrent Message B[1,4] |
| **0x08** | 0 | 1 | 0 | 0 | 0 | - | Overcurrent Status A[1] |
| **0x09** | 0 | 1 | 0 | 0 | 1 | - | Overcurrent Status B[1] |
| **0x0A** | 0 | 1 | 0 | 1 | 0 | - | A/D-Converter Data 1 |
| **0x0B** | 0 | 1 | 0 | 1 | 1 | - | A/D-Converter Data 2 |
| **0x0C** | 0 | 1 | 1 | 0 | 1 | Output Register A[1] | |
| **0x0D** | 0 | 1 | 1 | 1 | 0 | Output Register B[1] | |
| **0x0E** | 0 | 1 | 1 | 1 | 1 | Flash Pulse Enable A[1] | |
| **0x0F** | 1 | 0 | 0 | 0 | 0 | Flash Pulse Enable B[1] | |
| **0x10** | 1 | 0 | 0 | 0 | 1 | Interrupt-Enable Input Change A[1,5] | |
| **0x11** | 1 | 0 | 0 | 1 | 0 | Interrupt-Enable Input Change B[1,5] | |
| **0x12** | 1 | 0 | 0 | 1 | 1 | Interrupt-Enable Overcurrent A[1] | |
| **0x13** | 1 | 0 | 1 | 0 | 0 | Interrupt-Enable Overcurrent B[1] | |
| **0x14** | 1 | 0 | 1 | 0 | 1 | Control Word 1A (I/O Filter)[1] | |
| **0x15** | 1 | 0 | 1 | 1 | 0 | Control Word 1B (I/O Filter)[1] | |
| **0x16** | 1 | 0 | 1 | 1 | 1 | Control Word 2A (I/O Pin Functions)[1] | |
| **0x17** | 1 | 1 | 0 | 0 | 0 | Control Word 2B (I/O Pin Functions)[1] | |
| **0x18** | 1 | 1 | 0 | 0 | 1 | Control Word 3A (Flash Pulse Settings)[1] | |
| **0x19** | 1 | 1 | 0 | 1 | 0 | Control Word 3B (Flash Pulse Settings)[1] | |
| **0x1A** | 1 | 1 | 0 | 1 | 1 | Control Word 4 (Overcurrent Filter Settings) | |
| **0x1B** | 1 | 1 | 1 | 0 | 0 | Control Word 5 (I/O Stage Selection for AD Converter | |
| **0x1C** | 1 | 1 | 1 | 0 | 1 | Control Word 6 (AD Converter Settings) | |
| **0x1D** | 0 | 1 | 1 | 0 | 0 | - | Interconnection Error, Device-ID |
| **0x1E** | 1 | 1 | 1 | 1 | 0 | Test Register 1 | |
| **0x1F** | 1 | 1 | 1 | 1 | 1 | Test Register 2 | |

Table 7: Register assignment

1. A: I/O-Stages 1...8, B: I/O-Stages 9...16
2. Reads the inpus or reads back the outputs, depending on I/O pin mode
3. For I/O pins in input mode (register is ’0’ in output mode)
4. For I/O pins in output mode (register is ’0’ in input mode)
5. Only writable in input mode

| **Input Register A (read only)** | | | | | | | | **Adr. 0x00** |
|---|---|---|---|---|---|---|---|---|
| reading of inputs / output feedback | | | | | | | | |
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | IN8 | IN7 | IN6 | IN5 | IN4 | IN3 | IN2 | IN1 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | Input/Output IOx read '0' | (r) |
| IN8...1 | 1 | Input/Output IOx read '1' | |

| **Input Register B (read only)** | | | | | | | | **Adr. 0x01** |
|---|---|---|---|---|---|---|---|---|
| reading of inputs / output feedback | | | | | | | | |
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | IN16 | IN15 | IN14 | IN13 | IN12 | IN11 | IN10 | IN9 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | Input/Output IOx read '0' | (r) |
| IN16...9 | 1 | Input/Output IOx read '1' | |

INx indicates the state for IOx (via I/O filter or bypass).

| **Change-of-input Message A (read only)** | | | | | | | | **Adr. 0x02** |
|---|---|---|---|---|---|---|---|---|
| for I/O stages in input mode | | | | | | | | |
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DCH8 | DCH7 | DCH6 | DCH5 | DCH4 | DCH3 | DCH2 | DCH1 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | No change of state at the input IOx or no interrupt enable | (r) |
| DCH8...1 | 1 | Input IOx has had a change of state enabled for interrupt messages | |

| **Change-of-input Message B (read only)** | | | | | | | | **Adr. 0x03** |
|---|---|---|---|---|---|---|---|---|
| for I/O stages in input mode | | | | | | | | |
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DCH16 | DCH15 | DCH14 | DCH13 | DCH12 | DCH11 | DCH10 | DCH9 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | No change of state at the input IOx or no interrupt enable | (r) |
| DCH16...9 | 1 | Input IOx has had a change of state enabled for interrupt messages | |

| **Interrupt Status Register A (read only)** | | | | | | | | **Adr. 0x04** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | DCHI | IET2 | IET1 | ISCI | - | ET2 | ET1 | SCS |

| Change-of-input data, overtemperatur, overcurrent (interrupts stored) | | | |
|---|---|---|---|
| Bit7 | 0 | No message | (r) |
| DCHI | 1 | Interrupt through change-of input message | |
| Bit6 | 0 | No message | (r) |
| IET2 | 1 | Interrupt through excessive temperature level 2 | |
| Bit5 | 0 | No message | (r) |
| IET1 | 1 | Interrupt through excessive temperature level 1 | |
| Bit4 | 0 | No message | (r) |
| ISCI | 1 | Interrupt through overcurrent message | |

| Excessive temperature status, overcurrent status (real time signals, at the time of readout) | | | |
|---|---|---|---|
| Bit2 | 0 | No error message | (r) |
| ET2 | 1 | Excessive temperature level 2 (shutdown) | |
| Bit1 | 0 | No error message | (r) |
| ET1 | 1 | Excessive temperature level 1 (warning) | |
| Bit0 | 0 | No error message | (r) |
| SCS | 1 | Overcurrent status (e.g. caused by low-side short circuit) | |

| **Interrupt Status Register B (read only)** | | | | | | | | **Adr. 0x05** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | IEOC | ISD | IUSD | IUSA | - | EOC | USD | USA |

| A/D-Converter, Bursts, Undervoltage (interrupts stored) | | | |
|---|---|---|---|
| Bit7 | 0 | No message | (r) |
| IEOC | 1 | Interrupt by the A/D-Converter | |
| Bit6 | 0 | No message | (r) |
| ISD | 1 | Interrupt caused by bursts at VDD | |
| Bit5 | 0 | No message | (r) |
| IUSD | 1 | Interrupt caused by undervoltage at VDD | |
| Bit4 | 0 | No message | (r) |
| IUSA | 1 | Interrupt caused by undervoltage at VCC | |

| A/D-Converter, Undervoltage (real time signals, at the time of readout) | | | |
|---|---|---|---|
| Bit2 | 0 | No message | (r) |
| EOC | 1 | A/D conversion completed (End of Conversion) | |
| Bit1 | 0 | No message | (r) |
| USD | 1 | Undervoltage at VDD | |
| Bit0 | 0 | No message | (r) |
| USA | 1 | Undervoltage at VCC | |

Read access gates off changes to the register; the register is reenabled only when reset via EOI. Any successive interrupts which occur at DCHI, IET2, IET1, ISCI, IEOC, ISD, IUSD und IUSA during the read-out phase and before a reset with EOI are trapped by an interrupt pipeline. If this happens, the message at NINT resp. D1/SOC or D2/SOB cannot be deletet by EOI, i.e. NINT resp. D1/SOC or D2/SOB constantly remains on low. In this instance, EOI fills the overcurrent message from the pipeline.

| **Overcurrent Message A (read only)** | | | | | | | | **Adr. 0x06** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SCI8 | SCI7 | SCI6 | SCI5 | SCI4 | SCI3 | SCI2 | SCI1 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | No Message | (r) |
| SCI8...1 | 1 | Output IOx has had an overcurrent state enabled for interupt messages (short circuit) | |

| **Overcurrent Message B (read only)** | | | | | | | | **Adr. 0x07** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SCI16 | SCI15 | SCI14 | SCI13 | SCI12 | SCI11 | SCI10 | SCI9 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | No Message | (r) |
| SCI16...9 | 1 | Output IOx has had an overcurrent state enabled for interupt messages (short circuit) | |

Read access gates off changes to the register; the register is reenabled only when reset via EOI. Any successive interrupts which occur during the read-out phase and before a reset with EOI are trapped by an interrupt pipeline. If this happens, the message at NINT resp. D1/SOC or D2/SOB cannot be deletet by EOI, i.e. NINT resp. D1/SOC or D2/SOB constantly remains on low. In this instance, EOI fills the overcurrent message from the pipeline.

The SCIx bits may be erased selectable by reenabeling IENx after disable.
'0' is output for IOx pins in input mode. SCIx reports for IOx.

| **Overcurrent Status A (read only)** | | | | | | | | **Adr. 0x08** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry : 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SC8 | SC7 | SC6 | SC5 | SC4 | SC3 | SC2 | SC1 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | No overcurrent | (r) |
| SC8...1 | 1 | Overcurrent in output IOx, e.g. through a low-side short circuit | |

| **Overcurrent Status B (read only)** | | | | | | | | **Adr. 0x09** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SC16 | SC15 | SC14 | SC13 | SC12 | SC11 | SC10 | SC9 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | No overcurrent | (r) |
| SC16...9 | 1 | Overcurrent in output IOx, e.g. through a low-side short circuit | |

These signals act as error analysis and does not generate any interrupts (real time, no register). '0' is output for IOx pins in input mode. SCx reports for IOx.

| **A/D-Converter Data 1 (read only)** | | | | | | | | **Adr. 0x0A** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | Bit value is 0 | (r) |
| D9...2 | 1 | Bit value equals VREFi/1024 * $2^n$, with n = 9..2 | |

| **A/D-Converter Data 2 (read only)** | | | | | | | | **Adr. 0x0B** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | D1 | D0 | - | - | - | - | - | - |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | Bit value is 0 | (r) |
| D1...0 | 1 | Bit value equals VREFi/1024 * $2^n$, with n = 1..0 | |

Digitized result of the analog measurement for load current, I/O voltage, driver supply, internal voltage reference or temperature measurement. During the current measurement, VREFi corresponds to the saturation voltage of the internal reference transistor, otherwise it is either the internal reference voltage V(Vrefad) (bit SVREF = ' 0 ', control word 6) or the voltage at the pin Vref (bit SVREF = ' 1 ', control word 6).

| **Output-Register A**<br>for I/O stages with output function | | | | | | | | **Adr. 0x0C** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | OUT8 | OUT7 | OUT6 | OUT5 | OUT4 | OUT3 | OUT2 | OUT1 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | High-side driver "OFF" | (r) |
| OUT8...1 | 1 | High-side driver "ON", i.e. normally, IOx = 1 | |

| **Output-Register B**<br>for I/O stages with output function | | | | | | | | **Adr. 0x0D** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | OUT16 | OUT15 | OUT14 | OUT13 | OUT12 | OUT11 | OUT10 | OUT9 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | High-side driver "OFF" | (r) |
| OUT16...9 | 1 | High-side driver "ON", i.e. normally, IOx = 1 | |

OUTx switches the high-side driver for IOx.

| **Flash Pulse Enable A**<br>for I/O stages with output function | | | | | | | | **Adr. 0x0E** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PEN8 | PEN7 | PEN6 | PEN5 | PEN4 | PEN3 | PEN2 | PEN1 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | Flash pulse "DISABLED" | (r) |
| PEN8...1 | 1 | Flash pulse "ENABLED" | |

PENx enables the flash pulse for IOx.

| **Flash Pulse Enable B** for I/O stages with output function | | | | | | | | **Adr. 0x0F** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PEN16 | PEN15 | PEN14 | PEN13 | PEN12 | PEN11 | PEN10 | PEN9 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | Flash pulse "DISABLED" | (r) |
| PEN16...9 | 1 | Flash pulse "ENABLED" | |

PENx enables the flash pulse for IOx.

| **Change-of-input Interrupt Enable A** for I/O stages with input function | | | | | | | | **Adr. 0x10** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | IEN8 | IEN7 | IEN6 | IEN5 | IEN4 | IEN3 | IEN2 | IEN1 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | "DISABLED" for interrupt | (r) |
| IEN8...1 | 1 | "ENABLED" for interrupt:<br>A hi → lo or lo → hi change of state at the input IOx triggers an interrupt. | |

| **Change-of-input Interrupt Enable B** for I/O stages with input function | | | | | | | | **Adr. 0x11** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | IEN16 | IEN15 | IEN14 | IEN13 | IEN12 | IEN11 | IEN10 | IEN9 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | "DISABLED" for interrupt | (r) |
| IEN16...9 | 1 | "ENABLED" for interrupt:<br>A hi → lo or lo → hi change of state at the inut IOx triggers an interrupt. | |

IENx enables the input IOx for interrupt. The outputs IOx can not be enabled for interrupt. The registers can only be modified in input mode.

| **Overcurrent Interrupt Enable A** | | | | | | | | **Adr. 0x12** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SCEN8 | SCEN7 | SCEN6 | SCEN5 | SCEN4 | SCEN3 | SCEN2 | SCEN1 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | "DISABLED" for interrupt | (r) |
| SCEN8...1 | 1 | "ENABLED" for interrupt: a short-circuit at IOx triggers an interrupt. | |

| **Overcurrent Interrupt Enable B** | | | | | | | | **Adr. 0x13** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | SCEN16 | SCEN15 | SCEN14 | SCEN13 | SCEN12 | SCEN11 | SCEN10 | SCEN9 |

| | | | |
|---|---|---|---|
| Bit7...0 | 0 | "DISABLED" for interrupt | (r) |
| SCEN16...9 | 1 | "ENABLED" for interrupt: a short-circuit at IOx triggers an interrupt. | |

SCENx enables the output IOx for interrupt.

| **Control Word 1A (I/O filters)** | | | | | | | | **Adr. 0x14** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| | **Nibble 1: I/O-Pins 5..8** | | | | **Nibble 0: I/O-Pins 1..4** | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | BYP1 | - | FH1 | FH0 | BYP0 | - | FL1 | FL0 |

**Nibble 1**

| | | | | |
|---|---|---|---|---|
| Bit7 | 0 | I/O filters aktive | | (r) |
| BYP1 | 1 | Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state. | | |
| Bit5..4 | | FH1 | FH0 | Filter times[1] |
| FH1..0 | | 0 | 0 | $14.5 * tc(SECLK) \pm 1 * tc(SECLK)$ (r) |
| | | 0 | 1 | $896.5 * tc(SECLK) \pm 64 * tc(SECLK)$ |
| | | 1 | 0 | $3584.5 * tc(SECLK) \pm 256 * tc(SECLK)$ |
| | | 1 | 1 | $7168.5 * tc(SECLK) \pm 512 * tc(SECLK)$ |

**Nibble 0**

| | | | | |
|---|---|---|---|---|
| Bit3 | 0 | I/O filter aktive | | (r) |
| BYP0 | 1 | Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state. | | |
| Bit1..0 | | FL1 | FL0 | Filter times[1] |
| FL1..0 | | 0 | 0 | $14.5 * tc(SECLK) \pm 1 * tc(SECLK)$ (r) |
| | | 0 | 1 | $896.5 * tc(SECLK) \pm 64 * tc(SECLK)$ |
| | | 1 | 0 | $3584.5 * tc(SECLK) \pm 256 * tc(SECLK)$ |
| | | 1 | 1 | $7168.5 * tc(SECLK) \pm 512 * tc(SECLK)$ |

| **Control Word 1B (I/O filters)** | | | | | | | | **Adr. 0x15** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| | **Nibble 3: I/O-Pins 13..16** | | | | **Nibble 2: I/O-Pins 9..12** | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | BYP3 | - | FH1 | FH0 | BYP2 | - | FL1 | FL0 |

**Nibble 3**

| | | | | |
|---|---|---|---|---|
| Bit7 | 0 | I/O filters aktive | | (r) |
| BYP1 | 1 | Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state. | | |
| Bit5..4 | | FH1 | FH0 | Filter times[1] |
| FH1..0 | | 0 | 0 | $14.5 * tc(SECLK) \pm 1 * tc(SECLK)$ (r) |
| | | 0 | 1 | $896.5 * tc(SECLK) \pm 64 * tc(SECLK)$ |
| | | 1 | 0 | $3584.5 * tc(SECLK) \pm 256 * tc(SECLK)$ |
| | | 1 | 1 | $7168.5 * tc(SECLK) \pm 512 * tc(SECLK)$ |

**Nibble 2**

| | | | | |
|---|---|---|---|---|
| Bit3 | 0 | I/O filters aktive | | (r) |
| BYP0 | 1 | Bypass for I/O filters: the I/O signals are reprocessed in their unfiltered state. | | |
| Bit1..0 | | FL1 | FL0 | Filter times[1] |
| FL1..0 | | 0 | 0 | $14.5 * tc(SECLK) \pm 1 * tc(SECLK)$ (r) |
| | | 0 | 1 | $896.5 * tc(SECLK) \pm 64 * tc(SECLK)$ |
| | | 1 | 0 | $3584.5 * tc(SECLK) \pm 256 * tc(SECLK)$ |
| | | 1 | 1 | $7168.5 * tc(SECLK) \pm 512 * tc(SECLK)$ |

1. SECLK: see control word 3B on page 23

| **Control Word 2A (I/O pin funktions)** | | | | | | | | **Adr. 0x16** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x11 |
| | **Nibble 1: I/O-Pins 5..8** | | | | **Nibble 0: I/O-Pins 1..4** | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | NIOH | IH2 | IH1 | IH0 | NIOL | IL2 | IL1 | IL0 |

**Nibble 1**

| | | | | | | |
|---|---|---|---|---|---|---|
| Bit7 | 0 | Input mode | | | | (r) |
| NIOH | 1 | Output mode | | | | |
| Bit6..4 | | IH2 | IH1 | IH0 | current sources | |
| IH2..0 | | 0 | 0 | 0 | 0µA Pull-Down | |
| | | 0 | 0 | 1 | 200µA Pull-Down | (r) |
| | | 0 | 1 | 0 | 600µA Pull-Down | |
| | | 0 | 1 | 1 | 2mA Pull-Down | |
| | | 1 | 0 | 0 | 0µA Pull-Up | |
| | | 1 | 0 | 1 | 200µA Pull-Up | |
| | | 1 | 1 | 0 | 600µA Pull-Up | |
| | | 1 | 1 | 1 | 2mA Pull-Up | |

**Nibble 0**

| | | | | | | |
|---|---|---|---|---|---|---|
| Bit3 | 0 | Input mode | | | | (r) |
| NIOL | 1 | Output mode | | | | |
| Bit2..0 | | IL2 | IL1 | IL0 | Current sources | |
| IL2..0 | | 0 | 0 | 0 | 0µA Pull-Down | |
| | | 0 | 0 | 1 | 200µA Pull-Down | (r) |
| | | 0 | 1 | 0 | 600µA Pull-Down | |
| | | 0 | 1 | 1 | 2mA Pull-Down | |
| | | 1 | 0 | 0 | 0µA Pull-Up | |
| | | 1 | 0 | 1 | 200µA Pull-Up | |
| | | 1 | 1 | 0 | 600µA Pull-Up | |
| | | 1 | 1 | 1 | 2mA Pull-Up | |

| **Control Word 2B (I/O-Pinfunktion)** | | | | | | | | **Adr. 0x17** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x11 |
| | **Nibble 3: I/O-Pins 13..16** | | | | **Nibble 2: I/O-Pins 9..12** | | | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | NIOH | IH2 | IH1 | IH0 | NIOL | IL2 | IL1 | IL0 |

**Nibble 3**

| | | | | | | |
|---|---|---|---|---|---|---|
| Bit7 | 0 | Input mode | | | | (r) |
| NIOH | 1 | Output mode | | | | |
| Bit6..4 | | IH2 | IH1 | IH0 | Current sources | |
| IH2..0 | | 0 | 0 | 0 | 0µA Pull-Down | |
| | | 0 | 0 | 1 | 200µA Pull-Down | (r) |
| | | 0 | 1 | 0 | 600µA Pull-Down | |
| | | 0 | 1 | 1 | 2mA Pull-Down | |
| | | 1 | 0 | 0 | 0µA Pull-Up | |
| | | 1 | 0 | 1 | 200µA Pull-Up | |
| | | 1 | 1 | 0 | 600µA Pull-Up | |
| | | 1 | 1 | 1 | 2mA Pull-Up | |

**Nibble 2**

| | | | | | | |
|---|---|---|---|---|---|---|
| Bit3 | 0 | Input mode | | | | (r) |
| NIOL | 1 | Output mode | | | | |
| Bit2..0 | | IL2 | IL1 | IL0 | Current sources | |
| IL2..0 | | 0 | 0 | 0 | 0µA Pull-Down | |
| | | 0 | 0 | 1 | 200µA Pull-Down | (r) |
| | | 0 | 1 | 0 | 600µA Pull-Down | |
| | | 0 | 1 | 1 | 2mA Pull-Down | |
| | | 1 | 0 | 0 | 0µA Pull-Up | |
| | | 1 | 0 | 1 | 200µA Pull-Up | |
| | | 1 | 1 | 0 | 600µA Pull-Up | |
| | | 1 | 1 | 1 | 2mA Pull-Up | |

| **Control Word 3A (flash pulse settings)** | | | | | | | | **Adr. 0x18** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Reset-Zustand : 0x00 |
| | **Nibble 3: I/O-Pins 13..16** | | **Nibble 2: I/O-Pins 9..12** | | **Nibble 1: I/O-Pins 5..8** | | **Nibble 0: I/O-Pins 1..4** | |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | PN31 | PN30 | PN21 | PN20 | PN11 | PN10 | PN01 | PN00 |

**Nibble 1**

| Nibble3, Bit7..6<br>Nibble2, Bit5..4<br>Nibble1, Bit3..2<br>Nibble0, Bit1..0 | PN31<br>PN21<br>PN11<br>PN01 | PN30<br>PN20<br>PN10<br>PN00 | Flash frequency<br><br><br>SEBLQ = 0 | Flash frequency<br><br><br>SEBLQ = 1[1] | |
|---|---|---|---|---|---|
| | 0 | 0 | f(BLFQ) | $f(SECLK)/2^{19}$ | (r) |
| | 0 | 1 | f(BLFQ/2) | $f(SECLK)/2^{20}$ | |
| | 1 | 0 | f(BLFQ/4) | $f(SECLK)/2^{21}$ | |
| | 1 | 1 | f(BLFQ/16) | $f(SECLK)/2^{23}$ | |

1. SEBLQ: see control word 3B

| **Control Word 3B (reference clock)** | | | | | | | | **Adr. 0x19** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry: 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | - | - | - | - | SECLK1 | SECLK0 | - | SEBLQ |

| Bit0 | SEBLQ | Settings for flash frequency | |
|---|---|---|---|
| SEBLQ | 0 | The flashing pulse is derived from the external clock signal at BLFQ | (r) |
| | 1 | The flashing pulse is derived from the system clock SECLK | |

| Bit3..2 | SECLK1 | SECLK0 | Settings for system clock SECLK | |
|---|---|---|---|---|
| SECLK1..0 | 0 | 0 | Operation with the clock signal at CLK | (r) |
| | 0 | 1 | Operation with the internal clock signal ICLK | |
| | 1 | 0 | Operation without the clock signal at CLK (filterung etc. deactivated) | |
| | 1 | 1 | reserved | |

| **Control Word 4 (filter settings for overcurrent message)** | | | | | | | | **Adr. 0x1A** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry : 0x00 |
| | | | | | **Nibble3** | **Nibble2** | **Nibble1** | **Nibble0** |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | EOI | - | - | BYPSCF | SCF3 | SCF2 | SCF1 | SCF0 |

| | | | |
|---|---|---|---|
| Bit7<br>EOI | 0<br>1 | No effect<br>"DELETE"s the interrupt message (change-of-input message;<br>interrupt status register, overcurrent message)<br>accepts successive interrupts from the pipeline, deletes the<br>messages at NINT resp. D1/SOC or D2/SOB when the pipeline is empty.<br><br>Bit automatically resets to '0'. | (r) |
| Bit4<br>BYPSCF | 0<br>1 | Filters for the overcurrent message are active<br>Bypass for the filters: overcurrent messages are reprocessed in their unfiltered state. | (r) |
| Bit3<br>SCF3 | 0<br>1 | **Nibble 3**<br>Overcurrent message with 2.3ms filtering<br>Overcurrent message with 4.6ms filtering<br>Gives the filter times with the clock frequency at SECLK [1], i.e. 1.25MHz:<br>2.3ms aus $(2689.5 \pm 192) * tc(SECLK)$ bzw.<br>4.6ms aus $(5378.5 \pm 384) * tc(SECLK)$ | (r) |
| Bit2<br>SCF2 | 0<br>1 | **Nibble 2**<br>Overcurrent message with 2.3ms filtering<br>Overcurrent message with 4.6ms filtering | (r) |
| Bit1<br>SCF1 | 0<br>1 | **Nibble 1**<br>Overcurrent message with 2.3ms filtering<br>Overcurrent message with 4.6ms filtering | (r) |
| Bit1<br>SCF0 | 0<br>1 | **Nibble 0**<br>Overcurrent message with 2.3ms filtering<br>Overcurrent message with 4.6ms filtering | (r) |

1. SECLK: see control word 3B on page 23

| **Control Word 5 (selects I/O stage for ADC-measurements)** | | | | | | | | **Adr. 0x1B** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry : 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | - | - | - | - | SELES3 | SELES2 | SELES1 | SELES0 |

| Bit3..0 | SELES3 | SELES2 | SELES1 | SELES0 | Selection of I/O stage | |
|---|---|---|---|---|---|---|
| SELES3..0 | 0 | 0 | 0 | 0 | I/O stage 1 | (r) |
| | 0 | 0 | 0 | 1 | I/O stage 2 | |
| | 0 | 0 | 1 | 0 | I/O stage 3 | |
| | 0 | 0 | 1 | 1 | I/O stage 4 | |
| | 0 | 1 | 0 | 0 | I/O stage 5 | |
| | 0 | 1 | 0 | 1 | I/O stage 6 | |
| | 0 | 1 | 1 | 0 | I/O stage 7 | |
| | 0 | 1 | 1 | 1 | I/O stage 8 | |
| | 1 | 0 | 0 | 0 | I/O stage 9 | |
| | 1 | 0 | 0 | 1 | I/O stage 10 | |
| | 1 | 0 | 1 | 0 | I/O stage 11 | |
| | 1 | 0 | 1 | 1 | I/O stage 12 | |
| | 1 | 1 | 0 | 0 | I/O stage 13 | |
| | 1 | 1 | 0 | 1 | I/O stage 14 | |
| | 1 | 1 | 1 | 0 | I/O stage 15 | |
| | 1 | 1 | 1 | 1 | I/O stage 16 | |

| **Control Word 6 (ADC settings)** | | | | | | | | **Adr. 0x1C** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry : 0x00 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | - | - | SVREF | EW | EME | SELAD2 | SELAD1 | SELAD0 |

| Bit2..0 | SELAD2 | SELAD1 | SELAD0 | Settings for ADC measurements | |
|---|---|---|---|---|---|
| SELAD2..0 | 0 | 0 | 0 | A/D-Converter disabled | (r) |
| | 0 | 0 | 1 | Current measurement IO[1] | |
| | 0 | 1 | 0 | Voltage measurement high at IO[1] | |
| | 0 | 1 | 1 | Overall voltage measurement range at IO[1] | |
| | 1 | 0 | 0 | Voltage measurement low at IO [1] | |
| | 1 | 0 | 1 | VBy voltage measurement (y:1..4)[2] | |
| | 1 | 1 | 0 | VBG voltage measurement | |
| | 1 | 1 | 1 | Temperature measurement | |
| Bit3<br>EME | 0<br>1 | Measurement range extention "OFF" (for voltages up to 0.6V)<br>Measurement range extention "ON" (for voltages up to 5V)<br><br>For voltage measurements, the range extention can be either High or Low . | | | (r) |
| Bit4<br>EW | 0<br>1 | A/D converter "OFF"<br>A/D converter activated<br>Bit automatically resets to ’0’. | | | (r) |
| Bit5<br>SVREF | 0<br>1 | Internal reference voltage V(VREFAD) is used<br>External reference voltage at Pin VREF is used | | | (r) |

1. The corresponging I/O stage is selected via bit (3:0) of control word 5.
2. VBy is selected in control word via bits SELES(3:0). VB1 measurements apply to SELES(3:0) = 0x0...0x3, VB2 measurements apply to SELES(3:0) = 0x4...0x7, VB3 measurements apply to SELES(3:0) = 0x8...0xB and VB4 measurements apply to SELES(3:0) = 0xC...0xF.

| **Interconnection Error, Device Identification (read only)** | | | | | | | | **Adr. 0x1D** |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | | reset entry : 0x15 |
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Name | IBA | USVB | NRESA | DID4 | DID3 | DID2 | DID1 | DID0 |

| Bit7<br>IBA | 0<br>1 | No message<br>Interconnection error, broken bond wire at GNDA or GNDD | (r) |
|---|---|---|---|
| Bit6<br>USVB | 0<br>1 | No message<br>Undervoltage at VB4, VB3, VB2 or VB1 | (r) |
| Bit5<br>NRESA | 0<br>1 | No message<br>NRES is 0 | (r) |
| Bit4..0<br>DID4..0 | | Device ID for iC-JX: 0b10101 | (r) |

’-’ spare storage space with no funktion; ’0’ after reset.
(r) reset entry

## DESCRIPTION OF FUNCTIONS

### Interfaces

iC-JX can be operated with either a serial or parallel interface. This is set using pin NSP. When this pin is connected to VDD the device works in parallel mode. With NSP connected to ground iC-JX operates in serial mode.

### Operation with a parallel interface

The parallel interface in iC-JX consists of 8 data, 5 address and 3 control lines. Address lines A4...0 are used to select the registers in iC-JX. The addresses are accepted with the falling edge of chip select signal NCS. Control lines NRD and NWR govern read and write access. A circuit diagram of the parallel microcontroller interface is given in Figure 6.

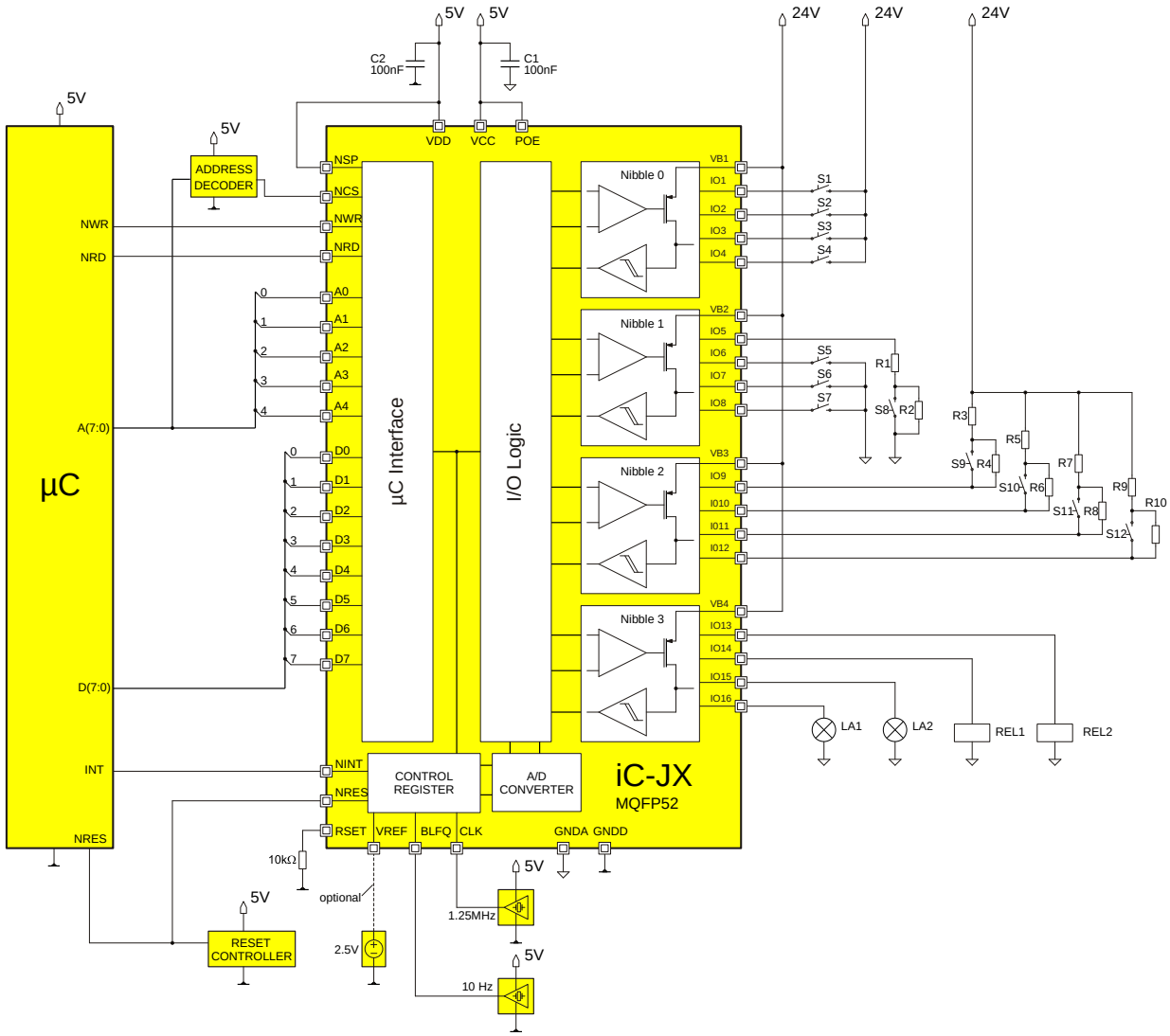



Figure 6: Example application using a parallel interface

### Operation with a serial interface

To reduce the number of lines running between the microcontroller and iC-JX and thus to economize on the use of optocouplers between the former and either one or several iCs in a unit, for example, an extended serial-peripheral interface (SPI) has been integrated into iC-JX. In order to ensure communication between the iC-JX and standard micro controllers, address and data words are both eight bit wide. A possible wiring is shown in Figure 7.

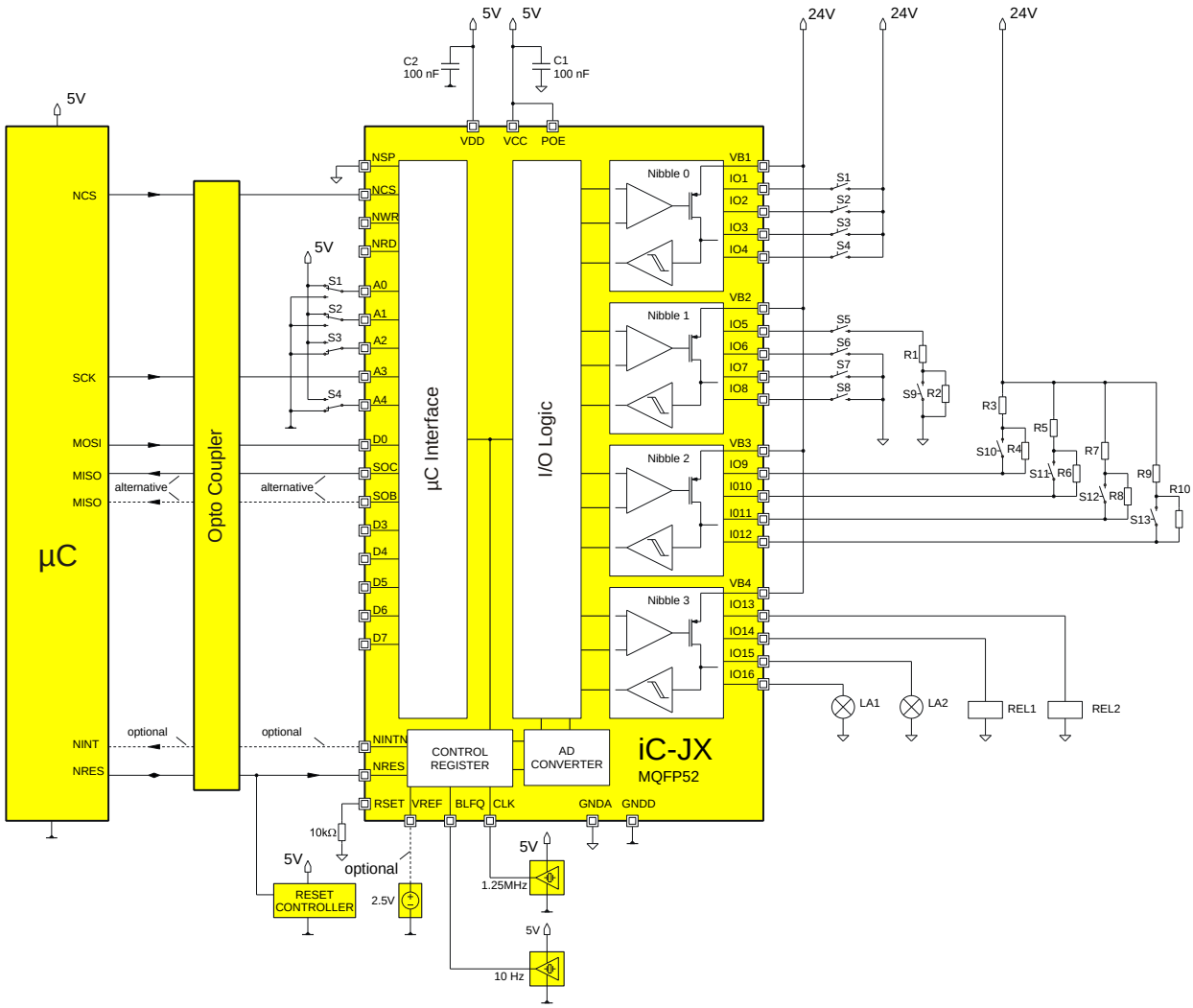



Figure 7: Example application using a serial interface

Several iC-JXs can be operated on an SPI. If the devices are to be configured as a chain, up to three can be placed in a row; with buses, four devices can be used. To this end iC-JX's SPI has both a clock input (SCK) and chip select input (NCS) and a data input (SI) and data output for chain operation (SOC, Serial Out Chain) and bus operation (SOB, Serial Out Bus).
The configuration is set using pin A2. If this is at 0, the devices are in chain operation; if this is at '1', the chips switch to bus configuration.
In chain configuration (see Figure 8, top) output SOC of a device is connected up to the SI data input of the following chip; output SOB is not used. During the addressing sequence (1 byte of communication) all iC-JXs are switched through transparently so that all devices receive the transmitted address simultaneously. Only the addressed chip then goes into data transfer mode; the others remain transparent so that communication between the controller and addressed iC-JX can take place without delay. It must be noted here that even in transparent mode each iC-JX has a certain transmit time which has an effect on the maximum data frequency of the overall system. The advantage of this configuration lies in the fact that it is possible to read out the values of an address in all devices very quickly.
In bus configuration (see Figure 8, bottom ) all SI inputs and SOB outputs are switched in parallel; the SOC outputs are not used. Addressing the devices ensures that only one of the chips outputs data to SOB; the outputs of the inactive iCs are switched to tristate. This type of configuration differs from chain configuration in that it permits higher clock rates and also allows up to four iC-JXs to be connected up to an SPI bus.

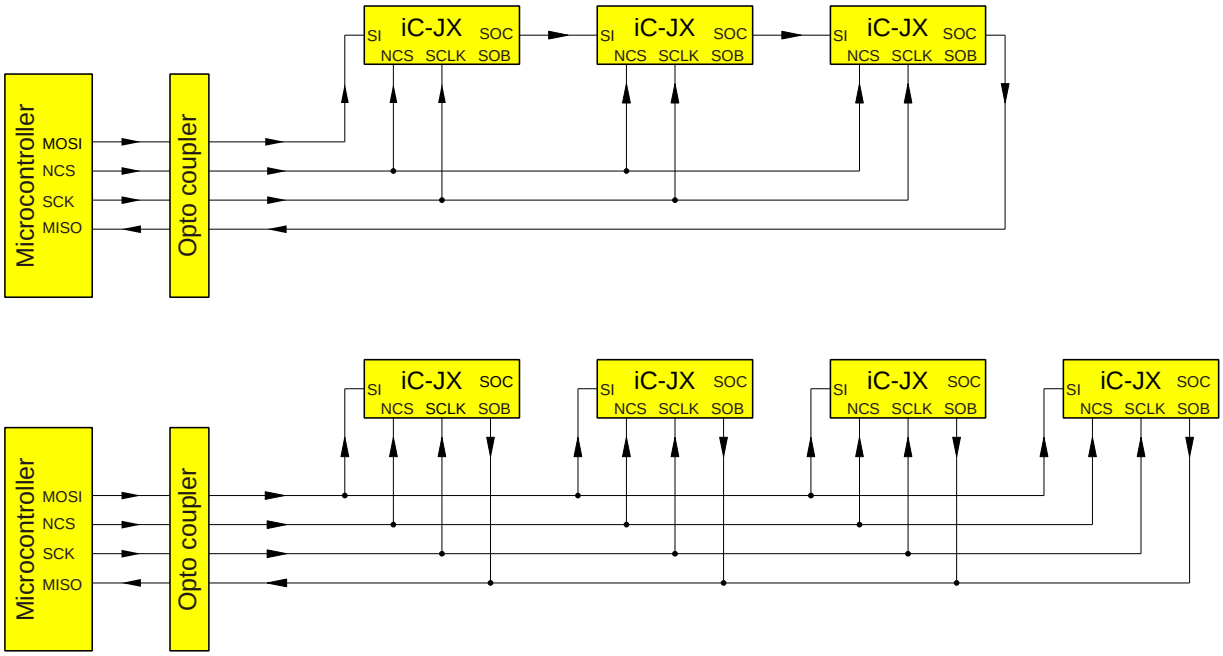



Figure 8: Possible SPI configurations

If no communication takes place on the SPI the chips can send interrupts to the controller by switching the master MISO line to 0. To this end all iC-JXs in chain configuration are switched through transparently (see Figure 9). In bus configuration the relevant chip drives a 0 at its SOB output towards the pull-up resistors at the outputs of the other devices.

Using pin A4 settings can be made as to whether interrupts are signaled to the master via the SOB or SOC (0 = no interrupt message; 1 = interrupt message). The message must be deactivated in bus configuration if further devices are present on the SPI bus as otherwise data can collide on the bus which is not desirable here.

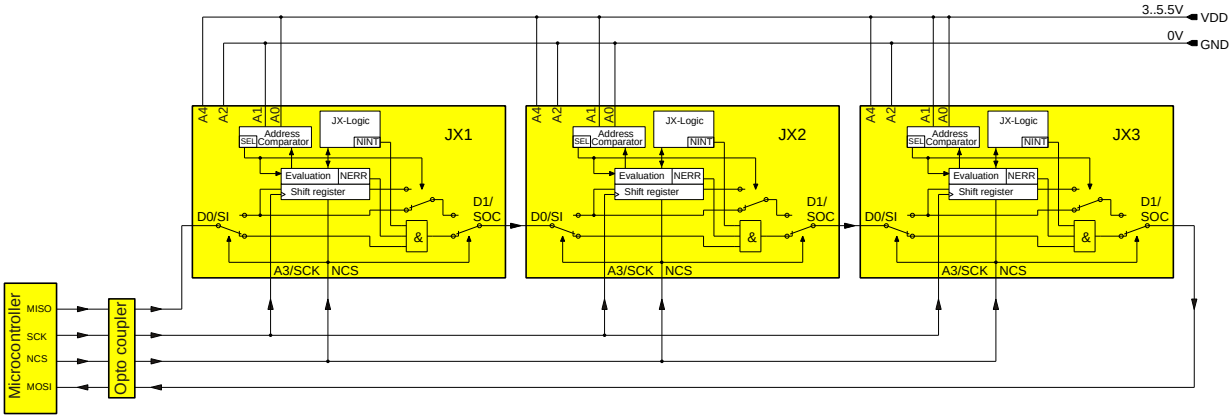



Figure 9: Addressing and interrupt messaging scheme in chain configuration

The first byte of communication (see Figure 10) consists of the 2-bit chip address (BA1:0), the 5-bit register address (RA4:0) and a read-not-write (RNW) bit. The device ID is set for each chip using pins A(1:0).

Note must be taken here of the fact that in chain configuration the device ID 0b00 is not permissible. If it is set, the device acts as if it did not exist (and is permanently transparent). This makes it possible to test the deactivation of a chip without blocking the interface. Used in chain configuration, the address 0b00 addresses all iC-JXs simultaneously in a process known as broadcasting (see page **??**); the other addresses are used to select an individual chip. In chain configuration up to three devices can thus be driven on an SPI master. In bus configuration address 0b00 has no special function, making it possible to address four iC-JXs with one NCS line.

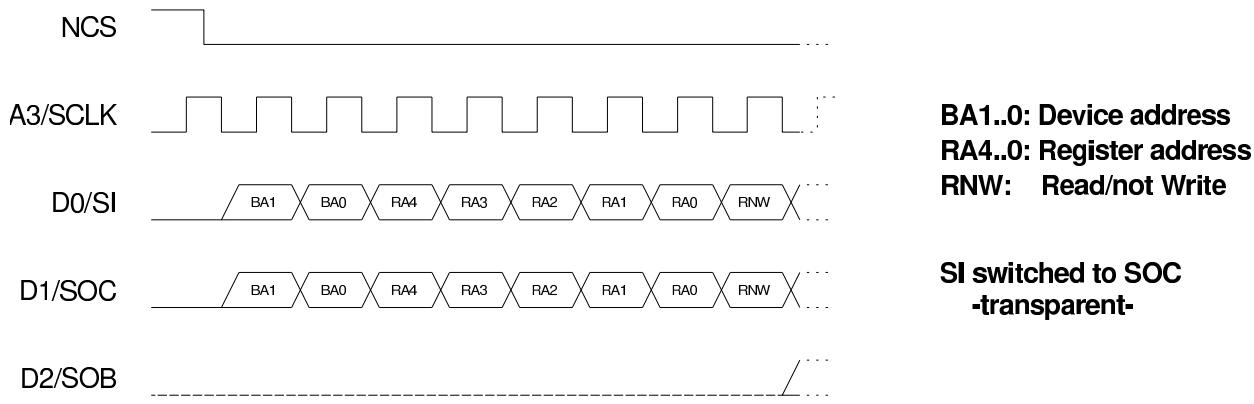



Figure 10: Addressing sequence

**Reading from an iC-JX** (Figure 11):

In both types of configuration one or more values can be read during a transmit cycle. The first byte sent by the controller (master) is the address the data is to be read out from. The activated iC-JX (slave) sends the address back in the next byte by way of verification while the master sends an NOP (no operating) byte. The slave then sends the required data. The master sends the number of bytes to be read out minus one (in this case the value 0). To increase security the number byte is split into two nibbles which are encoded with the original and inverted value (0 → 0b00001111).

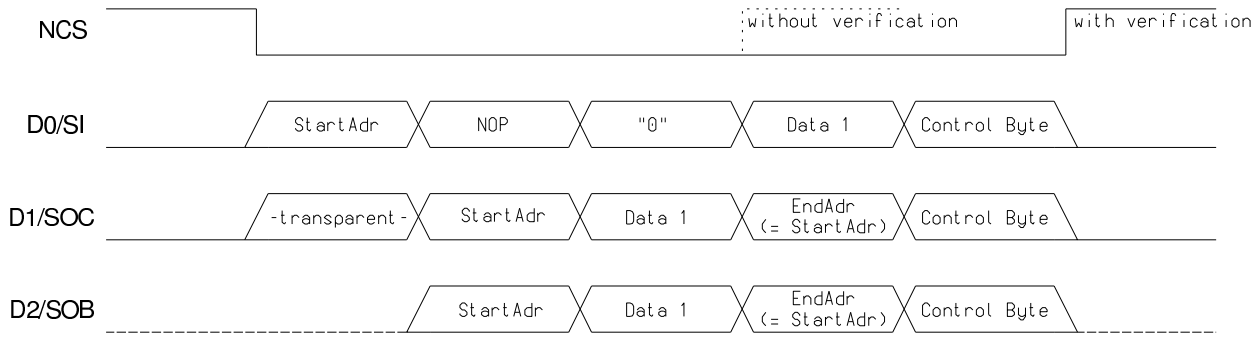



Figure 11: Reading a single register value

If verification in whatever form is dispensed with, the master can end the read cycle at this point. The master otherwise sends the received data back to the slave which then returns the address of the read register (in this instance the start address) by way of verification. If this does not match the one originally sent by the master, the master can then abort communication and repeat if necessary. If the address is correct, in the next stage of the procedure the master transmits the control byte optimized for maximum error recognition (0b01011001).

For its part the slave checks that the returned data is correct; if this is so, it then also transmits the control byte 0b01011001. In the event of error an inverted value of 0b10100110 is sent. During the transmission of this control byte the setup also checks whether the signals at SI and SOx are synchronous. If this is not the case (due to a spike occurring at SCK, for example), the slave transmits the inverted control byte as soon as it has detected the error.
The master recognizes a correct transmission by the fact that the control byte has reached it without error.

If data from several consecutive registers is to be read out (see Figure 12), the autoincrement function enables an abbreviated transmission protocol to be run using iC-JX. Here the master does not send a 0 code after the address of the first register value and the NOP byte but the number of registers to be read out minus one (an entry of 1..15 results in a readout of 2..16 bytes). Here, too, the inverted value is transmitted in the second nibble of the byte. The addressed iC-JX then transmits the consecutive register values and after one byte checks the data returned from the master for errors. Once the required number of register values has been sent the slave transmits the address of the last register addressed, followed by the control byte 0b01011001 with error-free transmission or the inverted value 0b10100110 with an error in transmission. During transmission of the control byte the synchronism of the signals at SI and SOx is again checked; if these are not synchronous, on recognition of this fact the slave then transmits the inverted control byte.

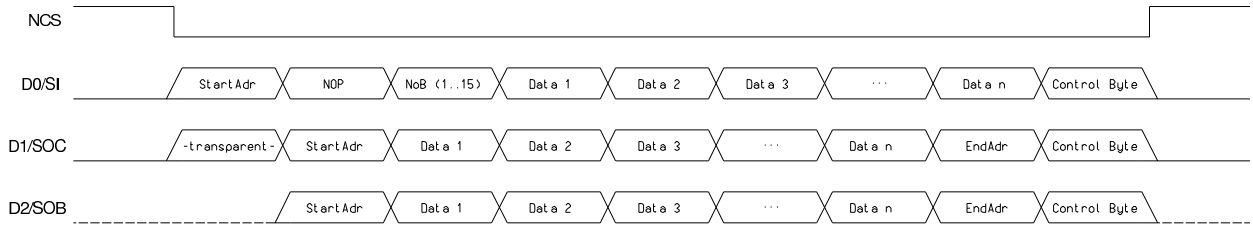



Figure 12: Reading several values of consecutive register addresses (autoincrement)

**Writing to an iC-JX** (Figure 13, Figure 14):

In the write process one or several registers can be written to during a transmit cycle. To this end the master first sends the start address and the numerical amount of data to be transmitted minus one. As in the read process this value is transmitted as two nibbles (non-inverted and inverted) to increase security. Data from consecutive addresses is then sent. iC-JX returns the master data with a delay of one byte, allowing the master to constantly monitor whether an error has occurred during the addressing sequence or data transmission. If an error is detected, the master can prevent the faulty data being accepted by the slave registers by ending communication.

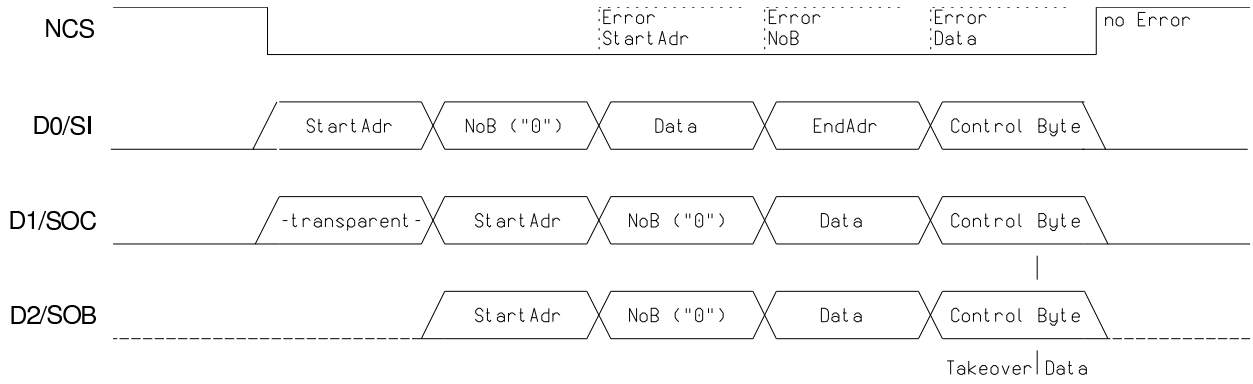



Figure 13: Writing one register value

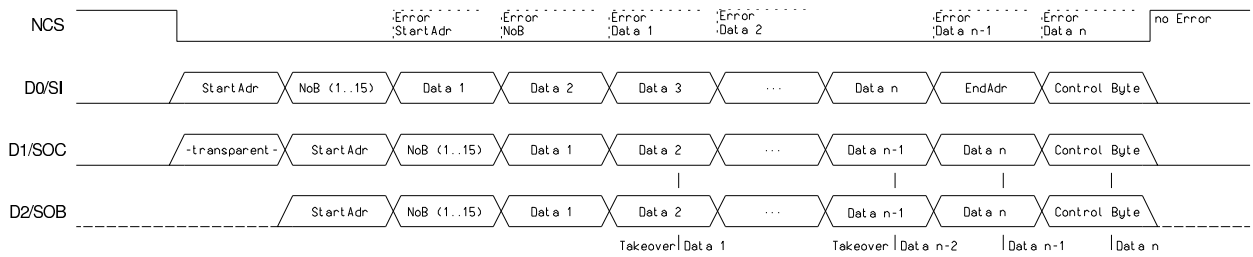



Figure 14: Writing several register values

**Error handling**

In order to reduce processing time complex technology, such as CRC, etc., is not used for error handling. The transmitted addresses and data are instead returned by the recipient to the sender where they are compared to the original data transmitted.

Should the master detect an error, it can abort communication in such a way so as to prevent incorrect values being written to the slaves.

If an individually addressed slave determines that the data it has sent has been returned to it incorrectly or that the number of clock pulses is not a multiple of 8 bits, it can signal this error to the master by inverting the closing control byte.

**RSET settings**
iC-JX can either generate an internal reference current or permit external current settings via pin RSET. Setting the current externally is the more precise option here; to this end it is recommended that pin RSET be linked up to a 10 kΩ resistor connected to ground..

**I/O stages in input mode funktion**
Input registers (add. 0x00 and 0x01: reading the inputs
A high at IOx generates a high signal at bit INx. Any change to an input signal is accepted via digital filtering only after the selected filter time has expired. Here, the input comparator of each I/O stage reverses the count direction of a 3-bit counter. The counter output changes only when the final status has been reached. The counters are reset to a value of 3 by a low signal at reset input NRES. The counter is clocked externally by pin CLK or by clock ICLK, generated internally.

The scaling factor for the clock frequency and the input filter bypass can be programmed separately for all four nibbles (see control word 1, addresses 0x14 and 0x15). Switching the bypass (BYP1...4) permits operation without an external clock signal (see below).

Once the change-of-input message has been enabled in the change-of-input interrupt enable register (addresses 0x10 and 0x11) a change of level at one of the I/O pins is signaled to the microcontroller. If iC-JX is operated at the parallel interface the level at pin NINT is set to 0. If the device is operated at the serial interface a change of level is indicated by a 0 at pin SO(D1) resp SOB (D2), depending upon configuration (see SPI interfacd, page 26). The microcontroller can determine which I/O stage has had a change of input by reading out the input register.

**I/O stages in output mode**
Input registers (addresses 0x00 and 0x01): reading the output feedback
A high at IOx generates a high signal at INx. This allows the microcontroller to make a direct check of the switching state and, with the help of the programmable high-side current sources of 200 µA, 600 µA and 2 mA, to monitor the channel for any cable fractures. As with the reading of inputs the feedback signals can be output in their filtered or unfiltered state. The microcontroller can determine which I/O stage has had a change of input by reading out the input register.

**Programmable Current Sources**
(Adr. 0x16 und 0x17)
The programmable pull-up- resp. pull-down current sources can be set independently of the I/O mode (either input or output mode). In both modes current values of 200 µA, 600 µA or 2 mA are available either as pull-up or pull down.

**ADC measurements**
**ADC measurements: measuring current (Adr. 0x1C)**
In this mode the current in each output stage can be measured. Here, the saturation voltage from an internal reference transistor is used for comparison. Each output stage has its own reference transistor in order to guarantee a precise value. The reference voltage is equivalent to the saturation voltage of the output stage transistor with a nominal current of 150 mA; the output digital value thus corresponds to the current intensity in the output stage.

To evaluate current variations in the output stage the controller must perform an initial measurement with a known reference current. Based on this value a monitoring of the load current can then be performed. The output stage thereby is selected via SELES(3:0) in control word 5 (Adr. 0x1B).

**ADC measurements: measuring voltage (Adr. 0x1C)**
iC-JX enables voltage at the I/O stage to be recorded. The range for voltage measured at the output stage lies between VB - 5 V and VB (bit EME = 1) and between VB - 0.6 V and VB (EME = 0). When measuring in conjunction with pull-up current sources the range lies between 0 V and 5 V (EME = 1) and between 0 V and 0.6 V (EME = 0).

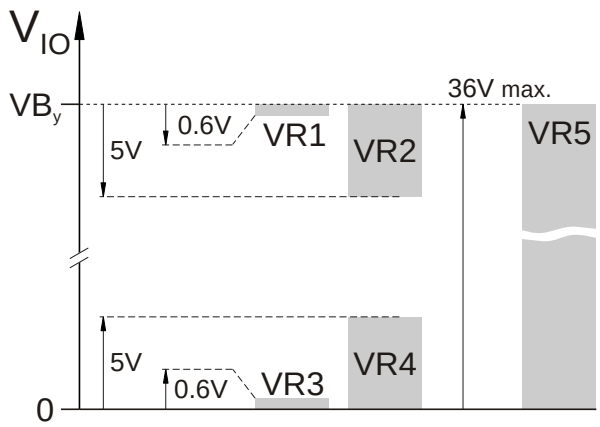



Figure 15: ADC measurement ranges

The iC-JX measures voltages at the I/O stages in different ranges. The range "Voltage Measurement High at IO" is between VB – 5 V and VB (Bit EME = 1) resp. between VB – 0.6 V and VB (EME = 0). In the mode "Voltage Measurement Low at IO" the range is between 0 and 5 V (Bit EME = 1) resp. between 0 and 0.6 V and VB (EME = 0).

For the mode "Overall Voltage Measurement at IO" the voltage at the selected I/O stage is downscaled first by a factor of 1/15 using a resistive voltage divider to permit measurement of the full voltage range from rail to rail. The user must be aware of a input current drawn by the voltage divider of approimately V(IO)/200kΩ. The selection of the I/O stage is done via control word 5 (Adr. 0x1B).

**ADC Measurements: VBy and VBG Measurements (Adr. 0x1C)**
The internal reference voltage VBG and the external supply voltages VB1 to VB4 can also be measured. For VB1 to VB4, the voltage is downscaled first by a factor of 1/15. Selection is done via SELES (3:0) in control word 5 (Adr. 0x1B) as described in the following table.

| SELES(3:0) | VB - Messung |
|---|---|
| 0x0 .. 0x3 | VB1 |
| 0x4 .. 0x7 | VB2 |
| 0x8 .. 0xB | VB3 |
| 0xC .. 0xF | VB4 |

**ADC Measurements: Temperature Measurement (Adr. 0x1C)**
In this feature the internal chip temperature can be determined.

**ADC Measurements: External Vref (Adr. 0x1C)**
To improve accuracy of the A/D conversion, an external reference voltage at pin VREF can be used by setting the bit SVREF to '0b1'. The value of the external voltage reference should be about 2.5V ±0.2%.

**ADC Measurements: Output**
A 10 bit digital value as a result of A/D convertion is available for output currents and output voltages at a selected I/O stage, for chip temperature and supply voltages Vby and the internal bandgap voltage VBG. Except for the current measurement, the internal voltage V(VREFAD) (for Bit SVREF = '0') or an external voltage at pin Vref (for Bit SVREF = '1') are used as reference. The end of A/D conversion is signalled by a low signal '0' at NINT resp. D1/SOC or D2/SOB.

**Output register (Adr. 0x0C und 0x0D):**
Switches the various output stages on and off (for POE = 1).

**Flash pulse enable (addresses 0x0E und 0x0F):**
Enables flash mode
This function enables each of the various output stages to be set to flash mode, providing the value of the corresponding output register is 1. The flash frequency is derived from BLFQ or, alternatively, can be generated from CLK or from the internally generated ICLK (via SEBLQ in control word 3B, address 0x1A). Different flash frequencies can be set for all four nibbles.

**Interrupts**
Interrupt readings at NINT can be triggered by a change of (filtered) input signal, by an overcurrent message signaled at an I/O pin (due to a short circuit, for example), by undervoltage at VCC or VDD, by bursts at VDD, by the end of A/D conversion or by exceeding maximum temperature thresholds (2 stages).
Interrupt outputs for each individual I/O stage can be caused by a change of input, or, with stages in output mode, by a short circuit. The relevant interrupt enables determine which messages are stored and which are displayed. The display of interrupt messages caused by excessive temperature, A/D conversion, undervoltage or bursts is not maskable; this particular function is permanently enabled.
When an event occurs which is enabled to produce an interrupt message pin NINT is set to 0 when a parallel interface is used. If the device is being operated with a serial interface outputs D1/SOC or D2/SOB are set to 0 when an interrupt occurs if no communication is made via the interface itself and pin A4 ist set to '1' .
By reading out the interrupt status register (addresses 0x04 and 0x05) the nature of the message can be determined and the I/O stage causing the interrupt located. Thus with a change-of-input message the problematic I/O stage is shown in the corresponding register (addresses 0x02 and 0x03); with an overcurrent interrupt the overcurrent status register (addresses 0x06 and 0x07) pinpoints the I/O stage with a short circuit.
Interrupts are deleted by simply setting EOI in control word 4 (address 0x1A). This bit then automatically resets to 0. If during operation the I/O mode is switched, i.e. from input to output mode, all interrupt messages are deleted via EOI.
To avoid interrupt messages caused by other sources in the time between the readout of a status register and the deletion of the current interrupt being overlooked successive interrupts are stored in a pipeline. If successive interrupts occur outputs NINT resp. D1/SOC or D2/SOB remain at 0 after the present interrupt has been deleted using EOI. The new interrupt source is displayed in the interrupt status register and in the specific status registers.

**Overcurrent messages**
If an overload occurs at one of the outputs the current in IOx is limited. In this instance an interrupt message is triggered, providing relevant interrupt enables have been set for overcurrent messages (addresses 0x12 and 0x13) and the filter time set with control word 4 (address 0x1A) has elapsed. ISCI is then set in the interrupt status register (address 0x04) and the relevant bit for the I/O stage causing the problem is set

in the overcurrent message register (addresses 0x06 and 0x07).

At addresses 0x08 and 0x09 the actual, unfiltered overcurrent status of each I/O stage can be read; a global scan of all I/O stages is also possible via bit SCS in the interrupt status register. This shows whether any of the I/O stages have overcurrent at the time of the readout. This short-circuit messaging allows permanent monitoring of the output transistors and clear allocation of error message to affected I/O stage. Filtering of the overcurrent message can be shutdown using a bypass; this bypass can be activated for all I/O stages together using BYPSCF in control word 4 (address 0x1A).

**Temperature monitoring**
iC-JX has a two-stage temperature monitor circuit.

Stage 1: A warning interrupt is generated if the first temperature threshold (Toff1 at ca. 132 °C) is exceeded. Suitable measures to decrease the power dissipation of the driver can be implemented using the microcontroller.

Stage 2: If the second temperature threshold is exceeded (Toff2 at ca. 152 °C), a second interrupt is generated. At the same time the output transistors and the I/O stage current sources are shutdown and the output register and flash pulse enable deleted. Once the temperature has returned to below the level of Toff1 the current sources are reactivated. The output register and flash pulse enable have to be respecified to reactivate the output stages

The interrupt status register (address 0x04) provides information as to the temperature interrupt stage but also on the current status of the temperature monitor. ET2 and ET1 statically indicate when Toff2 and Toff1 are exceeded, whereby stored interrupt messages IET2 and IET1 and the display at NINT via EOI = 1 can be deleted (control word 4, address 0x1A).

**Undervoltage detection: VCC and VDD**
When the supply voltage at VCC or VDD is switched on the output transistors are only released by the undervoltage detector after power-on enables VCCon or VDDon have been reached. Should the supply voltage drop to VCCoff or VDDoff during operation the I/O stages are disabled, i.e. the output transistors are turned off and the device reset. At the same time interrupt outputs are set. USD and USA in interrupt status register B (address 0x05) statically indicate undervoltage at VCC and VDD. Stored interrupt messages IUSD and IUSA and the display at NINT or SO(D1) can be deleted by setting EOI to 1 in control word 4 (address 0x1A). Should the supply voltage then again rise to VCCon or VDDon, iC-JX assumes a reset state.

**Undervoltage detection: VB1...4**
In order to guarantee the fail-safe operation of connected loads voltage VB is also monitored. If the voltage drops below threshold VBoff the I/O outputs are disabled. Neither a device reset nor an interrupt message to the microcontroller are then triggered. Once voltage VB again rises above VBon the I/O outputs are re-enabled. The microcontroller can read out the status of voltage VB at bit DID1 in the device ID register (address 0x0C). In the event of error (VB < VBoff) this bit is set to 1.

**Pin monitoring GNDD and GNDA**
iC-JX includes a pin watchdog circuit which monitors the connection between the two ground pins GNDA and GNDD. The microcontroller can detect a possible error, such as a disconnected iC lead, for example, by reading bit IBA in the device ID register. In the event of error this is set to 1. If such a case of an error is present, then the potential of the missing ground pin is raised, which can lead to the shift of the trigger levels.

**Burst detection at VDD**
As in principle bursts at VDD can influence the contents of registers iC-JX monitors spikes in the supply. If any hazard is detected interupt outputs are set to 0. Stored interrupt message ISD (interrupt status register B, address 0x05) can be deleted by setting EOI to 1 in control word 4 (address 0x1A).

**Device identification**
An identification code has been introduced to enable identification of iC-JX. Bit pattern 0b10101 can be read out at address 0x0D.

**Reset**
A reset (NRES = 0) sets the register entries to the reset values given in the tables.

**Operation without the BLFQ signal**
Should no clock signal be available at pin BLFQ iC-JX can generate an internal flash pulse from the external clock signal at pin CLK or from clock signal ICLK which is generated internally. For the flash frequency to be derived from the system clock pulse bit SEBLQ in control word 3B (address 0x19) must be set to 1. The flash period is then calculated by dividing by $2^{19}$.

**Operation without the CLK signal**
iC-JX can also be operated without a clock pulse at pin CLK. Using control word 3B (address 0x1A) the device can be set to an internally generated clock frequency; In this instance all filter functions remain fully available.

Via SECLK(1:0) in control word 3B the clocked filtering for the I/O signals and overcurrent messaging can also be deactivated. The same behavior can be obtained by setting BYP0, BYP1, BYP2 and BYP3 in control word 1 (addresses 0x14 and 0x15) together with BYPSCF in control word 4 (address 0x1A); all filters are avoided by way of a bypass circuit. Here it must be noted that interferences in the line can lead to the unwanted display of interrupts.

**Forced shutdown of output stages**
The output stages can be forcibly shutdown at input POE. A '1' enables logic access to the drivers; a '0' disables this. This function allows a processor-independent watchdog to lock the outputs in the event of error, for example. An integrated pull-down resistor increases safety.

## DESIGN REVIEW: Notes On Chip Functions

| **iC-JX X2** (and previous) | | |
|---|---|---|
| No. | Function, Parameter/Code | Description and Application Hints |
| 1 | Leakage current beyond operating conditions (Electrical Characteristics Item No. 019 | During operation, supply voltages VCC, VDD and VB1..VB4 must already be present and stable to avoid elevated leakage currents at pins IOx (x=1..16). |

Table 8: Notes on chip functions regarding iC-JX chip version X2 and previous versions

| **iC-JX X3** | | |
|---|---|---|
| No. | Function, Parameter/Code | Description and Application Hints |
| 1 | Leakage current beyond operating conditions (Electrical Characteristics Item No. 019 | Leakage currents < 200 µA |

Table 9: Notes on chip functions regarding iC-JX version X3

## ORDERING INFORMATION

| Type | Package | Order Designation |
|---|---|---|
| iC-JX | MQFP52 | iC-JX MQFP52 |
| Evaluation Board | - | iC-JX EVAL JX2D |

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