Tel: 886-2-66296288
Fax: 886-2-29174598
URL: http://www.princeton.com.tw

DESCRIPTION

PT8211 is a dual channel, 16 bit Digital-to-Analog Converter IC utilizing CMOS technology specially designed for the digital audio applications. The internal conversion architecture is based on a R-2R resister ladder network, internal circuit is well matched and a 16 bit dynamic range is achieved even in whole supply voltage range. PT8211 also enhanced the performance of timing responsibility in digital serial bus, in a company with the fast switching R-2R network that make 8X oversampling audio signal is also supported.

PT8211 can be supported wide range of sample frequency, it is compatible with TDA1311 by functionally. It's digital input timing format is Least Significant Bit Justified (LSBJ), or so called Japanese input format. Digital code format is two's complement and MSB first. PT8211 is available in 8-pin SOP or DIP.

FEATURES

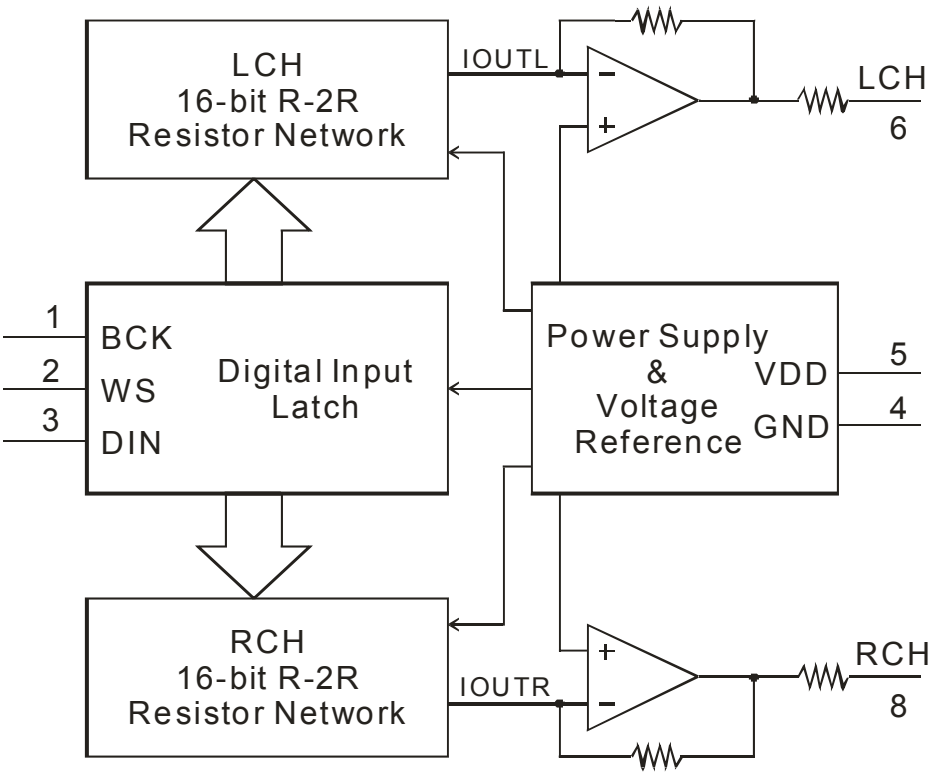
- CMOS technology
- Support 3.3V bus input level
- Low power consumption
- Two audio channel output in the same chip
- 16 bit dynamic range
- Low total harmonic distortion
- No phase shift between both output channel
- Available in 8 pins, SOP or DIP

APPLICATIONS

- Digital audio equipment
- CD ROM/VCD
- Multimedia sound card
- MPEG decoder card

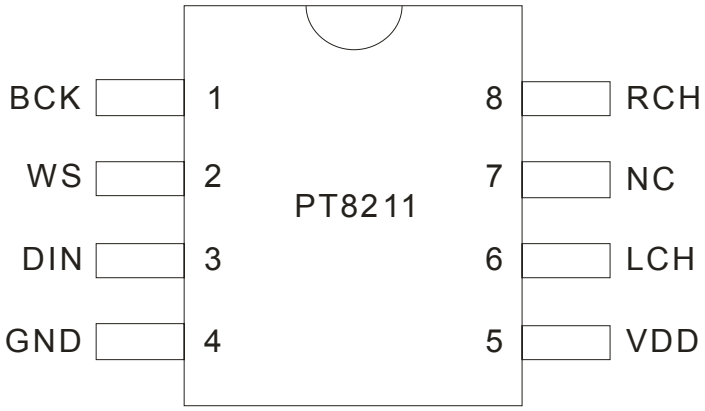
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BLOCK DIAGRAM



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PIN CONFIGURATION



PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.
BCK	I	Serial Bit Clock Input	1
WS	I	Word Select Clock Input Pin	2
DIN	I	Data Input Pin	3
GND	-	Ground	4
VDD	Power	Positive Power Supply	5
LCH	O	Left Channel Output	6
NC	-	No Connection	7
RCH	O	Right Channel Output	8

FUNCTION DESCRIPTION

The serial bus input data format of PT8211 is Japanese or called LSBJ (Least Significant Bit Justified) format. Each valid DIN data will be shifted to the input register in the rising edge of the BCK, only the first 16bit data (from MSB) is valid if the input data length is more than 16bits, other data bit will be truncated. The clock frequency of the BCK could run up to 20MHz and supported to 8× over-sampling in 48KHz WS clock rate. Both left and right data words are time multiplexed. Please refer to the diagrams for timing and input signal formats.

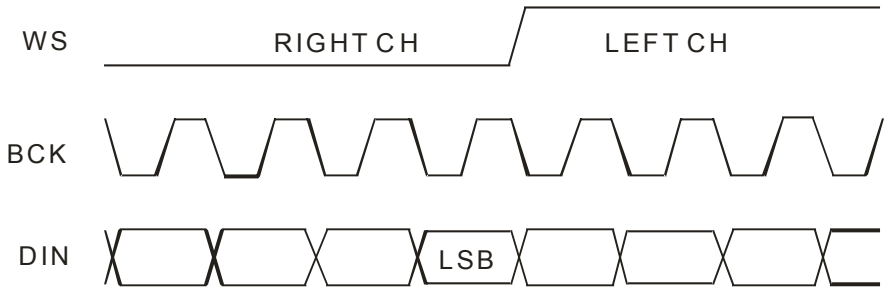


Figure 1. Japanese Input Signal Format

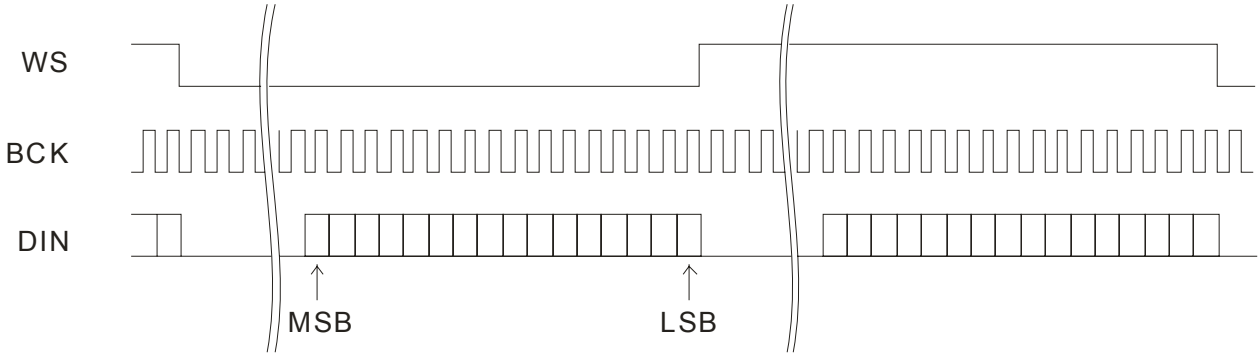


Figure 2. Timing and Input Signal Formats

The DIN data must be the 2's complementary format and the MSB (Most Significant Bit) must be the first. When the Word Select (WS) clock in the Low level, the DIN data will be shifted to the right input register. likewise, the DIN data will be shifted to the left input register when WS clock in the High level. The buffered DIN data then feeding to the DAC after both input register are all settled down, this can eliminated the phase shift happened between two channel output. DAC output is generated by a 16 bit R-2R resistor ladder network. This signal is driven to the Right/Left Channel (RCH/LCH) via the buffer operational amplifier.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Power supply voltage	V_{DD}	-0.3 ~ 7.0	V
Input voltage	V_I	-0.3 ~ V_{DD}+0.3	V
Operating temperature	Topr	-40 ~ +85	℃
Storage temperature	Tstg	-65 ~ +150	℃

DC CHARACTERISTICS

(Test Conditions: Ta=25℃, VDD=5.0V, unless otherwise specified)

Parameter	Symbol	Condition	Min	Typ	Max.	Unit
Power supply voltage	VDD	THD<1%	3	5	6	V
Operating current	Is	VDD=5V	10	13	18	mA
Digital input high level (see Note)	V_{IH}		1.8	2.2	Vcc	V
Digital input low level (see Note)	V_{IL}		GND	1.2	1.8	V

Note: Digital input level will changed due to supply voltage.

TIMING CHARACTERISTICS

(Please refer to the Figure 1)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Bit clock frequency	Fbck	BCK	-	-	18.4	MHz
Word clock frequency	Fws	WS	-	-	384	KHz
Input data rate	Fdin	DIN	-	-	18.4	Mbits/s
H Level time	tH		25			ns
Rise time	tR				20	ns
Fall time	tF				20	ns

ANALOG AUDIO CHARACTERISTICS

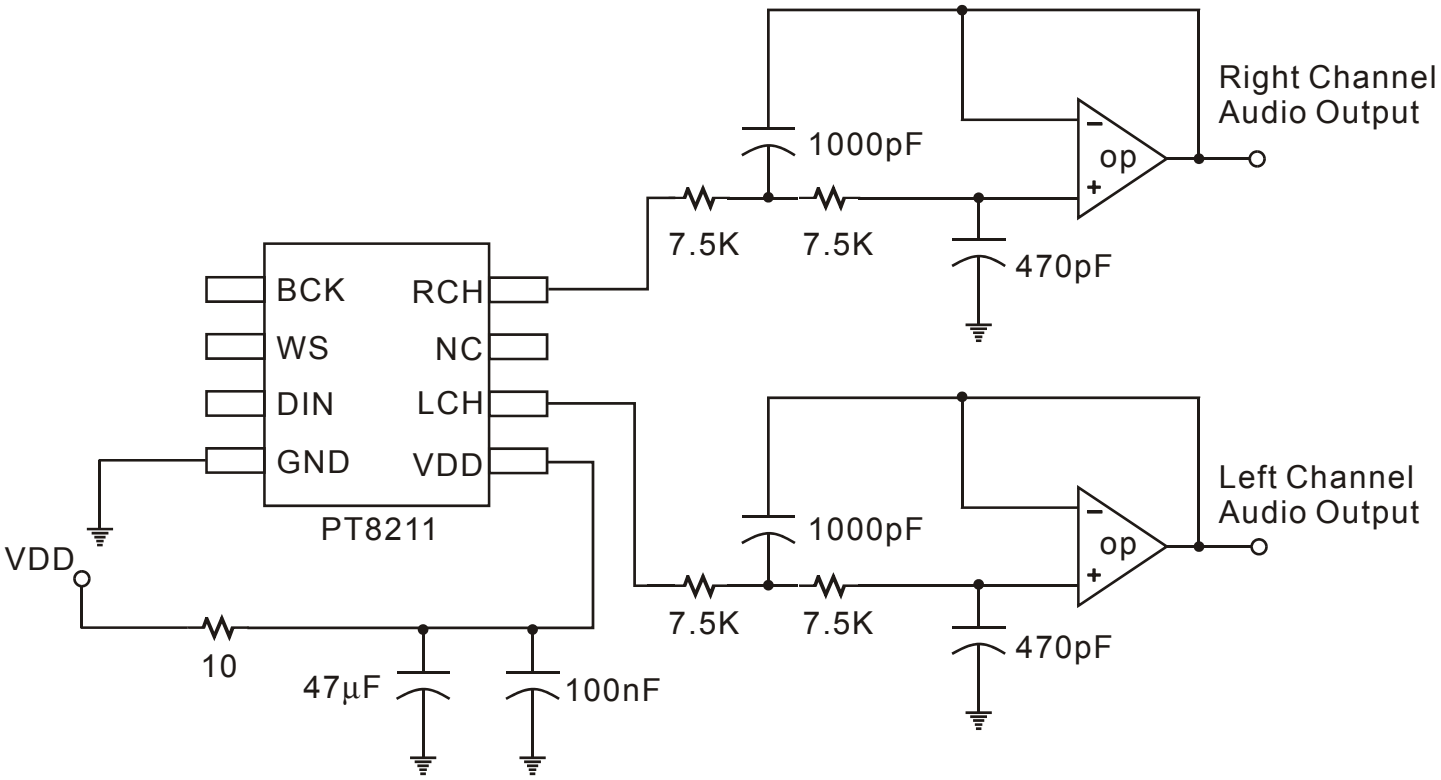
(Unless otherwise specified, Test Condition: Ta=25℃, VDD=5V)

Parameter	Symbol	Condition	Min.	Typ	Max.	Unit
Maximum output level	VO		2.2	2.5	2.7	VPP
Total harmonic distortion	THD	1KHz, 0dB FS	-	0.13	0.3	%
		1KHz, -10dB FS	0.08	0.1	0.2	%
		1KHz,-60dB FS	-	3	6	
Monotonicity	Mt				16	Bit
Dynamic range	DR		85	89	-	dB
Signal to noise ratio	S/N	Data=0000H	89	93	-	dB
		No clock input	-	95	97	
Cross talk	CTa	Both Output Channel	80	89	92	dB
	CTd	Digital in to Analog out	75	80	-	
Phase shift	Pd	Both Output Channel	-	0	0.2	μs

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APPLICATION CIRCUIT AND NOTE

To further suppress residual noise, we suggest placing an additional low pass filter after the analog output of PT8211. Please refer to the circuit diagram below. This is a simple second-order analog post filter. If low noise output is very important for your circuit design we suggest using a regulated power supply.



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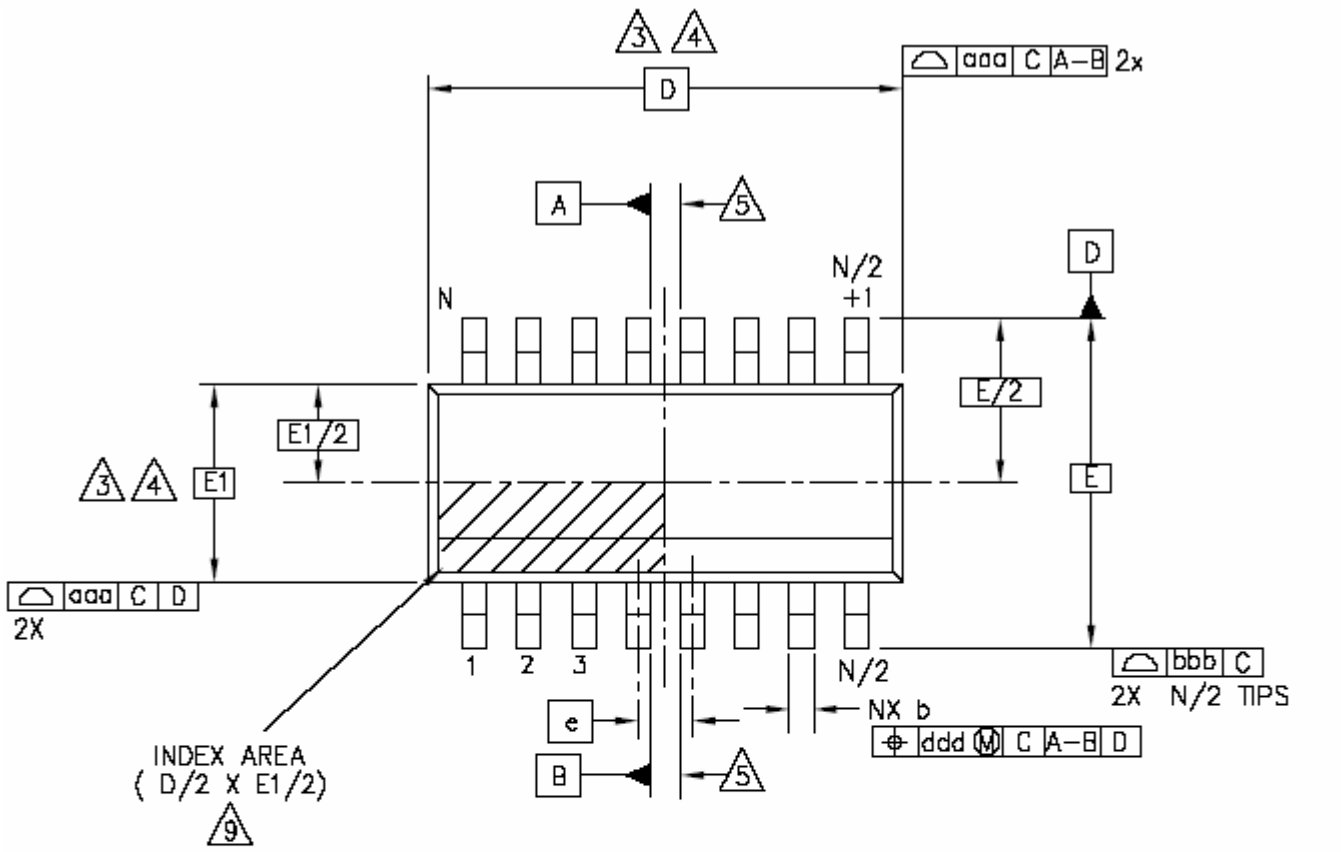
ORDER INFORMATION

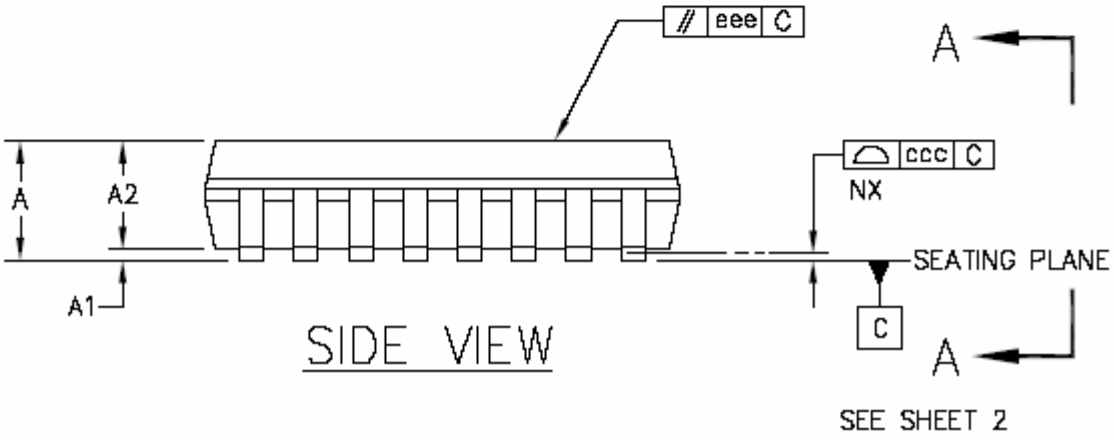
Valid Part Number	Package Type	Top Code
PT8211-S	8 Pins, SOP, 150mil	PT8211-S
PT8211	8 Pins, DIP, 300mil	PT8211

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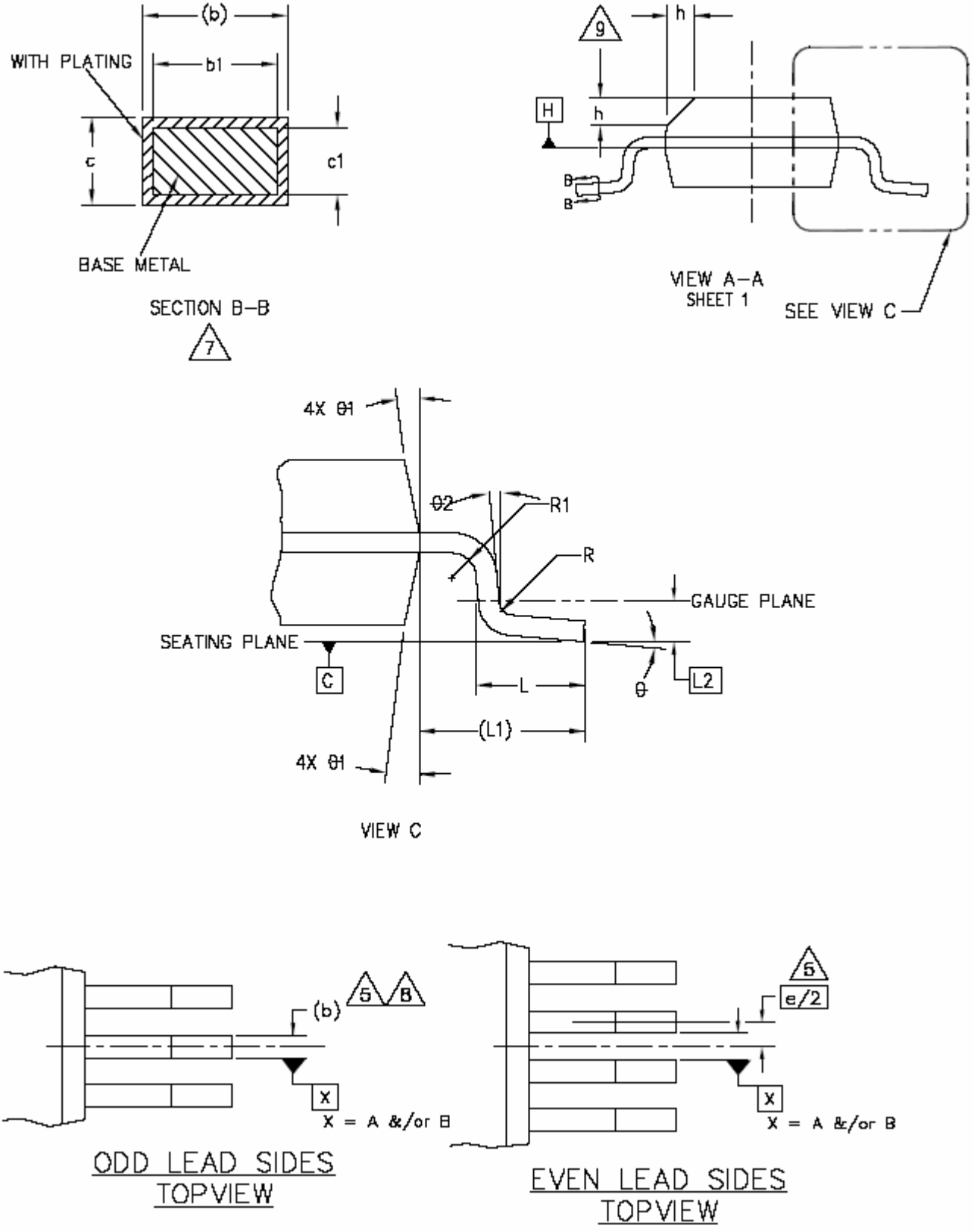
PACKAGE INFORMATION

8 PINS, SOP, 150MIL





SEE SHEET 2


(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
g
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

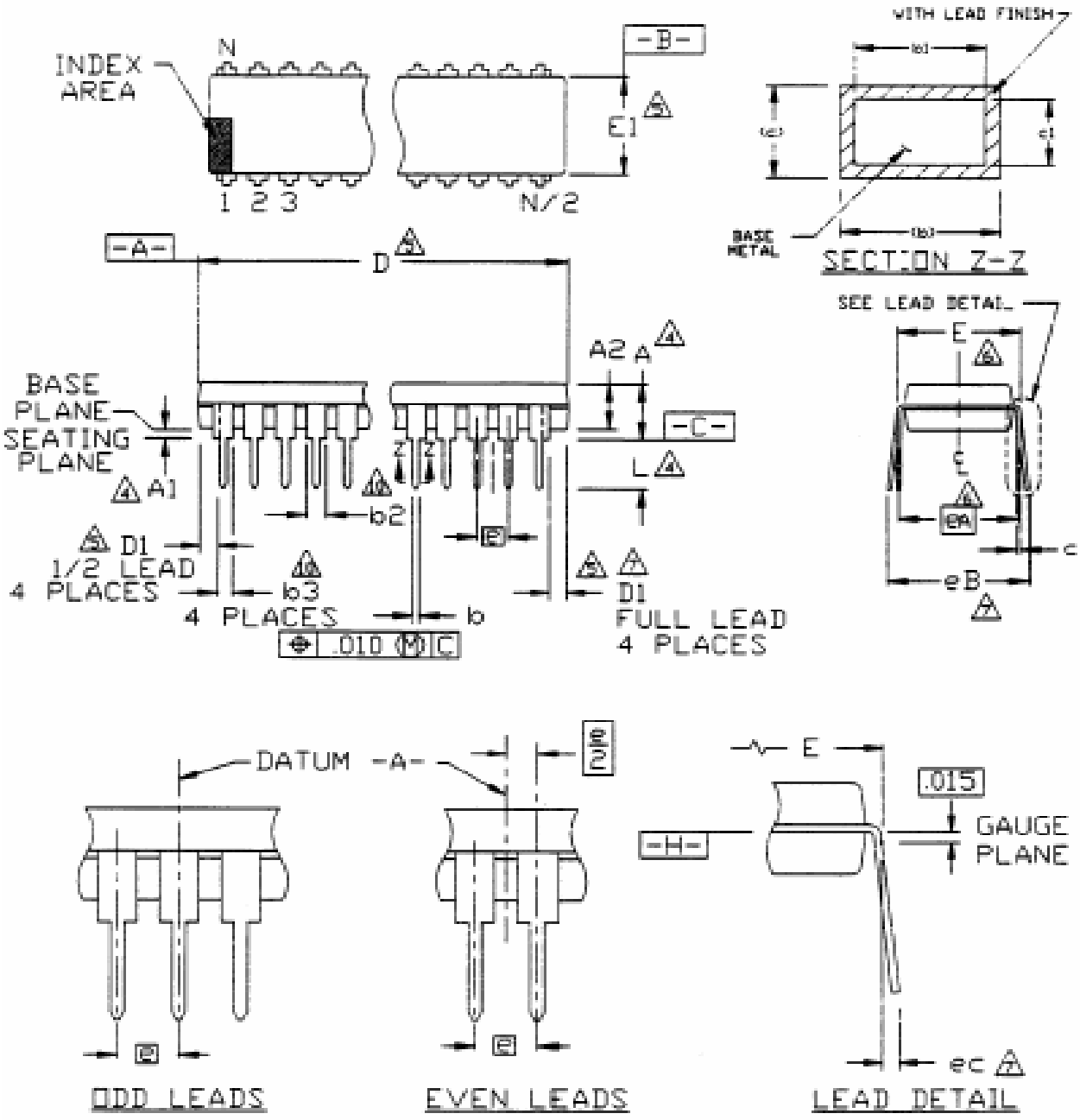
Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	4.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AA.

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8 PINS, DIP, 300MIL



Symbol	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.355	0.365	0.400
D1	0.005	-	
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 bsc.		
eA	0.300 bsc.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. Controlling Dimensions: INCHES.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol LIST” in Section 2.2 of Publication No.95.
4. Dimension A, A1 and L are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
5. D, D1 and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
6. E and eA measured with the leads constrained to be perpendicular to data -c- .
7. eB and eC are measured at the lead tips with the leads unconstrained.
8. N is the number of leads (N=8)
9. Pointed or rounded lead tips are preferred to ease insertion.
10. b2 and b3 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm)
11. Variation BA has a b3 dimension and is 1/2 lead package.
12. Distance between the leads including dambar protrusions to be 0.005 inch minimum.
13. Datum plane -H- coincident with the bottom of lead, where lead exits the body.
14. Refer to JEDEC MS-001, Variation BA.

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