

MOS FIELD EFFECT TRANSISTOR 2SK3113B

SWITCHING N-CHANNEL POWER MOS FET

DESCRIPTION

The 2SK3113B is N-channel MOS FET device that features a low gate charge and excellent switching characteristics, and designed for high voltage applications such as switching power supply, AC adapter.

FEATURES

• Low on-state resistance

 $R_{DS(on)} = 4.4 \Omega MAX. (V_{GS} = 10 V, I_{D} = 1.0 A)$

Low gate charge

 $Q_G = 7.9 \text{ nC TYP.}$ ($V_{DD} = 450 \text{ V}$, $V_{GS} = 10 \text{ V}$, $I_D = 2.0 \text{ A}$)

- Gate voltage rating: ±30 V
- Avalanche capability ratings

<R> ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE		
2SK3113B-S15-AY Note	Pure Sn (Tin)	Tube 70 p/tube	TO-251 (MP-3-a) typ. 0.39 g		
2SK3113B(1)-S27-AY Note		Tube 75 p/tube	TO-251 (MP-3-b) typ. 0.34 g		
2SK3113B-ZK-E1-AY Note		Tape 2500 p/reel	TO-252 (MP-3ZK) typ. 0.27 g		
2SK3113B-ZK-E2-AY Note					

Note Pb-free (This product does not contain Pb in external electrode.)

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

Drain to Source Voltage (Vgs = 0 V) 600 Gate to Source Voltage (VDS = 0 V) Vgss ±30 Drain Current (DC) (Tc = 25°C) ID(DC) ±2.0 Drain Current (pulse) Note1 ID(pulse) ±8.0 Total Power Dissipation (Tc = 25°C) P_{T1} 20 W Total Power Dissipation (T_A = 25°C) Note2 1.0 W PT2 150 °C **Channel Temperature** Tch Storage Temperature -55 to +150 °C Tstg Single Avalanche Current Note3 las 2.0 Α Single Avalanche Energy Note3 Eas 2.7 mJ







Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

- 2. Mounted on glass epoxy board of 40 mm × 40 mm × 1.6 mm
- 3. Starting T_{ch} = 25°C, V_{DD} = 150 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V

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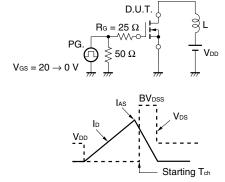
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ELECTRICAL CHARACTERISTICS (TA = 25°C)

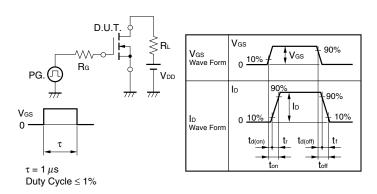
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	Ipss	V _{DS} = 600 V, V _{GS} = 0 V			100	μΑ
Gate Leakage Current	Igss	V _{GS} = ±30 V, V _{DS} = 0 V			±10	μΑ
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		3.5	V
Forward Transfer Admittance Note	y fs	V _{DS} = 10 V, I _D = 1.0 A	0.5	0.9		S
Drain to Source On-state Resistance Note	R _{DS(on)}	V _{GS} = 10 V, I _D = 1.0 A		3.2	4.4	Ω
Input Capacitance	Ciss	V _{DS} = 10 V		290		pF
Output Capacitance	Coss	V _{GS} = 0 V		75		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		7		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 150 V, I _D = 1.0 A		10.5		ns
Rise Time	t r	V _{GS} = 10 V		4.8		ns
Turn-off Delay Time	td(off)	R _G = 10 Ω		15.8		ns
Fall Time	tf	R _L = 10 Ω		10.5		ns
Total Gate Charge	Q _G	V _{DD} = 450 V		7.9		nC
Gate to Source Charge	Qgs	V _{GS} = 10 V		2.7		nC
Gate to Drain Charge	Q _{GD}	I _D = 2.0 A		3.2		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = 2.0 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	trr	I _F = 2.0 A, V _{GS} = 0 V		190		ns
Reverse Recovery Charge	Qrr	di/dt = 50 A/µs		500		nC

Note Pulsed

TEST CIRCUIT 1 AVALANCHE CAPABILITY

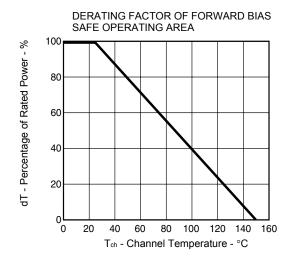


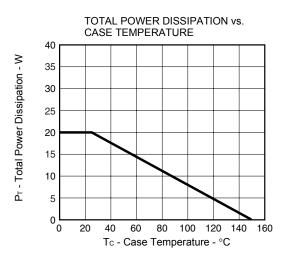
TEST CIRCUIT 2 SWITCHING TIME



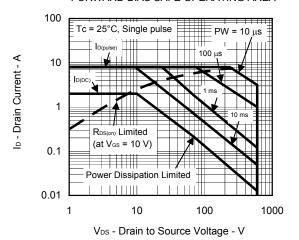
TEST CIRCUIT 3 GATE CHARGE

TYPICAL CHARACTERISTICS (TA = 25°C)

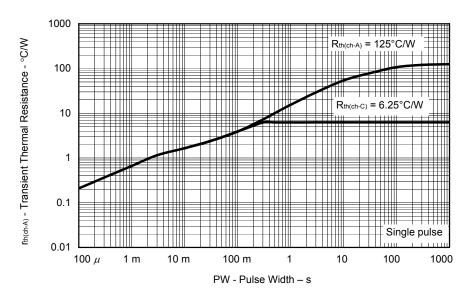




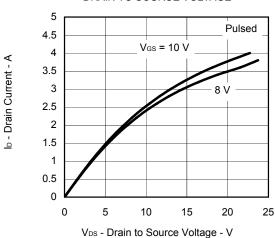
FORWARD BIAS SAFE OPERATING AREA



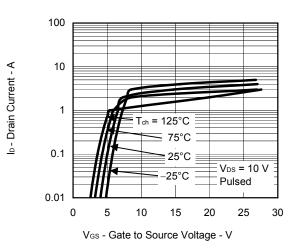
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



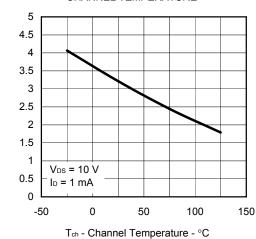
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



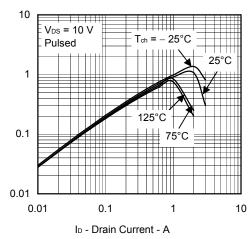
FORWARD TRANSFER CHARACTERISTICS



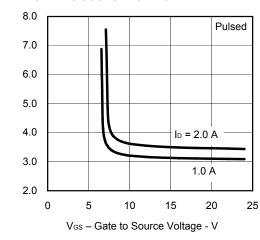
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



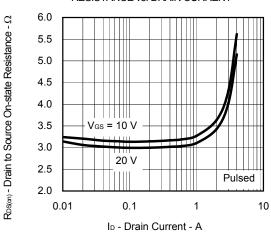
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



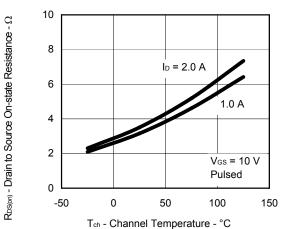
 $\mathsf{R}_{\mathsf{DS}(\varpi)}$ - Drain to Source On-state Resistance - Ω

VGS(off) - Gate Cut-off Voltage - V

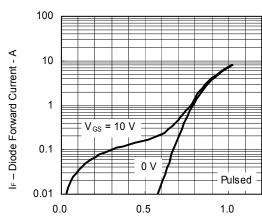
| yfs | - Forward Transfer Admittance - S

Coss, Crss - Capacitance - pF

DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

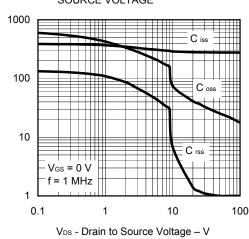


SOURCE TO DRAIN DIODE FORWARD VOLTAGE

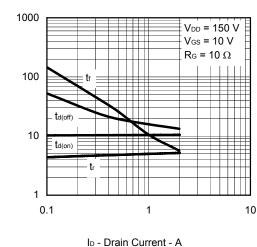


V_{F(S-D)} – Source to Drain Voltage - V

CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

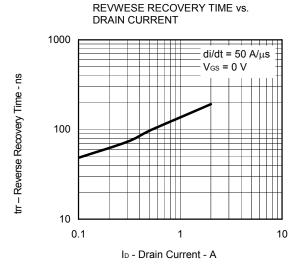


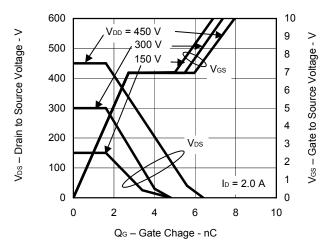
SWITCHING CHARACTERISTICS



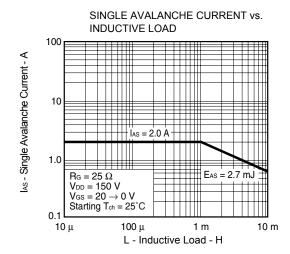
io - Diani Guitent -

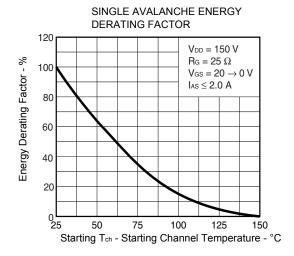
(d(on), tr, td(off), tr - Switching Time - ns



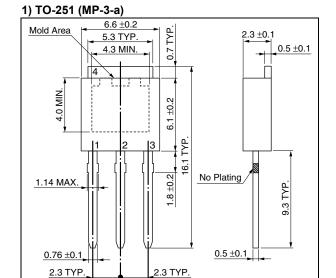


DYNAMIC INPUT/OUTPUT CHARACTERISTICS





<R> PACKAGE DRAWINGS (Unit: mm)

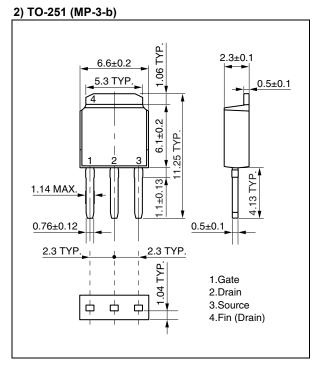


1.02

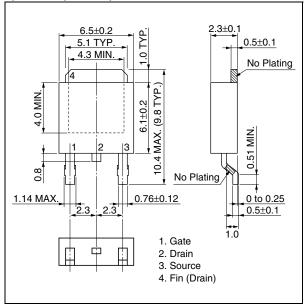
1. Gate

2. Drain

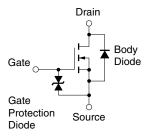
3. Source4. Fin (Drain)



3) TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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