N-Channel Depletion-Mode Vertical DMOS FETs

Ordering Information

BV_{DSX} / BV_{DGX}	$R_{DS(ON)}$ (max)	I_{DSS} (min)	Order Number / Package
			Die*
250V	20Ω	200mA	DN3125NW

* Die in wafer form.

Features

- ❏ High input impedance
- ❏ Low input capacitance
- ❏ Fast switching speeds
- ❏ Low on resistance
- ❏ Free from secondary breakdown
- ❏ Low input and output leakage

Advanced DMOS Technology

These low threshold depletion-mode (normally-on) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Applications

- ❏ Normally-on switches
- ❏ Solid state relays
- ❏ Converters
- ❏ Linear amplifiers
- ❏ Constant current sources
- ❏ Power supply circuits
- ❏ Telecom

Absolute Maximum Ratings

Drain-to-Source Voltage	BV_{DSX}
Drain-to-Gate Voltage	BV_{DGX}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C

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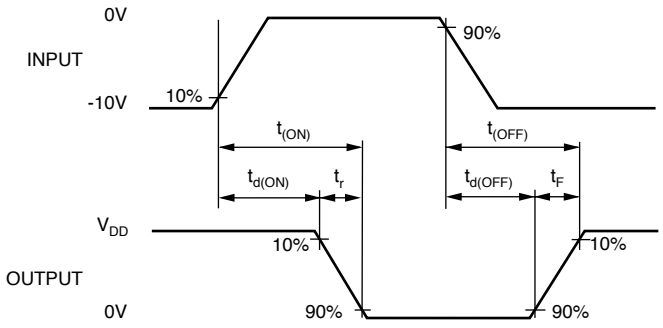
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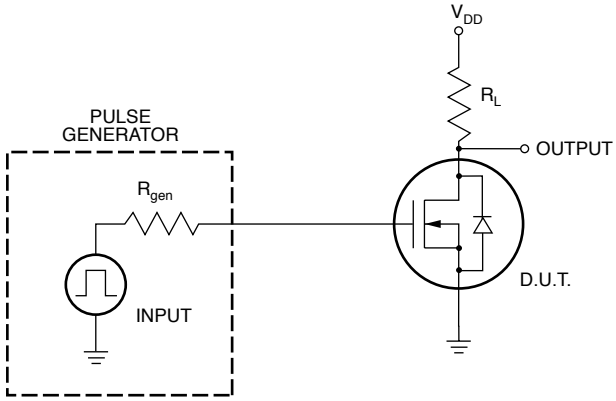
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSX}	Drain-to-Souce Breakdown Voltage	250			V	V_{GS} = -5.0V, I_D = 100μA
$V_{GS(OFF)}$	Gate-to-Source OFF Voltage	-1.5		-3.5	V	V_{DS} = 15V, I_D = 10μA
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with Temperature			4.5	mV/°C	V_{DS} = 15V, I_D = 10μA
I_{GSS}	Gate Body Leakage Current			100	nA	V_{GS} = ±20V, V_{DS} = 0V
$I_{D(OFF)}$	Drain-to-Source Leakage Current			1.0	μA	V_{GS} = -5.0V, V_{DS} = Max Rating
				1.0	mA	V_{GS} = -5.0V, V_{DS} = 0.8 Max Rating T_A = 125°C
I_{DSS}	Saturated Drain-to-Source Current	200			mA	V_{GS} = 0V, V_{DS} = 15V
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance			20	Ω	V_{GS} = 0V, I_D = 150mA
				20		V_{GS} = -0.8V, I_D = 50mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature			1.1	%/°C	V_{GS} = 0V, I_D = 150mA
G_{FS}	Forward Transconductance	150			m℧	I_D = 100mA, V_{DS}=10V
C_{ISS}	Input Capacitance		60	120	pF	V_{GS} = -5.0V, V_{DS} = 25V, f =1.0Mhz
C_{OSS}	Common Source Output Capacitance		6.0	15		
C_{RSS}	Reverse Transfer Capacitance		3.0	10		
$t_{d(ON)}$	Turn-ON Delay Time			10	ns	V_{DD} = 25V, I_D = 150mA, R_{GEN} = 25Ω, V_{GS} = 0V to -10V
t_r	Rise Time			15		
$t_{d(OFF)}$	Turn-OFF Delay Time			15		
t_f	Fall Time			20		
V_{SD}	Diode Forward Voltage Drop			1.8	V	V_{GS} = -5.0V, I_{SD} = 150mA
t_{rr}	Reverse Recovery Time		800		ns	V_{GS} = -5.0V, I_{SD} = 150mA

Notes:
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

Switching Waveforms and Test Circuit





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