I²C Programmable Boost and Single Inductor Inverting DC/DC Converters with OTP

FEATURES

- **Output Voltages:**
  - **3.2V to 12.775V and –1.2V to –13.95V (LT3582)**
  - **5V and –5V (LT3582-5)**
  - **12V and –12V (LT3582-12)**
- **Digitally Re-Programmable (LT3582) Via I²C for:**
  - **Output Voltages**
  - **Power Sequencing**
  - **Output Voltage Ramp Rates**
- **Power-up Defaults Settable with Non-volatile OTP (LT3582)**
- **I²C Compatible Interface (Standard Mode*)**
- **All Power Switches Integrated**
  - **350mA Current Limit (Boost)**
  - **600mA Current Limit (Inverting)**
- **All Feedback Resistors Integrated**
- **Input Voltage Range: 2.55V to 5.5V**
- Low Quiescent Current
  - 325µA in Active Mode
  - 0.01µA in Shutdown Mode
- Integrated Output Disconnect
- Tiny 16-pin 3mm × 3mm QFN Package

APPLICATIONS

- AMOLED Power
- CCD Power
- General Purpose DC/DC Conversion

DESCRIPTION

The LT®3582/LT3582-5/LT3582-12 are dual DC/DC converters featuring positive and negative outputs and integrated feedback resistors. The LT3582, with its built in One Time Programming (OTP), has configurable output settings via the I²C interface, including output voltage settings, power up sequencing, power down discharge, and output voltage ramp rates. LT3582 settings can be changed adaptively in the final product, or set during manufacturing and made permanent using the built in non-volatile OTP memory. The positive output voltage can be set between 3.2V and 12.775V in 25mV steps. The negative output voltage can be set between –1.2V and –13.95V in –50mV steps. The LT3582-5 and LT3582-12 are pre-configured at the factory for ±5V and ±12V outputs respectively.

The LT3582 series includes two monolithic converters, one Boost and one Inverting. The Boost converter has an integrated power switch and output disconnect switch. The Inverting converter uses a single inductor topology and includes an integrated power switch. Both Boost and Inverting converters use a novel** control scheme resulting in low output voltage ripple while allowing for high conversion efficiency over a wide load current range. The LT3582 series is available in a 16-pin 3mm x 3mm QFN.

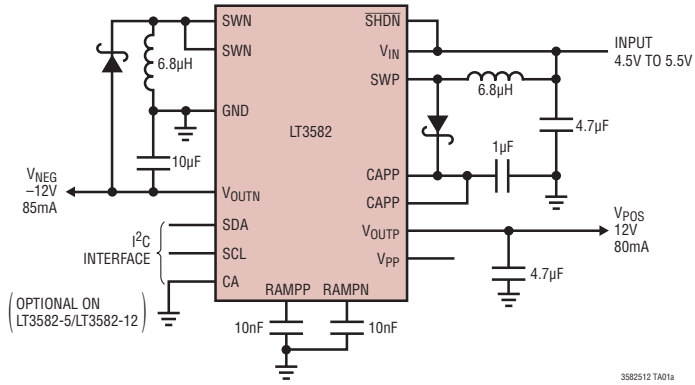
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* Input thresholds are reduced to allow communication with low voltage digital ICs. (See Electrical Characteristics).

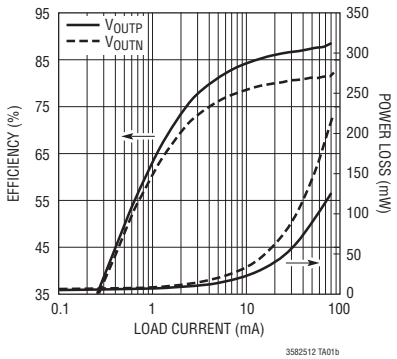
**Patent Pending

TYPICAL APPLICATION

±12V Supplies from a Single 5V Input



Efficiency and Power Loss

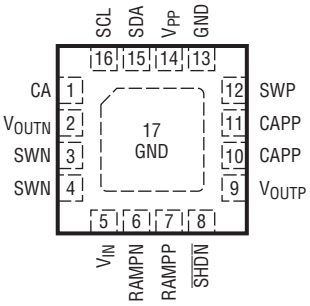


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 6V
SWP Voltage 15V
SWN Voltage ..... –16.5V
CAPP Voltage 15V
CAPP-V_{OUTP} Voltage ..... –0.8V to 8V
$I_{CAPP-VOUTP}$ ..... ±300mA
V_{OUTP} Voltage 15V
V_{OUTN} Voltage ..... –16.5V
RAMPP Voltage 3V
RAMPN Voltage 3V
$\overline{SHDN}$ Voltage ..... –0.5 to 6V
V_{PP} Voltage ..... –0.2 to 16V
SDA, CA, SCL Voltage ..... –0.5 to 6V
Operating Junction Temperature Range (Notes 3, 5)
LT3582E ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UD PACKAGE
16-PIN (3mm × 3mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 68°C/W
EXPOSED PAD (PIN #17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3582EUD#PBF	LT3582EUD#TRPBF	LDDB	16-Pin (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3582EUD-5#PBF	LT3582EUD-5#TRPBF	LDVG	16-Pin (3mm × 3mm) Plastic QFN	–40°C to 125°C
LT3582EUD-12#PBF	LT3582EUD-12#TRPBF	LDVH	16-Pin (3mm × 3mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted. (Note 3)

Switching Regulator Characteristics

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN_MIN}	Minimum Operating Voltage		●	2.4	2.475	2.55	V
V_{IN_MAX}	Maximum Operating Voltage		●	5.5			V
I_{VIN}	V_{IN} Quiescent Current	Ramp Current Configured to 1µA, SWOFF Bit Active			325	450	µA
I_{VIN_SHDN}	V_{IN} Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0			0.01	0.5	µA
I_{CAPP_SHDN}	CAPP Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0, V_{CAPP} = 5.0V, V_{OUTP} = 0V			0	0.5	µA
T_{OFF_MINP}	Minimum Switch Off Time	Boost Switch			100		ns
T_{OFF_MINN}	Minimum Switch Off Time	Inverting Switch			125		ns
T_{ON_MAX}	Maximum Switch On Time	Inverting and Boost Switches			10		µs
I_{LIMIT_P}	Boost Switch Current Limit		●	285	350	430	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted. (Note 3)

Switching Regulator Characteristics

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{LIMIT_N}	Inverting Switch Current Limit		●	490	600	720	mA
R_{ON_P}	Boost Switch On Resistance	I_{SWP} = 200mA			500		mΩ
R_{ON_N}	Inverting Switch On Resistance	I_{SWN} = –400mA			560		mΩ
I_{OFF_P}	Boost Switch Leakage Current into SWP pin	V_{SWP} = 5V			0.01	0.5	µA
I_{OFF_N}	Inverting Switch Leakage Current out of SWN pin	V_{IN} = 5.0, V_{SWN} = 0.0			0.01	1	µA
R_{ON_DIS}	Output Disconnect Switch On Resistance	V_{CAPP} = 10V, RAMPP > 1.4V			1.4		Ω
I_{LIMIT_DIS}	Output Disconnect Current Limit		●	124	155	186	mA
I_{VOUTP_PDS}	V_{OUTP} Power-Down Discharge Current	V_{OUTP} = 8V		2.4	4.8	8.8	mA
I_{CAPP_PDS}	CAPP Power-Down Discharge Current	CAPP = 8V		1.2	2.4	4.4	mA
I_{VOUTN_PDS}	V_{OUTN} Power-Down Discharge Current	V_{OUTN} = –8V		–1.4	–2.8	–4.2	mA
$T_{STARTUP}$	Configuration Startup Delay	V_{IN}> V_{IN_MIN} & $\overline{SHDN}$ > $V_{\overline{SHDN}_VIH}$ to I^2C Enabled and Power-up Sequencing Start	●		64	128	µs

Programmable Output Characteristics[6]

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{VOUTP}	Positive Output Voltage	LT3582-5 LT3582-12	● ●	4.95 11.88	5 12	5.05 12.1	V V
N_V_{OUTP}	Positive V_{OUTP} Resolution[2]			9			Bits
V_{VOUTP_LSB}	V_{OUTP} LSB[2]				25		mV
V_{VOUTP_FS}	V_{OUTP} Full Scale Voltage[2]	Code = BFh, V_{PLUS} = 1	●	12.56	12.775	12.94	V
V_{VOUTP_MIN}	V_{OUTP} Minimum Voltage[2]	Code = 00h, V_{PLUS} = 0	●	3.152	3.20	3.248	V
V_{VOUTP_LR}	V_{OUTP} Line Regulation	Code = BFh, 2.575 < V_{IN} < 5.5			–0.02		%/V
V_{VOUTN}	Negative Output Voltage	LT3582-5 LT3582-12	● ●	–5.075 –12.1	–5 –12	–4.925 –11.868	V V
N_V_{OUTN}	Negative V_{OUTN} Resolution[2]			8			Bits
V_{VOUTN_LSB}	V_{OUTN} LSB[2]				–50		mV
V_{VOUTN_FS}	V_{OUTN} Full Scale Voltage[2]	Code = FFh	●	–14.2	–13.95	–13.7	V
V_{VOUTN_MIN}	V_{OUTN} Minimum Voltage[2]	Code = 00h	●	–1.23	–1.205	–1.18	V
V_{VOUTN_LR}	V_{OUTN} Line Regulation	Code = FFh, 2.575 < V_{IN} < 5.5			–0.01		%/V
INL_V_{OUTP}	V_{OUTP} Integral Nonlinearity[2, 4]		●			±0.6	LSB
DNL_V_{OUTP}	V_{OUTP} Differential Nonlinearity[2, 4]		●			±0.6	LSB
INL_V_{OUTN}	V_{OUTN} Integral Nonlinearity[2]		●			±0.85	LSB
DNL_V_{OUTN}	V_{OUTN} Differential Nonlinearity[2]		●			±0.85	LSB
I_{RAMP00}	RAMPP/RAMPN Pull Up Current IRMP Code = 00	V_{RAMPP} = 0.0V V_{RAMPN} = 0.0V	●	0.7	1.0	1.3	µA
I_{RAMP01}	RAMPP/RAMPN Pull Up Current[2] IRMP Code = 01	V_{RAMPP} = 0.0V V_{RAMPN} = 0.0V	●	1.4	2.0	2.6	µA

ELECTRICAL CHARACTERISTICS

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Programmable Output Characteristics

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{RAMP10}	RAMPP/RAMPN Pull Up Current[2] IRMP Code = 10	V_{RAMPP} = 0.0V V_{RAMPN} = 0.0V	●	2.8	4.0	5.2	µA
I_{RAMP11}	RAMPP/RAMPN Pull Up Current[2] IRMP Code = 11	V_{RAMPP} = 0.0V V_{RAMPN} = 0.0V	●	5.6	8.0	10.4	µA
V_{VPLUS}	V_{OUTP} Voltage Increase When V_{PLUS} Bit is Set from 0 to 1[2]				25		mV

Input/Output Pin Characteristics

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{\overline{SHDN}_VIH}$	$\overline{SHDN}$ Input Voltage High		●	1.1			V
$V_{\overline{SHDN}_VIL}$	$\overline{SHDN}$ Input Voltage Low		●			0.3	V
$V_{HYST_\overline{SHDN}}$	$\overline{SHDN}$ Input Hysteresis				50		mV
$I_{\overline{SHDN}_BIAS}$	$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 1V		2.5	4.5	6.5	µA
V_{CA_VIH}	CA Input Voltage High		●	0.7 × V_{IN}			V
V_{CA_VIL}	CA Input Voltage Low		●			0.3 × V_{IN}	V
V_{SDA_VIH}	SDA Input Voltage High		●	1.25			V
V_{SDA_VIL}	SDA Input Voltage Low		●			0.85	V
V_{SCL_VIH}	SCL Input Voltage High		●	1.25			V
V_{SCL_VIL}	SCL Input Voltage Low		●			0.85	V
V_{HYST}	Input Hysteresis	SDA, SCL Pins			80		mV
I_{LEAK_CA}	CA Input Leakage Current	CA = 0V & 5.5V	●			±1	µA
I_{LEAK_SCL}	SCL Input Leakage Current	SCL = 0V & 5.5V	●			±1	µA
I_{LEAK_SDA}	SDA Input Leakage Current	SDA = 0V & 5.5V	●			±1	µA
C_{IN}	Input Capacitance	SDA, SCL Pins			3		pF
V_{SDA_OL}	SDA Output Low Voltage	3mA into SDA Pin	●			0.4	V
V_{PP_RANGE}	V_{PP} Voltage Range for OTP Write[2]			13		15	V
V_{PPUVLO}	Under-voltage Lockout for V_{PP} Pin[2]		●	12.05	12.45	12.85	V

I²C Timing Characteristics

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SCL}	Serial Clock Frequency		●			100	kHz
t_{LOW}	Serial Clock Low Period		●	4.7			µs
t_{HIGH}	Serial Clock High Period		●	4.0			µs
t_{BUF}	Bus Free Time Between Stop and Start		●	4.7			µs
$t_{HD,STA}$	Start Condition Hold Time		●	4.0			µs
$t_{SU,STA}$	Start Condition Setup Time		●	4.7			µs
$t_{SU,STO}$	Stop Condition Setup Time		●	4.0			µs
$t_{HD,DATXMIT}$	Data Hold Time Transmitting	LT3582 Sending Data to Host	●	300			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 3.6V, $V_{\overline{SHDN}}$ = V_{IN} unless otherwise noted. (Note 3)

I²C Timing Characteristics

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{HD,DATRCV}$	Data Hold Time Receiving	LT3582 Receiving Data from Host	●	0			ns
$t_{SU,DAT}$	Data Setup Time		●	250			ns
t_F	SDA Fall Time	400pF load, $V_{IN} \geq 2.5V$	●			250	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: LT3582 only.

Note 3: The LT3582E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlations with statistical process controls.

Note 4: These specifications apply to the V_P trim bits in REG0 using a 50mV LSB and do not include the additional V_{PLUS} trim bit. See Registers and OTP in the Applications Information section.

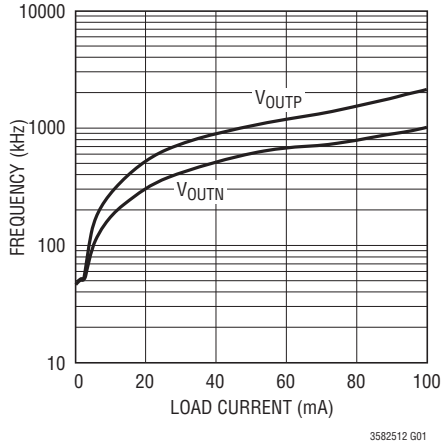
Note 5: This IC includes over-temperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when over-temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 6: Output voltage is measured under non-switching test conditions approximating a moderate load current from the output.

TYPICAL PERFORMANCE CHARACTERISTICS

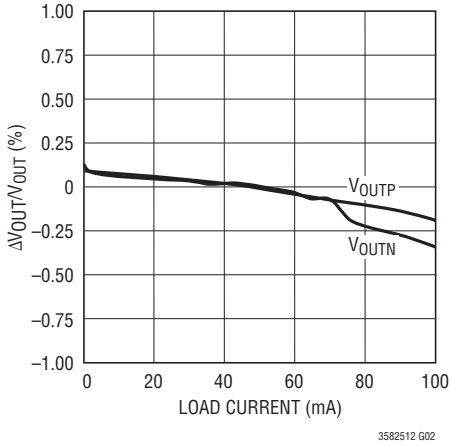
T_A = 25°C unless otherwise noted.

Switching Frequencies (Figure 13)



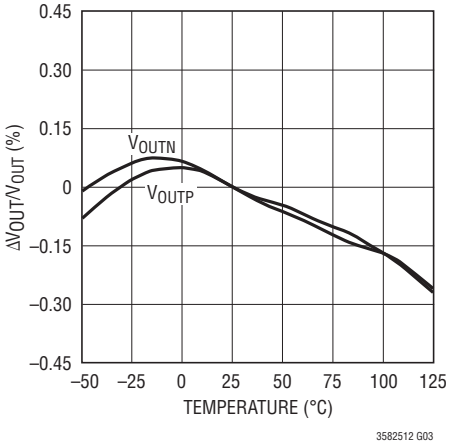
3582512 G01

Load Regulation (Figure 13)



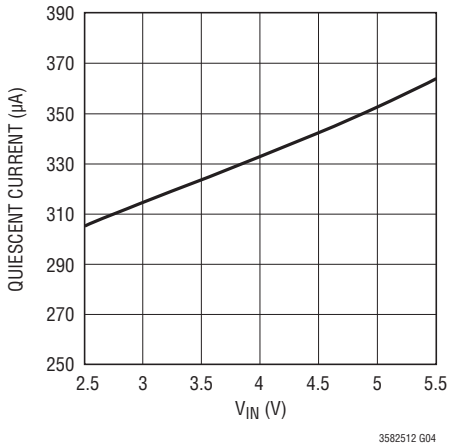
3582512 G02

Output Voltage (Figure 13)



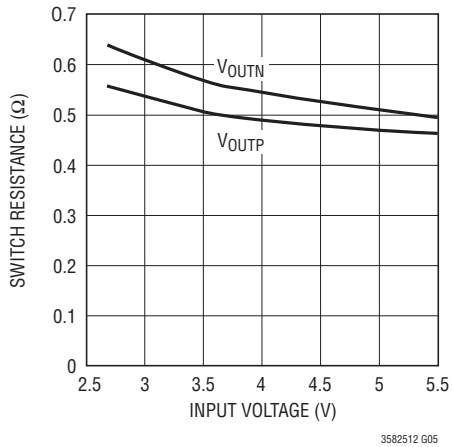
3582512 G03

Quiescent Current – Not Switching



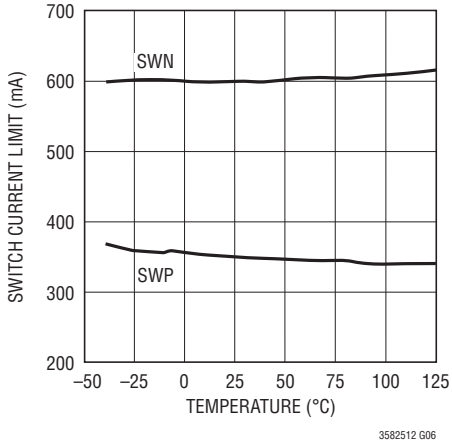
3582512 G04

Switch Resistance



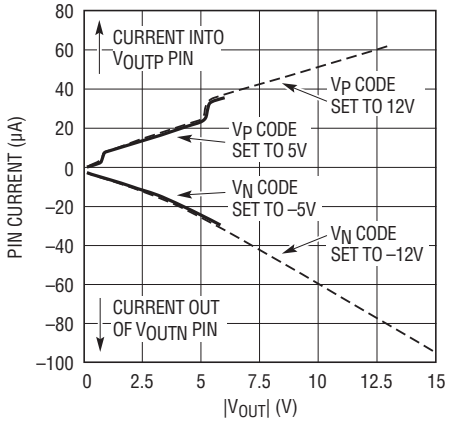
3582512 G05

Switch Current Limit



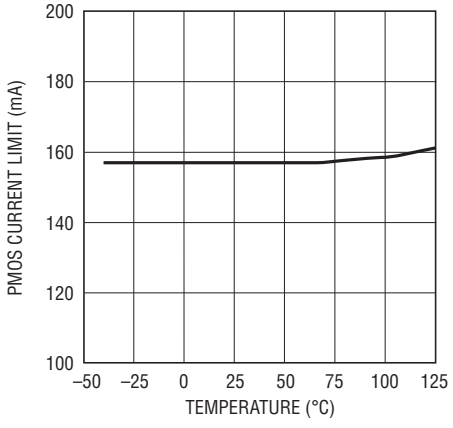
3582512 G06

V_{OUTP} and V_{OUTN} Pin Current During Normal Operation



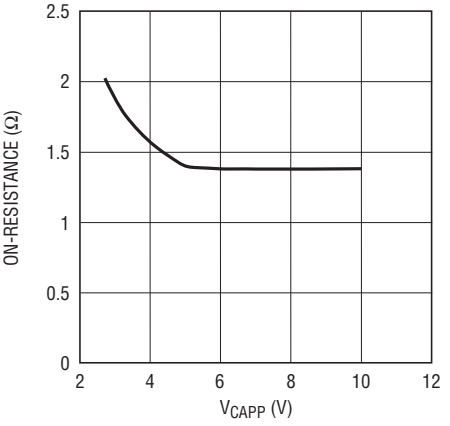
3582512 G07

Output Disconnect PMOS Current Limit During Normal Operation



3582512 G08

Output Disconnect PMOS On-Resistance

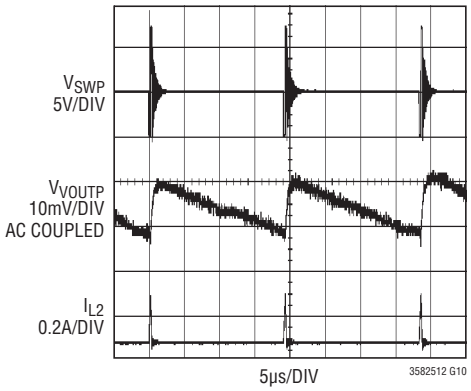


3582512 G09

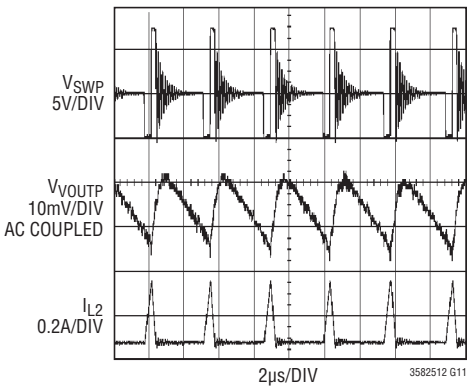
TYPICAL PERFORMANCE CHARACTERISTICS

Note: All waveforms on this page apply to Figure 13.

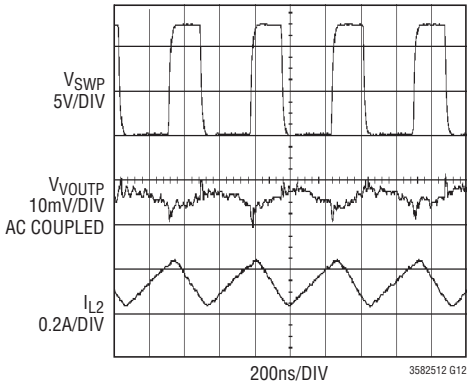
Switching Waveform at 1mA Load (Boost)



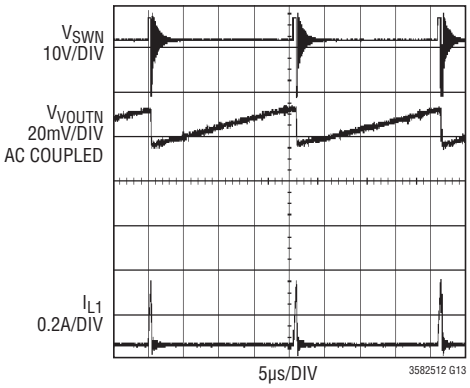
Switching Waveform at 10mA Load (Boost)



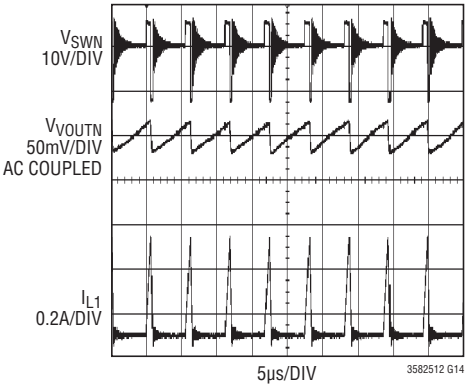
Switching Waveform at 100mA Load (Boost)



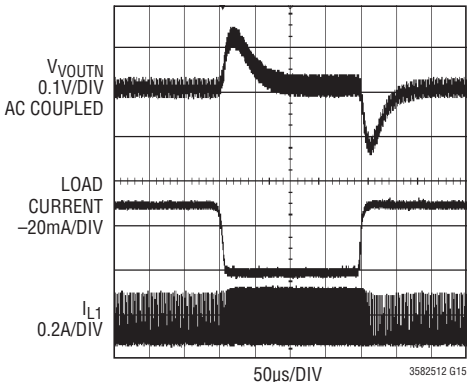
Switching Waveform at 1mA Load (Inverting)



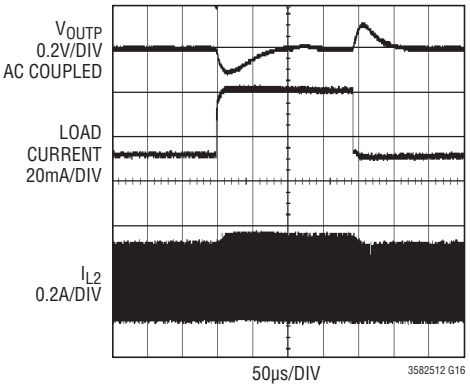
Switching Waveform at 10mA Load (Inverting)



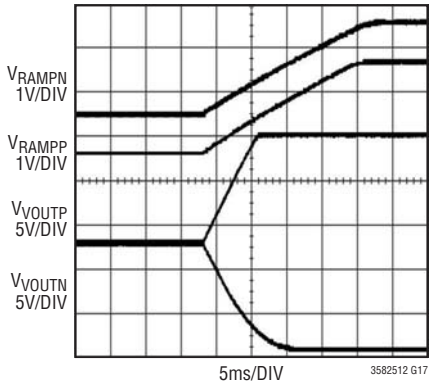
Load Transient, V_{OUTN}, 30mA to 60mA to 30mA Steps



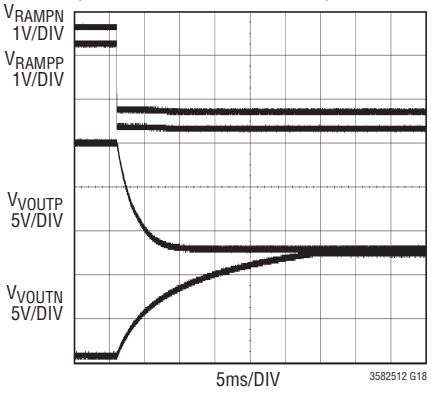
Load Transient, V_{OUTP}, 30mA to 60mA to 30mA Steps



Power-Up Sequencing Waveforms (PUSEQ = 11)



Power-Down Discharge Waveforms (PUSEQ = 11, PDDIS = 1)



PIN FUNCTIONS

CA (Pin 1): I^2C Address Select Pin. Tie this pin to V_{IN} to set the 7-bit address to 0110 001. Tie to GND for 1000 101.

V_{OUTN} (Pin 2): Negative Output Voltage Pin. When the converter is operating, this pin is regulated to the programmed negative output voltage. Place a ceramic capacitor from this pin to GND.

SWN (Pins 3 & 4): Negative switching node for the Inverting converter. This is the drain of the internal PMOS power switch. Connect one end of the Inverting inductor to these pins. Keep the trace area on these pins as small as possible.

V_{IN} (Pin 5): Input supply pin and source of the PMOS power switch. This pin must be bypassed locally with a ceramic capacitor. The operating voltage range of this pin is 2.55V to 5.5V.

RAMPN (Pin 6): Soft start ramp pin for the Inverting converter. Place a capacitor from this pin to GND. A programmable current of 1µA - 8µA (LT3582) or 1µA (LT3582-5/LT3582-12) charges this pin during startup, limiting the ramp rate of V_{OUTN}. This pin is discharged to GND during shutdown.

RAMPP (Pin 7): Soft start ramp pin for the Boost converter. Place a capacitor from this pin to GND. A programmable current of 1µA - 8µA (LT3582) or 1µA (LT3582-5/LT3582-12) charges this pin during startup, limiting the ramp rate of V_{OUTP}. This pin is discharged to GND in shutdown.

$\overline{SHDN}$ (Pin 8): Shutdown Pin. Drive this pin to 1.1V or higher to enable the part. Drive to 0.3V or lower to shut down. Includes an integrated 222k pulldown resistor.

V_{OUTP} (Pin 9): Output of the Boost converter output disconnect circuit. A ceramic capacitor should be placed from this node to GND. During shutdown, this pin is disconnected from the Boost network which allows this pin to discharge to GND, assuming a load is present to discharge the capacitance.

CAPP (Pins 10 & 11): Connect the Boost output capacitor from these pins to GND. During shutdown, the voltage on these pins will remain close to the input voltage due to the path through the Boost inductor and Schottky. During normal operation, CAPP will be boosted slightly higher than the programmed output voltage.

SWP (Pin 12): Positive switching node for the Boost converter. This is the drain of the internal NMOS power switch. Connect one end of the Boost inductor to this pin. Keep the trace area on this pin as small as possible.

GND (Pin 13): Ground Pin. Tie to a local ground plane. Proper PCB layout is required to achieve advertised performance; see Applications Information section for more information.

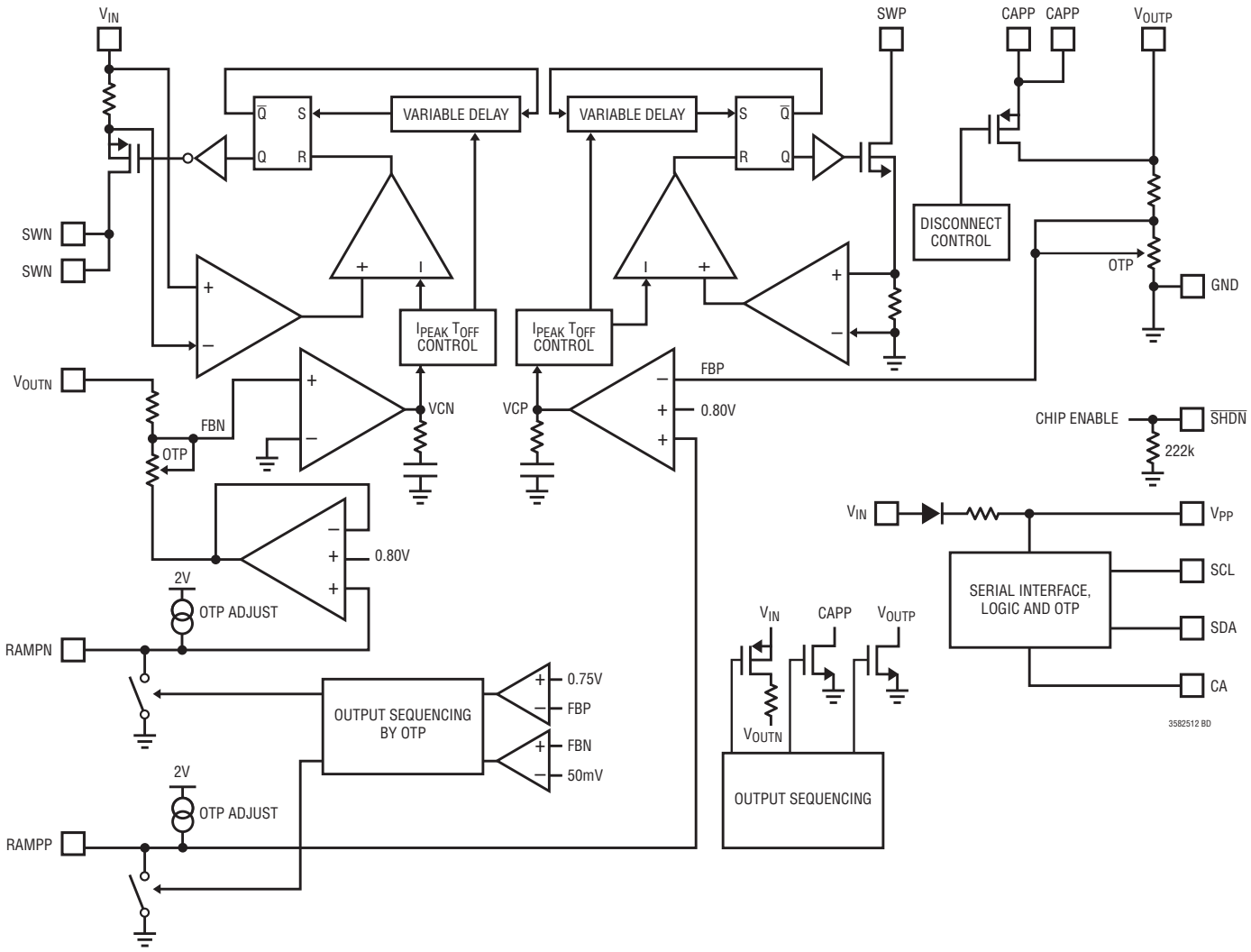
V_{PP} (Pin 14): Programming Voltage Pin. Drive this pin to 13-15V when programming the OTP memory. Float otherwise. A bypass capacitor should be placed from this node to GND if V_{PP} is used for programming. If V_{PP} falls below 13V during OTP programming, an internal FAULT bit, which can be read through the I^2C interface, can be set high.

SDA (Pin 15): I^2C Bidirectional Data Pin. Tie to GND or V_{IN} if unused.

SCL (Pin 16): I^2C Clock Pin. Tie to GND or V_{IN} if unused.

Exposed Pad (Pin 17): Ground Pin. Tie to a local ground plane. Proper PCB layout is required to achieve advertised performance; see Applications Information section for more information.

BLOCK DIAGRAM



OPERATION

The LT3582 series are dual DC/DC converters, each containing both a Boost and an Inverting converter. Operation can be best understood by referring to the Block Diagram. The Boost and Inverting converters each use a novel control technique, which simultaneously varies both peak inductor current and switch off time. This results in high efficiency over a large load range and low output voltage ripple. In addition, this technique further minimizes output ripple when the switching frequency is in the audio band.

Boost Converter: The Boost converter uses a grounded source NMOS power transistor as the main switching element. The current in the NMOS is constantly monitored and controlled, along with the off time of the switch to achieve regulation of V_{OUTP}. The V_{OUTP} voltage is divided by the internal programmable (LT3582 only) resistor divider to create FBP. The voltage on FBP is compared to an internal reference and amplified, creating an error signal on the VCP node which commands the appropriate peak inductor current and off time for the subsequent switching cycle.

Inverting Converter: The Inverting converter uses a power PMOS transistor with the source connected to V_{IN}. This topology requires only one external inductor, instead of the normally required two inductors plus flying capacitor. Regulation is achieved in a similar manner as the Boost.

Output Power-up Sequencing: After an initial startup delay ($T_{STARTUP}$ = 64µS typical), the outputs V_{OUTP} and V_{OUTN} rise (in magnitude) simultaneously with the LT3582-5/LT3582-12 or in one of four selectable sequences with the LT3582. Using the I^2C interface, the LT3582 outputs can be configured such that (1) they both rise simultaneously, (2) V_{OUTP} rises to regulation before V_{OUTN} rises, (3) V_{OUTN} rises to regulation before V_{OUTP} rises, or (4) neither output rises. The outputs of the LT3582-5 and LT3582-12 are pre-configured to rise simultaneously.

The ramp rates of the outputs are proportional to the ramp rates of their respective RAMP pins. A capacitor is placed between each RAMP pin and ground. The RAMP pins are discharged during shutdown. Once enabled, configurable (LT3582) or pre-configured (LT3582-5/LT3582-12) currents charge each RAMP pin in the desired sequence causing the outputs to rise.

Output Power-Down Discharge: The power-down discharge feature is permanently enabled on the LT3582-5 and LT3582-12 and can be enabled or disabled through I^2C on the LT3582. Upon $\overline{SHDN}$ falling, and when power-down discharge is enabled, internal transistors will activate to assist in discharging the outputs toward ground. When power-down discharge is disabled, the chip powers down immediately after $\overline{SHDN}$ falls and the outputs will discharge on their own depending on their external load capacitances and currents.

OTP Memory (LT3582 Only): The LT3582 includes 22 bits of user programmable output settings and 1 programming lockout bit. Parameters such as positive & negative output voltages and power sequencing settings can be changed in real time with the integrated I^2C interface. Settings can then be made permanent by programming to the on-chip non-volatile OTP (One Time Programmable) memory.

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I²C Interface

The LT3582 series contains an I²C compatible interface with reduced input threshold voltages to allow for direct communication with low voltage digital ICs (see Electrical Characteristics). I²C communication is disabled when $\overline{SHDN}$ is low. After $\overline{SHDN}$ rises, I²C communication is re-enabled after a delay of 64µs (typical). The chip is a read-write slave device which allows the user to read the current settings and, for the LT3582, write new ones. Most settings can be made permanent via the One-Time-Programmable memory. The chip will always enable using the data stored in OTP and the LT3582 can be reconfigured after power-up.

START and STOP Conditions

When the bus is idle, both SCL and SDA are high. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL is high, as shown in Figure 1. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

ACKnowledge

The acknowledge signal (ACK) is used in handshaking between transmitter and receiver to indicate that the most recent byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. When the slave is the receiver, it pulls down the SDA line so that it remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA high, then the master may abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master pulls down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received the master leaves the SDA line HIGH (not acknowledge) and issues a stop condition to terminate the transmission.

Device Addressing

The LT3582 series supports two 7-bit chip addresses depending on the logic state of the CA pin. The addresses are 0110 001 (CA=1) and 1000 101 (CA=0). Also, there are seven internal data byte locations as shown in Table 1. OTP0-OTP2 are the OTP memory bytes. REG0-REG2 are the corresponding volatile registers used for storing alternate settings. Finally, the Command Register (CMDR) is used for additional control of the chip.

All data bytes can be read from their assigned register addresses. Since they share the same register addresses, reads of the OTP and REG data bytes are differentiated by their corresponding RSEL (Register Select) bits in the

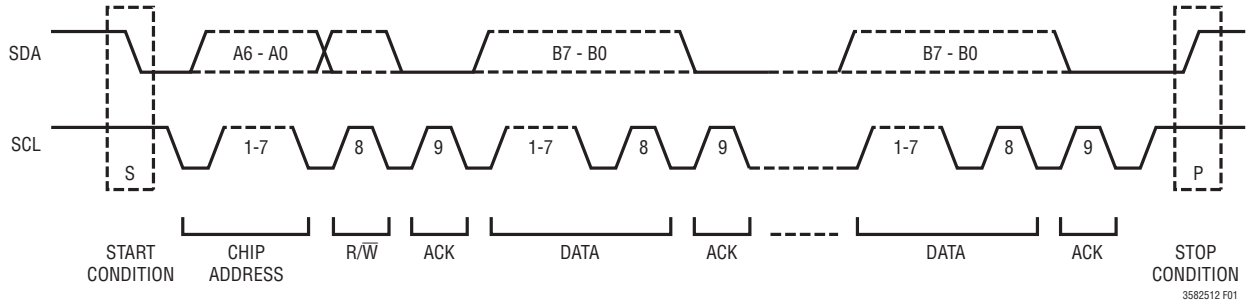


Figure 1. Data Transfer over I²C Bus

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CMDR register. All data written to register addresses 0-2 is stored in REG0-REG2. Regardless of the RSEL bits, OTP bytes cannot be written directly. See the OTP Programming section for more information.

Data Transfer Protocol

The LT3582 series supports 8-bit data transfers in the transaction formats shown in Figures 2 and 3 below. Multiple data bytes can only be transferred by issuing multiple transactions.

Figure 2 shows the required format for writing a byte of data to the LT3582 series. Again, the chip address depends on the CA pin logic state.

S	CHIP ADDR	$\overline{W}$	A	REG ADDR	A	DATA	A	P
	0110 001 OR 1000 101	0	0	00000b2:b0	0	b7:b0	0	

FROM MASTER TO SLAVE
FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)
$\overline{W}$ WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

Figure 2: I²C Byte Write Transaction

A byte of data is read from the LT3582 series using the format shown in Figure 3. This transaction requires four I²C bytes to read one byte of chip data and must be repeated for each subsequent byte of data that is read.

S	CHIP ADDR	$\overline{W}$	A	REG ADDR	A
	0110 001 OR 1000 101	0	0	00000b2:b0	0

S	CHIP ADDR	R	A	DATA	$\overline{A}$	P
	0110 001 OR 1000 101	1	0	b7:b0	1	

Figure 3: I²C Byte Read Transaction

LT3582 Chip Configuration

Settings such as output voltages and sequencing are digitally programmable. The chip uses settings from either the REG or OTP bytes, depending on the states of the corresponding RSEL bits (0 for OTP and 1 for REG).

During shutdown the RSEL bits are reset low. As a result, the initial configuration comes from the OTP data bytes. After power-up, the configuration can be changed by writing new settings to the appropriate REG data byte(s) then setting the corresponding RSEL bit(s).

Finally, data in the REG bytes can be permanently programmed to OTP by applying voltage to the V_{PP} pin and setting the WOTP bit in the Command Register. See the OTP Programming section for more information.

LT3582-5/LT3582-12 Chip Configuration

The LT3582-5/LT3582-12 are shipped from the factory with the OTP memory pre-programmed and LOCKed which prohibits subsequent changes to the configuration. The configuration can still be read through the I²C bus and the RST & SWOFF bits of the CMDR register (described later) are functional. The following sections describe the various configurable features of the LT3582. The LT3582-5 and LT3582-12 are pre-configured as follows: V_P and V_N are programmed for ±5V or ±12V respectively, LOCK = 1, IRMP = 00, PDDIS = 1, PUSEQ = 11 and V_{PLUS} may be 1 or 0. Since LOCK = 1, subsequent configuration changes are prohibited. See Configuration Lockout (LOCK Bit) for more information.

Registers and OTP

The registers and OTP bytes for the LT3582 series are organized as shown in Table 1. The CMDR is reset to 00h upon power up, during shutdown and during under-voltage and thermal lockouts. *REG0-REG2 are never reset and must always be loaded with valid data before use.* The LT3582's OTP memory is shipped with all 0's, and as a result, the PUSEQ bits are configured to disable the outputs. The PUSEQ bits must be reconfigured to enable the outputs.

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CMDR: The Command Register is used to control various functions of the chip. During shutdown and power-up the CMDR is initialized to 00h.

The RSEL (Register Select) bits are functional only for the LT3582. The LT3582-5 and LT3582-12 function as if the RSEL bits are always "0". These bits perform three functions:

- Each RSEL bit instructs the chip whether to use the configuration data from the corresponding OTP byte (RSELx=0) or the REG byte (RSELx=1). Changing an RSELx bit immediately updates the chip configuration.
- Each RSEL bit determines if I^2C reads return data from the corresponding OTP byte (RSELx=0) or the REG byte (RSELx=1).
- OTP programming only programs data to the bytes with corresponding RSEL bits set high.

Setting the SWOFF bit immediately disables the Boost and Inverting power switches and opens the output disconnect PMOS switch. It is recommended to set this bit before writing new configuration data. This can prevent unexpected chip behavior while modifying the configuration and also forces a soft-start after SWOFF is cleared (see Soft-Start and Power-up Sequencing). Writing "1" to the RST bit resets the internal I^2C logic and the CMDR register. Reading bit 6 of the CMDR returns the FAULT bit indicating if an OTP programming attempt may have failed. FAULT is cleared during reset, power-up, or by writing a "1" to the CF (Clear Fault) bit. Conditions that set the FAULT bit are (1) OTP programming in which the V_{PP} voltage is too low or (2) attempted OTP programming when the LOCK bit is set. *OTP write attempts that set the FAULT bit due to low V_{PP} voltage should be considered failures and the device should be discarded. Attempts to re-program the OTP memory after the FAULT bit has been set are not recommended.* Finally, setting the WOTP bit starts the OTP programming.

Table 1: LT3582 Series Register Map

REGISTER ADDRESS	REGISTER NAME	BIT	BIT NAME	DESCRIPTION
00h	REG0/ OTP0	7:0	V_P	V_{OUTP} Output Voltage (00h=3.2V, BFh = 12.75V)
01h	REG1/ OTP1	7:0	V_N	V_{OUTN} Output Voltage (00h=1.2V, FFh = 13.95V)
02h	REG2/ OTP2	7	-	Reserved, Write to 0
		6	LOCK	Lockout Bit: See "OTP Programming Lockout" Section.
		5	V_{PLUS}	V_{OUTP} Output Voltage Bit: Increase V_{OUTP} by ~25mV
		4:3	IRMP	RAMPP & RAMPN Pullup Current: I_{RAMP} = (2) ^{IRMP} µA
		2	PDDIS	Power-Down Discharge Enable. PUSEQ Must be 11 if Set.
		1:0	PUSEQ	Power-Up Sequencing: 00 = Outputs Disabled, 01 = V_{OUTN} Ramp 1st, 10 = V_{OUTP} Ramp 1st, 11 = Both Ramp Together
04h	CMDR	7	WOTP	Write OTP Memory
		6	CF/ FAULT	Clear Fault/OTP Programming Fault
		5	RST	Reset
		4	SWOFF	Switches-Off
		3	-	Reserved, Write to 0
		2	RSEL2	Register Select 2 (0=OTP2, 1=REG2)
		1	RSEL1	Register Select 1 (0=OTP1, 1=REG1)
		0	RSEL0	Register Select 0 (0=OTP0, 1=REG0)

OTP0/REG0 & OTP1/REG1: Data in addresses 00h & 01h is used to set the output voltages of the Boost and Inverting converters respectively. See Setting the Output Voltages for more information.

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OTP2/REG2: Data in address 02h configures the output voltage sequencing, sets a fine voltage adjust for V_{OUTP}, and determines if further OTP programming is permitted or not. Proper uses of the bits in address 02h are discussed in the following sections.

Setting the Output Voltages (V_P, V_{PLUS} and V_N bits)

The LT3582 series contains two resistor dividers which are programmable in the LT3582, to set the output voltages. The positive output voltage V_{OUTP} is adjustable in 25mV steps by setting the V_P bits in REG0/OTP0 in addition to the V_{PLUS} bit in REG2/OTP2.

$$V_{OUTP} = 3.2V + (V_P \bullet 50mV) + (V_{PLUS} \bullet 25mV)$$

where:

V_P = an integer value from 0 to 191
V_{PLUS} = 0 or 1

The V_{OUTN} voltage is adjustable in –50mV steps by setting the V_N bits in REG1/OTP1.

$$V_{OUTN} = -1.2V - (V_N \bullet 50mV)$$

where:

V_N = an integer value from 0 to 255

Dynamically Changing the Output Voltage (LT3582 Only): After output regulation has been reached, it's possible to change the output voltages by writing new values to the V_N or V_P bits. When reducing the magnitude of an output voltage, it will decay at a rate dependent on the load current and capacitance. Configuring a large increase in magnitude of an output voltage can cause a large increase in switch current to charge the output capacitor. Before reconfiguring the outputs, consider forcing a soft-start by asserting the SWOFF bit before writing the new V_P or V_N codes. Subsequently clearing SWOFF initiates the new soft-start sequence.

Soft-Start/Output Voltage Ramping (IRMP bits)

The LT3582 series contains soft-start circuitry to control the output voltage ramp rates, therefore limiting peak switch currents during start-up. High switch currents are inherent in switching regulators during startup since the feedback loop is saturated due to V_{OUT} being far from its final value. The regulator tries to charge the output capacitor as quickly as possible which results in large currents.

Capacitors must be connected from RAMPP & RAMPN to ground for soft-start. During shutdown or when the SWOFF bit is set, the RAMP capacitors are discharged to ground. After $\overline{SHDN}$ rises or SWOFF is cleared, the capacitors are charged by programmable (LT3582 only) currents, thus creating linear voltage ramps. The V_{OUT} voltages ramp in proportion to their respective RAMP voltages according to:

$$V_{OUT} \quad RAMP \quad RATE = \left(\frac{V_{OUT}}{0.8V}\right) \bullet \left(\frac{I_{RAMP}}{C_{RAMP}}\right) Volts / Sec$$

Proportionality Constant

RAMP pin ramp rate (V/Sec)

where:

I_{RAMP} = RAMP pin charging current set by IRMP bits (1µA, 2µA, 4µA or 8µA for LT3582, 1µA for LT3582-5/LT3582-12)
C_{RAMP} = External RAMP pin capacitor (Farads)
V_{OUT} = Output voltage during regulation

For example, selecting I_{RAMP} = 1µA, C_{RAMP} = 10nF and V_{OUTP} = 12V results in a power-up ramp rate of 1.5Volt/ms (see Figure 6).

Ramp rates less than 1-10V/ms generally result in good startup characteristics. The outputs should linearly follow the RAMPx voltages with no distortions. Figure 7 shows an excessive startup ramp rate of ~120V/ms in which several startup issues have occurred: A) the expected V_{OUTP} ramp up path is not followed B) inductor current ringing occurs C) the V_{OUTP} ramp rate is limited due to the output

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disconnect current limit being reached D) additional ringing occurs when the CAPP pin starts charging E) output voltage overshoot occurs because the inductor currents are maximized during the output ramp up.

In some cases it may be desirable to use only one RAMP pin capacitor. In cases where PUSEQ = 11 (see Power-Up Sequencing section) the RAMPP & RAMPN pins can be connected together and to a single capacitor. In this case the capacitor will charge with twice the current configured by the IRMP bits.

Ramping V_{OUTP} from Ground: The LT3582 series has the unique ability to generate a smooth V_{OUTP} voltage ramp starting from ground and continuing all the way up to regulation (see Figure 6). This ability is not possible with typical Boost converters in which the output is taken from the cathode of the Schottky diode (CAPP node in Figure 5).

The LT3582 series incorporates an output disconnect PMOS allowing V_{OUTP} to be grounded during shutdown.

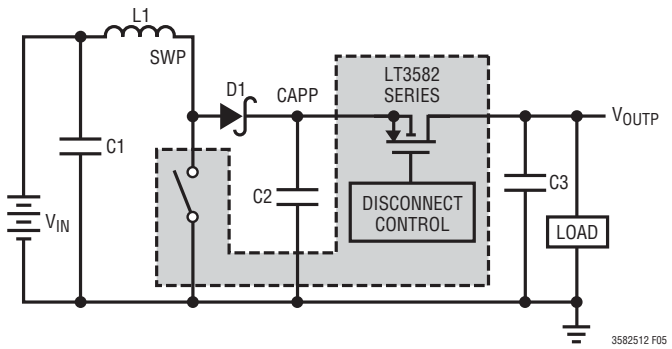


Figure 5: Boost Converter Topology

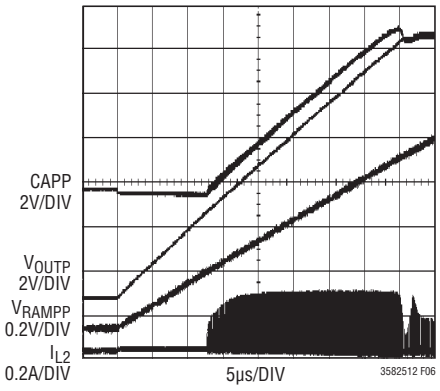


Figure 6: V_{OUTP} Soft-Start Ramping from Ground

Once enabled, the Disconnect Control circuit actively drives the PMOS gate allowing V_{OUTP} to ramp up linearly as shown in Figure 6. Once V_{OUTP} reaches regulation, the PMOS is fully turned "on" to reduce resistance and improve efficiency.

Power-Up Sequencing (PUSEQ bits)

Once enabled, the part requires a delay of $T_{STARTUP}$ (64µs typ) to properly configure itself. Once configured, the order in which V_{OUTP} and V_{OUTN} ramp to regulation is controlled by the PUSEQ bits. The combinations available for the LT3582 are shown in Table 2. The LT3582-5/LT3582-12 are pre-configured with the 11 combination.

Table 2. Power-Up Sequences

PUSEQ[1:0]	Power-Up Sequence
00	Outputs are disabled, neither output ramps up
01	V_{OUTN} ramps up 1st, followed by V_{OUTP}
10	V_{OUTP} ramps up 1st, followed by V_{OUTN}
11	Both V_{OUTP} & V_{OUTN} ramp up starting at the same time.

Selecting the 01 or 10 combinations cause one of the outputs to start ramping shortly after $\overline{SHDN}$ rises. The ramp rate of V_{OUT} is controlled by the RAMP pin as discussed in the Soft-Start section. After V_{OUT} nears its target regulation voltage, the remaining output is activated and ramps

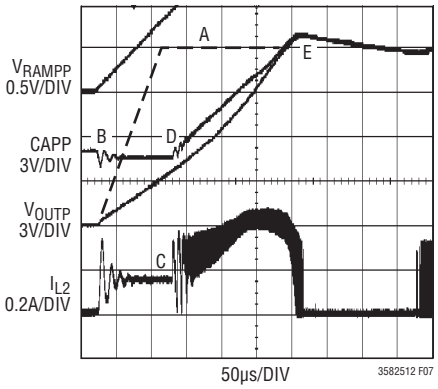


Figure 7: V_{OUTP} Soft-Start with Excessive Ramp Rate

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under control of its respective RAMP pin (see Figure 8 below). The power-up sequencing concludes when both outputs have reached regulation.

Evaluating PUSEQ Settings (LT3582 Only): After $\overline{SHDN}$ rises, the LT3582 uses the PUSEQ configuration found in OTP. The effects of differing PUSEQ settings can be observed without writing to OTP by taking the following actions:

1. Write the SWOFF bit high, stopping both converters and discharging the RAMP pins.
2. Write the desired settings to the PUSEQ bits in REG2.
3. Set the RSEL2 bit high which selects the REG2 configuration settings.
4. Write SWOFF low which restarts both converters.

This will initiate the desired power-up sequence that can be observed with an oscilloscope.

Power-Down Discharge (PDDIS bit)

The PDDIS bit is used to enable power down discharge. This bit is pre-configured to a "1" for the LT3582-5 and LT3582-12, thus enabling power-down discharge.Setting PDDIS = 0 disables the power-down discharge causing the chip to shut down immediately after $\overline{SHDN}$ falls. The PDDIS bit must only be set in conjunction with PUSEQ being set to 11. Driving $\overline{SHDN}$ low, with power-down discharge enabled (PDDIS = 1) causes the chip to power-down after first discharging the output voltages. Specifically, driving $\overline{SHDN}$ low causes the following sequence of events to happen:

1. Both converters are turned off.
2. Discharge currents are enabled to discharge the output capacitors
   - See Electrical Charateristics for $I_{VOUTP-PDS}$ and $I_{CAPP-PDS}$ which help discharge V_{OUTP} and CAPP
   - See Electrical Charateristics for $I_{VOUTN-PDS}$ which helps discharge V_{OUTN}
3. The chip waits until the output voltages have discharged to within ~0.5V to ~1.5V of ground.
4. Discharge currents are disabled and the LT3582 powers down.

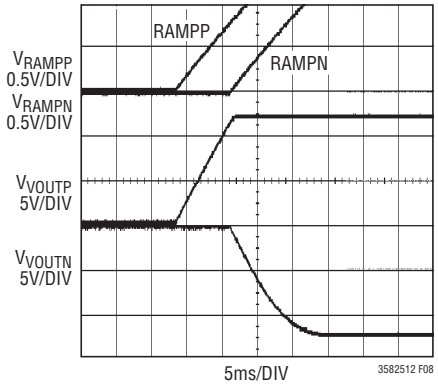


Figure 8: Power-up Sequencing (PUSEQ=10)

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Since the LT3582 series won't power-down until both outputs are discharged (when power-down sequencing is enabled), make sure V_{OUTP} & V_{OUTN} can be grounded. This is not a problem in most topologies. However, read the section Output Disconnect Operating Limits for additional information.

Configuration Lockout (LOCK bit)

After a desired configuration is programmed into OTP, the LOCK bit can be set to prohibit subsequent changes to the configuration. The LT3582-5 and LT3582-12 are preconfigured with the LOCK bit set to a logic "1" which:

- Forces the chip to use the OTP configuration only.
- Forces all I^2C reads from addresses 0-2 to return OTP data.
- Prohibits any further programming of the OTP memory. Any further attempts to program OTP leaves the OTP memory unchanged and sets the FAULT bit in the CMDR.

The LOCK OTP bit is set by programming a logic "1" into bit 6 of OTP2. Regardless of the RSEL2 setting, I^2C reads of the LOCK bit always indicate the LOCKed or unlocked state of the OTP memory.

OTP Programming (LT3582 only)

The LT3582 contains One Time Programmable non-volatile memory to permanently store the chip configuration. Before programming, it's recommended to set the SWOFF bit to disable switching activity and prevent unexpected chip behavior while the configuration is being changed. Programming involves the transfer of information from the REG bytes to the OTP bytes. Therefore, valid data must first be written to the desired REG bytes. After the REG bytes are written, they are selected by setting the corresponding RSEL bits in the CMDR. This forces the chip into the desired configuration and selects those bytes for programming to OTP. After 15V has been applied to V_{PP}, the WOTP bit is set in the CMDR to start the programming. Finally, the WOTP bit is cleared to finish the programming. An example programming algorithm is given below.

OTP programming draws about 3-6mA per bit from the V_{PP} pin. It is possible to program all 23 bits simultaneously (up to ~138mA), but it is recommended that one byte is programmed at a time to reduce noise on V_{PP} caused by the sudden change in current. A 1-10µF V_{PP} bypass capacitor is also recommended to prevent voltage droop after programming begins. Also, avoid hot-plugging V_{PP} which results in very fast voltage ramp rates and can lead to excessive voltage on the V_{PP} pin.

Example OTP Programming Algorithm:

1. Apply 15V to the V_{PP} pin. This can be done at any time before step 5.
2. Write 50h to the CMDR. This disables the power switches during programming by setting the SWOFF bit in the CMDR. This also clears the FAULT bit.
3. Write desired data to REG0-REG2.
4. Write 11h to the CMDR. This selects REG0 for programming while keeping the switches off.
5. Write 91h to the CMDR. This programs the REG0 data to OTP0.
6. Write 11h to the CMDR. This command can be sent immediately after step 5. This stops the programming.
7. Read the CMDR and verify that the FAULT bit is not set.
8. Repeat steps 4-7 for the remaining bytes that need programming.
9. Write 10h to the CMDR. This selects the OTP data for read verification.

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10. Read the OTP data and verify the contents.
11. Write 00h to CMDR. This enables the power switches and the chip will operate from the OTP configuration.
12. Float the V_{PP} pin. This can be done at any time after step 8.

Choosing Inductors

Several series of inductors that work well with the LT3582 series are listed in Table 3. This table is not complete, and there are many other manufacturers and parts that can be used. Consult each manufacturer for more detailed information and for their entire selection of related parts, as many different sizes and shapes are available.

Table 3: Inductor Manufacturers

Coilcraft	LPS3008-LPS4018 Series, XPL2010 Series	www.coilcraft.com
Murata	LQH32C, LQH43C Series	www.murata.com
Sumida	CDRH26D09, CDRH26D11, CDRH3D14 Series	www.sumida.com
TDK	VLF and VLCF Series	www.tdk.com
Würth Elektronik	WE-TPC Series Type T, TH, XS and S	www.we-online.com

Inductances of 2.2µH-10µH typically result in a good tradeoff between inductor size and system performance. More inductance typically yields an increase in efficiency at the expense of increased output ripple. Less inductance may be used in a given application depending on required efficiency and output current. For higher efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Also to improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroidal or shielded inductor (note that the inductance of shielded types will drop more as current increases, and will saturate more easily).

Peak Current Rating: Real inductors can experience a drop in inductance as current and temperature increase. The inductors should have saturation current ratings higher than the peak inductor currents. The peak inductor currents can be calculated as:

$$I_{PK} \cong I_{LIMIT} + \frac{V_{LSWON} \bullet T_{OS}}{L} mA$$

where:

I_{PK} = Peak inductor current
I_{LIMIT} = Typically 350mA for Boost and 600mA for Inverting
L = Inductance in µH
V_{LSWON} = Maximum inductor voltage when the power switch is "on". Typically max V_{IN} for the Boost and Inverting converters.
T_{OS} = 100 for Boost and 125 for Inverting

Maximum Load Currents: Use one of the following equations to estimate the maximum output load current for the positive and negative output voltages:

$$I_{OUTP} = \left(\frac{V_{IN(MIN)}}{V_{OUTP}}\right) \bullet \left(I_{PK} - \frac{T_{OFF_MIN} \bullet (V_{OUTP} + 0.5 - V_{IN(MIN)})}{2 \bullet L}\right) \bullet 0.8\eta$$

$$\text{or } I_{OUTN} = \left(\frac{V_{IN(MIN)}}{V_{IN(MIN)} + |V_{OUTN}|}\right) \bullet \left(I_{PK} - \frac{T_{OFF_MIN} \bullet (|V_{OUTN}| + 0.5)}{2 \bullet L}\right) \bullet 0.8\eta$$

APPLICATIONS INFORMATION

Where…

V_{OUT} = Regulation voltage
$V_{IN(MIN)}$ = Minimum input voltage.
I_{PK} = Peak inductor current. See prior section Peak Current Rating. Use minimum I_{Limit} rating for these calculations.
η = Power conversion efficiency (about 88% for Boost or 78% for Inverting)
T_{OFF_MIN} = Minimum switch off time. Typically 100ns for Boost and 125ns for Inverting.
I_{OUT} = Output load current

For example, if V_{OUTP} = 10V, V_{OUTN} = –10V, V_{IN} = 5V, and L = 4.7µH then I_{OUTP} = 117mA and I_{OUTN} = 105mA.

Note: The 155mA (Typ) current limit of the output disconnect PMOS (see Electrical Characteristics) may limit maximum I_{OUTP} unless CAPP is shorted to V_{OUTP}. See Improving Boost Converter Efficiency.

Maximum Slew Rate: Lower inductance causes higher current slew rates which can lead to current limit overshoot. Choose an inductance higher than L_{MIN} to limit the overshoot:

$$L_{MIN} = V_{IN(MAX)} \bullet 0.2\mu H$$

where $V_{IN(MAX)}$ is the maximum input voltage. Using the previous example V_{IN} = 3V, L_{MIN} = 0.6µH.

Capacitor Selection

The small size and low ESR of ceramic capacitors makes them suitable for most LT3582 series applications. X5R and X7R types are recommended because they retain their capacitance over wider voltage and temperature ranges than other types such as Y5V or Z5U. A 4.7µF input capacitor and a 2.2µF-10µF output capacitor are sufficient for most LT3582 series applications. Always use a capacitor with a sufficient voltage rating. Many capacitors rated at 2.2µF to 10µF, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Generally a 1206 capacitor will be adequate. A 0.22µF to 1µF capacitor placed on the CAPP node is recommended to filter the inductor current while the larger 2.2µF to 10µF placed on the V_{OUTP} & V_{OUTN} nodes will give excellent transient response and stability. Avoid placing large value capacitors (generally > 6.8µF) on **both** CAPP and V_{OUTP}. This configuration can be less stable since it creates two poles, one at the CAPP pin and the other at the V_{OUTP} pin, which can be near each other in frequency. Table 4 shows a list of several capacitor manufacturers. Consult the manufacturers for more detailed information and for their entire selection of related parts.

Table 4: Ceramic Capacitor Manufacturers

MANUFACTURER	PHONE	URL
Kemet	408-986-0424	www.kemet.com
Murata	814-237-1431	www.murata.com
Taiyo Yuden	408-573-4150	www.t-yuden.com
TDK	847-803-6100	www.tdk.com

Diode Selection

Schottky diodes, with their low forward voltage drops and fast switching speeds, are recommended for use with the LT3582 series. The Diodes Inc. B0540WS is a very good choice in a small SOD-323 package. This diode is rated to handle an average forward current of 500mA and performs well across a wide temperature range. Schottky diodes with very low forward voltage drops are also available. These diodes may improve efficiency at moderate and cold temperatures, but will likely reduce efficiency at higher temperatures due to excessive reverse leakage currents.

APPLICATIONS INFORMATION

Output Disconnect Operating Limits

The LT3582 series has a PMOS output disconnect switch connected between CAPP and V_{OUTP}. During normal operation, the switch is closed and current is internally limited to about 155mA (see Figure 9). Make sure that the output load current doesn't exceed the PMOS current limit. Exceeding the current limit causes a significant rise in PMOS power consumption which may damage the device.

During shutdown, the PMOS switch is open and CAPP is isolated from V_{OUTP} up to a voltage difference of 5-5.5V. In most cases this allows V_{OUTP} to discharge to ground. However, when the Boost inductor input exceeds 5.5V, the CAPP-V_{OUTP} voltage may exceed 5V allowing some current flow through the PMOS switch. In addition, applying CAPP-V_{OUTP} voltages in excess of 5.7V(typical) may activate internal protection circuitry which turns the PMOS "on" (see Figure 10). If the current is not limited, this can lead to a sharp increase in the PMOS power consumption and may damage the device. If this situation cannot be avoided, limit PMOS power consumption to less than 1/3 Watt (about 50mA at 7V) to avoid damaging the device. Refer to the Absolute Maximum Ratings table for maximum limits on CAPP-V_{OUTP} voltages and currents.

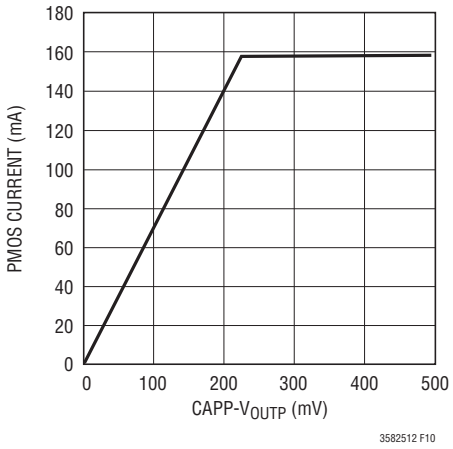


Figure 9: PMOS Current vs. Voltage During Normal Operation

Improving Boost Converter Efficiency

The efficiency of the Boost converter can be improved by shorting the CAPP pin to the V_{OUTP} pin (see Figure 11). The power loss in the PMOS disconnect circuit is then made negligible. In most applications, the associated CAPP pin capacitor can be removed and the larger V_{OUTP} capacitor can adequately filter the output voltage.

Note that the ripple voltage on V_{OUTP} will typically increase in this configuration since the output disconnect PMOS, when not shorted, helps to create an RC filter at the output. Also, if the V_{OUTP} pin is shorted to CAPP, the power-down discharge should not be enabled. V_{OUTP} cannot be discharged to ground during shutdown due to the path from V_{IN} to V_{OUTP} through the external inductor

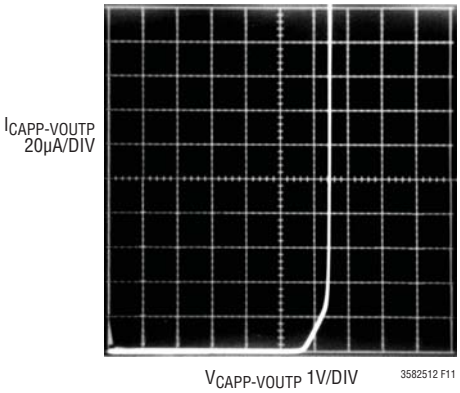


Figure 10: PMOS Current vs. Voltage During Shutdown

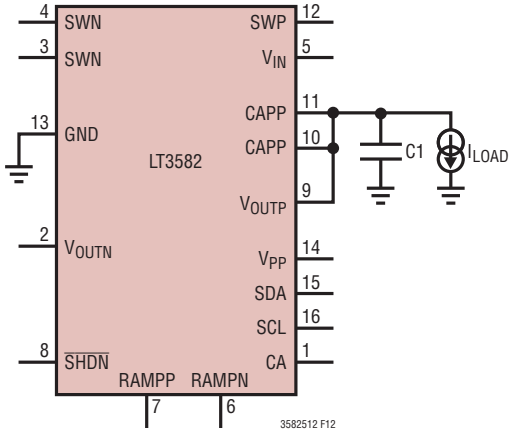


Figure 11: Improved Efficiency

APPLICATIONS INFORMATION

and diode. Finally, due to the path from V_{IN} to V_{OUTP}, current will flow through the integrated feedback resistor whenever voltage is present on V_{IN}.

Inrush Current

When the Boost inductor input voltage (usually V_{IN}) is stepped from ground to the operating voltage, a high level of inrush current may flow through the inductor and Schottky diode into the CAPP capacitor. Conditions that increase inrush current include a larger more abrupt voltage step at the inductor input, larger CAPP capacitors and inductors with low inductances and/or low saturation currents. For circuits that use output capacitor values within the recommended range and have input voltages of less than 5V, inrush current remains low, posing no hazard to the devices. In cases where there are large input voltage steps (more than 5V) and/or a large CAPP capacitor is used, inrush current should be measured to ensure safe operation.

Thermal Lockout

If the die temperature reaches approximately 147°C, the part will go into thermal lockout. In this event, the chip is reset which turns off the power switches and starts to discharge the RAMP capacitors. The part will be re-enabled when the die temperature drops by about 3.5°C.

Board Layout Considerations

As with all switching regulators, careful attention must be paid to the PCB board layout and component placement. To maximize efficiency, switch rise and fall times are made as short as possible. To prevent electromagnetic interference (EMI) problems, proper layout of the high frequency switching path is essential. The voltage signals of the SWP and SWN pins have sharp rising and falling edges. Minimize the length and area of all traces connected to the SWP/SWN pins and always use a ground plane under the switching regulator to minimize interplane coupling. Suggested component placement is shown in Figure 12. Make sure to include the ground plane cuts as shown in Figure 12. The switching action of the regulators can cause large current steps in the ground plane. The cuts reduce noise by recombining the current steps into a continuous flow under the chip, thus reducing di/dt related ground noise in the ground plane.

APPLICATIONS INFORMATION

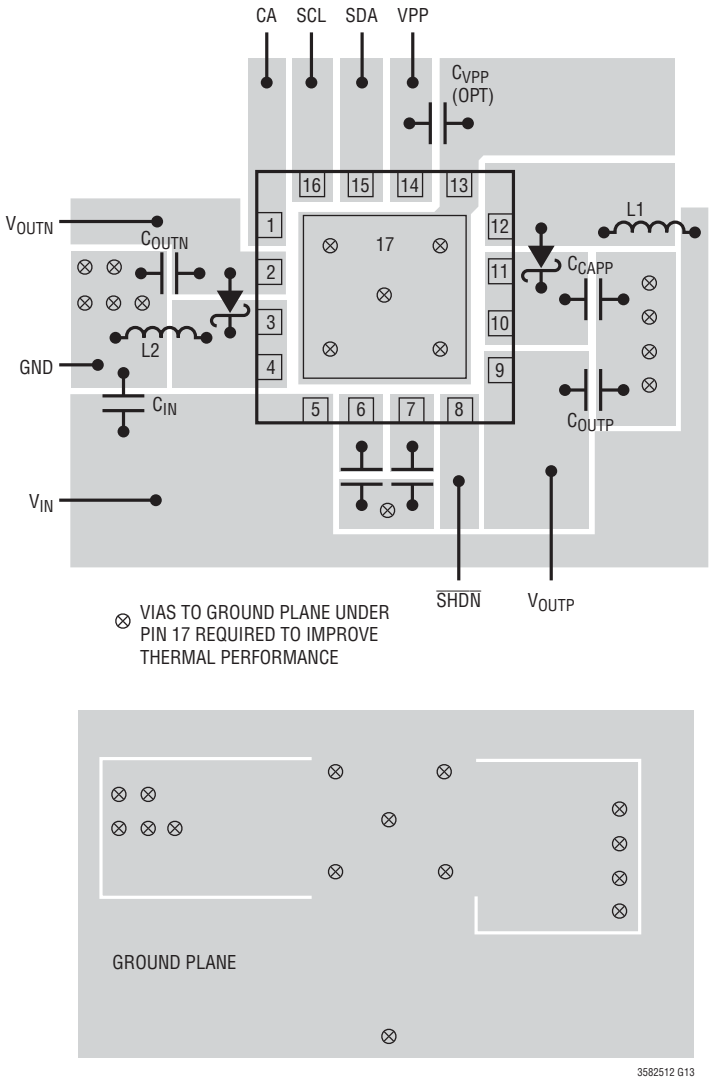
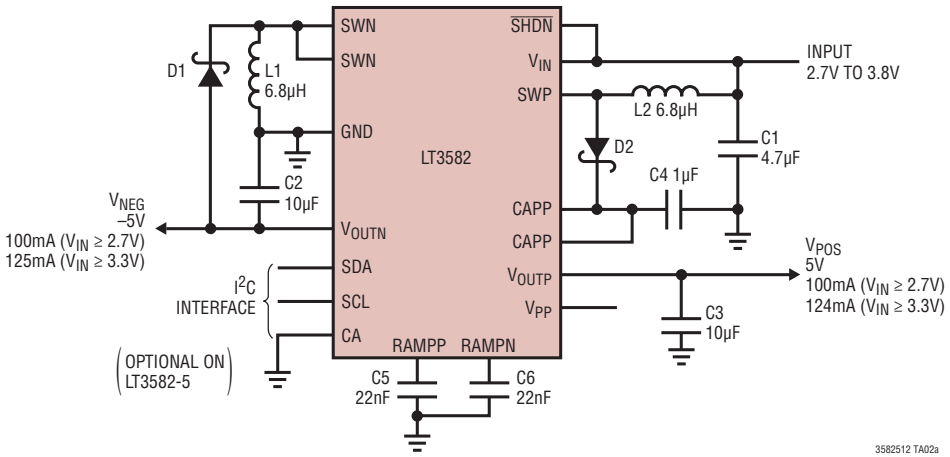


Figure 12: Suggested Component Placement (not to scale)

TYPICAL APPLICATION

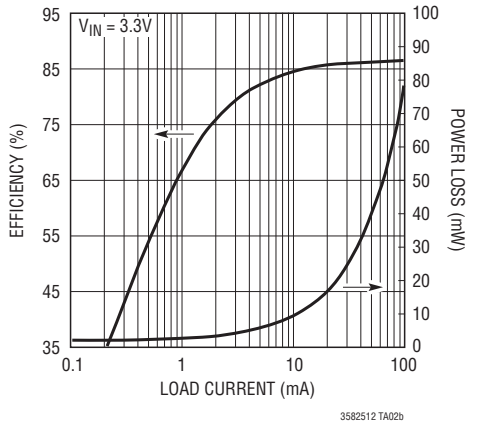
±5V Outputs from a Single 2.7V to 3.8V Input



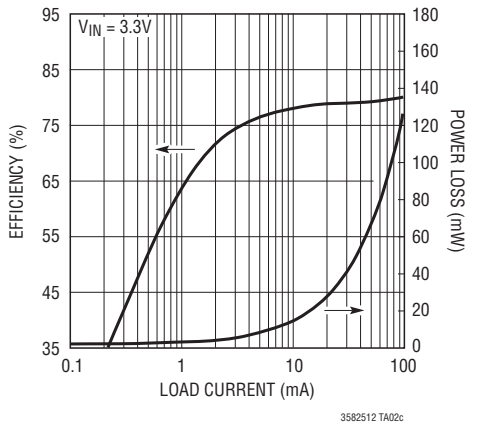
REG0/OTP0 = 24h
REG1/OTP1 = 4Ch
REG2/OTP2 = 03h

D1-D2: DIODES INC. B0540WS-7
L1-L2: COILCRAFT LPS4018-682ML
C1: 4.7µF, 6.3V, X5R, 0805
C2-C3: 10µF, 6.3V, X5R 0805
C4: 1µF, 6.3V, X5R, 0603
C5-C6: 22nF, 0603

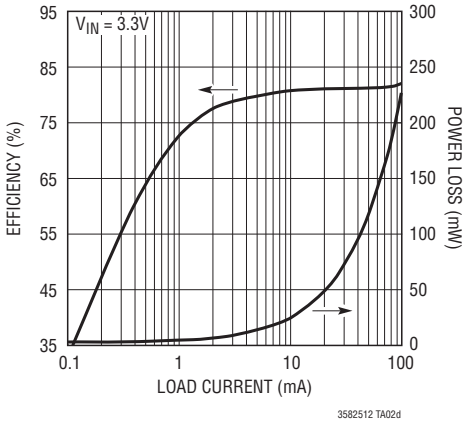
Efficiency and Power Loss, Load from V_{OUTP} to GND



Efficiency and Power Loss, Load from V_{OUTN} to GND

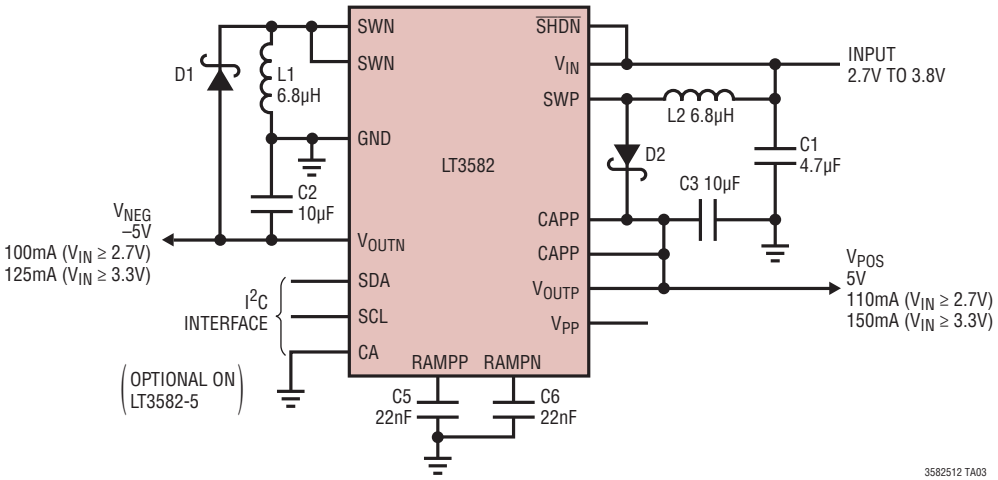


Efficiency and Power Loss, Load from V_{OUTP} to V_{OUTN}



TYPICAL APPLICATION

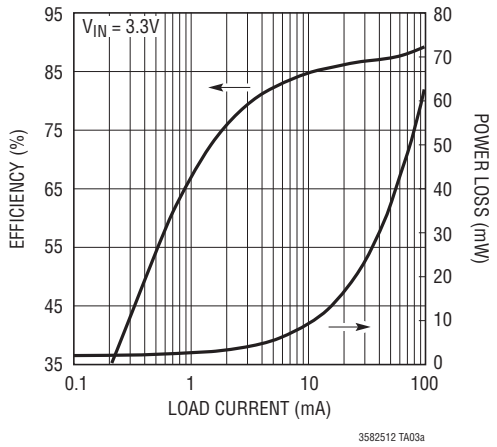
±5V Outputs from a Single 2.7V to 3.8V Input (Improved Efficiency)



REG0/OTP0 = 24h
REG1/OTP1 = 4Ch
REG2/OTP2 = 03h

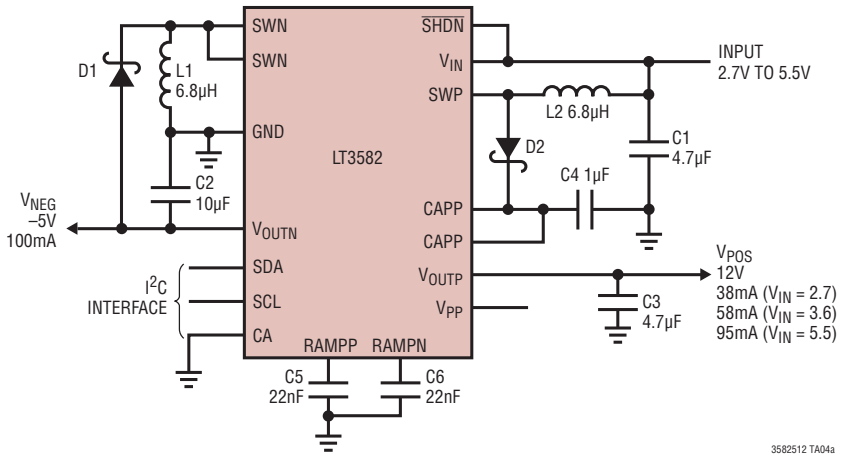
D1-D2: DIODES INC. B0540WS-7
L1-L2: COILCRAFT LPS4018-682ML
C1: 4.7µF, 6.3V, X5R, 0805
C2-C3: 10µF, 6.3V, X5R, 0805
C4: 1µF, 6.3V, X5R, 0603
C5-C6: 22nF, 0603

Efficiency and Power Loss, Load from V_{OUTP} to GND



TYPICAL APPLICATION

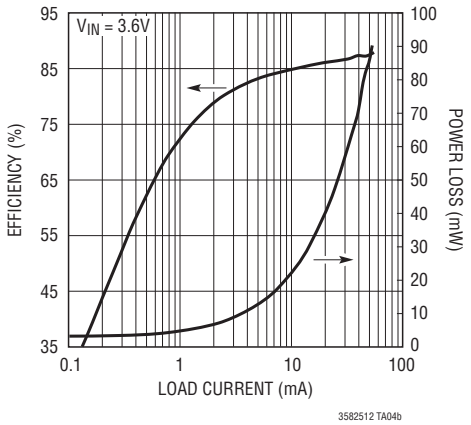
12V and –5V Outputs from a Single 2.7V to 5.5V Input



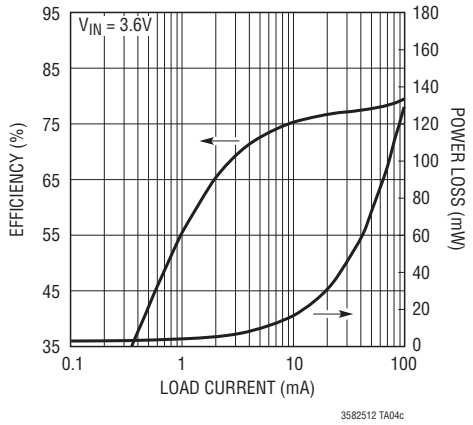
REG0/OTP0 = B0h
REG1/OTP1 = 4Ch
REG2/OTP2 = 0Bh

D1-D2: DIODES INC. B0540WS-7
L1-L2: COILCRAFT LPS4018-682ML
C1: 4.7µF, 6.3V, X5R, 0805
C2: 10µF, 6.3V, X5R, 0805
C3: 4.7µF, 16V, X5R, 0805
C4: 1µF, 16V, X5R, 0603
C5-C6: 22nF, 0603

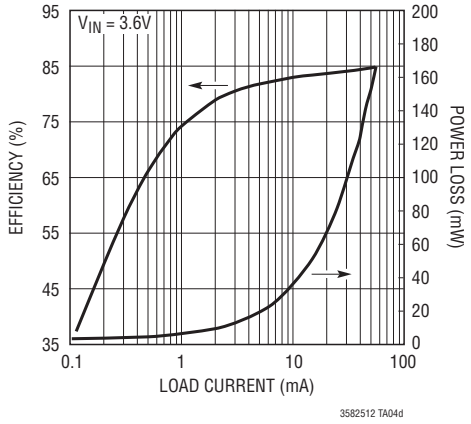
Efficiency and Power Loss, Load from V_{OUTP} to GND



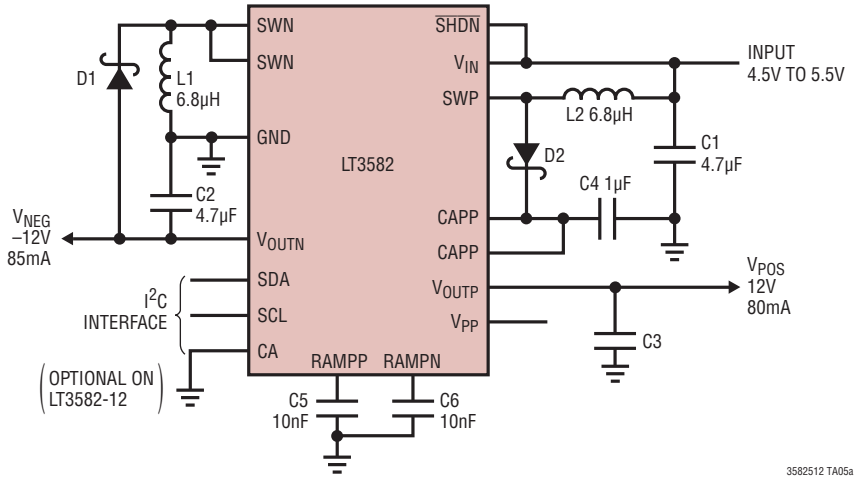
Efficiency and Power Loss, Load from V_{OUTN} to GND



Efficiency and Power Loss, Load from V_{OUTP} to V_{OUTN}



TYPICAL APPLICATION

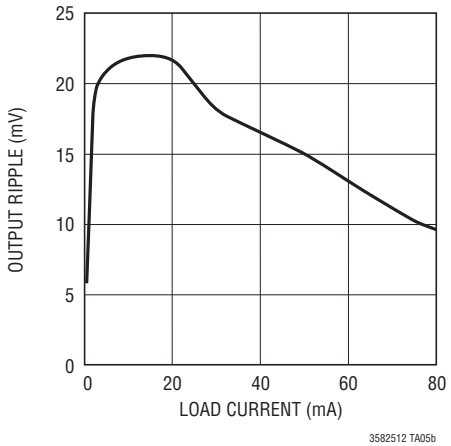


REG0/OTP0 = B0h
REG1/OTP1 = D8h
REG2/OTP2 = 03h

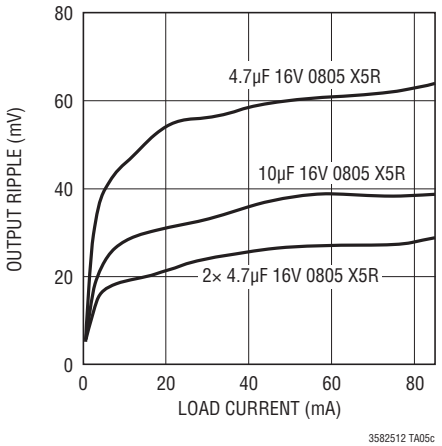
D1-D2: DIODES INC. B0540WS-7
L1-L2: COILCRAFT XPL2010-682
C1: 4.7µF, 6.3V, X5R, 0805
C2: 4.7µF, 16V, X5R, 0805
C3: 1× 4.7µF OR 2× 4.7µF OR 10µF 16V, X5R, 0805
C4: 1µF, 16V, X5R, 0603
C5-C6: 10nF, 0603

Figure 13. ±12V Outputs from a Single 5V Input

V_{OUTP} Ripple



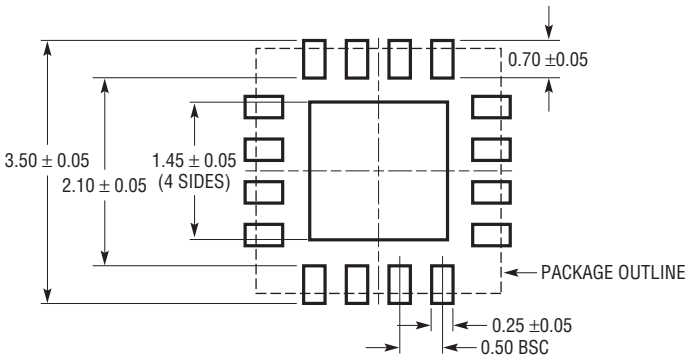
V_{OUTN} Ripple and C2 Selection



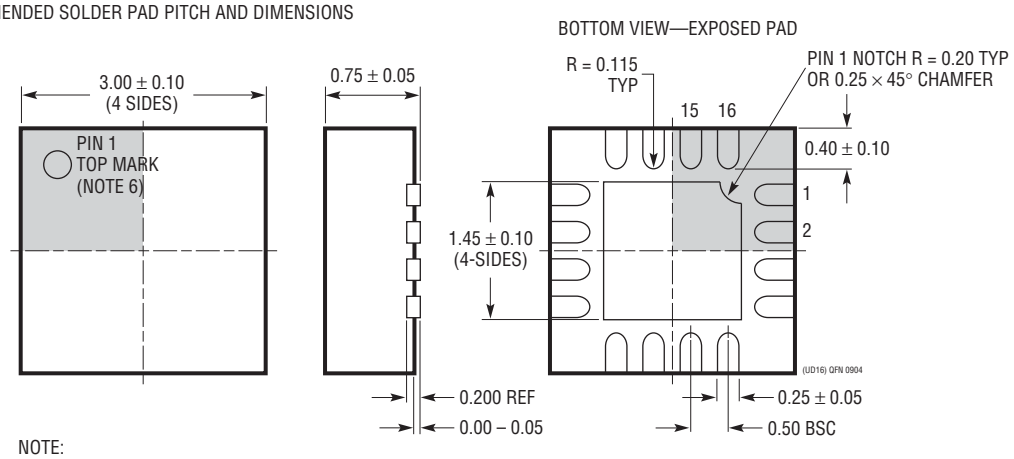
Also See Typical Characteristics and Front Page for Additional Data

PACKAGE DESCRIPTION

UD Package
16-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1691)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

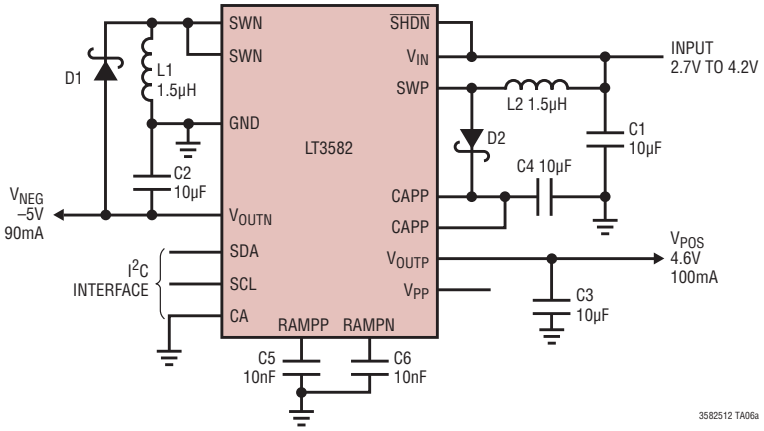


NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-2)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

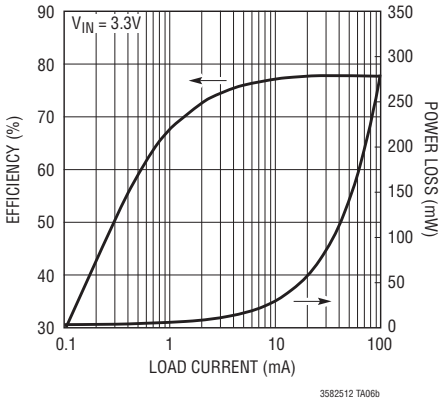
Tiny AMOLED Power Supply is 0.8mm (Max) Thin



REG0/OTP0 = 1Ch
REG1/OTP1 = 4Ch
REG2/OTP2 = 07h

D1-D2: PANASONIC M21D3800L LOW V_F SCHOTTKY
L1-L2: TDK MLP3216S1R5L
C1-C4: TAIYO YUDEN JMK212BJ106MK, 6.3V, X5R 0805
C5-C6: 0402 X5R

Efficiency and Power Loss, Load from V_{OUTP} to V_{OUTN}



RELATED PARTS

PART	DESCRIPTION	COMMENTS
LT1944/-1(Dual)	Dual Output 350mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = 34V, I_Q = 20µA, I_{SD} <1µA, MS10
LT1945(Dual)	Dual Output, Pos/Neg, 350mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$ = ±34V, I_Q = 20µA, I_{SD} <1µA, MS10
LT3463/A	Dual Output, Boost/Inverter, 250mA I_{SW}, Constant Off-Time, High Efficiency Step-Up DC/DC Converter with Integrated Schottkys	V_{IN}: 2.4V to 15V, $V_{OUT(MAX)}$ = ±40V, I_Q = 40µA, I_{SD} <1µA, DFN
LT3471	Dual Output, Boost/Inverter, 1.3A I_{SW}, 1.2MHz, High Efficiency Boost-Inverting DC/DC Converter	V_{IN}: 2.4V to 16V, $V_{OUT(MAX)}$ = ±40V, I_Q = 2.5mA, I_{SD} <1µA, DFN
LT3472	Dual Output, Boost/Inverter, 0.35A I_{SW}, 1.2MHz, High Efficiency Boost-Inverting DC/DC Converter	V_{IN}: 2.2V to 16V, $V_{OUT(MAX)}$ = ±34V, I_Q = 2.8mA, I_{SD} <1µA, DFN
LT3477	42V, 3A, 3.5MHz Boost, Buck-Boost, Buck LED Driver	V_{IN}: 2.5V to 25V, $V_{OUT(MAX)}$ = 40V, I_Q = Analog/PWM, I_{SD} <1µA, QFN, TSSOP-20E
LT3494/A	180/350mA (I_{SW}), Low Noise High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.3V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 65µA, I_{SD} <1µA, 2mm × 3mm DFN
LT3495/ LT3495B/ LT3495-1/ LT3495B-1	650/350mA (I_{SW}), Low Noise High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.5V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 60µA, I_{SD} <1µA, 2mm × 3mm DFN
LT1930/A	1A (I_{SW}), 1.2/2.2MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2/5.5mA, I_{SD} <1µA, ThinSOT
LT1931/A	1A (I_{SW}), 1.2/2.2MHz, High Efficiency Inverting DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 4.2/5.5mA, I_{SD} <1µA, ThinSOT
LT3467/A	1.1A (I_{SW}), 1.3/2.1MHz, High Efficiency Step-Up DC/DC Converter with Soft-Start	V_{IN}: 2.4V to 16V, $V_{OUT(MAX)}$ = 40V, I_Q = 1.2mA, I_{SD} <1µA, ThinSOT
LT1618	1.5A (I_{SW}), 1.4MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.6V to 18V, $V_{OUT(MAX)}$ = 35V, I_Q = 1.8mA, I_{SD} <1µA, MS10, DFN
LT1946/A	1.5A (I_{SW}), 1.2/2.7MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.6V to 16V, $V_{OUT(MAX)}$ = 34V, I_Q = 3.2mA, I_{SD} <1µA, MS8E

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
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