KK82C55

CHMOS PROGRAMMABLE PERIPHERAL INTERFACE

The Integral KK82C55AN is a high-performance, CHMOS version of the industry standard KK82C55AN general purpose programmable I/O device which is designed for use with all Intel and most other microprocessors. It provides 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation.

In MODE 0, each group of 12 I/O pins may be programmed in sets of 4 and 8 to be inputs or outputs. In MODE 1, each group may be programmed to have 8 lines of input or output. 3 of the remaining 4 pins are used for handshaking and interrupt control signals. MODE 2 is a strobed bi-directional bus configuration.

FEATURES

- Compatible with all Intel and Most Other Microprocessors
- High Speed, «Zero Wait State» Operation with 8MHz 8086/88 and 80186/188
- 24 Programmable I/O Pins
- Low Power CHMOS
- Completely TTL Compatible
- Control Word Read-Back Capability
- Direct Bit Set/Reset Capability
- 2.5mA DC Drive Capability on all I/O Port Outputs
- Available in 40-Pin DIP
- Available in EXPRESS
  - Standard Temperature Range
  - Extended Temperature Range
  -

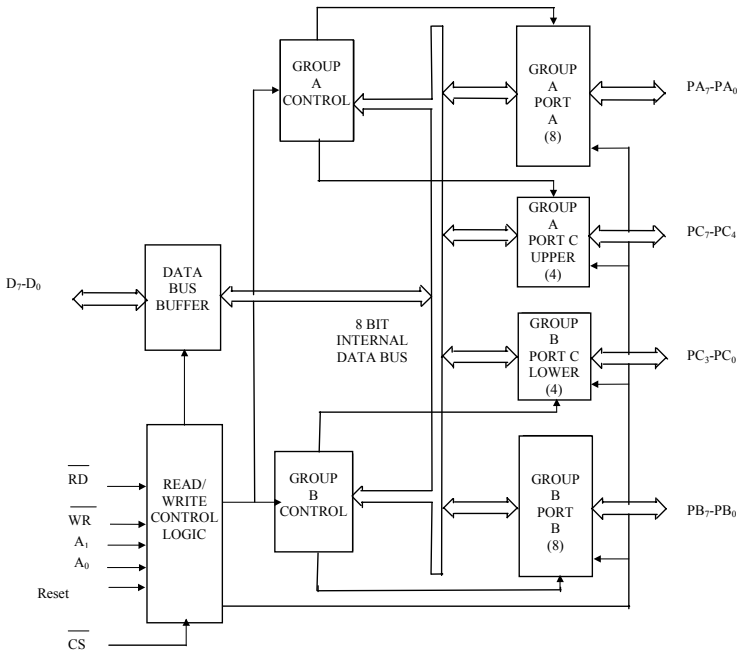


Figure 1

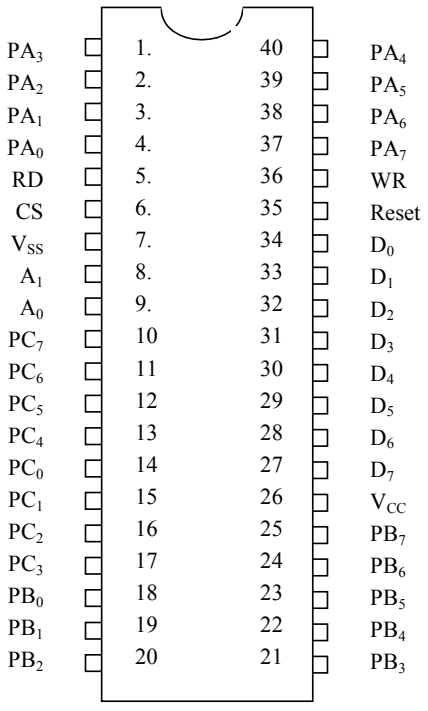


Figure 2

<table>
<tr><th>Symbol</th><th>Pin number</th><th>Type</th><th>Name and Function</th></tr>
<tr><td>PA_{3-0}</td><td>1-4</td><td>I/O</td><td>PORT A, PINS 0-3: Lower nibble of an 8-bit data output latch buffer and an 8-bit data input latch.</td></tr>
<tr><td>$\overline{RD}$</td><td>5</td><td>I</td><td>READ CONTROL: This input is low during CPU read operations.</td></tr>
<tr><td>$\overline{CS}$</td><td>6</td><td>I</td><td>CHIP SELECT: A low on this input enables the 82C55A to respond to $\overline{RD}$ and $\overline{WR}$ signals RD and WR are ignored otherwise.</td></tr>
<tr><td>GND</td><td>7</td><td></td><td>System Ground.</td></tr>
<tr><td>A_{1-0}</td><td>8-9</td><td>I</td><td>ADDRESS: These input signals in conjunction $\overline{RD}$ and $\overline{WR}$ control the selection of one of the three ports or the control word registers.
<table>
<tr><th>A_1</th><th>A_0</th><th>$\overline{RD}$</th><th>$\overline{WR}$</th><th>$\overline{CS}$</th><th>Input Operation (Read)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port A - Data Bus</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Port B - Data Bus</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Port C - Data Bus</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Control Word - Data Bus</td></tr>
<tr><td colspan="5"></td><td>Output Operation (Write)</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port A</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port B</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Data Bus - Port C</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Data Bus – Control</td></tr>
<tr><td colspan="5"></td><td>Disable Function</td></tr>
<tr><td>x</td><td>x</td><td>x</td><td>x</td><td>1</td><td>Data Bus-3-State</td></tr>
<tr><td>x</td><td>x</td><td>1</td><td>1</td><td>0</td><td>Data Bus-3-State</td></tr>
</table></td></tr>
<tr><td>PC_{7-4}</td><td>10-13</td><td>I/O</td><td>PORT C, PINS 4-7: Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.</td></tr>
<tr><td>PC_{0-3}</td><td>14-17</td><td>I/O</td><td>PORT C, PINS 0-3: Lower nibble of Port C.</td></tr>
<tr><td>PB_{0-7}</td><td>18-25</td><td>I/O</td><td>PORT B, PINS 0-7: An 8-bit data output latch/buffer and an 8-bit data input buffer</td></tr>
<tr><td>VCC</td><td>26</td><td></td><td>SYSTEM POWER: +5V Power Supply</td></tr>
<tr><td>D_{7-0}</td><td>27-34</td><td>I/O</td><td>DATA BUS: Bi-directional, tri-state data bus lines, connected to system data bus</td></tr>
<tr><td>RESET</td><td>35</td><td>I</td><td>RESET: A high on this input clears the control register and all ports are set to the input mode</td></tr>
<tr><td>$\overline{WR}$</td><td>36</td><td>I</td><td>WRITE CONTROL: This input is low during CPU write operations</td></tr>
<tr><td>PA_{7-4}</td><td>37-40</td><td>I/O</td><td>PORT A PINS 4-7: Upper nibble of an 8-bit data output latch/buffer and an 8-bit data input latch</td></tr>
</table>

KK82C55AN FUNCTIONAL DESCRIPTION

General

The KK82C55AN is a programmable peripheral interface device designed for use in Intel microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the KK82C55AN is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the KK82C55AN to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU “outputs” a control word to the KK82C55AN. The control word contains information such as “mode”, “bit set”, “bit reset”, etc., that initializes the functional configuration of the 82C55A. Each of the Control blocks (Group A and Group B) accepts “commands” from the Read/Write Control Logic, receives “control words” from the internal data bus and issues the proper commands to its associated ports.

Control Group A - Port A and Port C upper (C7 - C4)

Control Group B - Port B and Port C lower (C3 - C0)

The control word register can be both written and read as shown in the address decode table in the pin descriptions. Figure 6 shows the control word format for both Read and Write operations. When the control word is read, bit D7 will always be a logic “1”, as this implies control word mode information.

Ports A, B, and C

The KK82C55AN contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or “personality” to further enhance the power and flexibility of the KK82C55AN.

Port A. One 8-bit data output latch/buffer and one 8-bit input latch/buffer. Both “pull-up” and “pull-down” bus hold devices are present on Port A.

Port B. One 8-bit data input/output latch/buffer. Only “pull-up” bus hold devices are present on Port B.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B. Only “pull-up” bus hold devices are present on Port C.

See Figure 4 for the bus-hold circuit configuration for Port A, B, and C.

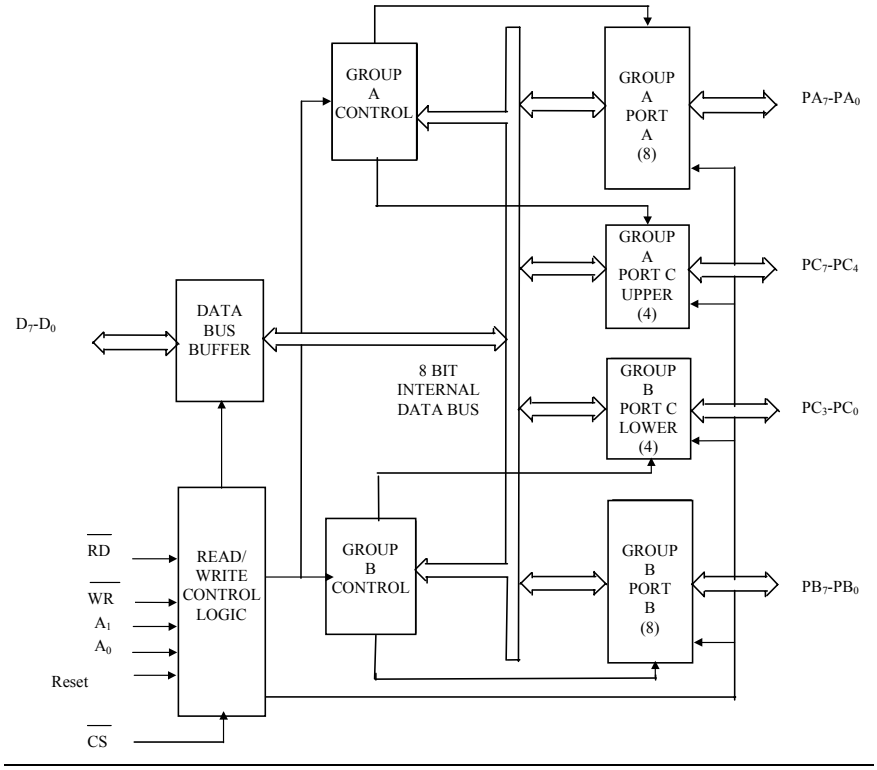
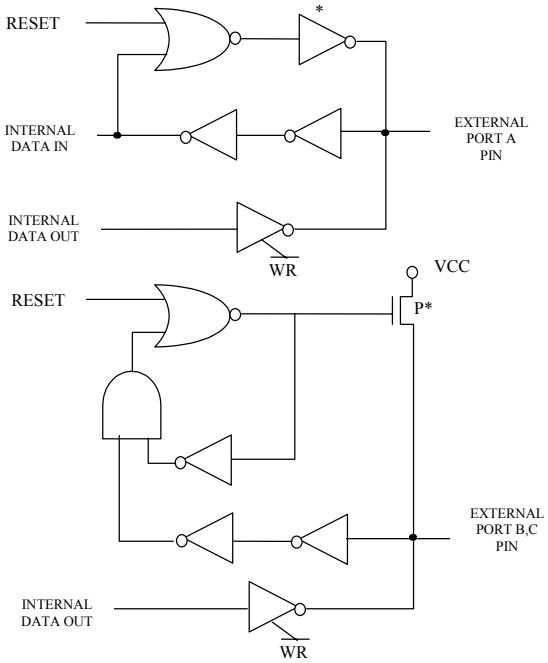


Figure 3.KK82C55AN Block Diagram Showing Data Bus Buffer and Read Write Control Logic Functions



*NOTE:
Port pins loaded with more than 20pF capacitance may not have their logic level guaranteed following a hardware reset.

Figure 4. Port A, B, C, Bus-hold Configuration

KK82C55AN OPERATIONAL DESCRIPTION

Mode Selection

There are three basic modes of operation that can be selected by the system software:

Mode 0 - Basic input/output

Mode 1 - Strobed Input/output

Mode 2 - Bi-directional Bus

When the reset input goes “high” all ports will be set to the input mode with all 24 port lines held at a logic “one” level by the internal bus hold devices (see Figure 4 Note). After the reset is removed the KK82C55AN can remain in the input mode with no additional initialization required. This eliminates the need for pullup or pulldown devices in “all CMOS” designs. During the execution of the system program, any of the other modes may be selected by using a single output instruction. This allows a single KK82C55AN to service a variety of peripheral devices with a simple software maintenance routine.

The modes for Port A and Port B can be separately defined, while Port C is divided into two portions as required by the Port A and Port B definitions. All of the output registers, including the status flip-flops, will be reset whenever the mode is changed. Modes may be combined so that their functional definition can be “tailored” to almost any I/O structure. For instance; Group B can be programmed in Mode 0 to monitor simple switch closings or display computational results, Group A could be programmed in Mode 1 to monitor a keyboard or tape reader on an interrupt-driven basis.

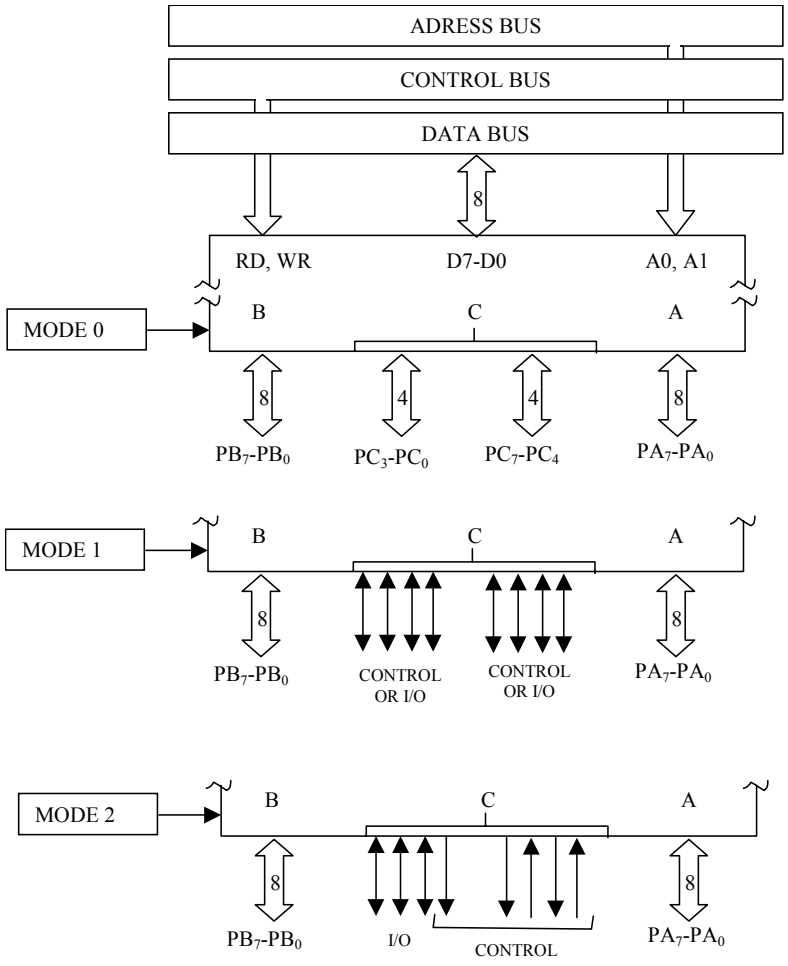


Figure 5. Basic Mode Definitions and Bus Interface

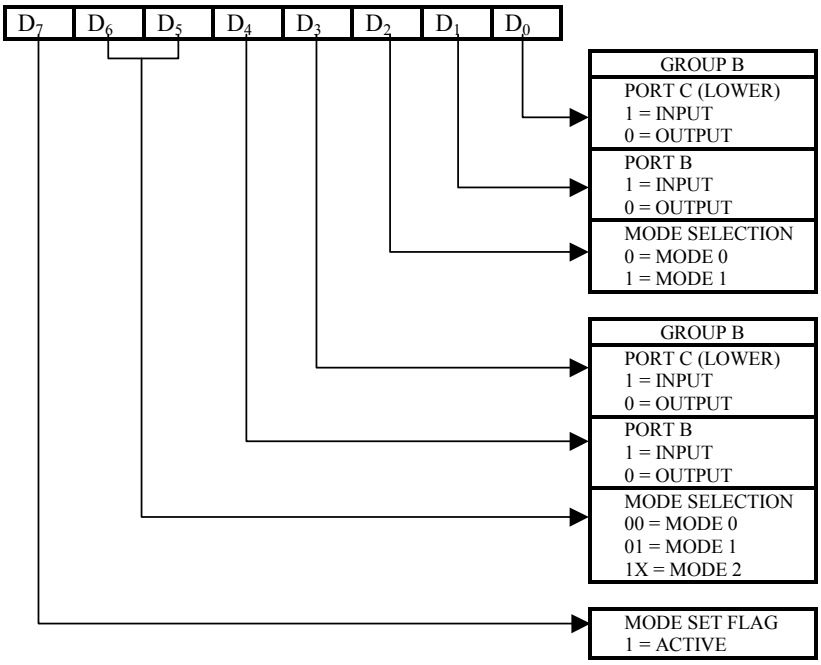


Figure 6. Mode Definition Format

The mode definitions and possible mode combinations may seem confusing at first but after a cursory review of the complete device operation a simple, logical I/O approach will surface. The design of the 82C55A has taken into account things such as efficient PC board layout, control signal definition vs PC layout and complete functional flexibility to support almost any peripheral device with no external logic. Such design represents the maximum use of the available pins.

Single Bit Set/Reset Feature

Any of the eight bits of Port C can be Set or Reset using a single OUTput instruction. This feature reduces software requirements in Control-based applications.

When Port C is being used as status/control for Port A or B, these bits can be set or reset by using the Bit Set/Reset operation just as if they were data output ports.

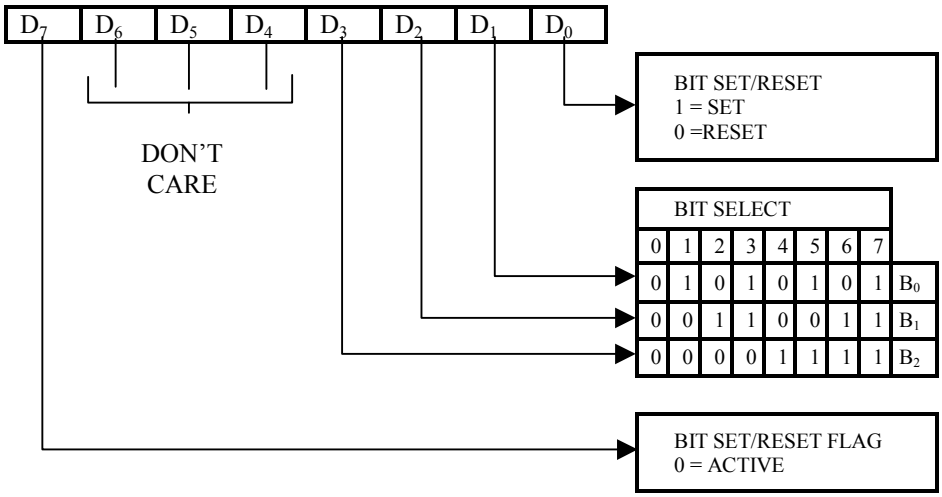


Figure 7. Bit Set/Reset Format

Interrupt Control Functions

When the KK82C55AN is programmed to operate in mode 1 or mode 2, control signals are provided that can be used as interrupt request inputs to the CPU. The interrupt request signals, generated from port C, can be inhibited or enabled by setting or resetting the associated INTE flip-flop, using the bit set/reset function of port C.

This function allows the Programmer to disallow or allow a specific I/O device to interrupt the CPU without affecting any other device in the interrupt structure.

INTE flip-flop definition:

(BIT-SET) - INTE is SET - Interrupt enable

(BIT-RESET) – INTE is RESET - Interrupt disable

Note:

All Mask flip-flops are automatically reset during mode selection and device Reset.

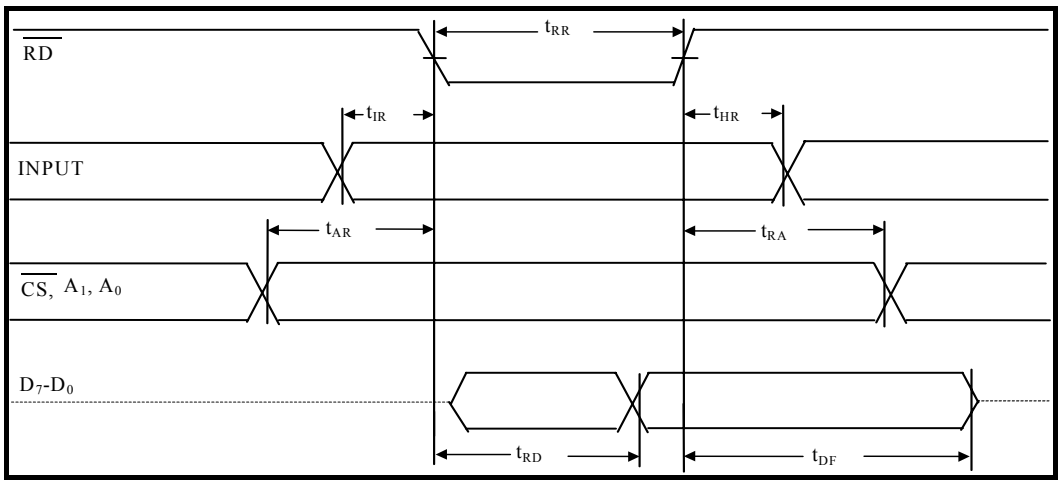
Operating Modes

Mode 0 (Basic Input/Output). This functional configuration provides simple input and output operations for each of the three ports. No "handshaking" is required, data is simply written to or read from a specified port.

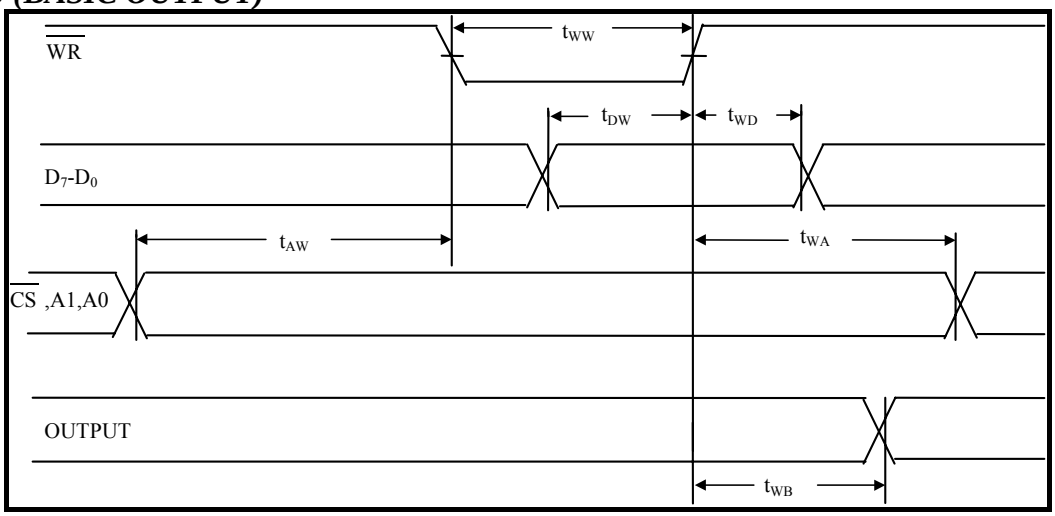
Mode 0 Basic Functional Definitions:

- Two 8-bit ports and two 4-bit ports.
- Any port can be input or output.
- Outputs are latched.
- Inputs are not latched.
- 16 different Input/Output configurations are possible in this Mode.

MODE 0 (BASIC INPUT)



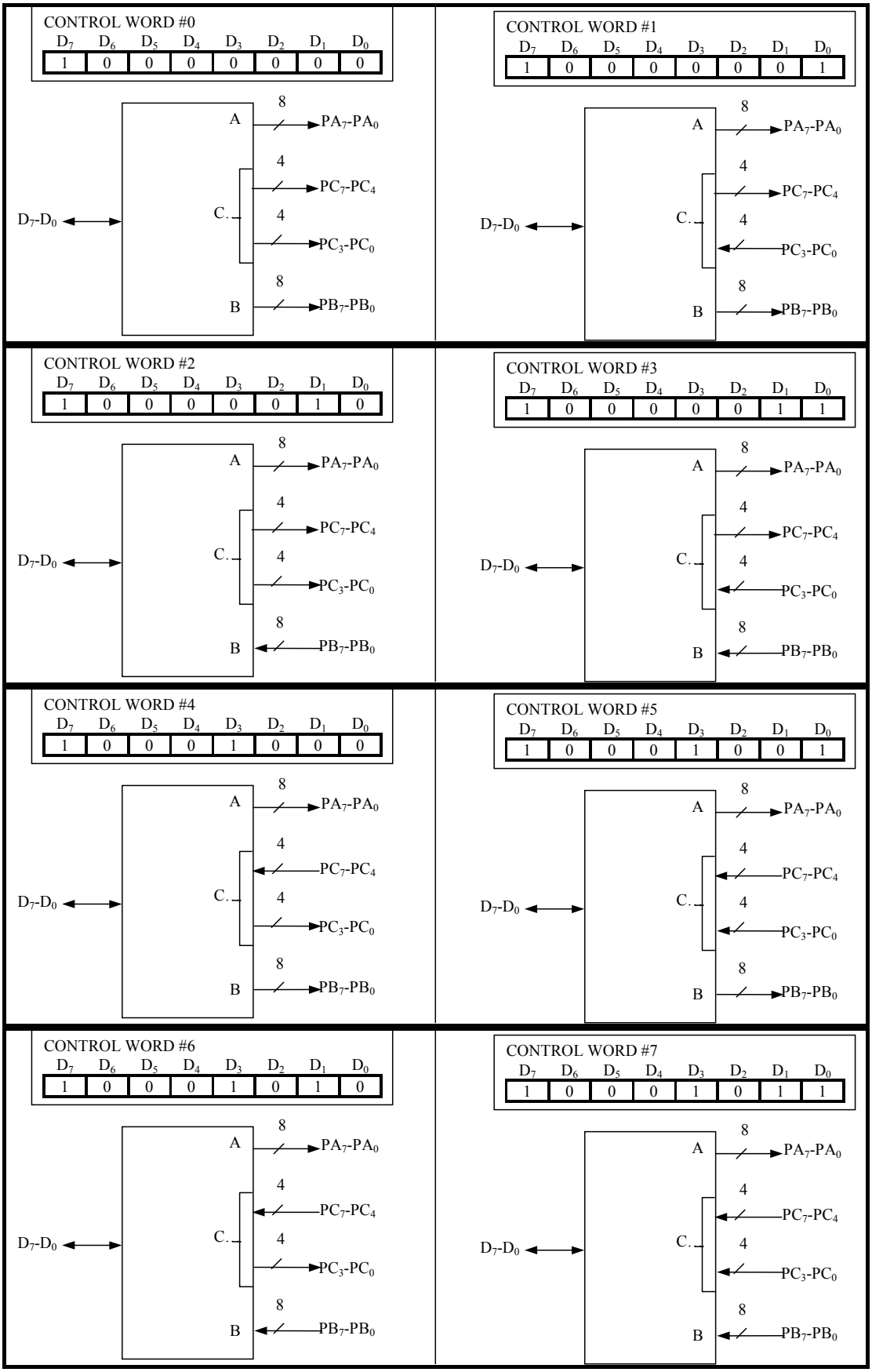
MODE 0 (BASIC OUTPUT)



MODE 0 Port Definition

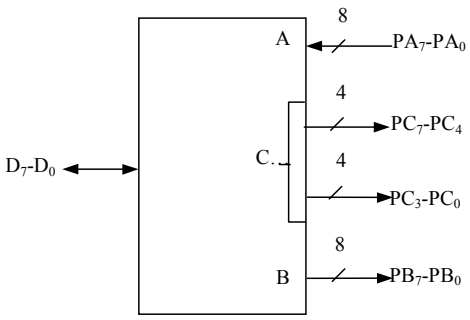
A		B		GROUP A			GROUP B	
D4	D3	D1	D0	PORT A	PORT C (UPPER)	#	PORT B	PORT C (LOWER)
0	0	0	0	OUTPUT	OUTPUT	0	OUTPUT	OUTPUT
0	0	0	1	OUTPUT	OUTPUT	1	OUTPUT	INPUT
0	0	1	0	OUTPUT	OUTPUT	2	INPUT	OUTPUT
0	0	1	1	OUTPUT	OUTPUT	3	INPUT	INPUT
0	1	0	0	OUTPUT	INPUT	4	OUTPUT	OUTPUT
0	1	0	1	OUTPUT	INPUT	5	OUTPUT	INPUT
0	1	1	0	OUTPUT	INPUT	6	INPUT	OUTPUT
0	1	1	1	OUTPUT	INPUT	7	INPUT	INPUT
1	0	0	0	INPUT	OUTPUT	8	OUTPUT	OUTPUT
1	0	0	1	INPUT	OUTPUT	9	OUTPUT	INPUT
1	0	1	0	INPUT	OUTPUT	10	INPUT	OUTPUT
1	0	1	1	INPUT	OUTPUT	11	INPUT	INPUT
1	1	0	0	INPUT	INPUT	12	OUTPUT	OUTPUT
1	1	0	1	INPUT	INPUT	13	OUTPUT	INPUT
1	1	1	0	INPUT	INPUT	14	INPUT	OUTPUT
1	1	1	1	INPUT	INPUT	15	INPUT	INPUT

MODE 0 Configurations



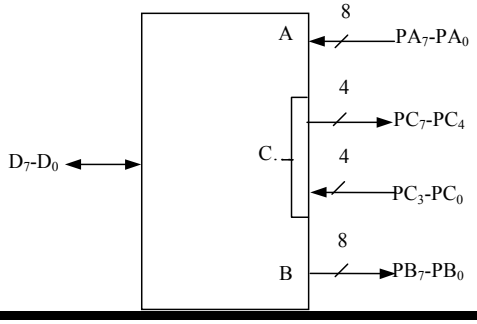
CONTROL WORD #8

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	0



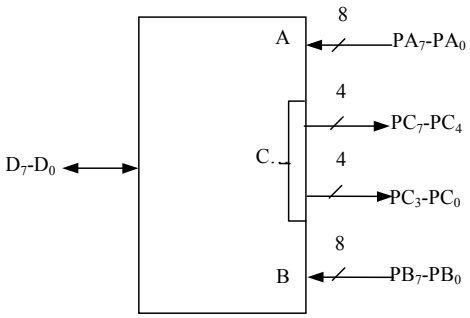
CONTROL WORD #9

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	0	1



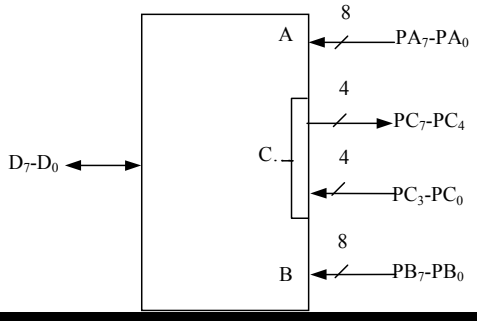
CONTROL WORD #10

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	0



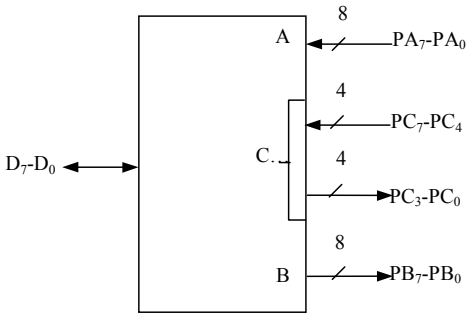
CONTROL WORD #11

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	0	0	1	1



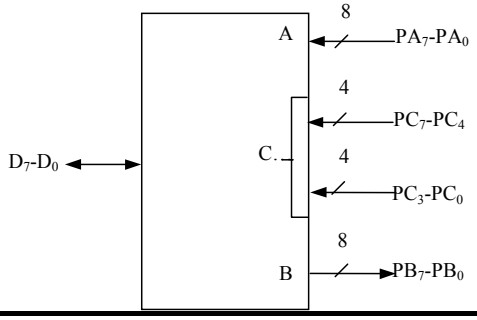
CONTROL WORD #12

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	0



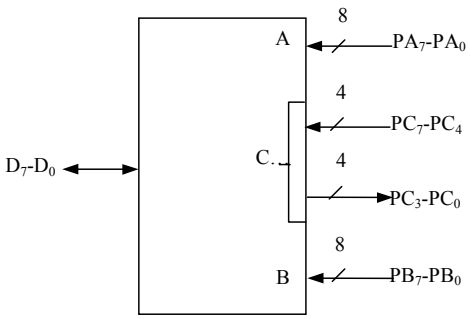
CONTROL WORD #13

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	0	1



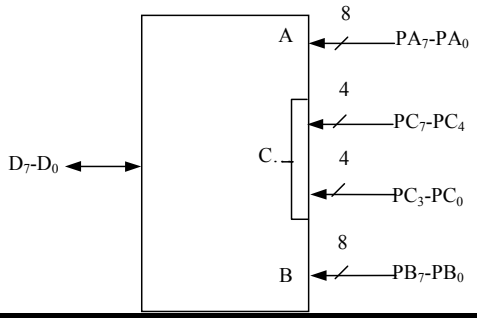
CONTROL WORD #14

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	0



CONTROL WORD #15

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	0	0	1	1	0	1	1



Operating Modes

MODE 1 (Strobed Input/Output). This functional configuration provides a means for transferring I/O data to or from a specified port in conjunction with strobes or "handshaking" signals. In mode 1, Port A and Port B use the lines on Port C to generate or accept these "handshaking" signals.

Mode 1 Basic functional Definitions:

- Two Groups (Group A and Group B).
- Each group contains one 8-bit data port and one 4-bit control/data port.
- The 8-bit data port can be either input or output
- Both inputs and outputs are latched.
- The 4-bit port is used for control and status of the
- 8-bit data port.

Input Control Signal Definition

$\overline{STB}$ (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F)

A "high" on this output indicates that the data has been loaded into the input latch; in essence, an acknowledgement. IBF is set by $\overline{STB}$ input being low and is reset by the rising edge of the $\overline{RD}$ input.

INTR (Interrupt Request)

A "high" on this output can be used to interrupt the CPU when an input device is requesting service. INTR is set by the $\overline{STB}$ is a "one", IBF is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{RD}$. This procedure allows an input device to request service from the CPU by simply strobing its data into the port.

INTE A

Controlled by bit set/reset of PC_4.

INTE B

Controlled by bit set/reset of PC_2

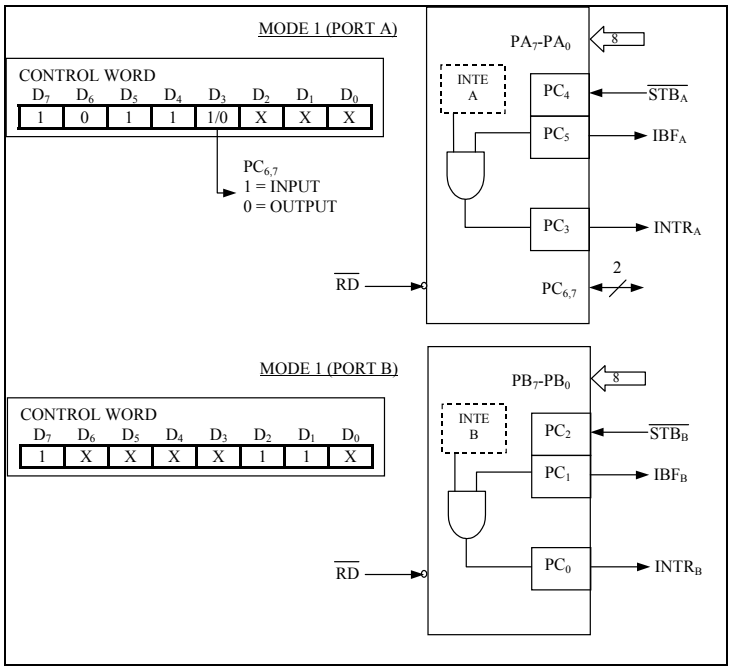


Figure 8. MODE 1 Input

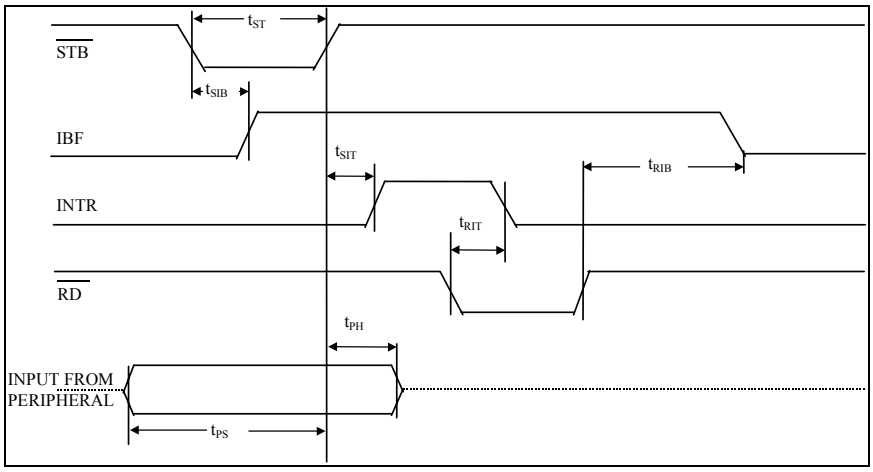


Figure 9. MODE 1 (Strobed Input)

Output Control Signal Definition

$\overline{OBF}$ **(Output Buffer Full F/F).** The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to the specified port. The $\overline{OBF}$ F/F will be set by the rising edge of the $\overline{WR}$ input and reset by $\overline{ACK}$ Input being low.

$\overline{ACK}$ **(Acknowledge Input).** A "low" on this input informs the KK82C55AN that the data from Port A or Port B has been accepted. In essence, a response from the peripheral device indicating that it has received the data output by the CPU.

INTR (Interrupt Request). A "high" on this output can be used to interrupt the CPU when an output device has accepted data transmitted by the CPU. INTR is set when $\overline{ACK}$ is a "one", $\overline{OBF}$ is a "one" and INTE is a "one". It is reset by the falling edge of $\overline{WR}$.

INTE A

Controlled by bit set/reset of PC_6.

INTE B

Controlled by bit set/reset of PC_2.

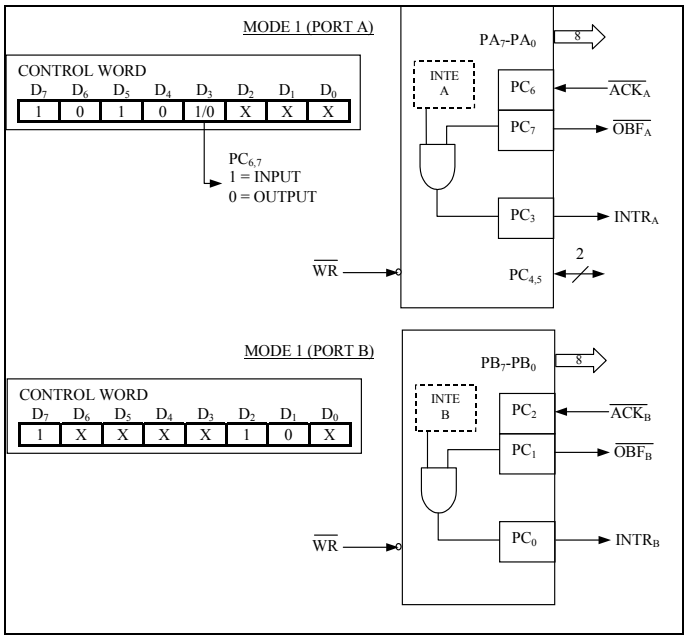


Figure 10. MODE 1 Output

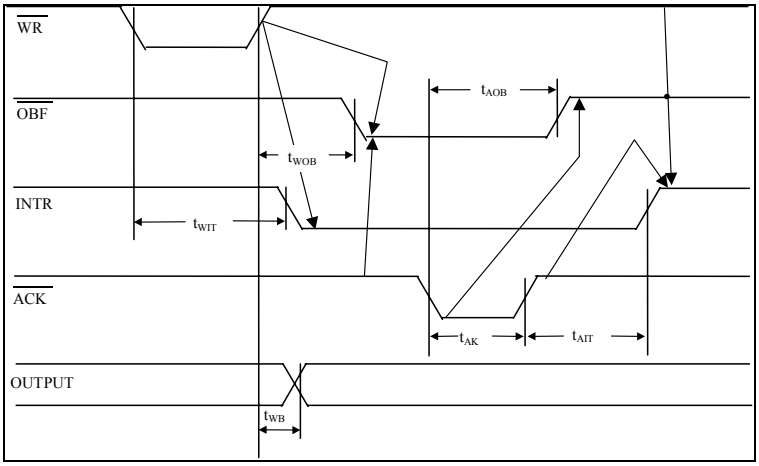


Figure 11. MODE 1 (Strobed Output)

Combinations of MODE 1

Port A and Port B can be individually defined as input or output in Mode 1 to support a wide variety of strobed I/O applications.

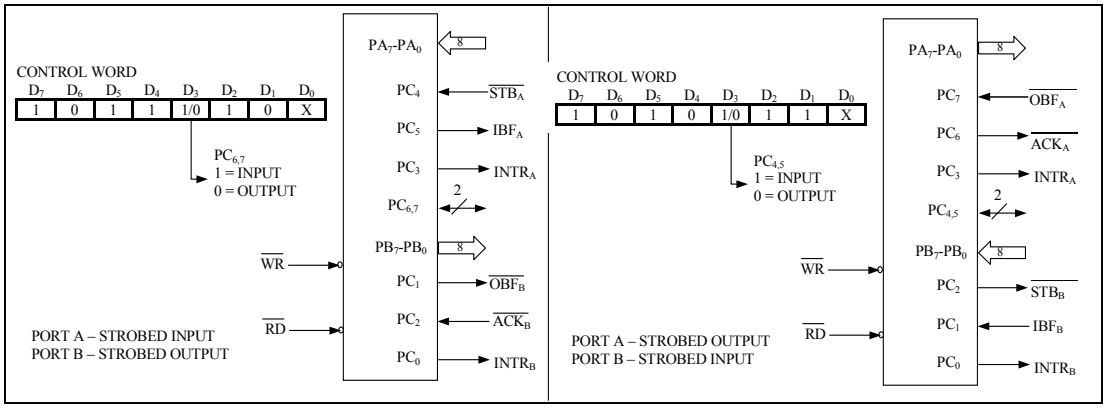


Figure 12. Combinations of MODE 1

Operating Modes

MODE 2 (Strobed Bidirectional Bus I/O). This functional configuration provides a means for communicating with a peripheral device or structure on a single 8-bit bus for both transmitting and receiving data (bidirectional bus I/O). "Handshaking" signals are provided to maintain proper bus flow discipline in a similar manner to MODE 1. Interrupt generation and enable/disable functions are also available.

MODE 2 Basic Functional Definitions:

- Used in Group A only.
- One 8-bit, bi-directional bus port (Port A) and a 5- bit control port (Port C).
- Both inputs and outputs are latched.
- The 5-bit control port (Port C) is used for control and status for the 8-bit, bi-directional bus port (Port A).

Bidirectional Bus I/O Control Signal Definition

INTR (Interrupt Request). A high on this output can be used to interrupt the CPU for input or output operations.

Output Operations

$\overline{OBF}$ **(Output Buffer Full)**. The $\overline{OBF}$ output will go "low" to indicate that the CPU has written data out to port A.

$\overline{ACK}$ **(Acknowledge).** A "low" on this input enables the tri-state output buffer of Port A to send out the data. Otherwise, the output buffer will be in the high impedance state.

INTE 1 (The INTE Flip-Flop Associated with $\overline{OBF}$). Controlled by bit set/reset of PC_6.

Input Operations

STB (Strobe Input). A "low" on this input loads data into the input latch.

IBF (Input Buffer Full F/F). A "high" on this output indicates that data has been loaded into the input latch.

INTE 2 (The INTE Flip-Flop Associated with IBF). Controlled by bit set/reset of PC_4.

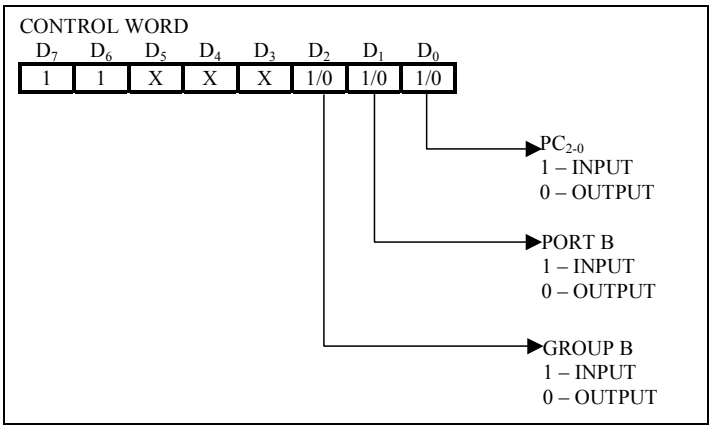


Figure 13. MODE Control Word

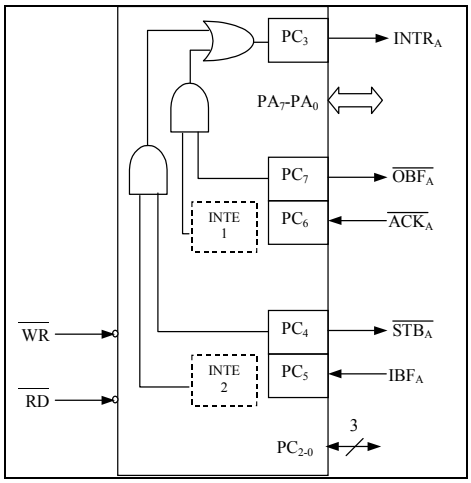


Figure 14. MODE 2

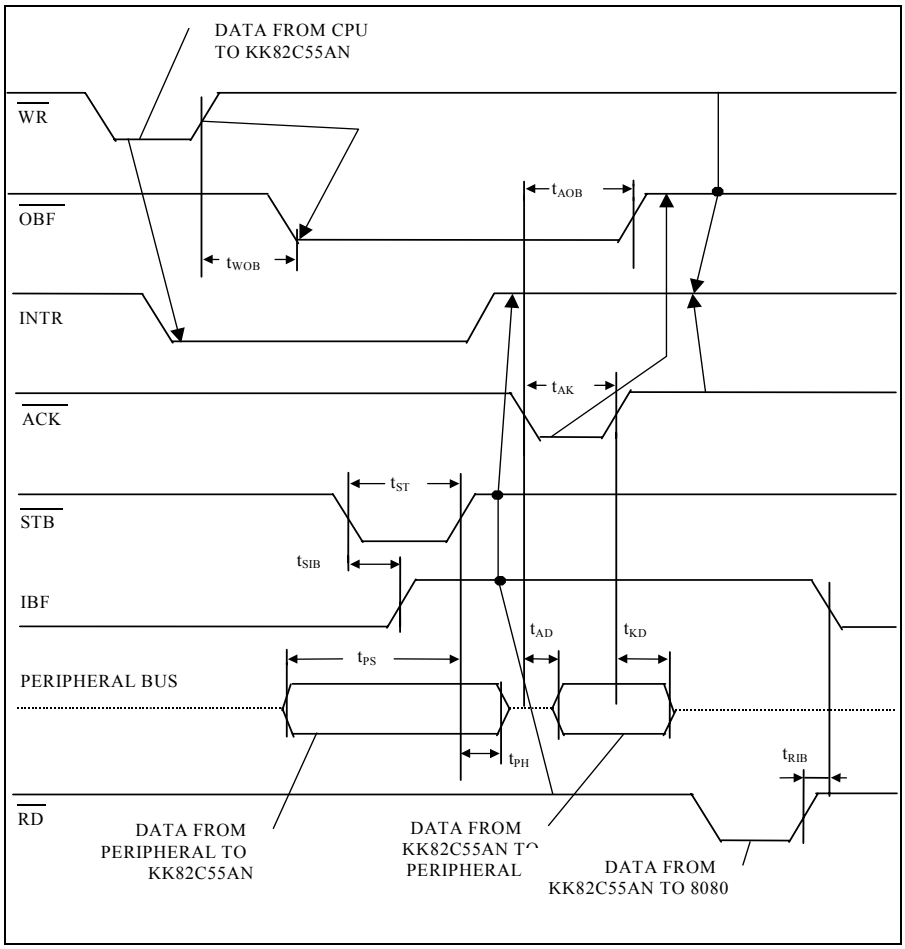


Figure 15. MODE 2 (Bidirectional)

NOTE:

Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$, and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.

($INTR = IBF * \overline{MASK} * \overline{STB} * \overline{RD} + \overline{OBF} * \overline{MASK} * \overline{ACK} * \overline{WR}$)

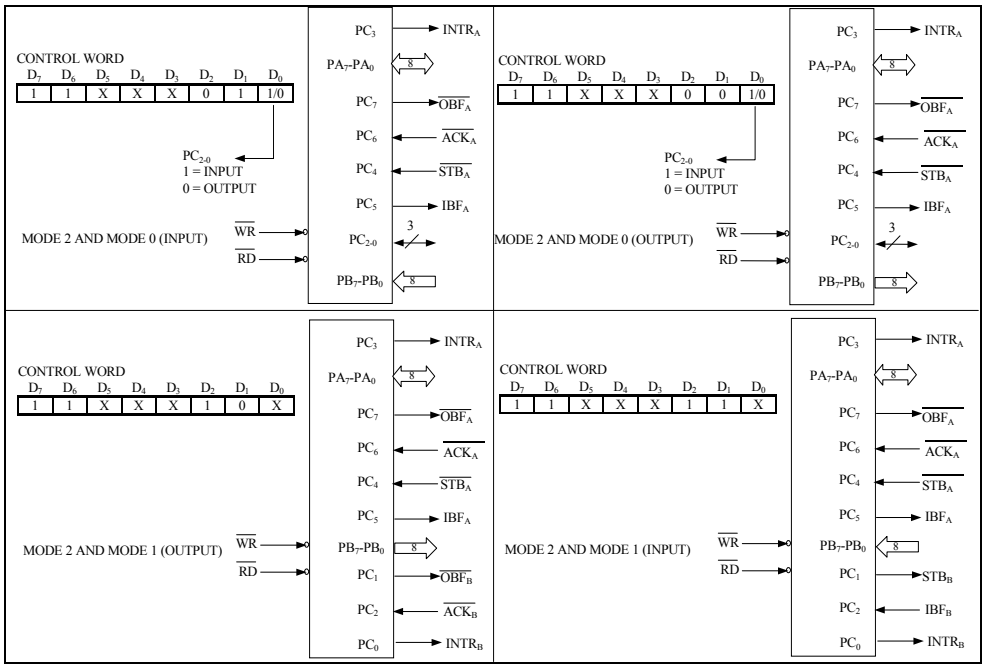


Figure 16. MODE 1/4 Combinations

Mode Definition Summary

	MODE0		MODE1			MODE2	
	IN	OUT	IN	OUT		GROUP A ONLY	
PA_0	IN	OUT	IN	OUT		↔	
PA_1	IN	OUT	IN	OUT		↔	
PA_2	IN	OUT	IN	OUT		↔	
PA_3	IN	OUT	IN	OUT		↔	
PA_4	IN	OUT	IN	OUT		↔	
PA_5	IN	OUT	IN	OUT		↔	
PA_6	IN	OUT	IN	OUT		↔	
PA_7	IN	OUT	IN	OUT		↔	
PB_0	IN	OUT	IN	OUT		-	MODE 0 OR MODE1 ONLY
PB_1	IN	OUT	IN	OUT		-	
PB_2	IN	OUT	IN	OUT		-	
PB_3	IN	OUT	IN	OUT		-	
PB_4	IN	OUT	IN	OUT		-	
PB_5	IN	OUT	IN	OUT		-	
PB_6	IN	OUT	IN	OUT		-	
PB_7	IN	OUT	IN	OUT		-	
PC_0	IN	OUT	$INTR_B$	$INTR_B$		I/0	
PC_1	IN	OUT	IBF_B	$\overline{OBF}_B$		I/O	
PC_2	IN	OUT	$\overline{STB}_B$	$\overline{ACK}_B$		I/O	
PC_3	IN	OUT	$INTR_A$	$INTR_A$		$INTR_A$	
PC_4	IN	OUT	$\overline{STB}_A$	I/O		$\overline{STB}_A$	
PC_5	IN	OUT	IBF_A	I/O		IBF_A	
PC_6	IN	OUT	I/O	$\overline{ACK}_A$		$\overline{ACK}_A$	
PC_7	IN	OUT	I/O	$\overline{OBF}_A$		$\overline{OBF}_A$	

Special Mode Combination Considerations

There are several combinations of modes possible. For any combination, some or all of the Port C lines are used for control or status. The remaining bits are either inputs or outputs as defined by a "Set Mode" command.

During a read of Port C, the state of all the Port C lines, except the $\overline{ACK}$ and $\overline{STB}$ lines, will be placed on the data bus. In place of the $\overline{ACK}$ and $\overline{STB}$ line states, flag status will appear on the data bus in the PC_2, PC_4, and PC_6 bit positions as illustrated by Figure 18.

Through a "Write Port C" command, only the Port C pins programmed as outputs in a Mode 0 group can be written. No other pins can be affected by a "Write Port C" command, nor can the interrupt enable flags be accessed. To write to any Port C output programmed as an output in a Mode 1 group or to change an interrupt enable flag, the "Set/Reset Port C Bit" command must be used.

With a "Set/Reset Port C Bit" command, any Port C line programmed as an output (including INTR, IBF and $\overline{OBF}$) can be written, or an interrupt enable flag can be either set or reset. Port C lines programmed as inputs, including $\overline{ACK}$ and $\overline{STB}$ lines, associated with Port C are not affected by a "Set/Reset Port C Bit" command. Writing to the corresponding Port C bit positions of the $\overline{ACK}$ and $\overline{STB}$ lines with the "Set/Reset Port C Bit" command will affect the Group A and Group B interrupt enable flags, as illustrated in Figure 18.

Current Drive Capability

Any output on Port A, B or C can sink or source 2.5mA. This feature allows the KK82C55AN to directly drive Darlington type drivers and high-voltage displays that require such sink or source current.

Reading Port C Status

In Mode 0, Port C transfers data to or from the peripheral device. When the KK82C55AN is programmed to function in Modes 1 or 2, Port C generates or accepts "hand-shaking" signals with the peripheral device. Reading the contents of Port C allows the programmer to test or verify the "status" of each peripheral device and change the program flow accordingly.

There is no special instruction to read the status information from Port C. A normal read operation of Port C is executed to perform this function.

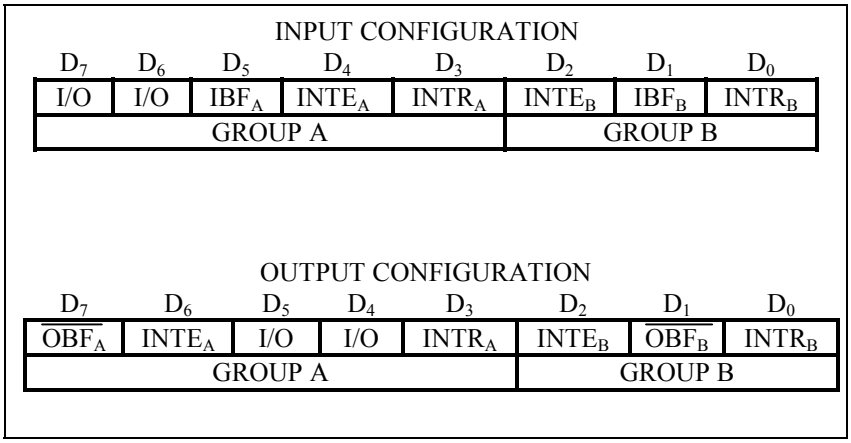


Figure 17a. MODE 1 Status Word Format

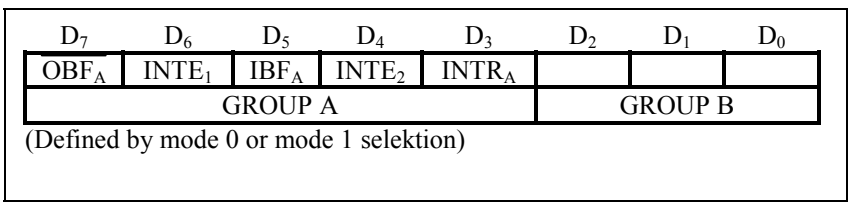


Figure 17b. MODE 2 Status Word Format

Interrupt Enable Flag	Position	Alternate
$INTE_B$	PC_2	$\overline{ACK}_B$ (Output Mode 1) or $\overline{STB}_B$ (Input Mode 1)
$INTE_{A2}$	PC_4	$\overline{STB}_A$ (Input Mode 1 or Mode 2)
$INTE_{A1}$	PC_6	$\overline{ACK}_A$ (Output Mode 1 or Mode 2)

Figure 18. Interrupt Enable Flags in Modes 1 and 2

*ABSOLUTE MAXIMUM RATINGS**

Ambient Temperature Under Bias	0^OC to + 70^OC
Storage Temperature	- 65^OC to + 150^OC
Supply Voltage	- 0.5 to + 8.0V
Operating Voltage	+ 4V to + 7V
Voltage on any Input	GND-2V to + 6.5V
Voltage on any Output	GND-0.5V to V_{CC} + 0.5V
Power Dissipation	1Watt

NOTICE: This is a production data sheet. The specifications are subject to change without notice.

**WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

D.C. CHARACTERISTICS

$T_A = 0^OC$to70^OC, V_{CC} =+5V ±10%, GND = 0V (T_A =-40^OC to +85^OC for Extended Temperature)

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4	V	I_{OL} = 2.5mA
V_{OH}	Output High Voltage	3.0 V_{CC} - 0.4		V V	I_{OH} =-2.5mA I_{OH} =-100µA
I_{IL}	Input Leakage Current		±1	µA	V_{IN} = V_{CC} to 0V (Note 1)
I_{OFL}	Output Float Leakage Current		±10	µA	IN = V_{CC} to 0V (Note 2)
I_{DAR}	Darlington Drive Current	±2.5	(Note 4)	mA	Ports A,B,C R_{ext} = 500Ω V_{ext} = 1.7V
I_{PHL}	Port Hold Low Leakage Current	+50	+300	µA	V_{OUT} = 1.0V Port A only
I_{PHH}	Port Hold High Leakage Current	-50	-300	µA	V_{OUT} = 3.0V Ports A,B,C
I_{PHLO}	Port Hold Low Overdrive Current	-350		µA	V_{OUT} = 0.8V
I_{PHHO}	Port Hold High Overdrive Current	+350		µA	V_{OUT} = 3.0V
I_{CC}	V_{CC} Supply Current		10	mA	(Note 3)
I_{CCSB}	V_{CC} Supply Current-Standby		10	µA	V_{CC} = 5.5V V_{IN} = V_{CC} or GND Port Conditions If I/P = Open/High O/P = Open Only With Data Bus = High/Low CS = High Reset = Low Pure Inputs = Low/High

NOTES:

1. Pins A1, A0, CS, WR, RD, Reset
2. Data Bus; Ports B, C
3. Outputs open.
4. Limit output current to 4.0mA.

CAPACITANCE

$T_A = 25^OC$, $V_{CC} = GND = 0V$

Symbol	Parameter	Min	Max	Units	TestConditions
C_{IN}	Input Capacitance		10	pF	Unmeasured pins returned to GND f_C = 1MHz(5)
$C_{I/O}$	I/O Capacitance		20	pF	

NOTE:
5. Sampled not 100% tested.

A.C. CHARACTERISTICS

$T_A = 0^O$ to 70^OC, $V_{CC} = +5V \pm 10\%$, $GND = 0V$
$T_A = -40^OC$ to $+85^OC$ for Extended Temperature

BUS PARAMETERS

READ CYCLE

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AR}	Address Stable Before $\overline{RD}$_	0		ns	
t_{RA}	Address Hold Time After $\overline{RD}$_	0		ns	
t_{RR}	$\overline{RD}$ Pulse Width	150		ns	
t_{RD}	Data Delay from $\overline{RD}$_		120	ns	
t_{DF}	$\overline{RD}$_ to Data Floating	10	75	ns	
t_{RV}	Recovery Time between $\overline{RD}$/$\overline{WR}$	200		ns	

WRITE CYCLE

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Stable Before $\overline{WR}$_	0		ns	
t_{WA}	Address Hold Time After $\overline{WR}$_	20		ns	PortsAB
		20		ns	PortC
t_{WW}	$\overline{WR}$ Pulse Width	100		ns	
t_{DW}	Data Setup Time Before $\overline{WR}$_	100		ns	
t_{WD}	Data Hold Time After $\overline{WR}$_	30		ns	PortsAB
		30		ns	PortC

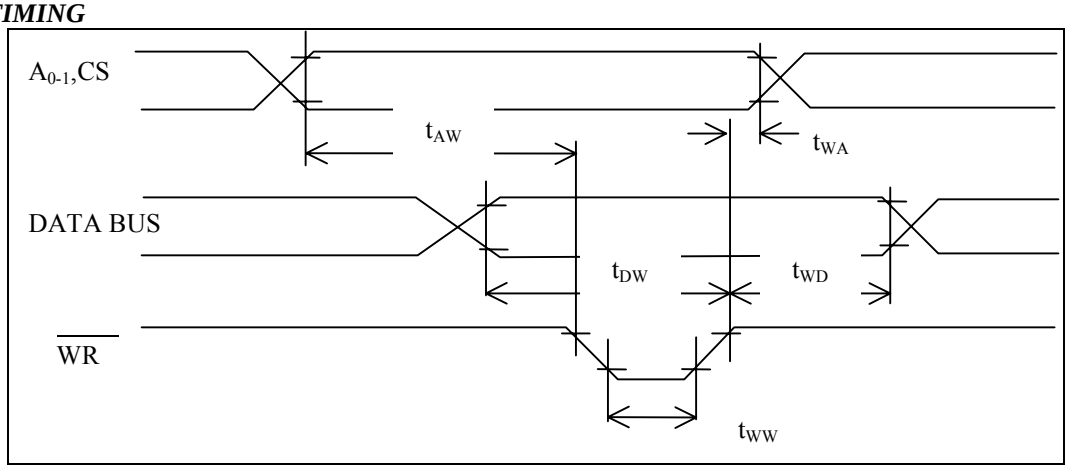
OTHER TIMINGS

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{WB}	$\overline{WR}$ = 1 to Output		350	ns	
t_{IR}	Peripheral Data Before $\overline{RD}$	0		ns	
t_{HR}	Peripheral Data After $\overline{RD}$	0		ns	
t_{AK}	$\overline{ACK}$ Pulse Width	200		ns	
t_{ST}	$\overline{STB}$ Pulse Width	100		ns	
t_{PS}	Per. Data Before $\overline{STB}$ High	20		ns	
t_{PH}	Per. Data After $\overline{STB}$ High	50		ns	
t_{AD}	$\overline{ACK}$ = 0 to Output		175	ns	
t_{KD}	$\overline{ACK}$ = 1 to Output Float	20	250	ns	
t_{WOB}	$\overline{WR}$ = 1 to $\overline{OBF}$ = 0		150	ns	
t_{AOB}	$\overline{ACK}$ = 0 to $\overline{OBF}$ = 1		150	ns	
t_{SIB}	$\overline{STB}$ = 0 to IBF = 1		150	ns	
t_{RIB}	$\overline{RD}$ = 1 to IBF = 0		150	ns	
t_{RIT}	$\overline{RD}$ = 0 to INTR = 0		200	ns	
t_{SIT}	$\overline{STB}$ = 1 to INTR = 1		150	ns	
t_{AIT}	$\overline{ACK}$ = 1 to INTR = 1		150	ns	
t_{WIT}	$\overline{WR}$ = 0 to INTR = 0		200	ns	see note1
t_{RES}	Reset Pulse Width	500		ns	see note2

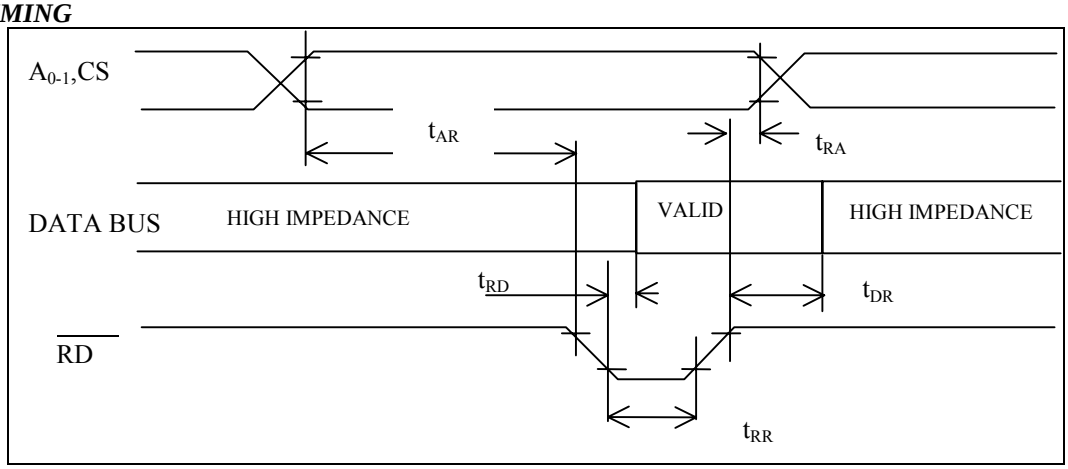
NOTE

1. INTR_ may occur as early as $\overline{WR}$ _.
2. Pulse width of initial Reset pulse after power on must be at least 50μSec. Subsequent Reset pulses may be 500ns minimum. The output Ports A B or C may glitch low during the reset pulse but all port pins will be held at a logic "one" level after the reset pulse.

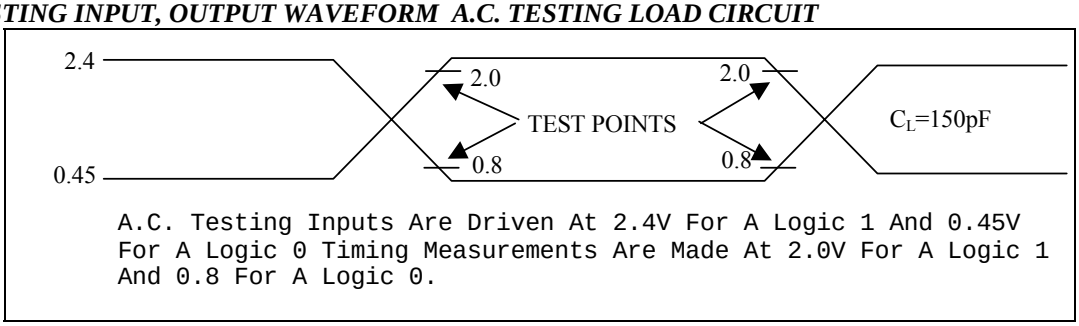
WRITE TIMING



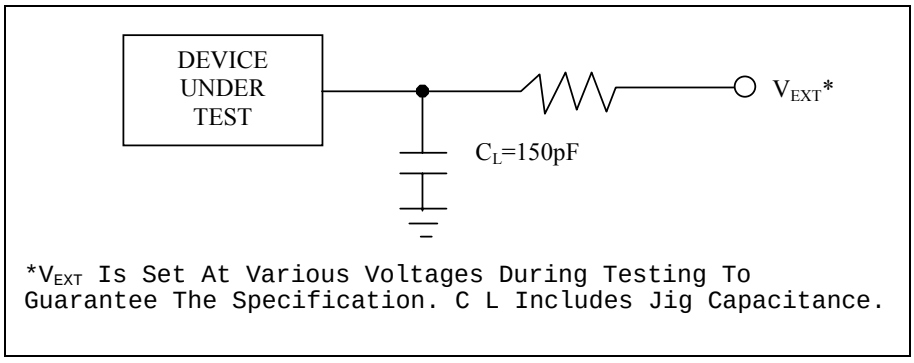
READ TIMING



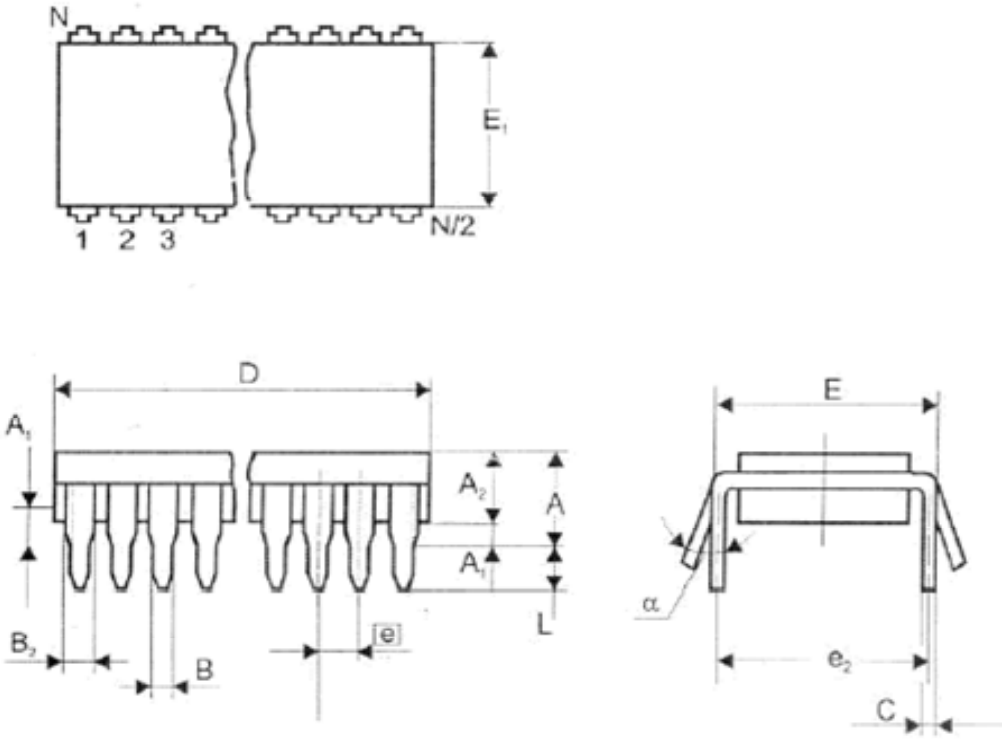
A.C. TESTING INPUT, OUTPUT WAVEFORM A.C. TESTING LOAD CIRCUIT



A.C. TESTING LOAD CIRCUIT



40-Pin Plastic Dual-in-Line



Dimension, mm		
A	max	6.35
A1	min	0.38
A2	min	3.18
	max	4.95
B	min	0.36
	max	0.56
B2	min	0.77
	max	1.78
C	min	0.20
	max	0.38
D	min	50.30
	max	53.20
E	min	15.24
	max	15.87
E1	min	12.32
	max	14.73
e	nom	2.54
e2	nom	15.24
L	min	2.92
	max	5.08
α	min	0°
	max	10°