WHITE LED DRIVER FOR LCD PANEL BACKLIGHT AP3068

General Description

The AP3068 is a white LED (WLED) driver with current balancing and dimming functions. It consists of a boost controller and 8-channel current sinks to drive WLED arrays with constant current from a wide power supply range. It can be used in middle and large-sized LCD panel backlight.

The full-scale LED current can be adjusted from 5mA to 100mA simply via a resistor. The 8 channels can be paralleled for higher current application. The AP3068 can support direct PWM dimming.

The AP3068 features LED open/short protection, Under Voltage Lockout (UVLO) protection, over output voltage protection and Over Temperature Protection (OTP).

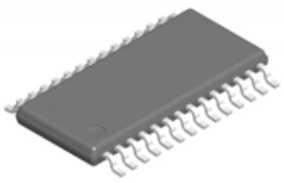
The AP3068 is available in TSSOP-28 (EDP) package.

Features

- Input Voltage Range: 6V to 27V
- Maximum Duty Cycle: 93%
- Maximum Channel Current: 100mA
- Current Matching Accuracy: ±1.5%
- Adjustable Operating Frequency: 200kHz to 1MHz
- Cycle-by-cycle Current Limit
- Unused LED Channel Auto-detection
- Open/Short LED Protection
- Programmable Soft-start
- Programmable UVLO Protection
- Programmable OVP
- Over Temperature Protection
- FBX and SDBX Pins Enable Parallel Application with AP3608E

Applications

- LCD Monitor
- LCD Display Module
- LCD TV



TSSOP-28 (EDP)

Figure 1. Package Type of AP3068

Pin Configuration

G Package
(TSSOP-28 (EDP))

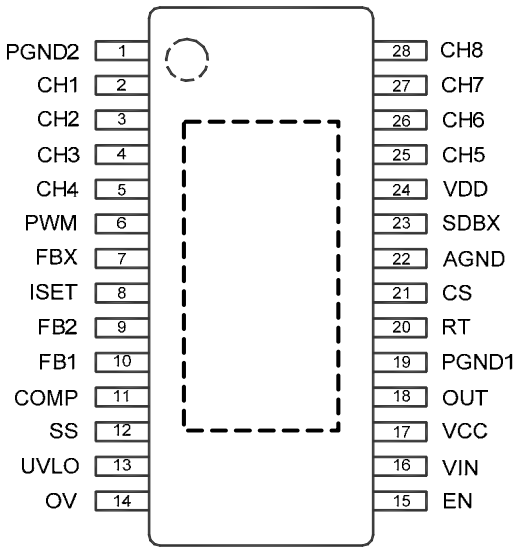


Figure 2. Pin Configuration of AP3068 (Top View)

Pin Description

Pin Number	Pin Name	Function
1	PGND2	Power ground pin of current sink section
2,3,4,5, 25,26,27,28	CH1 to CH8	White LED cathode connection pin. The current of each channel can be set from 5mA to 100mA. The channels can be paralleled for higher current application. These pins should be connected to GND if not used
6	PWM	PWM dimming control pin. Add a PWM signal to this pin to realize PWM dimming control
7	FBX	This pin is an interface terminal. Connect it with current sink device for parallel application. Leave it unconnected if not used
8	ISET	LED current setting pin. An external resistor can be connected to this pin to set LED current, the full-scale current can be adjusted from 5mA to100mA
9	FB2	Feedback pin. This pin is an interface terminal, which samples the voltage of each channel, and outputs the lowest voltage to DC/DC controller
10	FB1	Voltage feedback pin of the boost controller section. The reference voltage is 500mV

Pin Description (Continued)

Pin Number	Pin Name	Function
11	COMP	Boost controller compensation pin. This pin is the output of internal error amplifier
12	SS	Soft-start time control pin. An external soft-start time capacitor is placed between this pin and AGND, and is charged by an internal 12μA current source to control the soft-start time of regulator
13	UVLO	Under voltage lockout sense pin. The start-up and shutdown level can be set via two resistors respectively connected from this pin to AGND and VIN pin
14	OV	Over voltage sense pin
15	EN	Enable pin. Logic high enables the IC, while logic low disables the IC
16	VIN	Input supply pin of boost controller section. This pin must be locally bypassed. The input voltage ranges from 6V to 27V
17	VCC	6V linear regulator output pin. It is used to bias the gate driver for external MOSFET. If V_{IN} is less than 8.5V, V_{CC} is equal to V_{IN} minus dropout voltage across the bypass switch (V_{DROP}), in other words, $V_{CC}=V_{IN}-V_{DROP}$. This pin should be bypassed to GND (recommended to be connected to AGND pin) with a ceramic capacitor
18	OUT	External MOSFET gate driver output pin. The gate driver has 0.6A peak current capability
19	PGND1	Power ground pin of the boost controller section
20	RT	Frequency control pin. The operating frequency can be set via an external resistor placed between this pin and AGND
21	CS	Switch current sense pin. It is used for current mode control and current limit
22	AGND	Analog ground pin
23	SDBX	This pin is an interface terminal. Connect it with current sink device for parallel application. It should be connected to GND if not used
24	VDD	Input supply pin for current sink section. The input voltage ranges from 4.2V to 5.5V

Functional Block Diagram

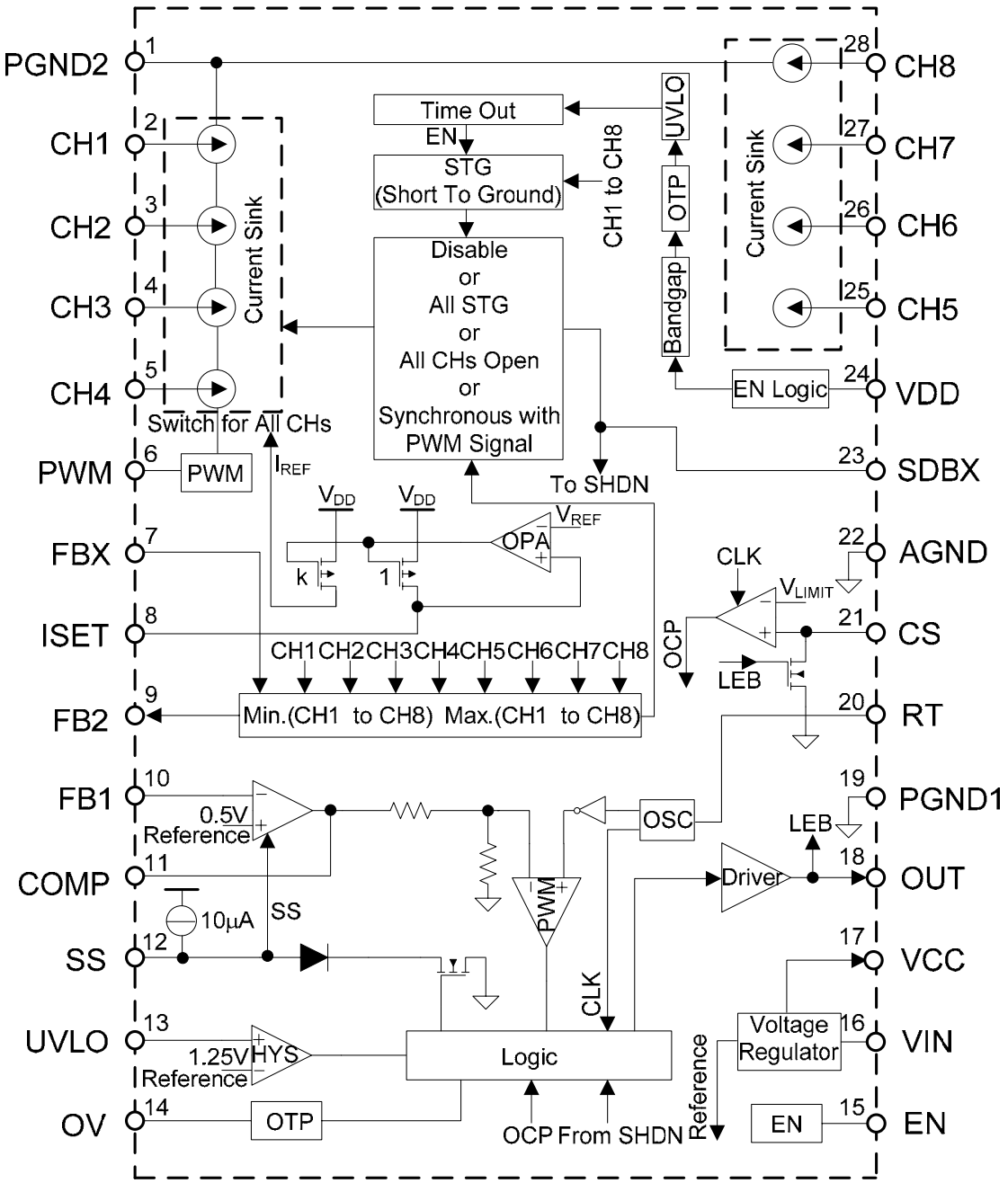
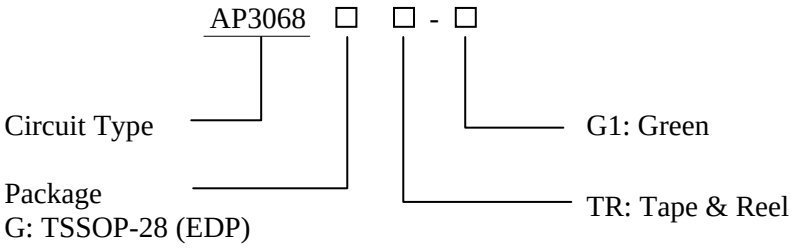


Figure 3. Functional Block Diagram of AP3068

Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
TSSOP-28 (EDP)	-40 to 85°C	AP3068GTR-G1	AP3068G-G1	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G1" suffix in the part number, are RoHS compliant and green.

Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Value	Unit
Input Voltage	V_{IN}	30	V
CH1 to CH8 Voltage (Note 2)	V_{DX}	-0.3 to 40	V
EN Pin Voltage	V_{EN}	-0.3 to 30	V
VDD Pin Voltage	V_{DD}	-0.3 to 6	V
ISET Pin Voltage	V_{ISET}	-0.3 to 6	V
PWM Pin Voltage	V_{PWM}	-0.3 to 6	V
COMP Pin Voltage	V_{COMP}	-0.3 to 6	V
SS Pin Voltage	V_{SS}	-0.3 to 6	V
UVLO Pin Voltage	V_{UVLO}	-0.3 to 7	V
VCC Pin Voltage	V_{VCC}	-0.3 to 10	V
OUT Pin Voltage	V_{OUT}	-0.3 to 10	V
CS Pin Voltage	V_{CS}	-0.3 to 7	V
RT Pin Voltage	V_{RT}	-0.3 to 7	V
OV Pin Voltage	V_{OV}	-0.3 to 7	V

Note 2: Breakdown Voltage

Absolute Maximum Ratings (Note 1) (Continued)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	T_J	150	ºC
Storage Temperature	T_{STG}	-65 to 150	ºC
Lead Temperature (Soldering, 10 sec)	T_{LEAD}	260	ºC
ESD (Machine Model)		200	V
ESD (Human Body Model)		2000	V

Note 1: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to "Absolute Maximum Ratings" for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Max	Unit
Input Voltage 1	V_{IN}	6	27	V
Input Voltage 2	V_{DD}	4.2	5.5	V
Operating Frequency	f_O	0.2	1	MHz
LED Channel Current	I_{CHX}	5	100	mA
PWM Dimming Frequency	f_{PWM}	0.1	25	kHz
Operating Temperature	T_A	-40	85	ºC

Electrical Characteristics

V_{IN} =12V, V_{DD}=5V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT SECTION						
Input Voltage	V_{IN}		6		27	V
Quiescent Current	I_Q	No Switching		3	5	mA
Shutdown Supply Current	I_{SHTD}	V_{EN} =V_{DD}=0V		1	2	μA

Electrical Characteristics (Continued)

V_{IN} =12V, V_{DD}=5V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
VIN UVLO Threshold	V_{UVLO}	Rising Edge	1.22	1.25	1.28	V
VIN UVLO Hysteresis Current Source	I_{HYS}		16	20	24	μA
VCC SECTION						
VCC Voltage	V_{CC}	6V≤V_{IN}≤9V	5			V
		9V≤V_{IN}≤27V	5.5	6	6.5	V
VCC Current Limit	I_{VCC_LIM}			50		mA
Dropout Voltage Across Bypass Switch	V_{DROP}	I_{CC}=0mA, f_{OSC}≤400kHz, 6V≤V_{IN}≤8.5V		300		mV
Bypass Switch Turn-off Threshold	V_{BYP_HI}	V_{IN} Rising		8.7		V
Bypass Switch Threshold Hysteresis	V_{BYP_HYS}	V_{IN} Falling		260		mV
VCC UVLO Threshold	V_{CC_UVLO}	Rising Edge		4.7		V
VCC UVLO Hysteresis	V_{CC_HYS}			300		mV
BOOST CONTROLLER SECTION						
RT Voltage	V_{RT}		1.20	1.25	1.30	V
Operating Frequency	f_O	Adjustable	0.2		1	MHz
Error Amplifier Transconductance	g_M			470		μA/V
Error Amplifier Output Resistance	R_O			1		Ω
Current Limit Threshold Voltage	V_{CS}		0.09	0.11	0.13	V
Maximum Duty Cycle	D_{MAX}		90	93		%
Soft-start Current Source	I_{SS}			12		μA
OUT Pin Rising Time	t_{RISING}	1nF Load		20		ns
OUT Pin Falling Time	$t_{FALLING}$	1nF Load		20		ns
Output High Voltage Level (V_{CC}-V_{OUT})	V_{OUT_H}	I_{OUT}=50mA		0.25	0.75	V
Output Low Voltage Level	V_{OUT_L}	I_{OUT} =100mA		0.25	0.75	V
OV Threshold	V_{OV}			1.25		V
OV Hysteresis Current Source	I_{OV_HYS}		16	20	24	μA

Electrical Characteristics (Continued)

V_{IN} =12V, V_{DD}=5V, T_A=25°C, unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
CURRENT SINK SECTION						
Input Voltage	V_{DD}		4.2		5.5	V
Quiescent Current	I_Q	No Load		0.5	1	mA
ISET Reference Voltage	V_{ISET}		1.17	1.194	1.218	V
Output/ISET Current Multiplication Ratio	k		370	400	430	
Maximum Output Current per Channel	$I_{CHX-MAX}$	V_{CHX}=0.5V	23	45		mA
		V_{CHX}=1V	65	70		
		V_{CHX}=1.5V	110	120		
Current Matching Accuracy Between Each Channel	$I_{CH-MATCH}$	I_{CHX}=60mA V_{CHX}=1V	-1.5		1.5	%
Current Sink Saturation Voltage per Channel	V_{CHX}	I_{CHX}=20mA			0.45	V
		I_{CHX}=60mA			0.8	
		I_{CHX}=100mA			1.2	
Output Current Line Regulation	$\Delta I_{CH}/(I_{CH}\times\Delta V_{DD})$	V_{DD}=4.2V to 5.5V			2	%/V
Output Current Load Regulation		V_{CHX}=0.5V to 2.8V			4	%
LED Open Detecting Voltage	V_{D_OPEN}			3		V
ENABLE AND PWM DIMMING SECTION						
EN High Level Threshold Voltage	V_{IH_EN}		2.0			V
EN Low Level Threshold Voltage	V_{IL_EN}				0.5	V
PWM High Level Threshold Voltage	V_{IH_PWM}		1.8			V
PWM Low Level Threshold Voltage	V_{IL_PWM}				0.8	V
PWM Dimming Frequency	f_{PWM}		0.1		25	kHz
Minimum PWM Duty Cycle	D_{PWM_MIN}		0.35			%
TOTAL DEVICE						
Thermal Shutdown Temperature	T_{OTSD}			160		ºC
Thermal Shutdown Hysteresis	T_{HYS}			20		ºC

Typical Performance Characteristics

V_{IN} =12V, V_{EN}=V_{DD}=5V, R_{IEST}=20kΩ, T_A=25°C, unless otherwise specified.

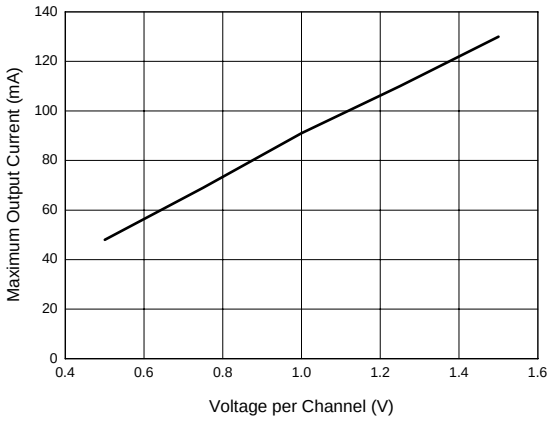


Figure 4. Maximum Output Current vs. Voltage per Channel

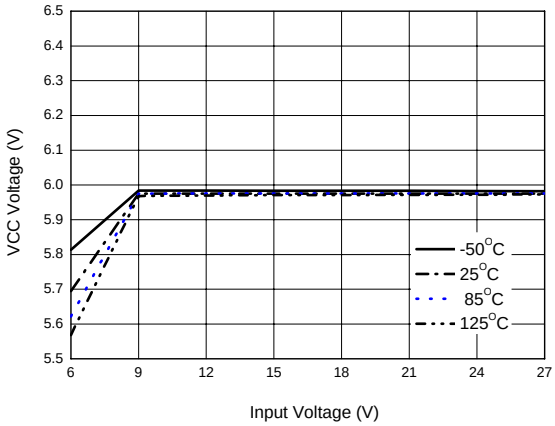


Figure 5. VCC Voltage vs. Input Voltage

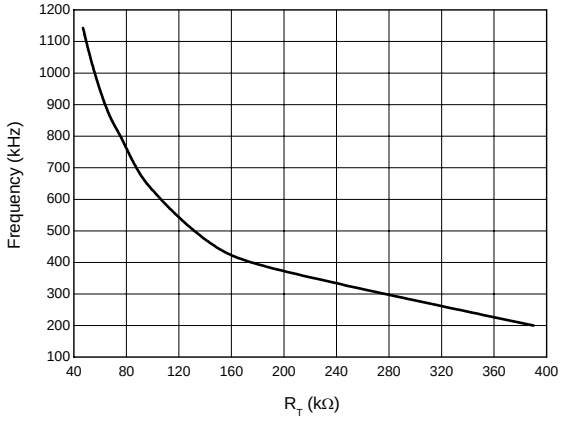


Figure 6. Frequency vs. R_T

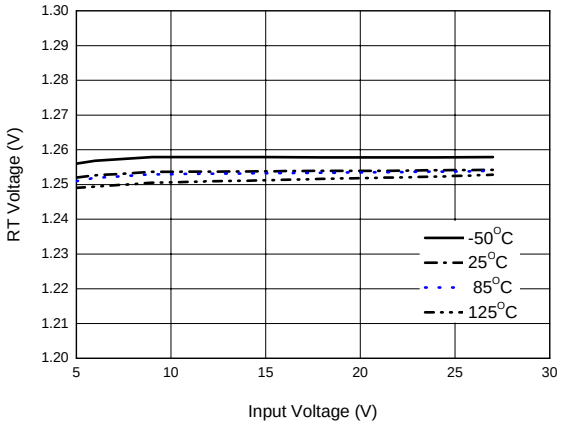


Figure 7. RT Voltage vs. Input Voltage

Application Information

1. Input Under-voltage Detector

The AP3068 integrates an UVLO circuit. Two resistors R_{UV1} and R_{UV2} are respectively connected from UVLO pin to GND and VIN pin (Figure 9). The resistor divider (R_{UV1} and R_{UV2}) must be designed such that the voltage on UVLO pin is higher than 1.25V when V_{IN} is in the desired operating range. If the voltage on UVLO pin is below the under voltage threshold, all functions of AP3068 will be disabled, while the system will remain in a low-power standby state. The UVLO hysteresis is realized through an internal 22μA current source, which switched on or off 22μA current flowed into the set-point divider. The current source will be instantly activated to raise the voltage on the UVLO pin (V_{UVLO}) when the UVLO threshold (T_{UVLO}) is exceeded, and will be turned off to lower V_{UVLO} when V_{UVLO} falls below T_{UVLO}. The formulas of UVLO can be expressed as blow:

$$V_{IN\_THRESHOLD} = \frac{(R_{UV1} + R_{UV2}) \times 1.25V}{R_{UV2}}$$

$$V_{IN\_HYSTERESIS} = R_{UV1} \times 22\mu A$$

Where $V_{IN\_THRESHOLD}$ is the input threshold voltage and $V_{IN\_HYSTERESIS}$ is the input hysteresis voltage.

2. Over Voltage Protection

The AP3068 integrates an OVP circuit. The OV pin is connected to the center tap of voltage-divider (R_{OV1} and R_{OV2}) that placed between high voltage output and GND (Figure 9). If the voltage on OV pin exceeds 1.25V, which may results from open loop or excessive output voltage, all the functions of AP3068 will be disabled with output voltage falling. The OVP hysteresis is realized by an internal 22μA current source and its operation mode behaves the same as UVLO. The formulas of OVP can be expressed as blow:

$$V_{OVP} = \frac{(R_{OV1} + R_{OV2}) \times 1.25V}{R_{OV2}}$$

$$V_{OVP\_HYSTERESIS} = R_{OV1} \times 22\mu A$$

Where V_{OVP} is the OVP voltage and $V_{OVP\_HYSTERESIS}$ is the OVP hysteresis voltage.

3. Frequency Selection

An external resistor R_T, placed between RT pin and GND, can be used to set the operating frequency (Figure 9). The operating frequency ranges from 200kHz to 1MHz (Table 1). The high frequency operation optimizes the regulator for the smallest-sized component application, while low frequency operation can help to reduce switch loss.

R_T (kΩ)	Operating Frequency (kHz)
390	200
147	400
95	600
68	800
51	1000

Table 1. Frequency Selection

4. Soft-start

The AP3068 integrates a soft-start circuit to limit the inrush current during start-up. The time of soft-start can be controlled by an internal 12μA current source and an external soft-start capacitor C_{SS} placed between SS pin and GND (Figure 9). The effective C_{SS} voltage for soft-start ranges from 0V to 2.3V, and the time of soft-start can be expressed as below:

$$t_{SS} = \frac{C_{SS} \times 2.3V}{12\mu A}$$

Where t_{SS} is the time of soft-start.

5. VCC Pin Application Description

The AP3068 includes an internal low-dropout linear regulator with an output pin VCC. This pin is used to power the internal PWM controller, control logic and MOSFET driver. On condition that $V_{IN} \geqslant 8.5V$, the regulator will generate a 6V supply; On condition that $6V \leqslant V_{IN} \leqslant 8.5V$, V_{CC} is equal to V_{IN} minus dropout voltage across bypass switch (V_{DROP}), in other words, $V_{CC}=V_{IN}-V_{DROP}$; On condition that $V_{IN} \leqslant 6V$, connect VCC pin to VIN pin directly.

Application Information (Continued)

6. LED Current Setting

The maximum LED current per channel can be adjusted up to 100mA via ISET pin. When ⩾100mA current is needed in application, two or more channels can be paralleled to provide larger drive current (Figure 10). Connect a resistor R_{ISET} between ISET pin and GND to set the reference current I_{SET}, and I_{SET} can be expressed as below:

$$I_{SET} = \frac{1.194V}{R_{ISET}}$$

This reference current is multiplied internally with a gain (k) of 400, and then be mirrored onto all enabled channels, which can set the maximum LED current, referred to as 100% current (I_{CHX_MAX}). And I_{CHX_MAX} can be expressed as below:

$$I_{CHX\_MAX} = k \times I_{SET}$$

The LED current can be reduced from 100% by PWM dimming control.

7. PWM Dimming Mode

Applying a PWM signal to PWM pin to adjust the LED current, that means, the LED current of all enabled channels can be adjusted at the same time and the LED brightness can be adjusted from 1%× I_{CHX_MAX} to 100% × I_{CHX_MAX}. During the "high level" period of PWM signal, the LED is turned on and 100% of the current flows through LED, while during the "low level" period of the PWM signal, the LED is turned off and almost no current flows through the LED, thus changing the average current through LED and finally adjusting LED brightness. The external PWM signal frequency applied to PWM pin is allowed to be 100Hz or higher.

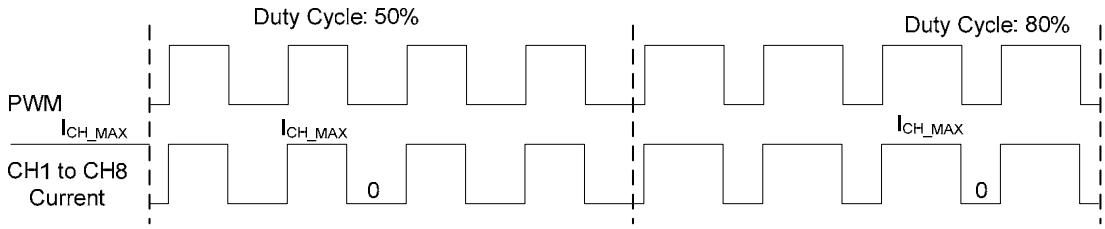


Figure 8. PWM Dimming of AP3068 (Example)

Typical Application

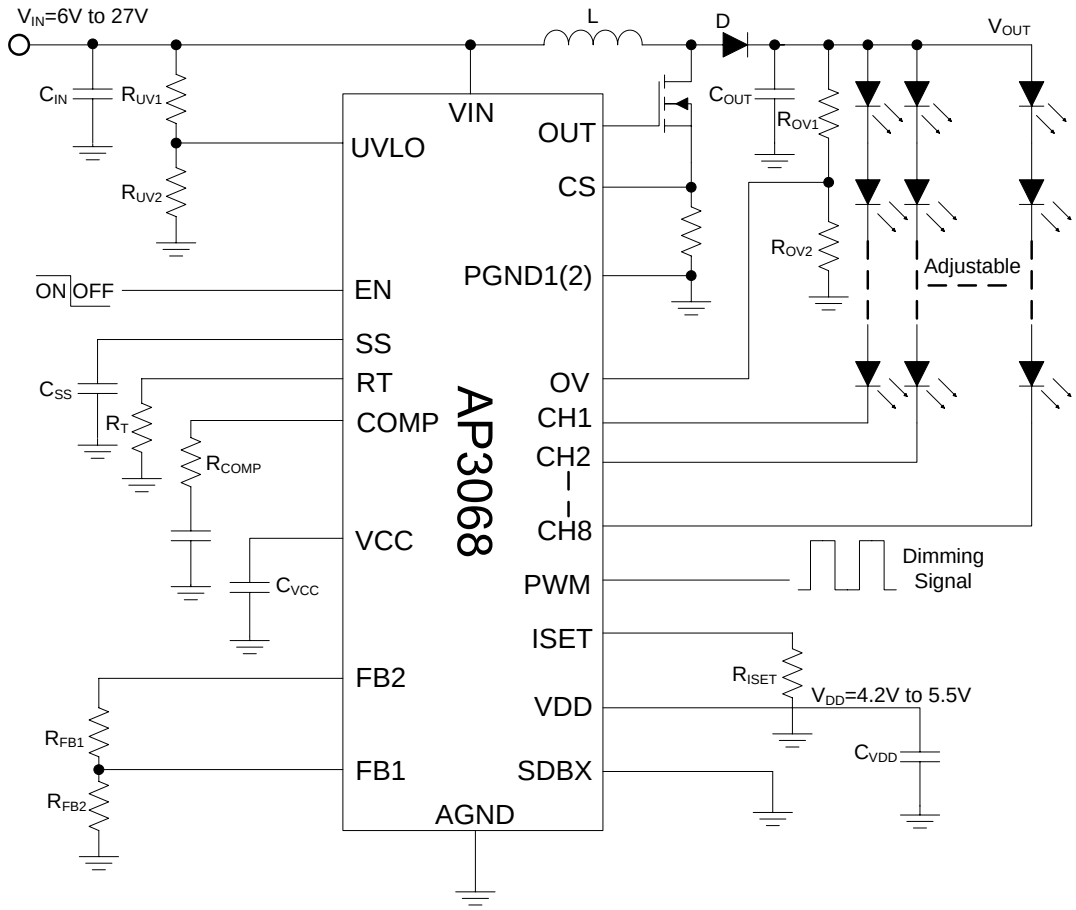


Figure 9. Typical Application Circuit of AP3068 (Single Channel Application)

Typical Application (Continued)

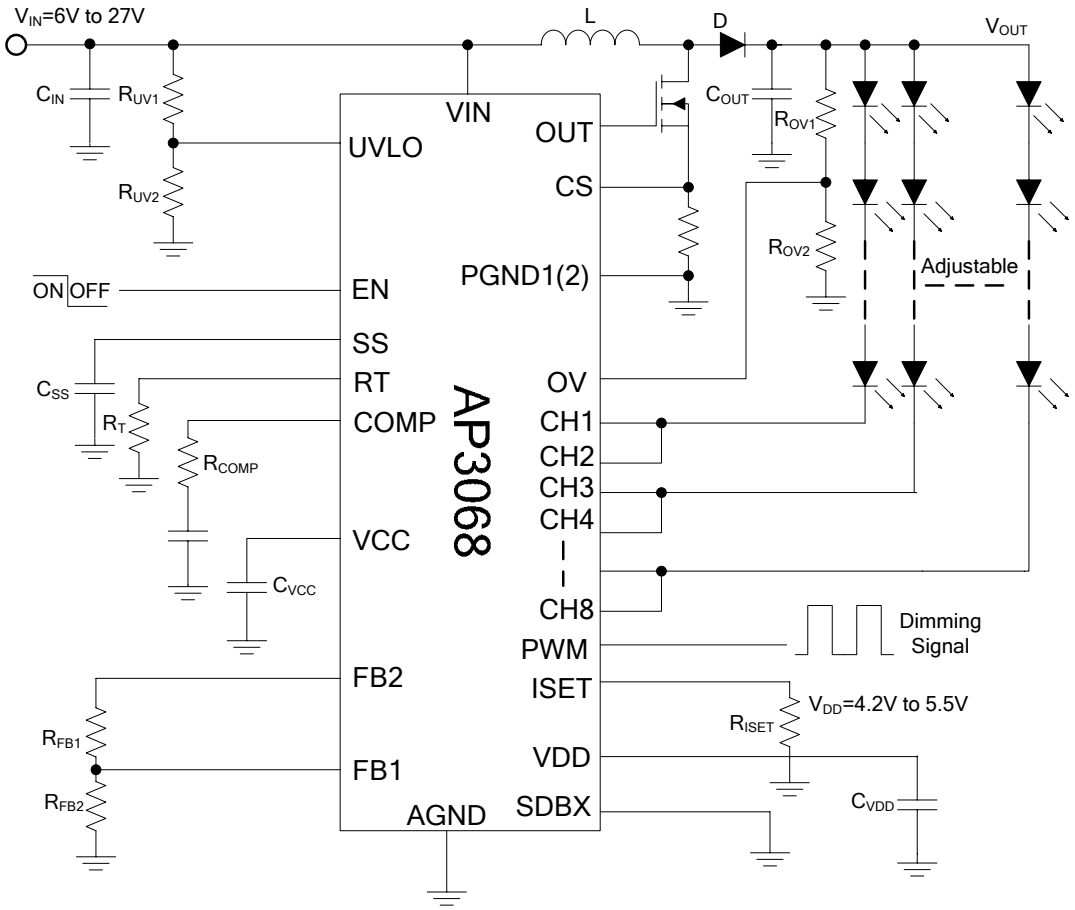
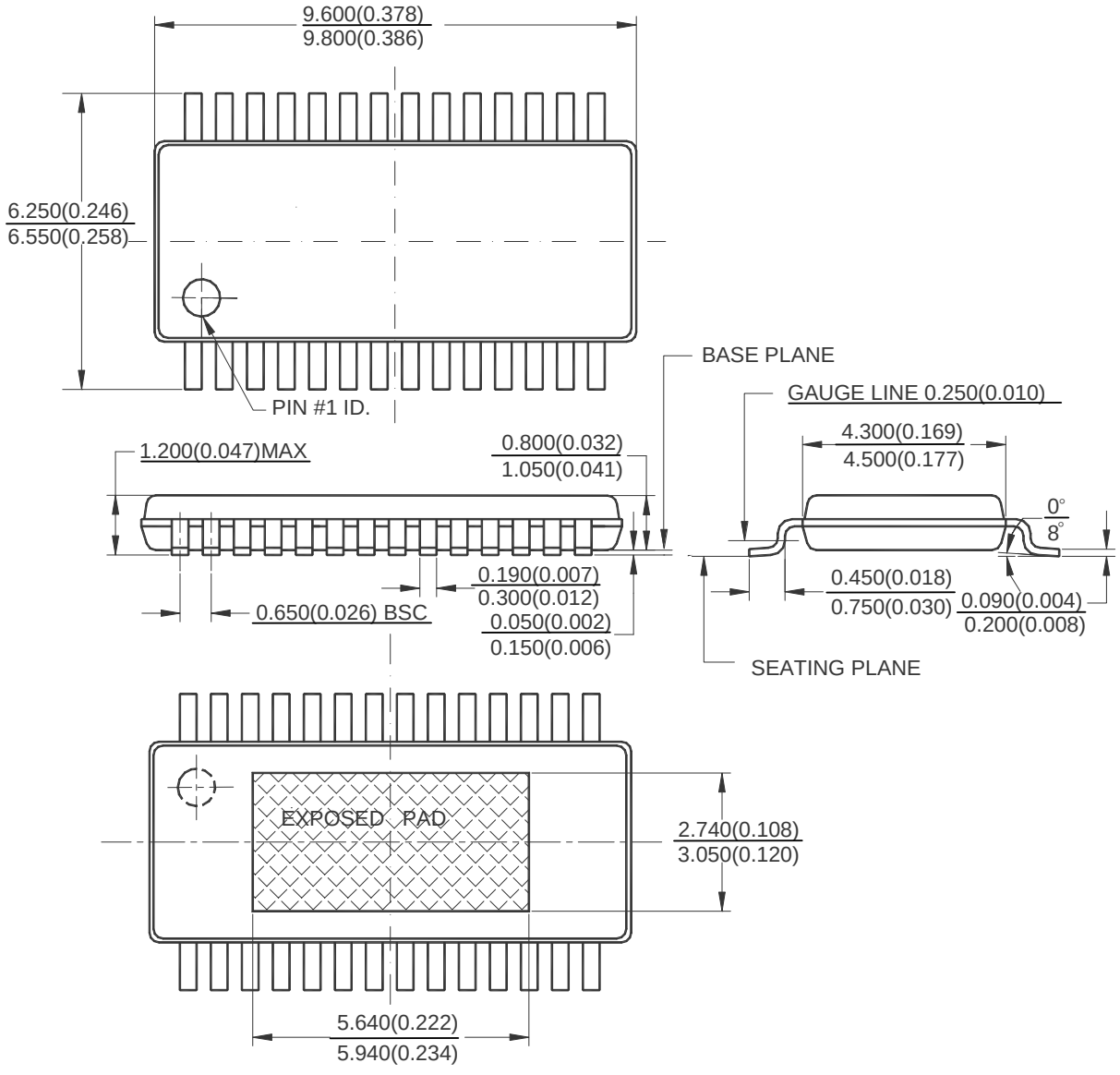


Figure 10. Typical Application Circuit of AP3068 (Paralleled Channel Application)

Mechanical Dimensions

TSSOP-28 (EDP) Unit: mm(inch)



Note: Eject hole, oriented hole and mold mark is optional.

BCD Semiconductor Manufacturing Limited

http://www.bcdsemi.com

IMPORTANT NOTICE

BCD Semiconductor Manufacturing Limited reserves the right to make changes without further notice to any products or specifications herein. BCD Semiconductor Manufacturing Limited does not assume any responsibility for use of any its products for any particular purpose, nor does BCD Semiconductor Manufacturing Limited assume any liability arising out of the application or use of any its products or circuits. BCD Semiconductor Manufacturing Limited does not convey any license under its patent rights or other rights nor the rights of others.

MAIN SITE

- Headquarters
BCD (Shanghai) Micro-electronics Limited
No. 1600, Zi Xing Road, Shanghai ZiZhu Science-based Industrial Park, 200241, P. R.C.
Tel: +86-021-2416-2266, Fax: +86-021-2416-2277

- Wafer Fab
Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd.
800 Yishan Road, Shanghai 200233, China
Tel: +021-6485-1491, Fax: +86-021-5450-0008

REGIONAL SALES OFFICE

Shenzhen Office
Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd., Shenzhen Office
Unit A Room 1203,Skyworth Bldg., Gaoxin Ave.1.S., Nanshan District
Shenzhen 518057, China
Tel: +86-0755-8660-4900, Fax: +86-0755-8660-4958

Taiwan Office (Taipei)
BCD Semiconductor (Taiwan) Company Limited
3F, No.17, Lane 171, Sec. 2, Jiu-Zong Rd., Nei-Hu Dist., Taipei(114), Taiwan, R.O.C
Tel: +886-2-2656 2808
Fax: +886-2-2656-2806/26562950

Taiwan Office (Hsinchu)
BCD Semiconductor (Taiwan) Company Limited
8F, No.176, Sec. 2, Gong-Dao 5th Road, East District
HsinChu City 300, Taiwan, R.O.C
Tel: +886-3-5160181, Fax: +886-3-5160181

USA Office
BCD Semiconductor Corp.
48460 Kato Road, Fremont, CA 94538, USA
Tel: +1-510-668-1950
Fax: +1-510-668-1990

Korea Office
BCD Semiconductor Limited Korea office.
Room 101-1112, Digital-Empire II, 486 Sin-dong,
Yeongtong-Gu, Suwon-city, Gyeonggi-do, Korea
Tel: +82-31-695-8430