

MM54HCT151/MM74HCT151 8-Channel Digital Multiplexer

General Description

This high speed Digital multiplexer utilizes advanced silicon-gate CMOS technology. Along with the high noise immunity and low power dissipation of standard CMOS integrated circuits, it possesses the ability to drive 10 LS-TTL loads. The MM54HCT151/MM74HCT151 selects one of the 8 data sources, depending on the address presented on the A, B, and C inputs. It features both true (Y) and complement (W) outputs. The STROBE input must be at a low logic level to enable this multiplexer. A high logic level at the STROBE forces the W output high and the Y output low.

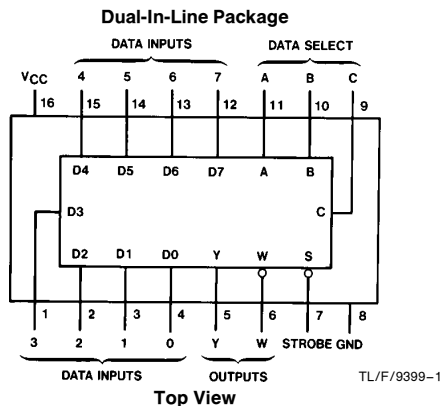
MM54HCT/MM74HCT devices are intended to interface between TTL and NMOS components and standard CMOS

devices. These parts are also plug-in replacements for LS-TTL devices and can be used to reduce power consumption in existing designs.

Features

- Typical propagation delay: 20 ns
- Low quiescent supply current: 40 μ A maximum (74HCT Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads
- TTL input compatible

Connection and Logic Diagrams

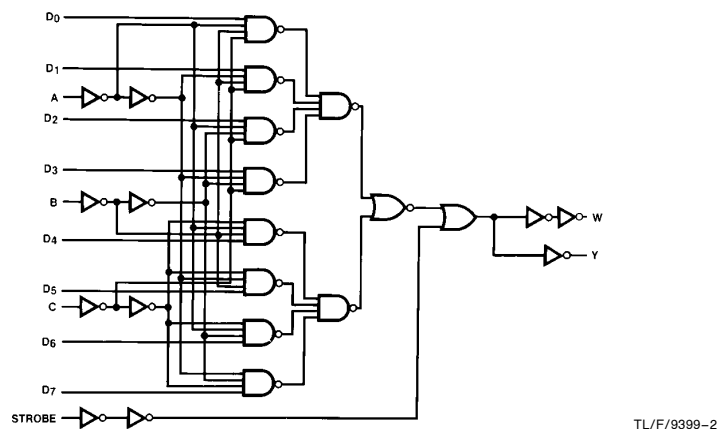


Truth Table

Inputs				Outputs	
Select			Strobe S	Y	W
C	B	A			
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

H = High Level, L = Low Level, X = Don't Care
D0, D1...D7 = the level of the respective D input

Order Number MM54HCT151 or MM74HCT151



Absolute Maximum Ratings (Notes 1 & 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Voltage (V_{IN})	−1.5V to $V_{CC} + 1.5V$
DC Output Voltage (V_{OUT})	−0.5V to $V_{CC} + 0.5V$
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per Pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per Pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering, 10 seconds)	260°C

Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	4.5	5.5	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temp. Range (T_A)			
MM74HCT	−40	+85	°C
MM54HCT	−55	+125	°C
Input Rise or Fall Times (t_r, t_f)		500	ns

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		74HCT	54HCT	Units
						T _A = −40°C to +85°C	T _A = −55°C to +125°C	
				Typ	Guaranteed Limits			
V _{IH}	Minimum High Level Input Voltage				2.0	2.0	2.0	V
V _{IL}	Maximum Low Level Input Voltage				0.8	0.8	0.8	V
V _{OH}	Minimum High Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 20 μA	4.5V		4.4	4.4	4.4	V
		V _{IN} = V _{IH} or V _{IL} I _{OUT} ≤ 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		I _{OUT} ≤ 4.8 mA	5.5V	5.2	4.98	4.84	4.7	V
V _{OL}	Maximum Low Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OUT} = 20 μA		0	0.1	0.1	0.1	V
		I _{OUT} = 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		I _{OUT} = 4.8 mA	5.5V	0.2	0.26	0.33	0.4	V
I _{IN}	Maximum Input Current	V _{IN} = V _{CC} or GND	6.0V		±0.1	±1.0	±1.0	μA
I _{CC}	Maximum Quiescent Supply Current	V _{IN} = V _{CC} or GND I _{OUT} = 0 μA			8.0	80	160	μA
		V _{IN} = 2.4V or 0.5V (Note 4)		0.25	0.4	0.55	0.65	mA

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic “N” package: −12 mW/°C from 65°C to 85°C; ceramic “J” package: −12 mW/°C from 100°C to 125°C.

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH} , and V_{OL}) occur for HCT at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at $V_{CC} = 5.5V$ and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN} , I_{CC} , and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

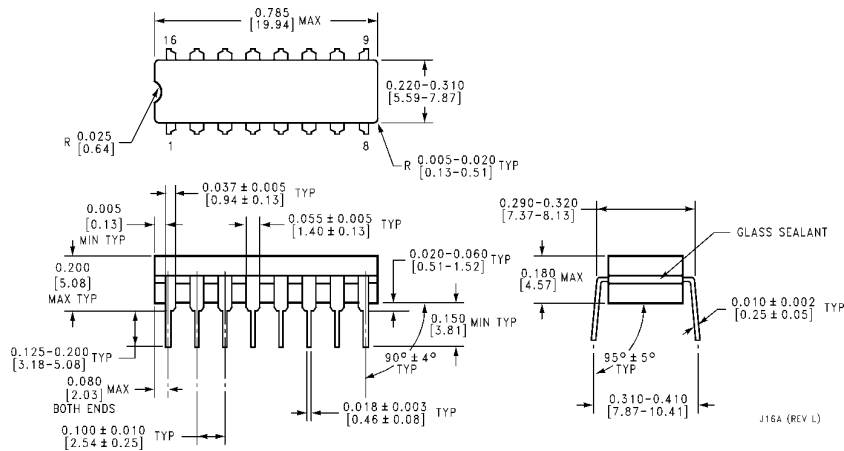
AC Electrical Characteristics $V_{CC} = 5V$, $T_A = 25^\circ C$, $C_L = 15\text{ pF}$, $t_r = t_f = 6\text{ ns}$

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
t_{PHL} , t_{PLH}	Maximum Propagation Delay A, B or C to Y		26	35	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay A, B or C to W		26	35	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Any D to Y		22	29	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay any D to W		22	29	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Strobe to Y		17	23	ns
t_{PHL} , t_{PLH}	Maximum Propagation Delay Strobe to W		17	23	ns

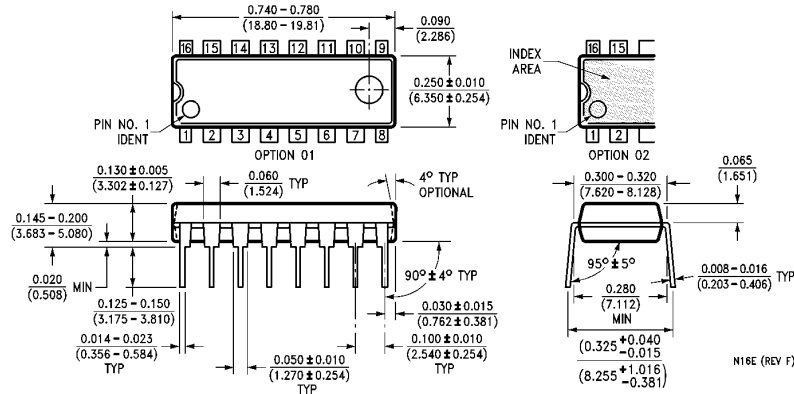
AC Electrical Characteristics $V_{CC} = 5.0V \pm 10\%$, $C_L = 50\text{ pF}$, $t_r = t_f = 6\text{ ns}$ (unless otherwise specified)

Symbol	Parameter	Conditions	T _A = 25°C		74HCT	54HCT	Units
			Typ	Guaranteed Limits			
t _{PHL} , t _{PLH}	Maximum Propagation Delay A, B or C to Y		33	46	58	69	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay A, B or C to W		33	46	58	69	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay any D to Y		27	39	49	59	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay any D to W		27	39	49	59	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Strobe to Y		21	28	35	42	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Strobe to W		21	28	35	42	ns
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		8	15	19	23	ns
C _{PD}	Power Dissipation Capacitance (Note 5)	(per package)	110				pF
C _{IN}	Maximum Input Capacitance		5	10			pF

Note 5: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Physical Dimensions inches, (millimeters)

Ceramic Dual-In-Line Package (J)
Order Number MM54HCT151J or MM74HCT151J
NS Package Number J16A



Molded Dual-In-Line Package (N)
Order Number MM74HCT151N
NS Package Number N16E

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National Semiconductor Corporation
 1111 West Bardin Road
 Arlington, TX 76017
 Tel: 1(800) 272-9959
 Fax: 1(800) 737-7018

National Semiconductor Europe
 Fax: (+49) 0-180-530 85 86
 Email: cnjwge@tevm2.nsc.com
 Deutsch Tel: (+49) 0-180-530 85 85
 English Tel: (+49) 0-180-532 78 32
 Français Tel: (+49) 0-180-532 93 58
 Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
 19th Floor, Straight Block,
 Ocean Centre, 5 Canton Rd.
 Tsimshatsui, Kowloon
 Hong Kong
 Tel: (852) 2737-1600
 Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
 Tel: 81-043-299-2309
 Fax: 81-043-299-2408

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