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ICB2FL01G

Smart Ballast Control IC for Fluorescent Lamp Ballasts

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Never stop thinking

ICB2FL01G

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38	38	Update 3.3 State Diagram
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53	53	BOM Update deleted Partnumbers of MOSFETs
54	54	Figure 42 Schematic of a serial Lamp Ballast Design
54	55	Figure 42 rename in Figure 43 and shift one page

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2nd Generation FL-Controller for Fluorescent Lamp Ballasts

Product Highlights

Lowest Count of external Components
900V-Half-Bridge driver with coreless Transformer Technology
Supports Customer In-Circuit Test Mode for reduced Tester Time
Supports Multi-Lamp Designs
Integrated digital Timers up to 40 seconds
Numerous Monitoring and Protection Features for highest Reliability
All Parameter are valid over a wide Temperature Range of T_J = - 25°C until + 125°C

Features PFC

Discontinuous Mode PFC for Load Range 0 to 100%
Integrated digital Compensation of PFC Control Loop
Improved Compensation for low THD of AC Input Current also in DCM Operation
Adjustable PFC Current Limitation

Features Lamp Ballast Inverter

Adjustable Detection of Overload and Rectifier Effect (EOL)
Detection of Capacitive Load operation
Improved Ignition Control allows Operation close to the magnetic Saturation of the lamp Inductors
Restart with skipped Preheating at short interruptions of Line Voltage (for Emergency Lighting)
Parameters adjustable by Resistors only
Pb-free Lead Plating; RoHS compliant

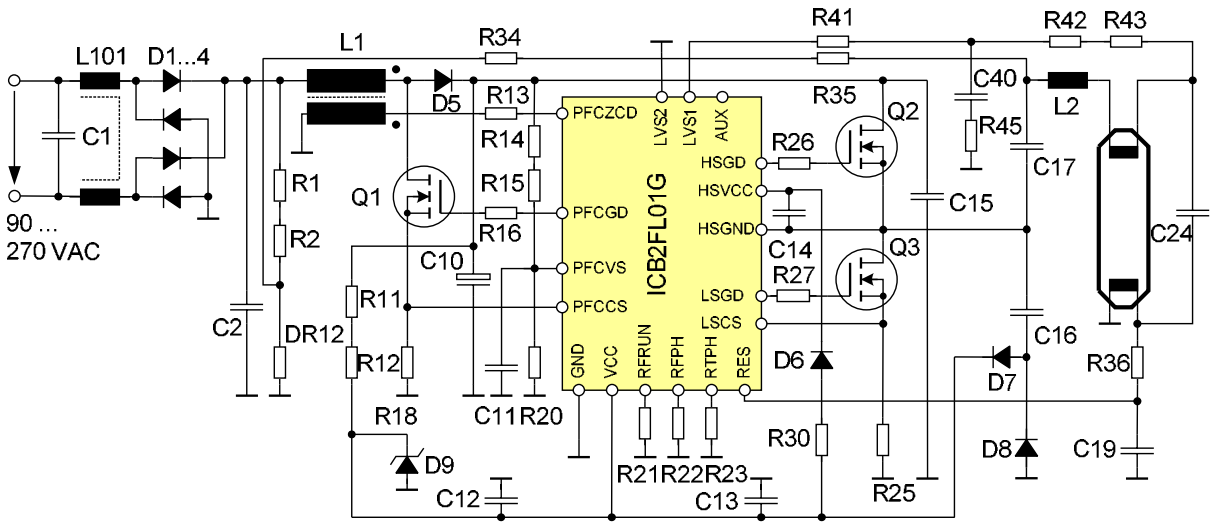


Figure 1: Typical Application Circuit of Ballast for a single Fluorescent Lamp

Description

The FL-Controller ICB2FL01G is designed to control fluorescent lamp ballast including a discontinuous mode Power Factor Correction (PFC), a lamp inverter control and a high voltage level shift half-bridge driver.
The control concept covers requirements for T5 lamp ballasts for single and multi-lamp designs. ICB2FL01G is based on the 1st Generation FL-Controller Technology, is easy to use and simply to design in. Therefore a basis for a cost effective solution for fluorescent lamp ballasts of high reliability. Figure 1 shows a typical application circuits of ballast for a single fluorescent T8 lamp with current mode preheat.

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1 Pin Configuration and Description

1.1 Pin Configuration

Pin	Symbol	Function
1	LSCS	Low side current sense (inverter)
2	LSGD	Low side Gate drive (inverter)
3	V_{CC}	Supply voltage
4	GND	Low side Ground
5	PFCGD	PFC Gate drive
6	PFCCS	PFC current sense
7	PFCZCD	PFC zero current detector
8	PFCVS	PFC voltage sense
9	RFRUN	Set R for run frequency
10	RFPH	Set R for preheat frequency
11	RTPH	Set R for preheating time
12	RES	Restart after lamp removal
13	LVS1	Lamp voltage sense 1
14	LVS2	Lamp voltage sense 2
15	AUX	Auxiliary output
16		Creepage distance
17	HSGND	High side ground
18	HSVCC	High side supply voltage
19	HSGD	High side Gate drive (inverter)
20		Not connected

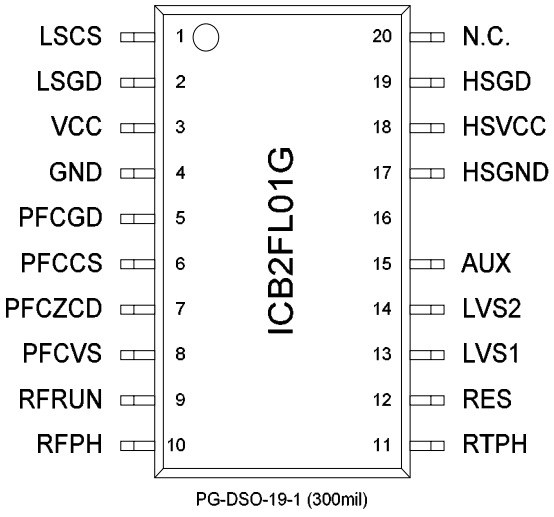


Figure 2: Package PG-DSO-19-1

1.2 Pin Description

LSCS (Low-side current sense, Pin 1)
This pin is directly connected to the shunt resistor which is located between the Source terminal of the low-side MOSFET of the inverter and ground.
Internal clamping structures and filtering measures allow for sensing the Source current of the low side inverter MOSFET without additional filter components.
There is a first threshold of 0.8V. If this threshold is exceeded for longer than 500ns during preheat or run mode, an inverter over current is detected and causes a latched shut down of the IC. The ignition control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8V threshold. This stops the decreasing of the frequency and waits for ignition. The ignition control is now continuously monitored by the LSCS PIN. The Ignition control is designed to handle a choke operation in saturation while ignition in order to reduce the choke size.
If the sensed current signal exceeds a second threshold of 1.6V for longer than 500ns during start-up, soft start, ignition mode and pre-run, the IC changes over into a latched shut down.
There are further thresholds active at this pin during run mode that detects a capacitive mode operation. A first threshold at 100mV needs to sense a positive current during the second 50% on-time of the low-side MOSFET for proper operation (Capload 1). A second threshold of -100mV senses the current before the high-side MOSFET is turned on. A voltage level below of this threshold indicates a faulty operation (Capload 2). Finally a third threshold at 2.0 V senses even short overcurrent during turn-on of the high-side MOSFET such as they are typical for reverse recovery currents of a diode (Capload 2). If one of these three comparator thresholds indicate wrong operating conditions for longer than 620µs (Capload 2) or 2500ms (Capload 1) in run mode, the IC turns off the Gates and changes into fault mode due to detected capacitive mode operation (non-zero voltage switching).
The threshold of -100mV is also used to adjust the dead time between turn-off and turn-on of the half-bridge drivers in a range of 1.25µs to 2.5µs during all operating modes.

LSGD (Low-side Gate drive, Pin 2)
The Gate of the low-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO (under voltage lockout) and a limitation of the max H-level at 11.0 V during normal operation. In order to turn-on the MOSFET softly (with a reduced di_{DRAIN}/dt); the Gate voltage rises within 220ns typically from L-level to H-level. The fall time of the Gate voltage is less than 50ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode parallel to a resistor in the Gate drive loop. It is recommended to use a resistor of typically 10Ω between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor. The dead time between LSGD signal and HSGD signal is self adapting between 1.25µs and 2.5µs.

Vcc (Supply voltage, Pin 3)
This pin provides the power supply of the ground related section of the IC. There is a turn-on threshold at 14.1V and an UVLO threshold at 10.6V. Upper supply voltage level is 17.5V. There is an internal zener diode clamping V_{CC} at 16.3V (at I_{VCC}=2mA typically). The maximum zener current is internally limited to 5mA. For higher current levels an external zener diode is required. Current consumption during UVLO and during fault mode is less than 170µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for Gate drive and logic signal currents. In order to use a skipped preheating after short interruptions of mains supply it is necessary to feed the start-up current (160µA) from the bus voltage. Note: for external V_{CC} supply see notes in flowchart chapter 3.3.

GND (Ground, Pin 4)
This pin is connected to ground and represents the ground level of the IC for supply voltage, Gate drive and sense signals.

PFCGD (PFC Gate drive, Pin 5)
The Gate of the MOSFET in the PFC preconverter designed in boost topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max H-level at 11.0 V during normal operation. In order to turn-on the MOSFET softly (with a reduced di_{DRAIN}/dt), the Gate drive voltage rises within 220ns from L-level to H-level. The fall time of the Gate voltage is less than 50ns in order to turn off quickly.
A resistor of typically 10Ω between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor is recommended.
The PFC section of the IC controls a boost converter as a PFC preconverter in discontinuous conduction mode (DCM). Typically the control starts with Gate drive pulses with a fixed on-time of typically 4.0µs at V_{ACIN} = 230V increasing up to 22.7µs and with an off-time of 47µs. As soon as sufficient zero current detector (ZCD) signals are available, the operation mode changes from a fixed frequent operation to an operation with variable frequency. The PFC works in a critical conduction mode operation (CritCM) when rated and / or medium load conditions are present. That means triangular shaped currents in the boost converter choke without gaps and variable operating frequency. During low load (detected by an internal compensator) we get an operation with discontinuous conduction mode (DCM) that means triangular shaped currents in the boost converter choke with gaps when reaching the zero current level and variable operating frequency in order to avoid steps in the consumed line current.

PFCCS (PFC current sense, Pin 6)
The voltage drop across a shunt resistor located between Source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1.0 V for longer than 200ns the PFC Gate drive is turned off as long as the zero current detector (ZCD) enables a new cycle. If there is no ZCD signal available within 52µs after turn-off of the PFC Gate drive, a new cycle is initiated from an internal start-up timer.

PFCZCD (PFC zero current detector, Pin 7)
This pin senses the point of time when the current through boost inductor becomes zero during off-time of the PFC MOSFET in order to initiate a new cycle.
The moment of interest appears when the voltage of the separate ZCD winding changes from positive to negative level which represents a voltage of zero at the inductor windings and therefore the end of current flow from lower input voltage level to higher output voltage level. There is a threshold with hysteresis, for increasing level 1.5V, for decreasing level 0.5V, which detects the change of inductor voltage.

A resistor, connected between ZCD winding and PIN 7, limits the sink and source current of the sense pin when the voltage of the ZCD winding exceeds the internal clamping levels (6.3V and -2.9V typically @ 5mA) of the IC.
If the sensed voltage level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 52µs after turn-off of the PFC Gate drive. The source current out of this pin during the on-time of the PFC-MOSFET indicates the voltage level of the AC supply voltage. During low input voltage levels the on-time of the PFC-MOSFET is enlarged in order to minimize gaps in the line current during zero crossing of the line voltage and improve the THD (Total Harmonic Distortion) of the line current. An optimization of the THD is possible by trimming of the resistor between this pin and the ZCD-winding.

PFCVS (PFC voltage sense, Pin 8)
The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for rated bus voltage is 2.5V. There are further thresholds at 0.3125V (12.5% of rated bus voltage) for the detection of open control loop and at 1.875V (75% of rated bus voltage) for the detection of an under voltage and at 2.725V (109% of rated bus voltage) for the detection of an overvoltage. The overvoltage threshold operates with a hysteresis of 100mV (4% of rated bus voltage). For the detection of a successful start-up the bus voltage is sensed at 95% (2.375V). It is recommended to use a small capacitor between this pin and GND as a spike suppression filter.
In run mode, a PFC overvoltage stops the PFC Gate drive within 5µs. As soon as the bus voltage is less than 105% of rated level, the Gate drives are enabled again. If the overvoltage lasts for longer than 625ms, an inverter overvoltage is detected and turns off the inverter the gate drives also. This causes a power down and a power up when V_{BUS}<109%.
A bus under- (V_{BUS}>75%) or inverter overvoltage during run mode is handled as fault U. In this situation the IC changes into power down mode and generates a delay of 100ms by an internal timer. Then start-up conditions are checked and if valid, a further start-up is initiated. If start-up conditions are not valid, a further delay of 100ms is generated.
This procedure is repeated maximum seven times. If a start-up is successful within these seven cycles, the situation is interpreted as a short interruption of mains supply and the preheating is skipped. Any further start-up attempt is initiated including the preheating.

RFRUN (Set R for run frequency, Pin 9)
A resistor from this pin to ground sets the operating frequency of the inverter during run mode. Typical run frequency range is 20 kHz to 120 kHz. The set resistor R_RFRUN can be calculated based on the run frequency f_{RUN} according to the equation:

$$R_{FRUN} = \frac{5 \cdot 10^8 \Omega Hz}{f_{RUN}}$$

RFPH (Set R for preheat frequency, Pin 10)
A resistor from this pin to ground sets together with the resistor at pin 9 the operating frequency of the inverter during preheat mode. Typical preheat frequency range is run frequency (as a minimum) to 150 kHz. The set resistor R_RFPH can be calculated based on the preheat frequency f_{PH} and the resistor R_{RFRUN} according to the equation:

$$R_{RFPH} = \frac{R_{RFRUN}}{\frac{f_{PH} \cdot R_{RFRUN}}{5 \cdot 10^8 \Omega Hz} - 1}$$

RTPH (Set R for preheating time, Pin 11)
A resistor from this pin to ground sets the preheating time of the inverter during preheat mode. A set resistor range from zero to 25kΩ corresponds to a range of preheating time from zero to 2500ms subdivided in 127 steps.

$$R_{RTPH} = \frac{t_{\mathrm{Pr}eHeating}}{100 \frac{ms}{k\Omega}}$$

RES (Restart, Pin 12)
A source current out of this pin via resistor and filament to ground monitors the existence of the low-side filament of the fluorescent lamp for restart after lamp removal. A capacitor from this pin directly to ground eliminates a superimposed AC voltage that is generated as a voltage drop across the low-side filament. With a second sense resistor the filament of a paralleled lamp can be included into the lamp removal sense. Note: during start up, the chip supply voltage Vcc has to be below 14.1V before V_{RES} reaches the filament detection level.

During typical start-up with connected filaments of the lamp a current source I_{RES3} (-21.3 µA) is active as long as V_{CC} > 10.6V and V_{RES} < V_{RES1} (1.6V). An open low-side filament is detected, when V_{RES} > V_{RES1}. Such a condition will prevent the start-up of the IC. In addition the comparator threshold is set to V_{RES2} (1.3V) and the current source changes to I_{RES4} (-17.7 µA). Now the system is waiting for a voltage level lower than V_{RES2} at the RES pin that indicates a connected low-side filament, which will enable the start-up of the IC.
An open high-side filament is detected when there is no sink current $I_{LVSSINK}$ (>18 µA) into both of the LVS pins before the V_{CC} Start-up threshold is reached. Under these conditions the current source at the RES pin is I_{RES1} (-42.6µA) as long as V_{CC} > 10.6V and V_{RES} < V_{RES1} (1.6V) and the current source is I_{RES2} (-35.4 µA) when the threshold has changed to V_{RES2} (1.3V). In this way the detection of the high-side filament is mirrored to the levels on the RES pin.
There is a further threshold of 3.2V active at the RES pin during run mode. If the voltage level rises above this threshold for longer than 620µs, the IC changes over into latched fault mode.
In any case of fault detection with different reaction times the IC turns-off the Gate drives and changes into power down mode with a current consumption of 170µA max. An internal timer generates a delay time of 200ms, before start-up conditions are checked again. As soon as start-up conditions are valid, a second start-up attempt is initiated. If this second attempt fails, the IC remains in latched fault mode until a reset is generated by UVLO or lamp removal. The RES PIN can be deactivated via set the PIN to GND (durable).

LVS1 (Lamp voltage sense 1, Pin 13)
Before start-up this pin senses a current fed from the rectified line voltage via resistors through the high-side filaments of the lamp for the detection of an inserted lamp.
The sensed current fed into the LVS pin has to exceed 12 µA typically at a voltage level of 6.0 V at the LVS pin. The reaction on the high side filament detection is mirrored to the RES pin (see pin 12). In addition the detection of available mains supply after an interruption is sensed by this pin. Together with pin LVS2 and pin RES the IC can monitor the lamp removal of totally four lamps. If the functionality of this pin is not required, e.g. for single lamp designs, it can be disabled by connecting this pin to ground.

During run mode the lamp voltage is monitored with this pin by sensing a current proportional to the lamp voltage via resistors. An overload is indicated by an excessive lamp voltage. If the peak to peak lamp voltage effects a peak to peak current above a threshold of 21.3μA_{PP} for longer than 620µs, a fault EOL1 (end-of-life) is assumed. If the DC current at the LVS pin exceeds a threshold of ±42µA for longer than 2500ms, a fault EOL2 (rectifier effect) is assumed. The levels of AC sense current and DC sense current can be set separately by external RC network. Note, in case of a deactivation of the LVS1/2 PIN, a reactivation starts, when the current out the LVS1/2 PIN exceeds $V_{LVSEnable1}$ in RUN Mode.

LVS2 (Lamp voltage sense 2, Pin 14)
LVS2 has the same functionality as pin LVS1 for monitoring in parallel an additional lamp circuitry.

AUX (Auxiliary output, Pin 15)
This pin provides a control current for a NPN bipolar transistor during DCM operating mode of the PFC section. There is a source current of -450µA plus the current which is fed into pin PFCZCD from the detector winding available only during the enlarged off-time. That differ the discontinuous conduction mode (DCM) from the critical conduction mode (CritCM). With this transistor a resistor for damping oscillations can be switched to the ZCD winding in order to minimize the line current harmonics during DCM operating mode. If this function is not used, this pin has to be not connected.

Pin 16 Not Existing
PIN 16 does not exist, in order to provide a wider creepage distance to the high-side gate driver. Please pay attention to relevant standards.

HSGND (High-side ground, Pin 17)
This pin is connected to the Source terminal of the high-side MOSFET which is also the node of high-side and low-side MOSFET. This pin represents the floating ground level of the high-side driver and the high-side supply.

HSVCC (High-side supply voltage, Pin 18)
This pin provides the power supply of the high-side ground related section of the IC. An external capacitor between pin 17 and pin 18 acts like a floating battery which has to be recharged cycle by cycle via high voltage diode from low-side supply voltage during on-time of the low-side MOSFET. There is an UVLO threshold with hysteresis that enables high-side section at 10.1V and disables it at 8.4V.

HSGD (High-side Gate drive, Pin 19)
The Gate of the high-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max H-level at 11.0 V during normal operation. The switching characteristics are the same as described for LSGD (pin 2). It is recommended to use a resistor of about 10 Ω between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor. The dead time between LSGD signal and HSGD signal is self adapting between 1.25µs and 2.5µs (typically).

Not connected (Pin 20)
This pin is internally not connected.

2 Functional Description

2.1 Typical Application Circutry

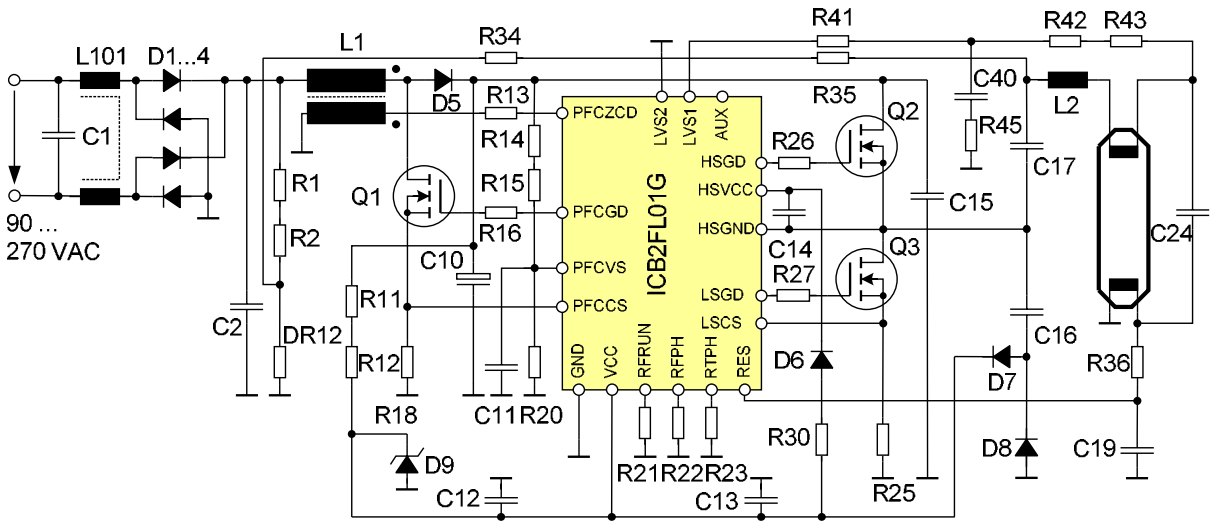


Figure 3: Application Circuit of Ballast for a single Fluorescent Lamp (FL)

The schematic in Figure 3 shows a typical application for a T5 single fluorescence lamp. It is designed for universal input voltage from 90 V_{AC} until 270 V_{AC}. The following chapters are explaining the components and referring to this schematic.

2.2 Normal Start Up

This chapter describes the basic operation flow (8 phases) from the UVLO (Under Voltage Lock Out) into Run Mode without any error detection. For detailed infromation see the following chapters 2.2.1 and 2.2.2. Figure 4 shows the 8 different phases during a typical start form UVLO (phase 1 Figure 4) to Run Mode (phase 8 Figure 4) into normal Operation (no failure detected).
In case the AC line input is switched ON, the V_{CC} voltage rises to the UVLO threshold V_{CC} = 10.6 V (no IC activities during UVLO). If V_{CC} exceeds the first threshold of V_{CC} = 10.6 V, the IC starts the first level of detection activity, the high and low side filament detection during the Start Up Hysteresis (phase 2 Figure 4).

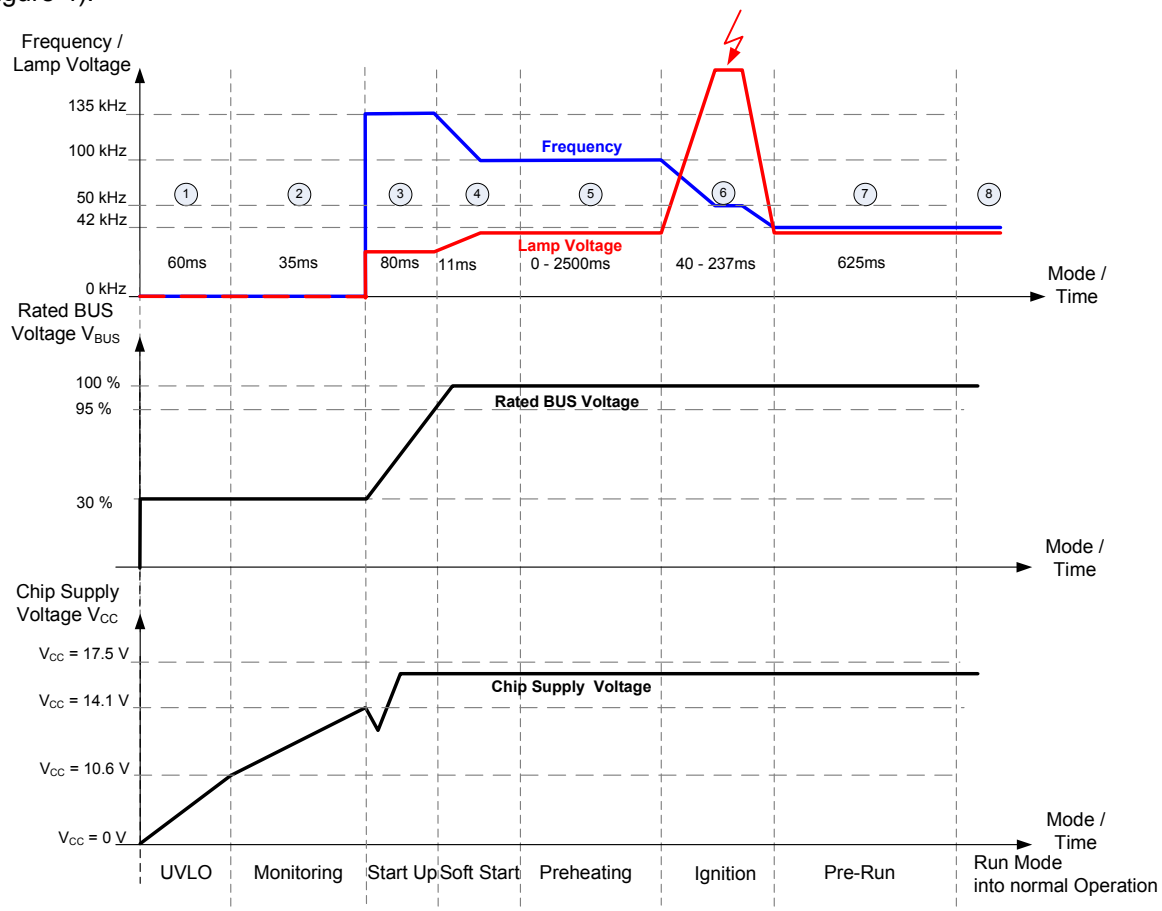


Figure 4: Typical Start Up Procedure in Run Mode (in normal Operation)

Followed by the end of the Start Up Hysteresis (phase 2 Figure 4) V_{CC} > 14.1 V and before phase 3 is active, a second level of detection activity senses for 80 µs (propagation delay of the IC) whether the rated bus voltage is below 12.5 % or above 105 %. If the previous bus voltage conditions are fulfilled and the filaments are detected, the IC starts the operation with an internally fixed startup frequency of typically 135 kHz (all gates are active). In case the bus voltage reaches a level of 95% of the rated bus voltage within latest 80ms (phase 3 Figure 4), the IC enters the Soft Start. During the Soft Start (phase 4 Figure 4), the Start Up frequency shifts from 135 kHz down to the set preheating frequency (chapter 2.2.2). In the Soft Start phase, the lamp voltage rises and the chip supply voltage reaches its working level from 10.6 V < V_{CC} < 17.5 V. After finish the Soft Start, the IC enters the Preheating mode (phase 5 Figure 4) for preheating the filaments (adjustable time) in order to extend the life cycle of the FL filaments. By finishing the preheating, the controller starts the Ignition (phase 6 Figure 4). During the Ignition phase, the frequency decreases from the set preheating frequency down to the set operation frequency (adjustable see chapter 2.2.2). If the Ignition is successful, the IC enters the Pre – Run mode (phase 7 Figure 4).

This mode is in order to prevent a malfunction of the IC due to an instable system e.g. the lamp parameters are not in a steady state condition. After finish the 625 ms Pre Run phase, the IC switches over to the Run mode (phase 8 Figure 4) with a complete monitoring.

2.2.1 Operating Levels from UVLO to Soft Start

This chapter describes the operating flow from phase 1 (UVLO) until phase 4 (Soft Start) in detail. The control of the ballast is able to start the operation within less than 100 ms (IC in active Mode). This is achieved by a small Start Up capacitor (about 1µF C12 and C13 – fed by start up resistors R11 and R12 in Figure 3) and the low current consumption during the UVLO (I_{VCC} = 130 µA – phase 1 Figure 5) and Start Up Hysteresis (I_{VCC} = 160 µA – defines the start up resistors – phase 2 Figure 5) phases. The chip supply stage of the IC is protected against over voltage via an internal Zener clamping network which clamps the voltage at 16.3 V and allows a current of 2.5 mA. For clamping currents above 2.5 mA, an external Zener diode (D9 Figure 3) is required.[1]

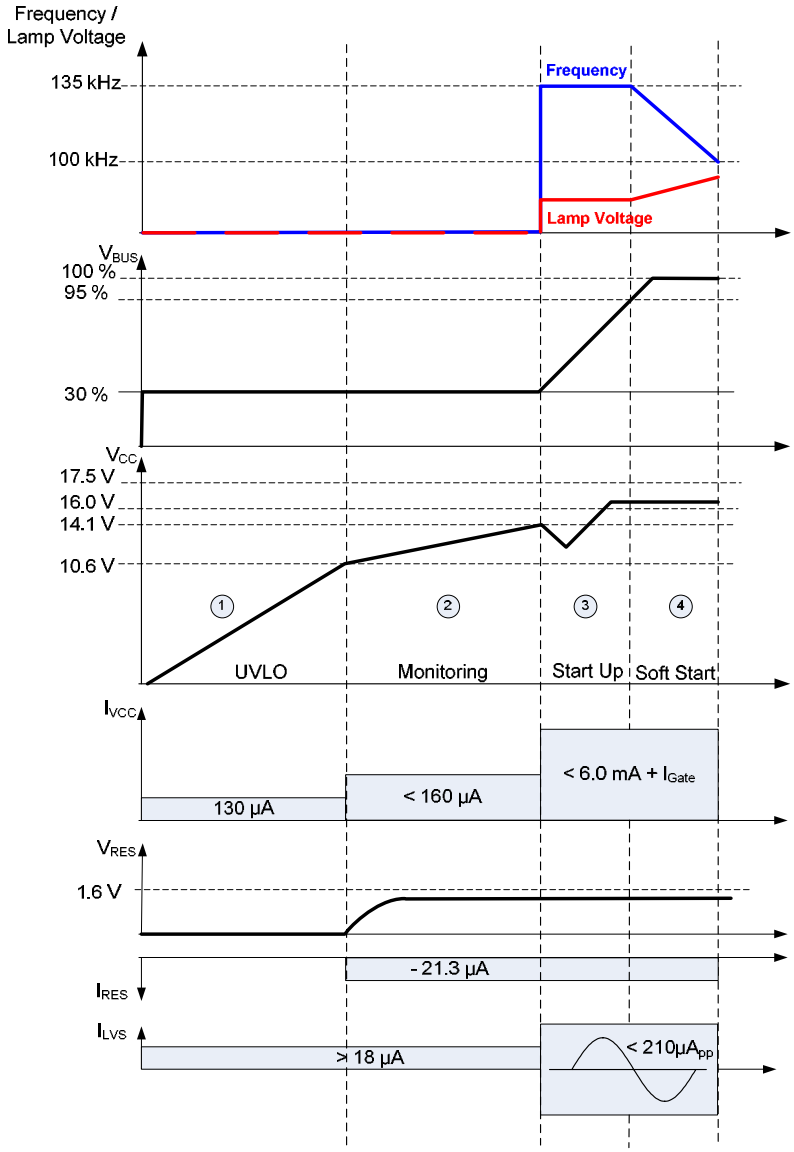


Figure 5: Progress of Level during a typical Start – UP

[1] I_{Gate} depends on MOSFET

In case of V_{CC} exceeds the 10.6 V level and stays below 14.1 V (Start up Hysteresis – phase 2 Figure 5), the IC checks whether the lamps are assembled by detecting a current across the filaments. The low side filaments are checked from a source current of typical I_{RES3} = - 21.3 µA out of PIN 12 RES
(Figure 5 I_{RES}). This current produces a voltage drop of V_{RES} < 1.6 V (filament is ok) at the low side filament sense resistor (R 36 in Figure 3), connected to GND (via low side filament). An open low side filament is detected (see chapter 2.3.2), when the voltage at the RES PIN exceeds the V_{RES} > 1.6V threshold (Figure 5 V_{RES}).
The high side filaments are checked by a current of I_{LVS} > 12 µA typically via resistors R41, R42 and R43 (Figure 3) into the LVS1 PIN 13 (for a single lamp operation) and LVS2 PIN 14 for a multi lamp operation. Note: in case of a single lamp operation, the unused LVS PIN has to be disabled via connection to GND. An open high side filament is detected (see 2.3.3) when there is no sink current into the LVS PIN. This causes a higher source current out of the RES PIN (typical 42.6 µA / 35.4 µA) in order to exceed V_{RES} > 1.6 V. In case of defect filaments, the IC keeps monitoring until there is an adequate current from the RES or the LVS PIN present (e.g. in case of removal a defect lamp).
When V_{CC} exceeds the 14.1 V threshold - by the end of the start up hysteresis in phase 2 Figure 5 - the IC waits for 80µs and senses the bus voltage. When the rated bus voltage is in the corridor of 12.5% < $V_{BUSrated}$ < 105% the IC powers up the system and enters phase 3 (Figure 5 $V_{BUSrated}$ > 95 % sensing) when not, the IC initiates an UVLO when the chip supply voltage is below V_{CC} < 10.6 V. As soon as the condition for a power up is fulfilled, the IC starts the inverter gate operation with an internal fixed Start Up frequency of 135 kHz. The PFC gate drive starts with a delay of app. 300µs. Now, the bus voltage will be checked for a rated level above 95 % for a duration of 80 ms (phase 3 Figure 5). When leaving phase 3, the IC enters the Soft Start phase and shifts the frequency from the internal fixed Start Up frequency of 135 kHz down to the set Preheating frequency e.g. f_{RFPH} = 100 kHz.

2.2.2 Operating Levels from Soft Start to Run Mode

This chapter describes the operating flow from phase 5 (Preheating mode) until phase 8 (Run mode) in detail. In order to extend the life time of the filaments, the controller enters - after the Soft Start Phase - the Preheating mode (phase 5 Figure 6). The preheating frequency is set by resistors R22 PIN RFPH to GND in combination with R21 (Figure 3) typ. 100 kHz e.g. R22 = 8.2 kΩ in parallel to R21 = 11.0 kΩ see Figure 3 at theR_{FRUN} - PIN). The preheating time can be selected by the programming resistor (R23 in Figure 3) at PIN RTPH from 0 ms up to 2500 ms (phase 5 Figure 6).

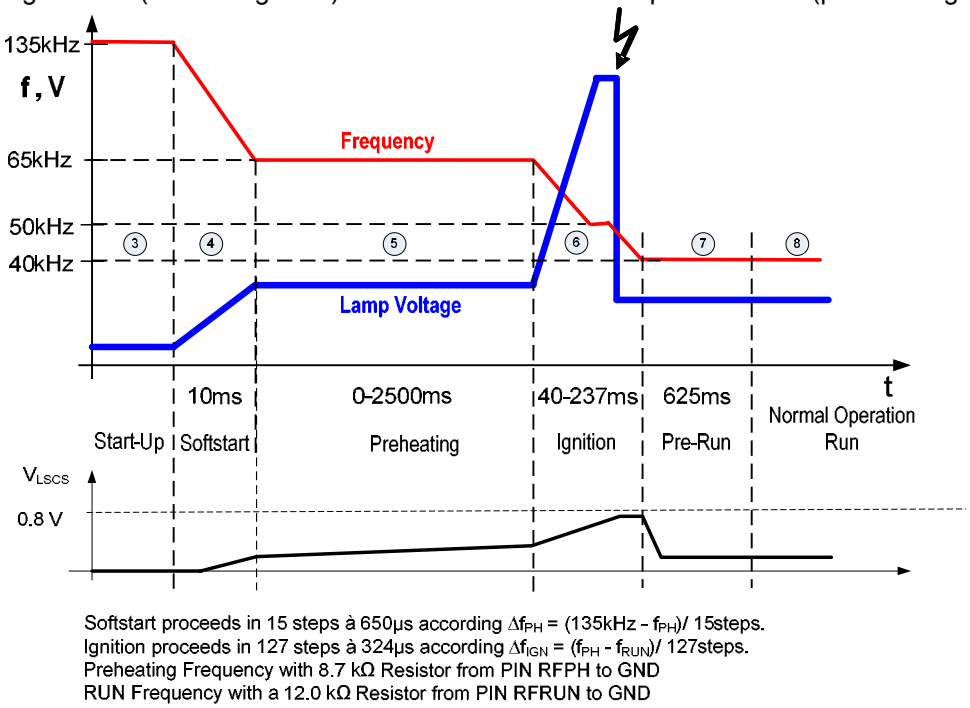


Figure 6: Typical Variation of Operating Frequency during Start Up

During Ignition (phase 6 Figure 6), the operating frequency of the inverter is shifted downward in t_{typ} = 40 ms (t_{max} = 237 ms) to the run frequency set by a resistor (R21 in Figure 3) at PIN RFRUN to GND (typical 45 kHz with 11.0 kΩ resistor). During this frequency shifting, the voltage and current in the resonant circuit will rise when the operation is close to the resonant frequency with increasing voltage across the lamp. The ignition control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8V threshold. This stops the decreasing of the frequency and waits for ignition. The ignition control is now continuously monitored by the LSCS PIN. The maximum duration of the Ignition procedure is limited to 237 ms. Is there no Ignition within this time frame, the ignition control is disabled and the IC changes over into the latched fault mode. Furthermore, in order to reduce the lamp choke, the ignition control is designed to operate with a lamp choke in magnetic saturation during ignition. For an operation in magnetic saturation during ignition; the voltage at the shunt at the LSCS pin 1 has to be V_{LSCS} = 0.75V when ingition voltage is reached. If the ignition is successful, the IC enters the Pre – Run mode (phase 7 Figure 6). The Pre Run mode is a safety mode in order to prevent a malfunction of the IC due to an instable system e.g. the lamp parameters are not in a steady state condition. After 625 ms Pre Run mode, the IC changes into the Run Mode (phase 8 Figure 6). The Run mode monitors the complete system regarding bus over- and under voltage, open loop, over current of PFC and / or Inverter, lamp over voltage (EOL1) and rectifier effect (EOL2) see chapter 2.5) and capacitive load 1 and 2 (see chapter 2.6).

Functional Description

Figure 7 shows the lamp voltage versus the frequency during the different phases from Preheating to the Run Mode. The lamp voltage rises by the end of the Preheating phase with a decreasing frequency (e.g. 100 kHz to 50 kHz) up to 700 V during Ignition. After Ignition, the lamp voltage drops down to its working level with continuo decreasing the frequency (Figure 7) down to its working level e.g. 45 kHz (set by a resistor at the R_{FRUN} pin to ground). After stops the decreasing of the frequency, the IC enters the Pre Run mode.

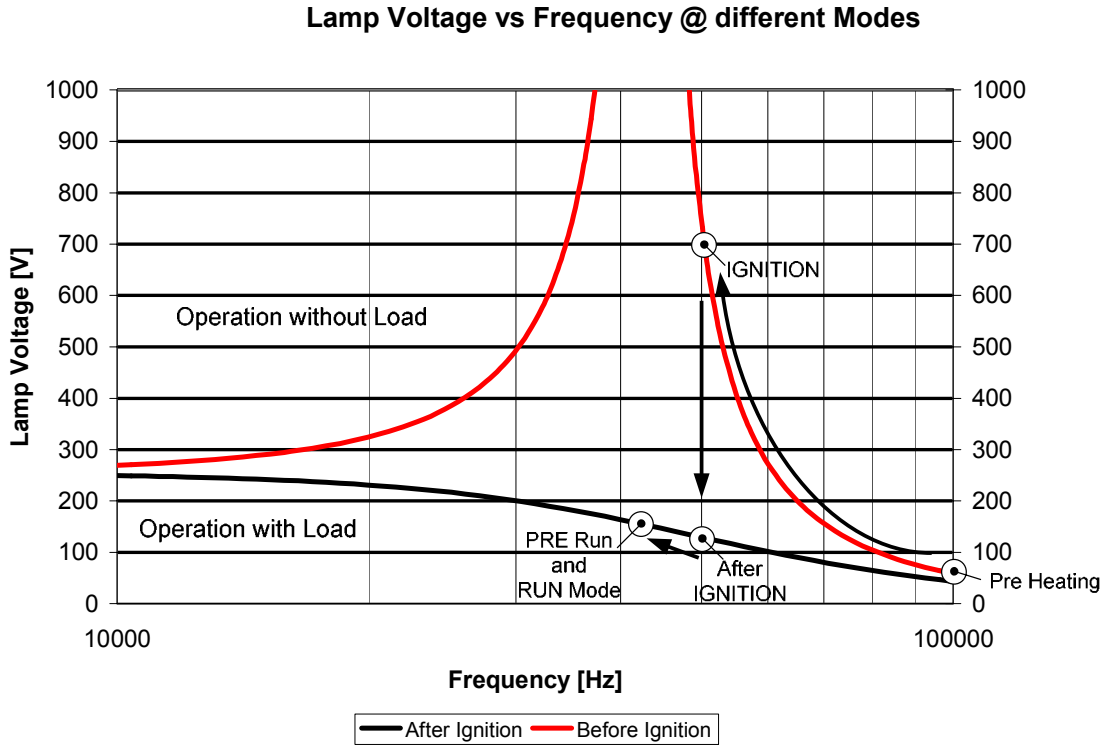


Figure 7: Lamp Voltage versus Frequency during the different Start up Phases

2.3 Filament Detection during Start Up and Run Mode

The low and high side filament detection is sensed via the RES and the LVS pins. The low side filament detection during start up and run mode is detected via the RES pin only. An open high side filament during start up will be sensed via the LVS and the RES pins.

2.3.1 Start Up with broken Low Side Filament

A source current of I_{RES3} = - 21.3 µA out of the RES pin (12) monitors during a start up (also in Run mode) the existence of a low side filament. In case of an open low side filament during the start up hysteresis (10.6V < V_{CC} < 14.1V) a capacitor (C19 in Figure 3) will be charged up via I_{RES3} = - 21.3 µA. When the voltage at the RES pin (12) exceeds V_{RES1} = 1.6 V, the controller prevents a power up and clamps the RES voltage internally at V_{RES} = 5.0 V. The gate drives of the PFC and inverter stage do not start working.

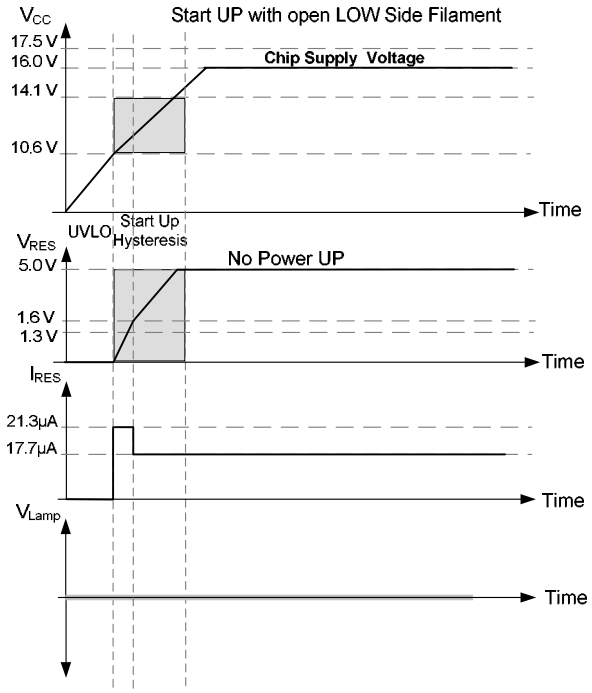


Figure 8: Startup with open Low Side Filament

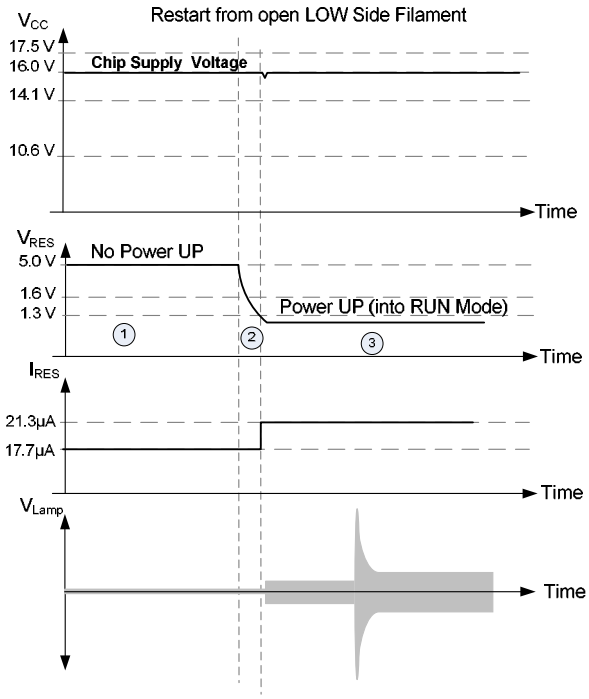


Figure 9: Restart from open Low Side Filament

The IC comparators are set now to a threshold of V_{RES1} = 1.3V and to I_{RES4} = - 17.7µA, the controller waits until the voltage at the RES pin drops below V_{RES1} = 1.3V.When a filament is present (Figure 9 section 2), the voltage drops below 1.3V and the value of the source current out of the RES pin is set from I_{RES4} = - 17.7 µA up to I_{RES3} = - 21.3 µA. Now the controller powers up the system including Soft Start and Preheating into the Run mode.

2.3.2 Low Side Filament Detection during Run Mode

In case of an open low side filament during Run mode, the current out of the RES pin I_{RES3} = - 21.3 µA charges up the capacitor C19 in Figure 3. If the voltage at the RES pin exceeds the V_{RES3} = 3.2V threshold, the controller detects an open low side filament and stops the gate drives after a delay of t = 620µs of an internal timer.

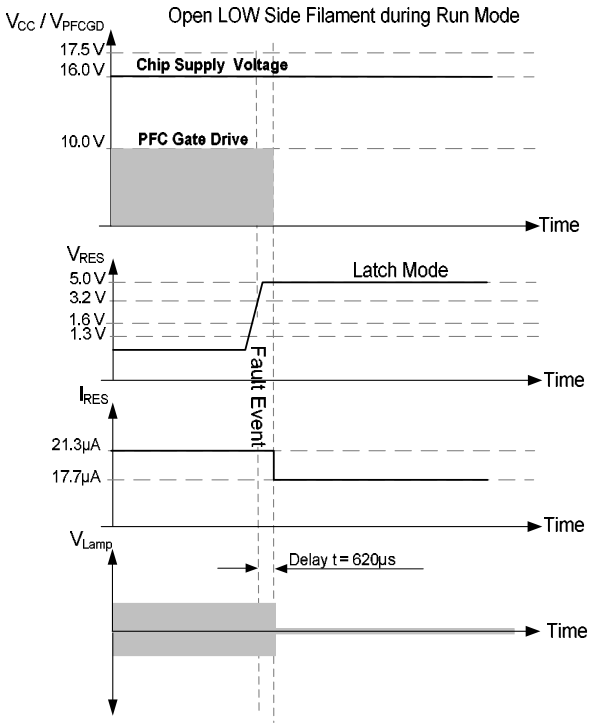


Figure 10: Open Low Side Filament Run Mode

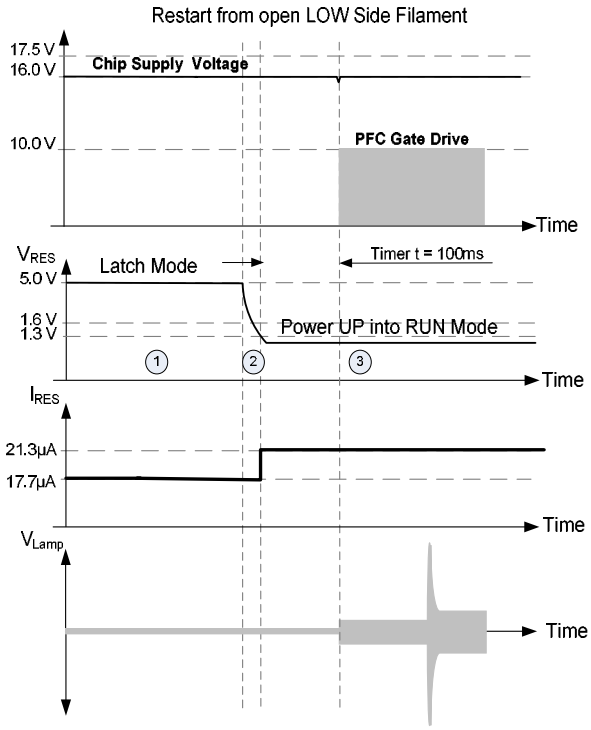


Figure 11: Restart from open LS Filament

A restart is initiated when a filament is detected e.g. in case of a lamp removal. In case of a filament is present (Figure 11 section 2), the voltage drops below 1.3V and the value of the source current out of the RES pin is set from I_{RES4} = - 17.7 µA up to I_{RES3} = - 21.3 µA. The controller powers up the system including Soft Start and Preheating into the Run mode (Figure 11 section 3).

2.3.3 Start Up with broken High Side Filament

An open high side filament during the start up hysteresis (10.6V < V_{CC} < 14.1V) is detected, when the current into the LVS pin 13 or 14 is below I_{LVS} = 12 µA (typically). In that case, the current out of the RES pin 12 rises up to I_{RES1} = - 42.6 µA. That causes a voltage at the RES pin crosses V_{RES1} = 1.6V. The source current is now set to I_{RES2} = - 35.4 µA and another threshold of V_{RES2} = 1.3V is active. The controller prevents a power up (see Figure 12), the gate drives of the PFC and inverter stage do not start working.

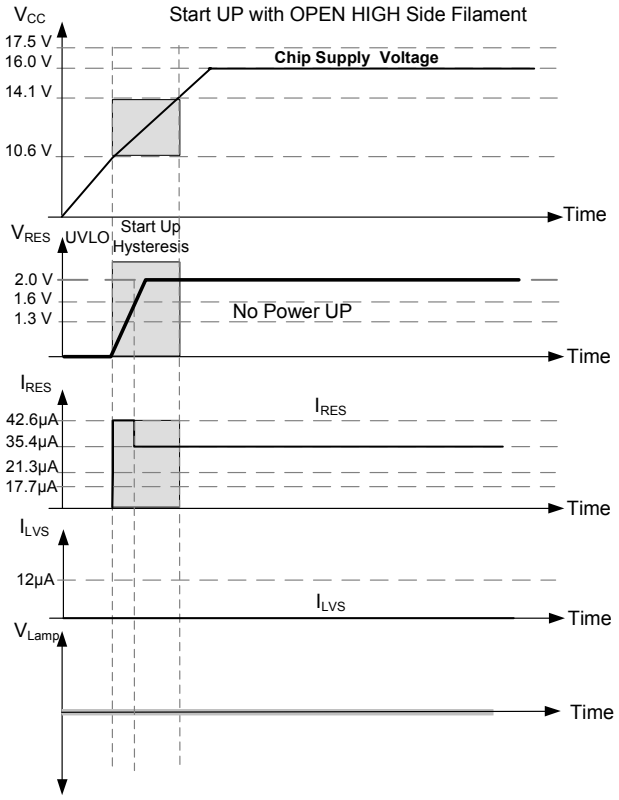


Figure 12: Start Up with open high Side Filament

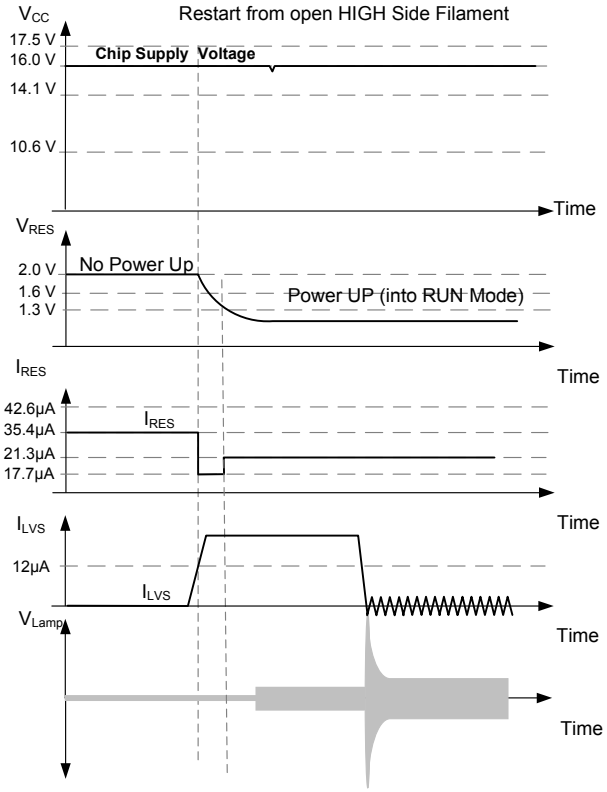


Figure 13: Restart from open high Side Filament

When the high side filament is present, e.g. insert a lamp, the current of the active LVS pins exceeds I_{LVS} > 12 µA (typically), the res current drops from I_{RES2} = - 35.4 µA down to I_{RES4} = - 17.7 µA (Figure 13). Now the controller senses the low side filament. When a low side filament is also present, and the controller drops (after a short delay due to a capacitor at the res pin) below V_{RES2} = 1.3V, the res current is set to I_{RES3} = - 21.3 µA, the controller powers up the system.

2.4 PFC Pre Converter

2.4.1 Discontinuous Conduction and Critical Conduction Mode Operation

The digital controlled PFC pre converter starts with an internally fixed ON time of typical t_{ON} = 4.0µs and variable frequency. The ON – time is enlarged every 280 µs (typical) up to a maximum ON – time of 22.7 µs. The control switches quite immediately from the discontinuous conduction mode (DCM) over into critical conduction mode (CritCM) as soon as a sufficient ZCD signal is available. The frequency range in CritCM is 22 kHz until 500 kHz, depending on the power (Figure 14) with a variation of the ON time from 22.7 µs > t_{ON} > 0.5µs.

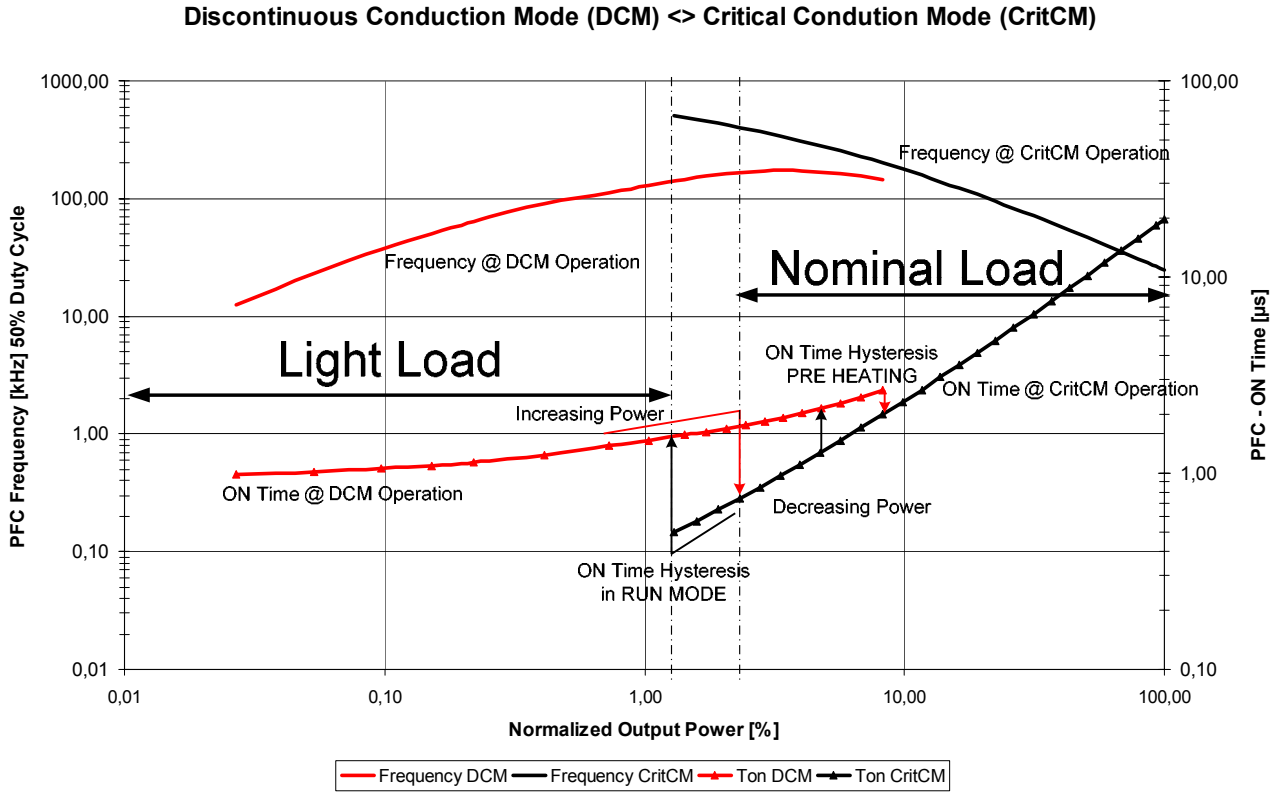


Figure 14: Operating Frequency and ON Time versus Power in DCM and CritCM Operation

For lower loads ($P_{OUTNorm}$ < 8 % from the normalized load[2]) the control operates in discontinuous conduction mode (DCM) with an ON – time from 4.0µs and increasing OFF – time. The frequency during DCM is variable in a range from 144 kHz down to typically 22 kHz @ 0.1 % Load (Figure 14). With this control method, the PFC converter enables a stable operation from 100 % load down to 0.1 %. Figure 14 shows the ON time range in DCM and CritCM (Critical Conduction Mode) operation. In the overlapping area of CritCM and DCM is a hysteresis of the ON time which causes a negligible frequency change.

[2] Normalized Power @ Low Line Input Voltage and maximum Load

2.4.2 PFC Bus Voltage Sensing

Over voltage, open loop, bus 95 % and under voltage states (Figure 15) of the PFC bus voltage are sensed at the PFCVS pin via the network R14, R15, R20 and C11 Figure 3 (C11 acts as a spike suppression filter).

2.4.2.1 Bus Over Voltage and PFC Open Loop

The bus voltage loop control is completely integrated (Figure 16) and provided by an 8 Bit sigma – delta A/D – converter with a typical sampling rate of 280 µs and a resolution of 4 mV/Bit. After leaving phase 2 (monitoring), the IC starts the power up (VCC > 14.1V). After power up, the IC senses for 80µs – 130µs the bus voltage below 12.5% (open loop) or above 105% (bus over voltage). In case of a bus over voltage ($V_{BUSrated}$ > 109 %) or open loop ($V_{BUSrated}$ < 12.5 %) in phases 3 until 8 the IC shuts off the gate drives of the PFC within 5µs respective in 1µs. In this case, the PFC restarts automatically when the bus voltage is within the corridor (12.5% < $V_{BUSrated}$ < 105 %) again. Is the bus voltage after the 80µs – 130µs valid, the bus voltage sensing is set to 12.5% < $V_{BUSrated}$ < 109 %. In case leaving these thresholds for longer than 1µ (open loop) or 5µs (overvoltage) the PFC gate drive stops working until the voltage drops below 105% or exceeds the 12.5% level. If the bus over voltage (> 109%) lasts for longer than 625ms in run mode, the inverter gates also shut off and a power down with complete restart is attempt (Figure 15).

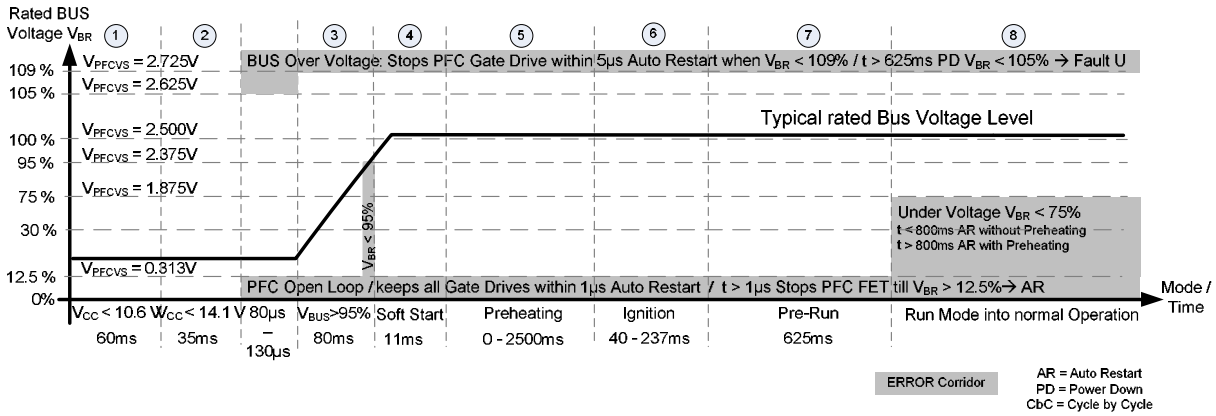


Figure 15: PFC Bus Voltage Operating Level and Error Detection

2.4.2.2 Bus Voltage 95% and 75% Sensing

When the rated bus voltage is in the corridor of 12.5% < $V_{BUSrated}$ < 109 %, the IC will check whether the bus voltage exceeds the 95 % threshold (Figure 15 phase 3) within 80 ms before entering the soft start phase 4. Another threshold is activated when the IC enters the run mode (phase 8). When the rated bus voltage drops below 75% for longer than 84 µs, a power down with a complete restart is attempted when a counter exceeds 800 ms. In case of a short term bus under voltage (the bus voltage reaches its working level in run mode before exceeding typically 800 ms (min. 500ms) the IC skips phases 1 until 5 and starts with ignition (condition for emergency lighting see 2.7.1). The internal reference level of the bus voltage sense V_{PFCVS} is 2.5 V (100 % of the rated bus voltage) with a high accuracy. A surge protection is activated in case of a rated bus voltage of V_{BUS} > 109% and a low side current sense voltage of V_{LSCS} > 0.8V for longer as 500ns in PRE RUN and RUN Mode.

2.4.3 PFC Structure of Mixed Signal

A digital NOTCH filter eliminates the input voltage ripple - independent from the mains frequency. A subsequent error amplifier with PI characteristic cares for a stable operation of the PFC pre converter (Figure 16).

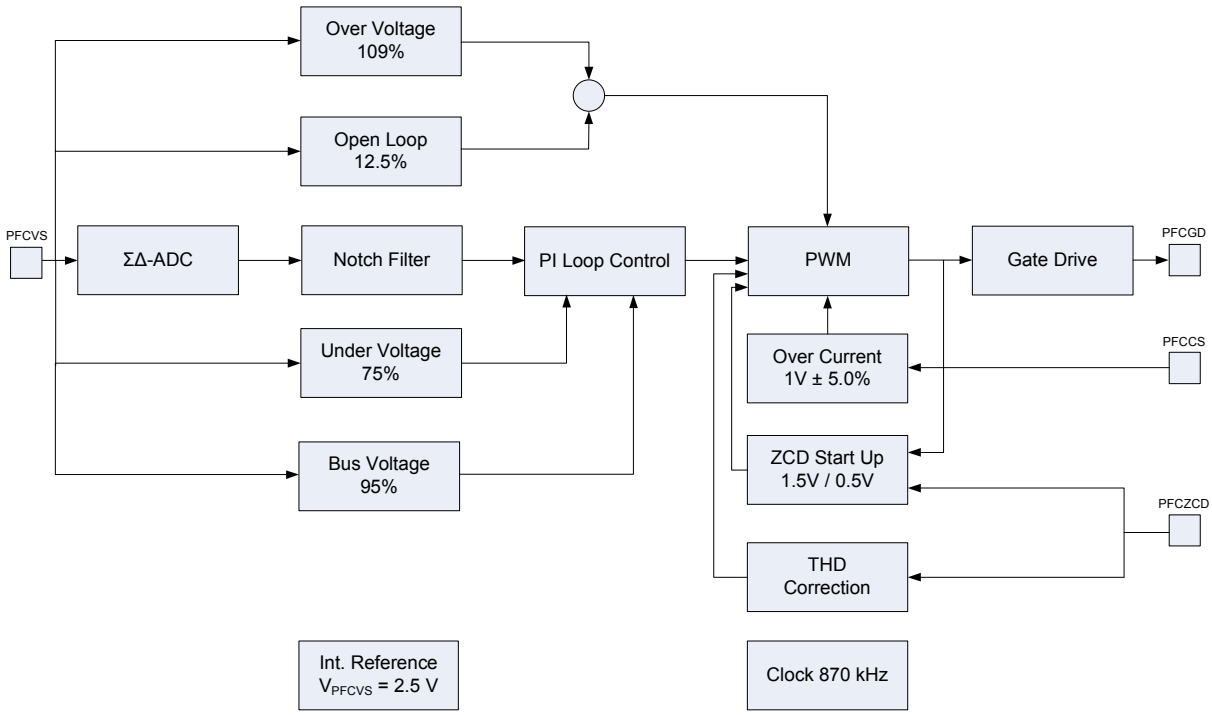


Figure 16: Structure of the mixed digital and analog control of the PFC pre converter

The zero current detection (ZCD) is sensed by the PFCZCD pin via R13 (Figure 3). The information of finished current flow during demagnetization is required in CritCM and in DCM as well. The input is equipped with a special filtering including a blanking of typically 500 ns and a large hysteresis of typically 0.5 V and 1.5 V V_{PFCZCD} (Figure 16).

2.4.4 THD Correction via ZCD Signal

An additional feature is the THD correction (Figure 16). In order to optimize the improved THD (especially in the zones A shown in Figure 17 ZCD @ AC Input Voltage), there is a possibility to extend pulse width of the gate signal (blue part of the PFC gate signal in Figure 17) via variable PFC ZCD resistor (see Resistor R13 in Figure 3) in addition to the gate signal controlled by the V_{PFCVS} signal (gray part of the PFC gate signal in Figure 17).

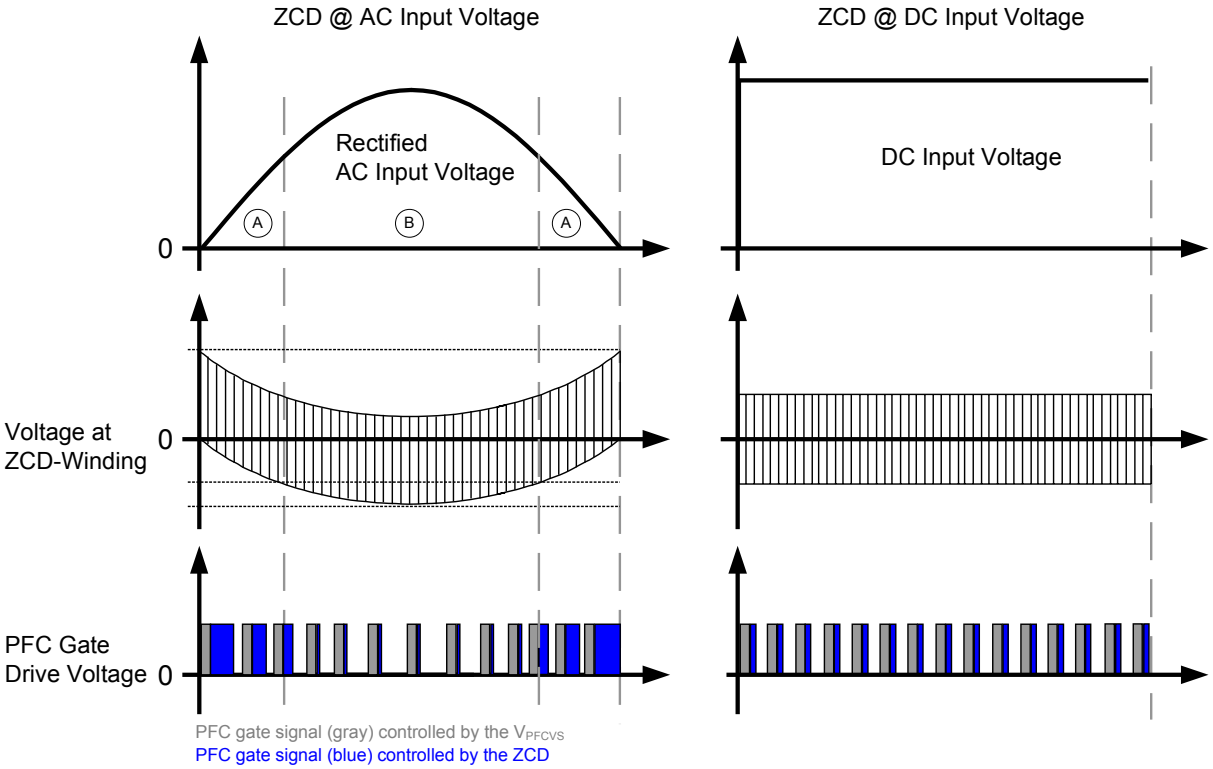


Figure 17: THD Optimization using adjustable Pulse Width Extension

In case of DC input voltage (see DC Input Voltage in Figure 17), the pulse width gate signal is fixed as a combination of the gate signal controlled by the V_{PFCVS} pin (gray) and the additional pulse width signal controlled by the ZCD pin (blue) shown in Figure 17 ZCD @ DC Input Voltage.
The PFC current limitation at pin PFCCS interrupts the ON – time of the PFC MOSFET if the voltage drop at the shunt resistors R18 (Figure 3) exceeds the V_{PFCCS} = 1.0 V (Figure 16). This interrupt will restart after the next sufficient signal from ZCD is available (Auto Restart). The first value of the resistor can be calculated by the ratio of the PFC mains choke and ZCD winding the bus voltage and a current of typically 1.5 mA (see equation below). An adjustment of the ZCD resistor causes an optimized THD.

$$R_{ZCD} = \frac{\frac{N_{ZCD}}{N_{PFC}} * V_{BUS}}{1.5mA}$$

Equation 1: R_{ZCD} a good pratical Value

The relationship between the extended PFC pulse width and the zero crossing detection current is shown in Figure 19.

2.4.5 Optional THD Correction dedicated for DCM Operation

For applications with a wide input voltage range and / or for applications using a wide variation of the power e.g. dimming, the application might work in the DCM (Discontinuous Conduction Mode). In order to minimize the high order harmonics during DCM, the detection of the DCM should be as close as possible at the point of inflection of the PFC drain source voltage shown in Figure 18. This can be realized with an optional damping network (R4, D10 and Q4 from the AUX pin to the ZCD resistor R13.

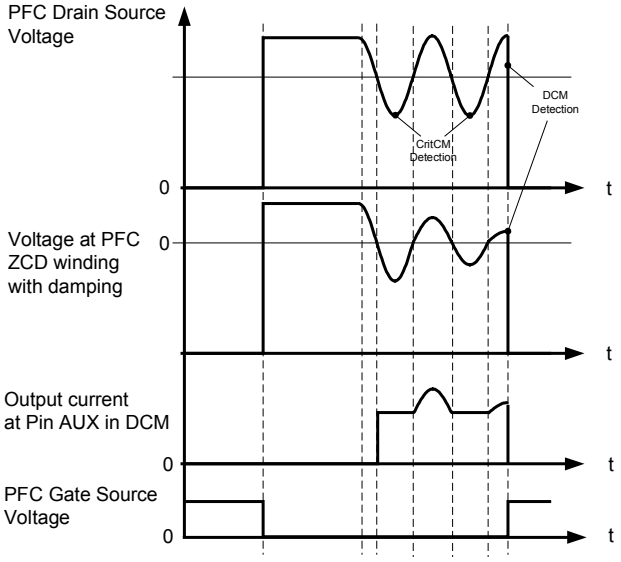


Figure 18: Signal Shapes with optional damping of oscillations during DCM operation of PFC

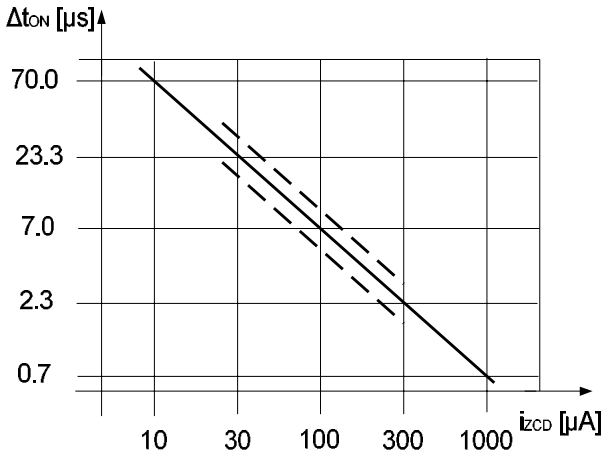


Figure 19: PFC ON Time Extension versus Zero Crossing Current Signal

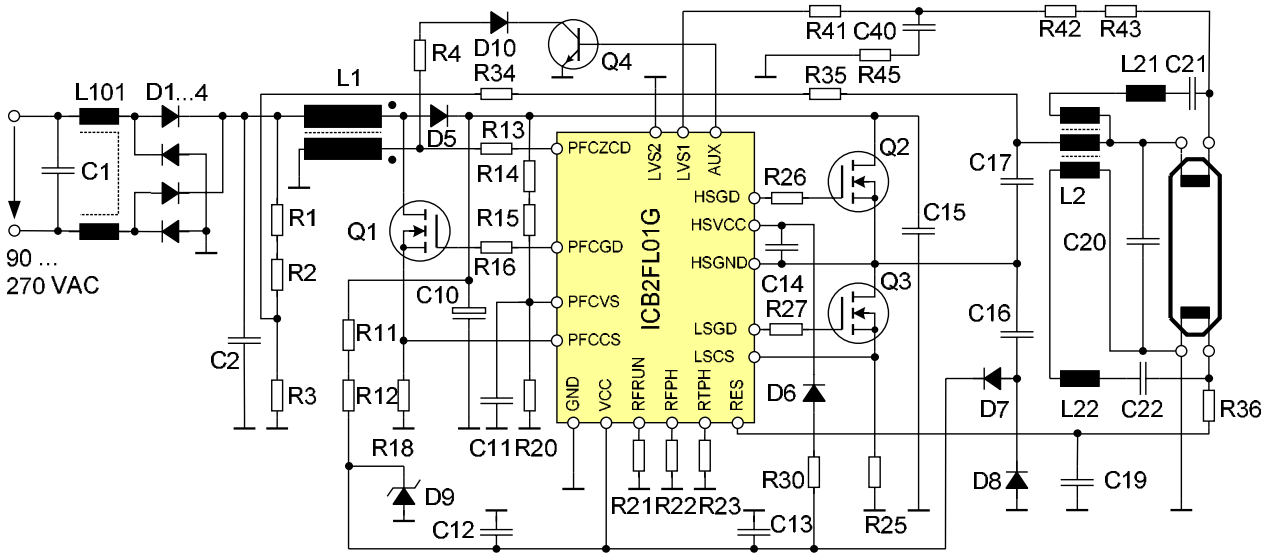


Figure 20: Optional Circuit for attenuating oscillations during DCM operation of PFC.

2.5 Detection of End-of-Life and Rectifier Effect

Two effects are present by End of Life (EOL): lamp over voltage (EOL1) and a rectifier effect (EOL2). After Ignition (see 1 in Figure 21), the lamp voltage breaks down to its run voltage level with decreasing frequency. By reaching the run frequency, the IC enters the Pre Run Mode for 625 ms. During this period, the EOL detection is still disabled. In the subsequent RUN Mode (2 in Figure 21) the detection of EOL1 (lamp over voltage see 3 Figure 21) and EOL2 (rectifier effect see 4 Figure 21) is complete enabled.

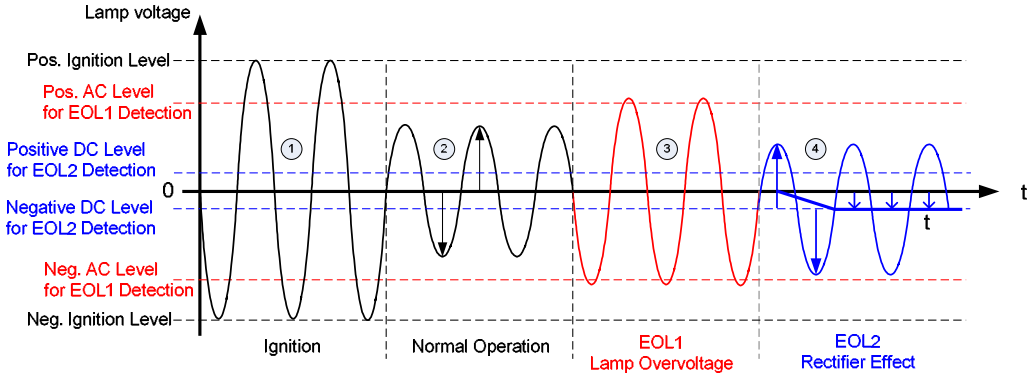


Figure 21: End of Life and Rectifier Effect

2.5.1 Detection of End of Life 1 (EOL1) – Lamp Overvoltage

The event of EOL1 is detected by measuring the positive and negative peak level of the lamp voltage via an AC current fed into the LVS pin (Figure 22). This AC current is fed into the LVS pins (LVS1 for single lamp and LVS2 for multi lamp applications) via Network R41, R42, R43 and the low pass filter C40 and R45 see Figure 3. If the sensed AC current exceeds 210 μA_{PP} for longer than 620 µs, the status of end-of-life (EOL1) is detected (lamp overvoltage / overload see Figure 22 LVSAC Current). The EOL1 fault results in a latched power down mode (after trying a single restart) the controller is continuously monitoring the status until EOL1 status changes e.g. a new lamp is inserted.

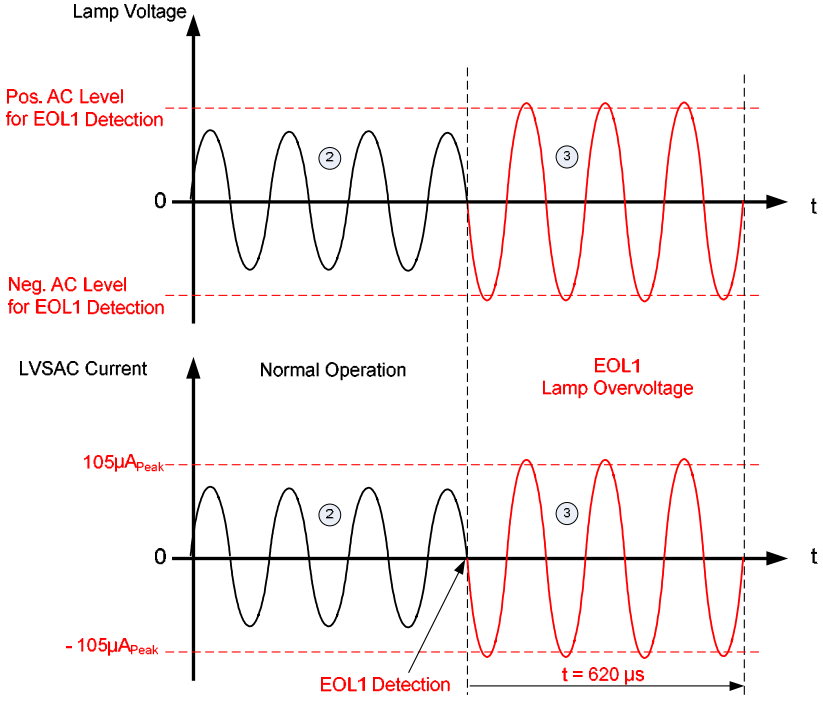


Figure 22: End of Life (EOL1) Detection, Lamp Voltage versus AC LVS Current

2.5.2 Detection of End-of-Life (EOL2) – Rectifier Effect

The rectifier effect (EOL2) is detected by measuring the positive and negative DC level of the lamp voltage via a current fed into the LVS pin (Figure 23). This current is fed into the LVS pins (LVS1 for single lamp and LVS2 for multi lamp applications) via Network R41, R42 and R43 (see Figure 3). If the sensed DC current exceeds ± 42 µA (Figure 23 LVSDC Current) for longer than 2500 ms, the status of end-of-life (EOL2) is detected. The EOL2 fault results in a latched power down mode (after trying a single restart) the controller is continuously monitoring. Only the insert of a new lamp resets the status of the IC.

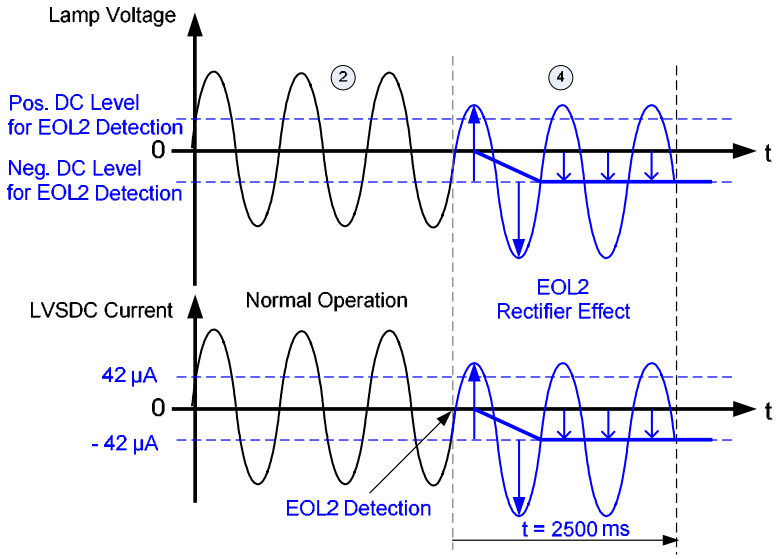


Figure 23: End of Life (EOL2) Detection, Lamp Voltage versus DC LVS Current

2.6 Detection of Capacitive Load

In order to prevent a malfunction in the area of Capacitive Load (see Figure 24) during Run Mode due to certain deviations from the normal load (e.g. harmed lamp, sudden break of the lamp tube …), the IC has three integrated thresholds – sensed only via the LSCS (pin 1). The controller distinguish between two different states of capacitive load, the detection of working without load (idling detection, CapLoad 1) and working with short over current (CapLoad 2). This state (CapLoad 2) is affecting an operation below the resonance in the capacitive load area (Figure 24). In both cases, the IC results in a latched power down mode after a single restart. After latching the power down mode, the controller is continuously monitoring the status of the fault and restarts after the fault disappears e.g. in case of inserting a new lamp.

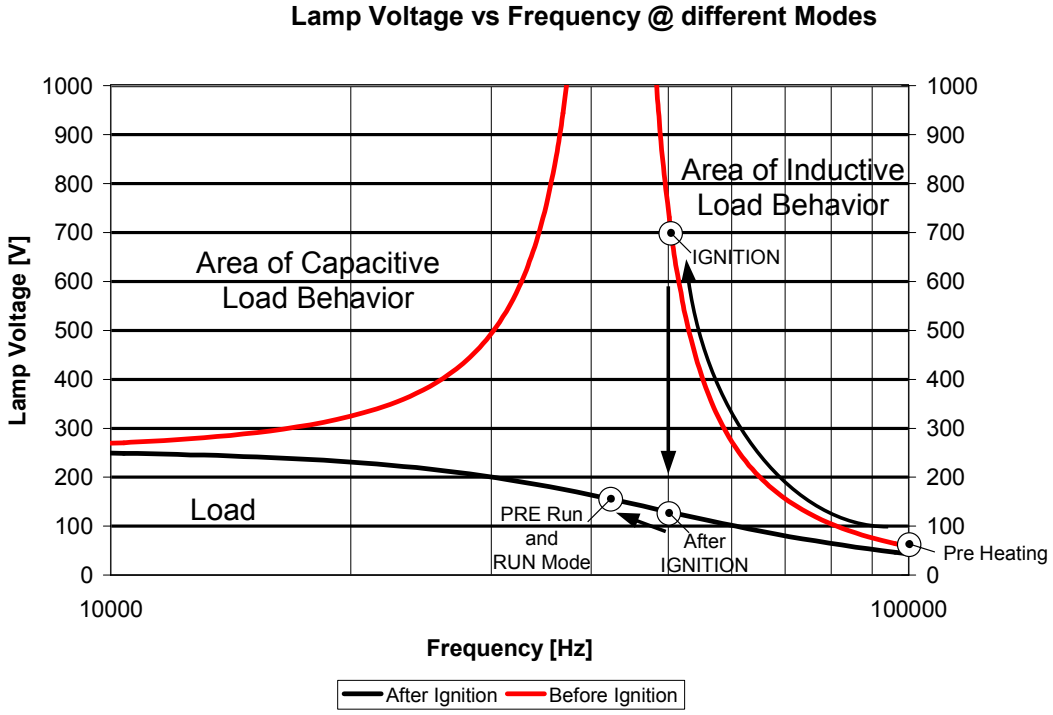


Figure 24: Capacitive and Inductive Operation

2.6.1 Capacitive Load 1 (Idling Detection – Current Mode Preheating)

A capacitive load 1 operation (idling) is detected when the voltage at the LSCS pin is below + 100 mV during the second 50% ON – time of the low side MOSFET (see Capacitive Load 1 (Idling) in Figure 25). If this status is present for longer than 2500 ms, the controller results a latched power down mode after trying a single restart. The controller is keep monitoring continuously the status until an adequate load is present (e.g. lamp removal), than the IC changes into a normal operation.

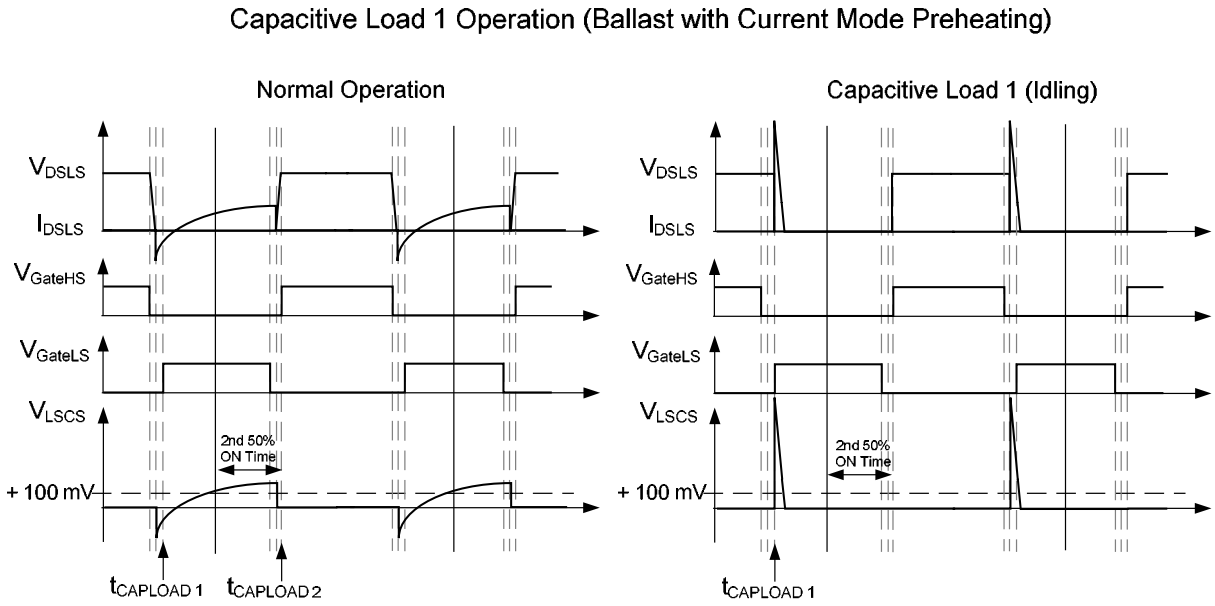


Figure 25: Capacitive Mode 1 Operation without load during Run Mode

2.6.2 Capacitive Load 2 (Over Current / Operation below Resonance)

A capacitive load 2 operation is detected if the voltage at the LSCS pin drops below a second threshold of V_{LSCS} = – 100 mV directly before the high side MOSFET is turned on or exceeds a third threshold of V_{LSCS} = 2.0 V during ON switching of the high side MOSFET. If this over current is present for longer than 620 µs, the IC results a latched power down mode after trying a single restart. The controller keeps monitoring continuously the status until an adequate load is present e.g. a new lamp is inserted, then the IC changes into a normal operation.

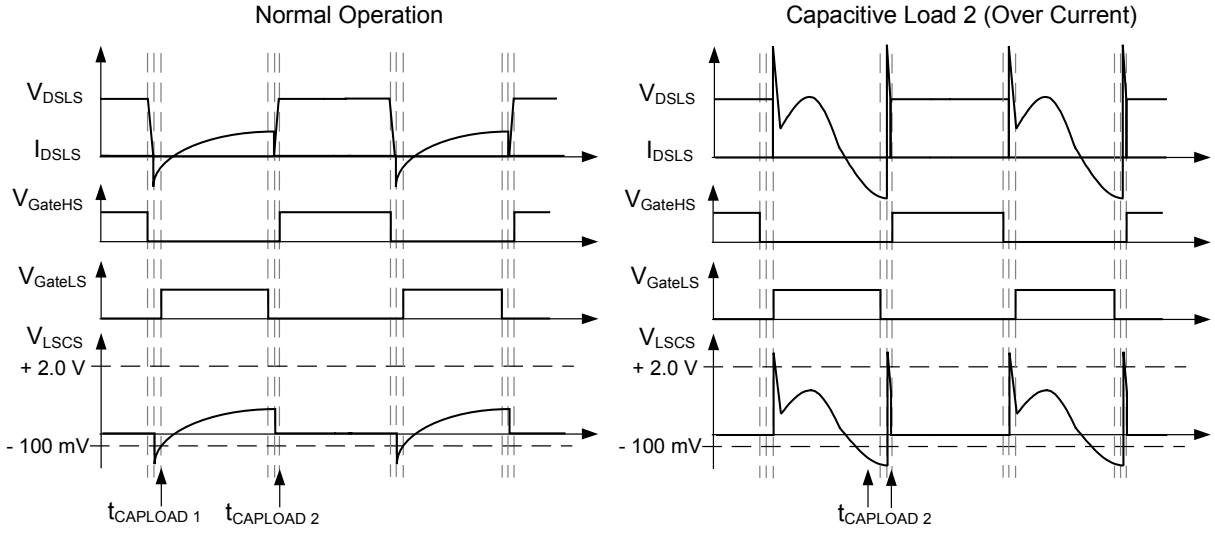


Figure 26: Capacitive Mode 2 – Operation with Over Current

2.6.3 Adjustable self adapting Dead Time

The dead time between the turn OFF and turn ON of the half – bridge drivers is adjustable (C16 see Figure 3) and detected via a second threshold (– 100 mV) of the LSCS voltage. The range of the dead time adjustment is 1.25 µs up to 2.5 µs during all operating modes. Start of the dead time measurement is the OFF switching of the high side MOSFET. The finish of the dead time measurement is, when V_{LSCS} drops for longer than typical 280ns (internal fixed propagation delay) below -100mV. This time will be stored (stored dead time) and the low side gate driver switches ON. The high side gate driver turns ON again after OFF switching of the low side switch and the stored dead time.

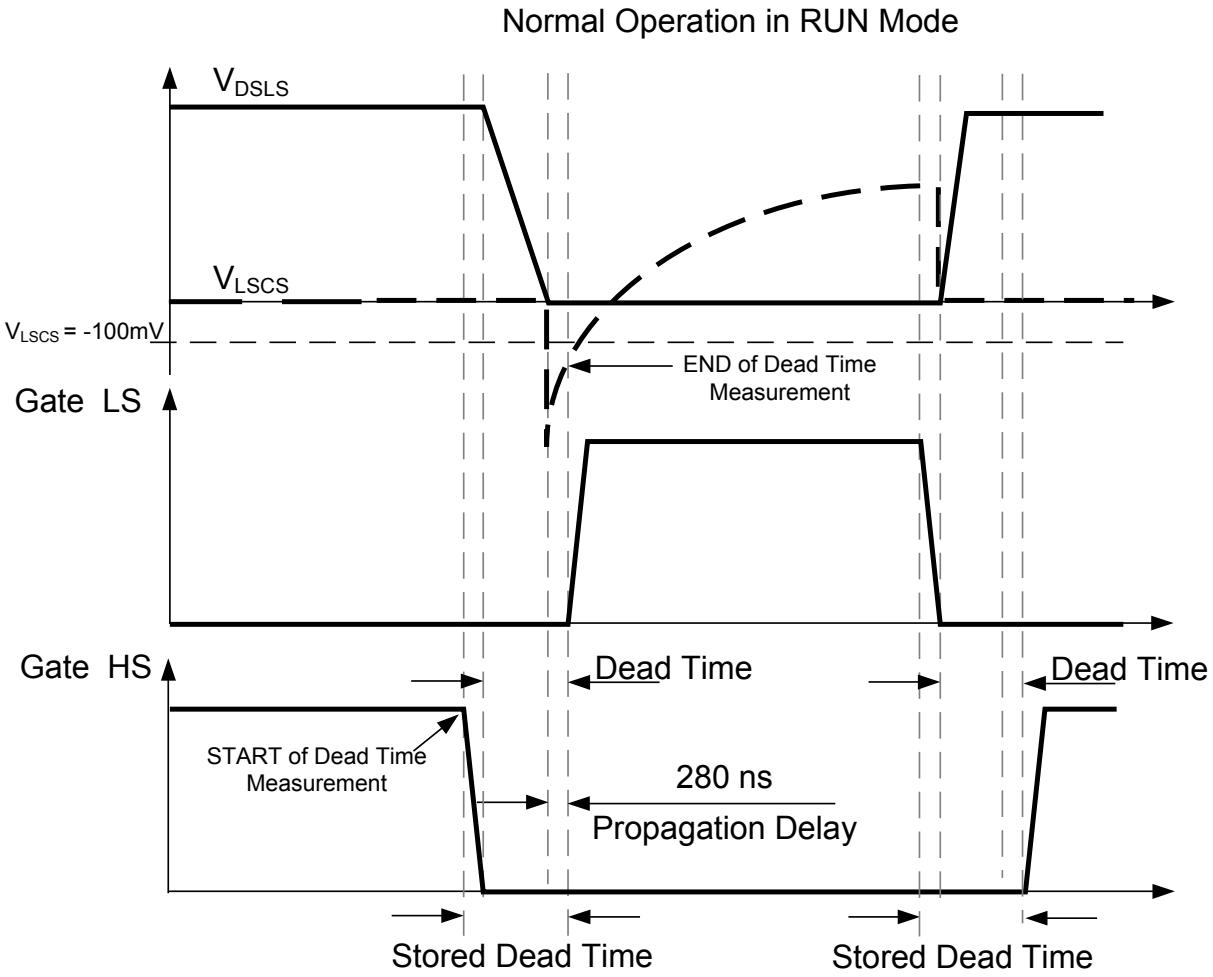


Figure 27: Dead Time of ON and OFF of the Half Bridge Drivers

2.7 Emergency Lighting

Line interruptions (bus voltage drops) are detected by the PFCVS. If the rated PFC bus voltage drops below $V_{BUSRated}$ < 75 % during run mode, the controller detects a PFC bus under voltage. In order to meets the emergency lighting standards, the controller distinguishes two different states of a PFC bus under voltage, a short and a long term PFC bus under voltage. A timer increases the time as long as a bus under voltage is present. A short term bus under voltage is detected if the timer value stays below t < 800ms typically (500ms min.) after the bus voltage reaches the nominal level again. These causes a restart without preheating (emergency standard of VDE0108) see Figure 28. When the timer exceeds t > 800 ms, the controller forces a complete restart of the system due to a long term bus under voltage (Figure 29).

2.7.1 Short Term PFC Bus Under Voltage

A short term PFC bus under voltage (Figure 28) is detected if the duration of the under voltage does not exceed 800 ms (timer stays below t < 800ms see Figure 28). In that case, the PFC and inverter drivers are immediately switched off and the controller is continuously monitoring the status of the bus voltage in a latched power down mode (I_{CC} < 170 µA). If the signal at the LVS PIN exceeds 18µA and the rated bus voltage is above 12.5% within the timer is below t < 800 ms, the controller restarts from power up without preheating. The timer resets to 0 when entering the Run Mode.

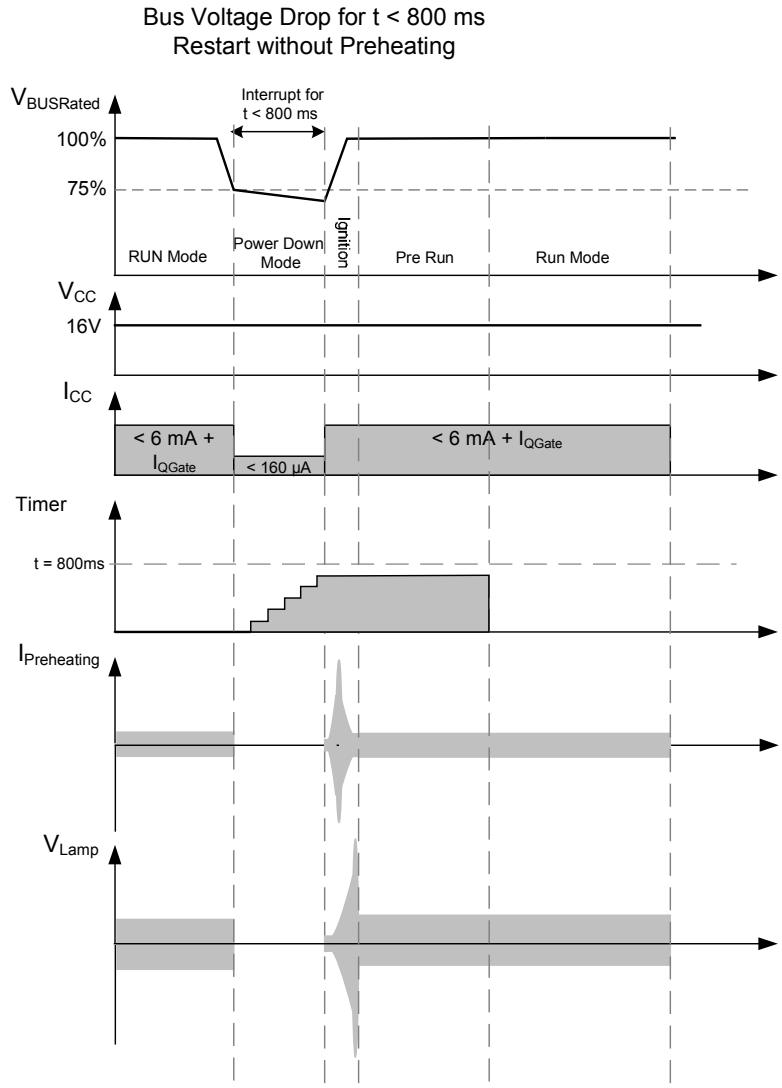


Figure 28: BUS Voltage Drop below 75% (rated Bus Voltage) for t < 800 ms during RUN Mode

2.7.2 Long Term PFC Bus Under Voltage

If the duration of the bus under voltage exceeds t > 800ms see Figure 29, the controller forces an under voltage lock out (UVLO). The chip supply voltage drops below V_{CC} = 10.6 V and the chip supply current is below I_{CC} < 130µA. When the Vcc voltage exceeds the 10.6V threshold again, the IC current consumption is below I_{CC} < 160µA. In that case, the controller resets the timer and restarts with the full start up procedure including Monitoring, Power Up, Start Up, Soft Start, Preheating, Ignition, Pre Run and Run Mode as shown in Figure 29.

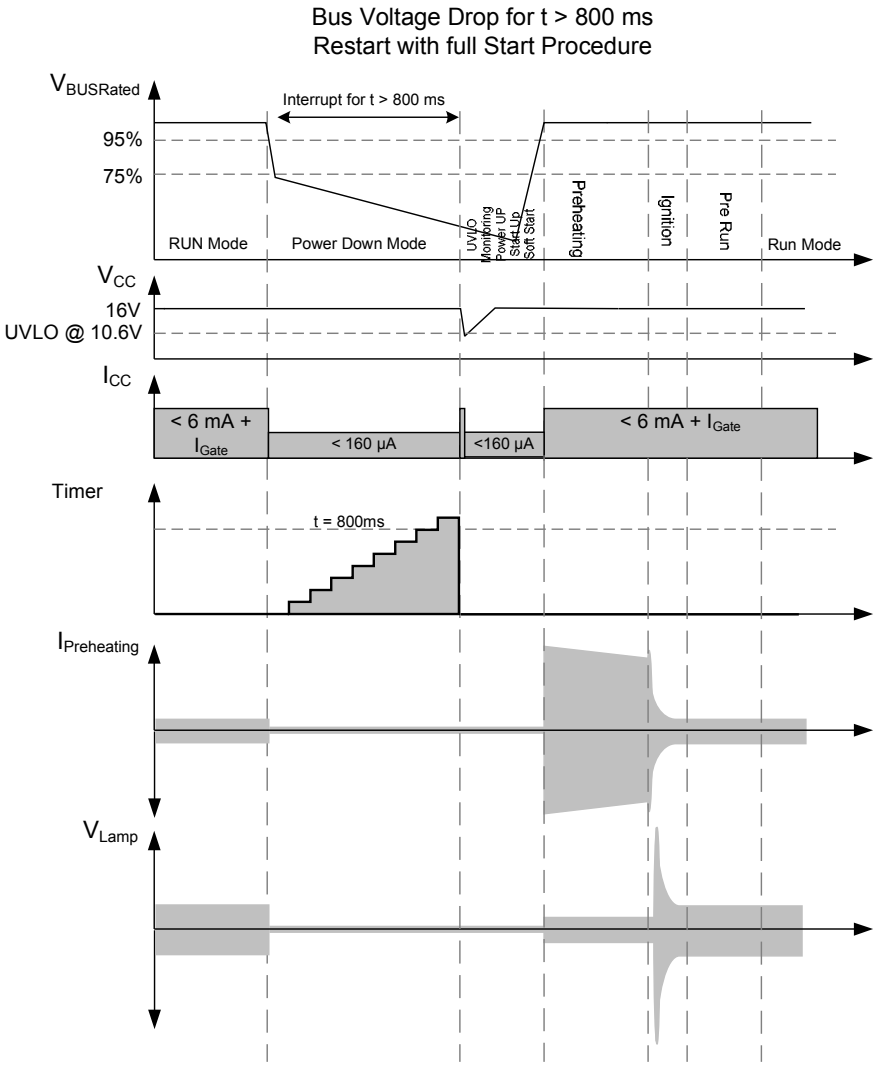


Figure 29: BUS Voltage Drop below 75% (rated Bus Voltage) for t > 800 ms during RUN Mode

2.8 Built in Customer Test Mode Operation

In order to decrease the final ballast testing time for customers, the 2nd generation of ballast IC supports an integrated built in Customer Test Mode and several functions to disable some features and states of the IC.

2.8.1 Pre Heating Test Mode

This feature forces the IC to stay in the pre heating mode (see chapter 2.8.1.2) or to starts the ignition immediately without any preheating (see chapter 2.8.1.1 skip pre heating). A resistor at this pin defines the duration of the pre heating phase. Normally, the pre heating phase is in a range of 0ms up to 2500ms set via a resistor R_{RTPH} = 0Ω up to 25kΩ from the RTPH pin to GND. The pre heating phase is skipped when the RTHP pin is set to GND. If the signal at this pin is V_{RTPH} > 5.0 V, the IC remains in the pre heating mode.

2.8.1.1 Skip the Pre Heating Phase – Set RTPH Pin to GND

The Pre Heating phase can be skipped in set the RTPH pin 11 to GND. Figure 30 shows a standard start up with a set pre heating time via resistor at the RTPH pin 11 to GND (e.g. 8.2 kΩ this is equal to a pre heating phase of app. 820ms). The pre heating phase can be skipped in setting the RTPH pin 11 directly to GND. In that case, the ignition is directly after the soft start phase.

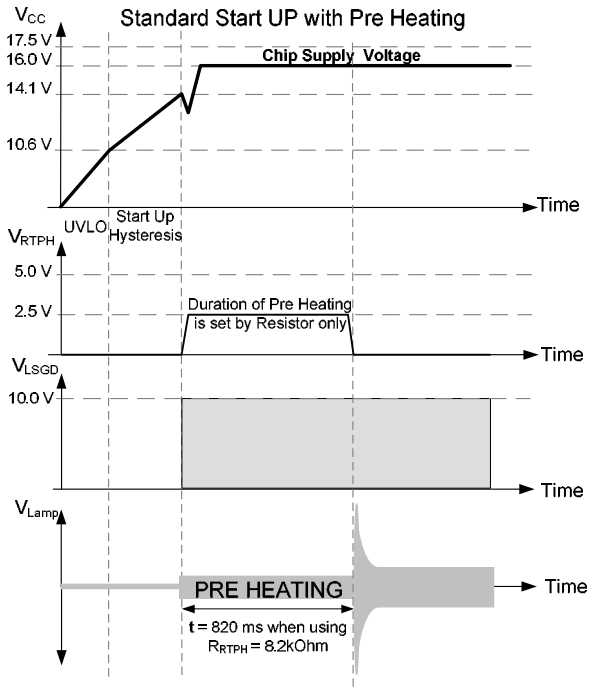


Figure 30: Start UP WITH Pre Heating

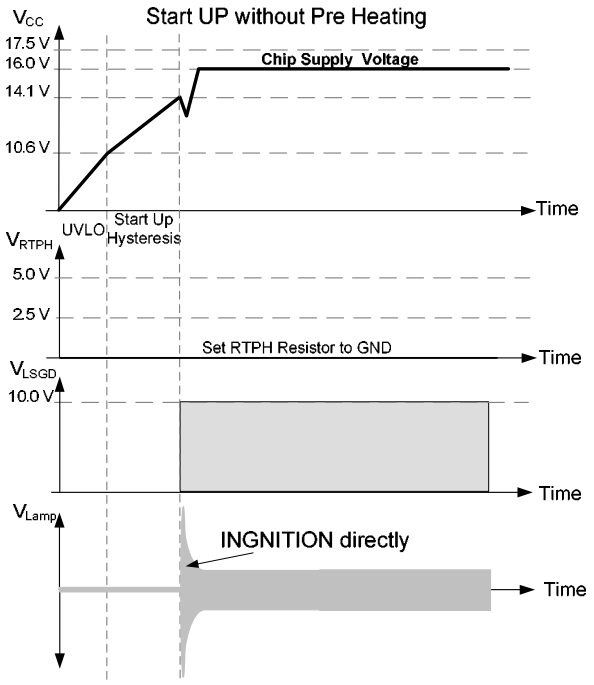


Figure 31: Start UP WITHOUT Pre Heating

2.8.1.2 IC remains in Pre Heating Phase

This feature gives the customer the flexibility to align the pre heating frequency to the filament power in the pre heating phase. Figure 32 shows a standard start up with the set preheating time of e.g. 820ms with an 8.2 kΩ resistor at the RTPH pin 11. To force the IC remains in pre heating, the voltage level at the RTPH pin 11 has to set to 5.0 V. The duration of this 5.0 V signal defines the time of the pre heating see $I_{PreHeat}$ in figure below.

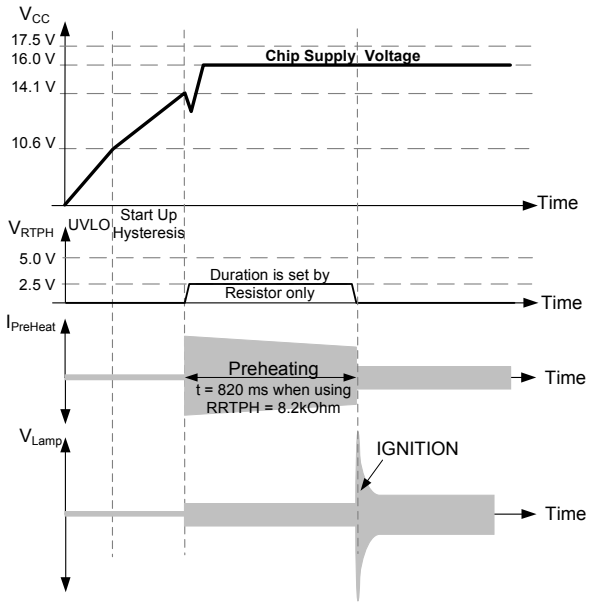


Figure 32: Start UP with Pre Heating

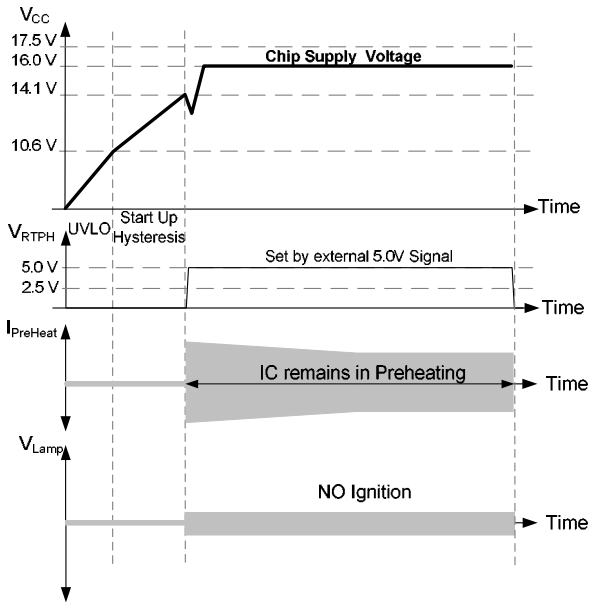


Figure 33: Start UP REMAINS in Pre Heating

2.8.2 Deactivation of the Filament Detection

In order to deactivate the filament detection of the low or high side filament, set the RES pin 12 or the LVS1 / LVS2 pin 13 / 14 to GND. In that case, the IC starts up into normal operation without checking the filaments e.g. when using an equivalent lamp resistive load instead of a load.

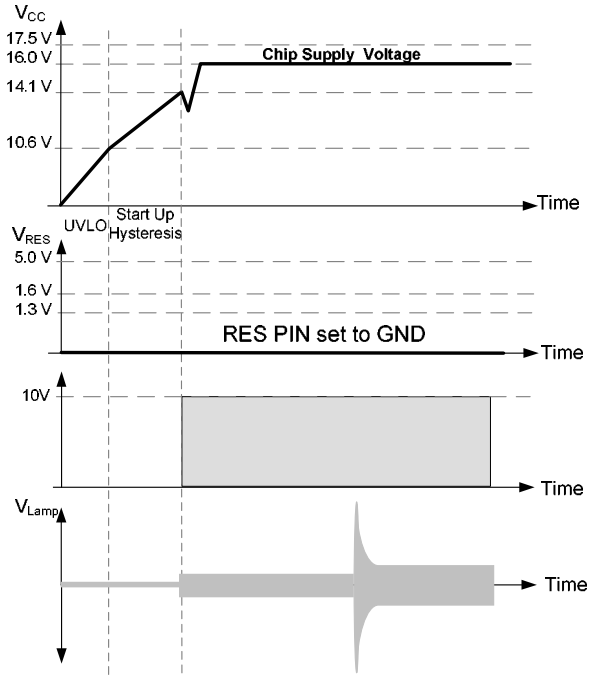


Figure 34: Deactivation via RES PIN

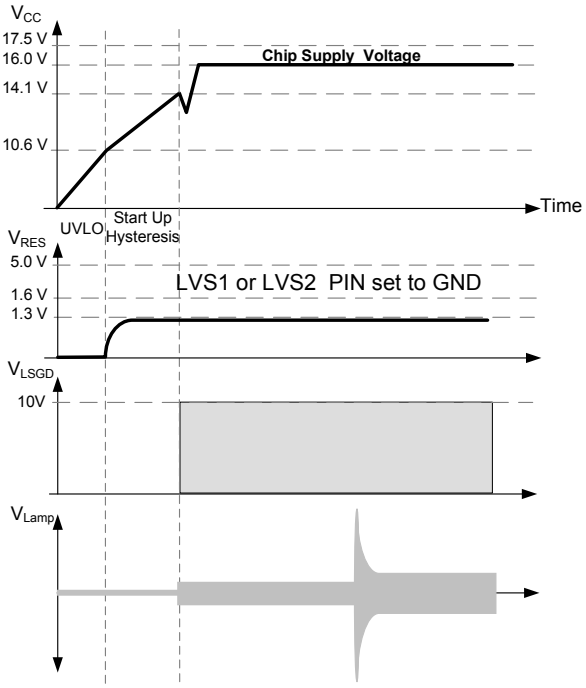


Figure 35: Deactivation via LVS1 / LVS2 PIN

Figure 34 shows the deactivation of the low and high side filament via set the RES pin 12 to GND.
Figure 35 shows the deactivation of the high side filament detection via set the LVS1 or LVS2 pin to GND.

Note

In case using just one path of a ballast design (single or dual lamp in series) one of the not used LVS pins has to be set to GND.

2.8.3 Built in Customer Test Mode (Clock Acceleration)

The built in customer test mode, supported by this IC, saves testing time for customers in terms of ballast end test. In that mode, the IC accelerates the internal clock in order to reduce the time of the 4 different procedures by the following factors (see Table 1).

Phase	Duration for Test [ms]	Acceleration Factor	Nominal Duration [ms]
Preheating	625	4	2500 (max)
Time Out Ignition	118.5	2	237
Pre Run Mode	41.7	15	625
EOL2	41.7	60	2500

Table 1: Specified Acceleration Factors

2.8.3.1 Enabling of the Clock Acceleration

The clock acceleration (Built in Customer Test Mode) is activated when the chip supply voltage exceeds V_{CC} > 14.1V and the voltages at the Run Frequency and Preheating Frequency pin are set to V_{RFRUN} = V_{RFPH} = 5.0 V (± 5 %) see Figure 35 “Enabling of Clock Acceleration”. A RES pin voltage of V_{RES} > 3.5 V up to 5.0 V (± 5 %) prevents a power up of the IC, the IC remains in a mode before powering up. This status is hold as long as the voltage at the RES pin is at V_{RES} > 3.5 V up to 5.0 V (± 5 %) – no power up. Note: after the activation of the clock acceleration mode, the voltage level of 5.0V at the Run Frequency and Preheating Frequency pin (V_{RFRUN} = V_{RFPH}) can be released.

2.8.3.2 Starting the Chip with accelerated Clock

In order to start the IC with an accelerated clock, set the voltage at the RES pin to GND (V_{RES} = 0 V). Figure 36 “Starting the Chip with an accelerated Clock”. The IC powers up the system and starts working with an accelerated clock. Now the duration of the different modes are accelerated by Factors shown in Table 1

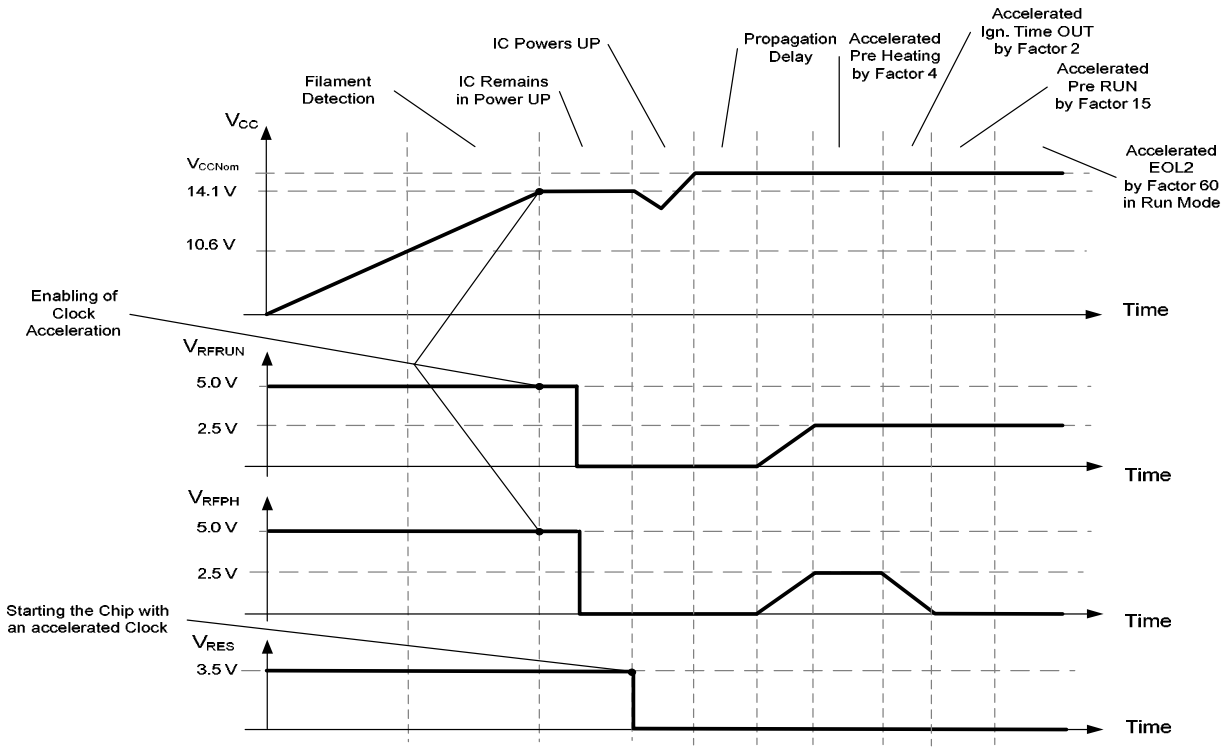
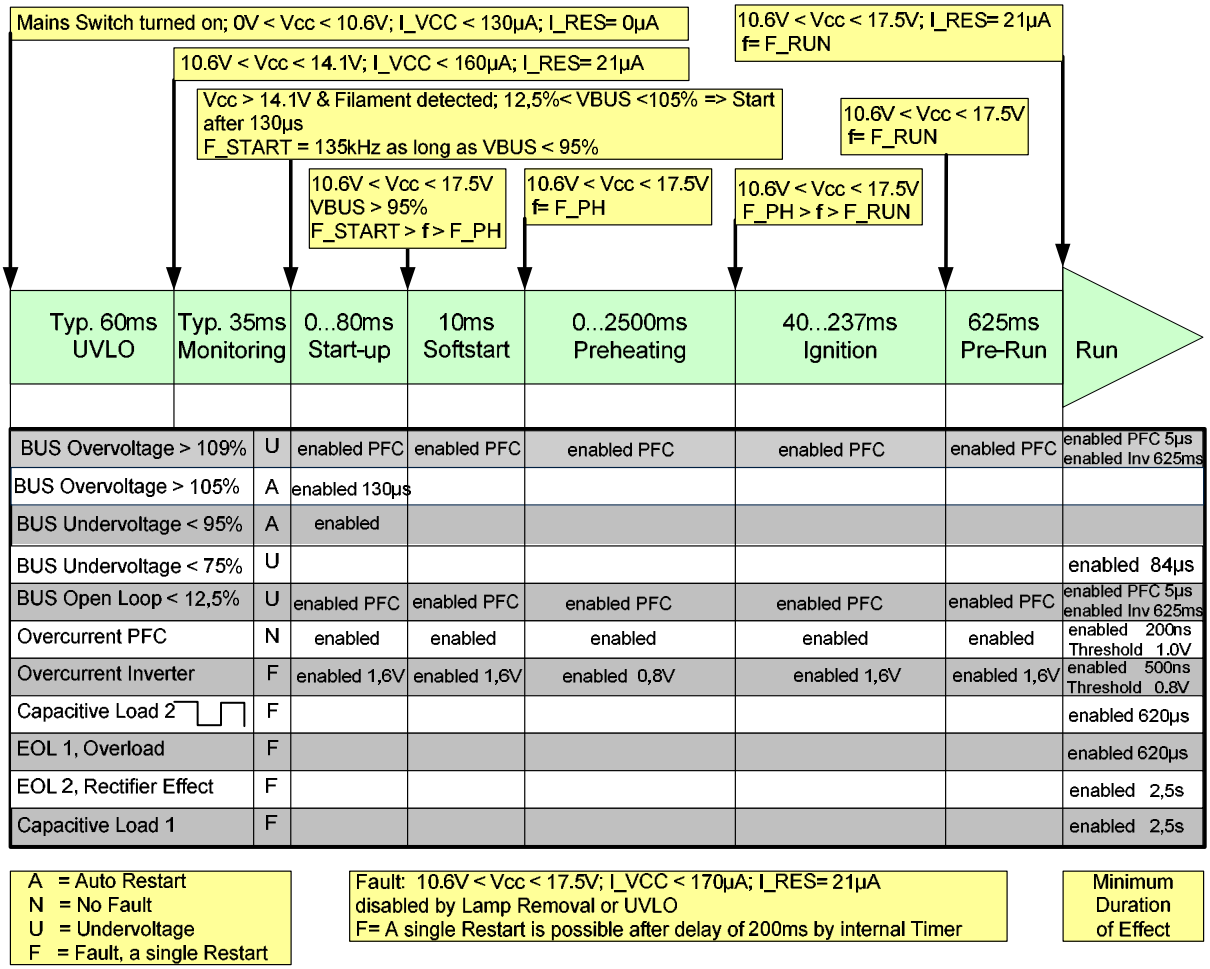


Figure 36: Clock Acceleration (Built in Customer Test Mode)

3 State Diagram

3.1 Features during different operating modes



BUS Overvoltage > 109%	U	enabled PFC	enabled PFC	enabled PFC	enabled PFC	enabled PFC	enabled PFC 5µs enabled Inv 625ms
BUS Overvoltage > 105%	A	enabled 130µs					
BUS Undervoltage < 95%	A	enabled					
BUS Undervoltage < 75%	U						enabled 84µs
BUS Open Loop < 12,5%	U	enabled PFC	enabled PFC	enabled PFC	enabled PFC	enabled PFC	enabled PFC 5µs enabled Inv 625ms
Overcurrent PFC	N	enabled	enabled	enabled	enabled	enabled	enabled 200ns Threshold 1.0V
Overcurrent Inverter	F	enabled 1,6V	enabled 1,6V	enabled 0,8V	enabled 1,6V	enabled 1,6V	enabled 500ns Threshold 0.8V
Capacitive Load 2	F						enabled 620µs
EOL 1, Overload	F						enabled 620µs
EOL 2, Rectifier Effect	F						enabled 2,5s
Capacitive Load 1	F						enabled 2,5s

A = Auto Restart
N = No Fault
U = Undervoltage
F = Fault, a single Restart

Fault: 10.6V < Vcc < 17.5V; I_VCC < 170µA; I_RES= 21µA
disabled by Lamp Removal or UVLO
F= A single Restart is possible after delay of 200ms by internal Timer

Minimum Duration of Effect

Figure 37: Monitoring Features during different operating Modes

3.2 Operating Flow of the Start UP Procedure into the Run Mode

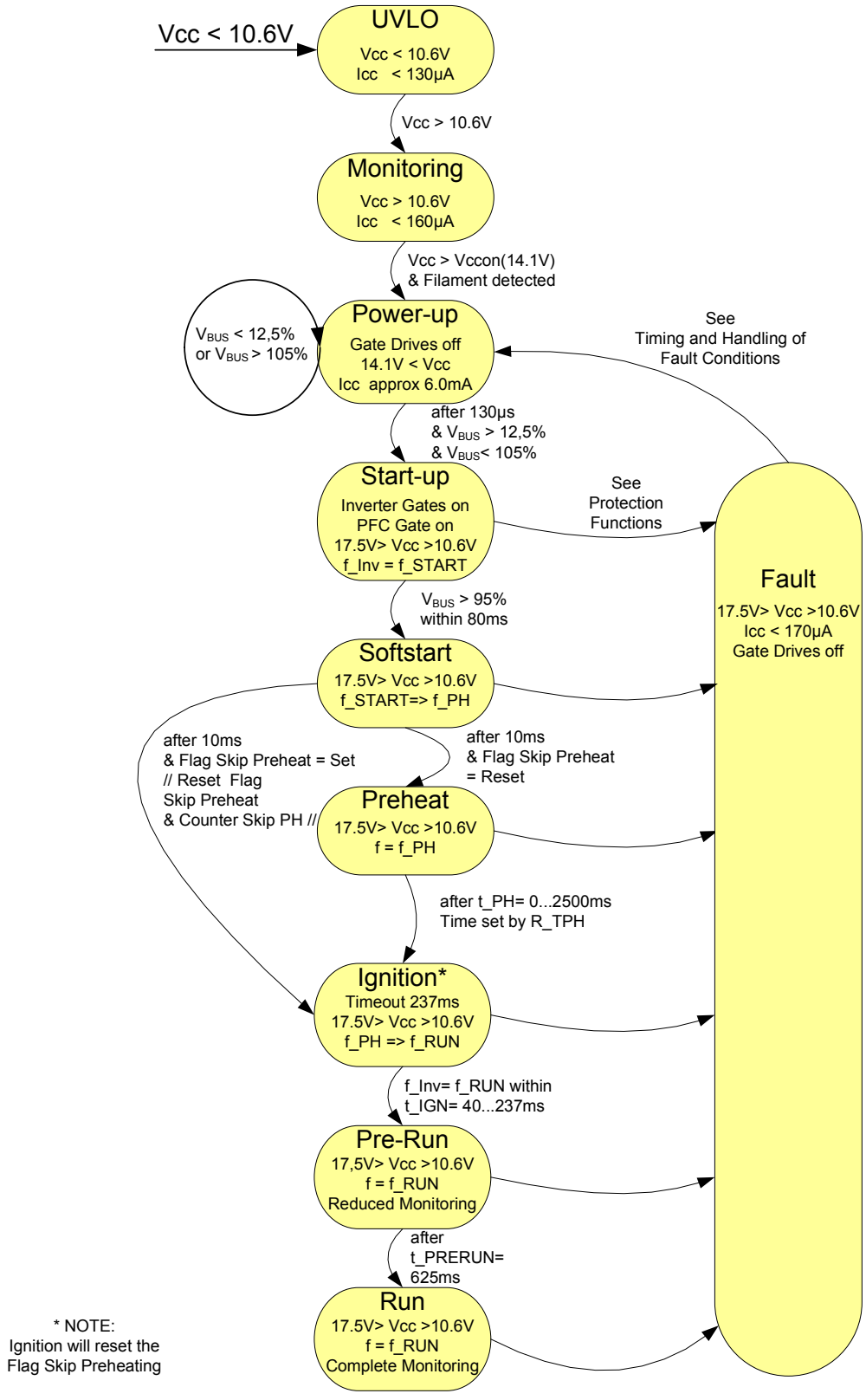


Figure 38: Operating Flow during Start-up Procedure

3.3 Auto Restart and Latched Fault Condition Mode

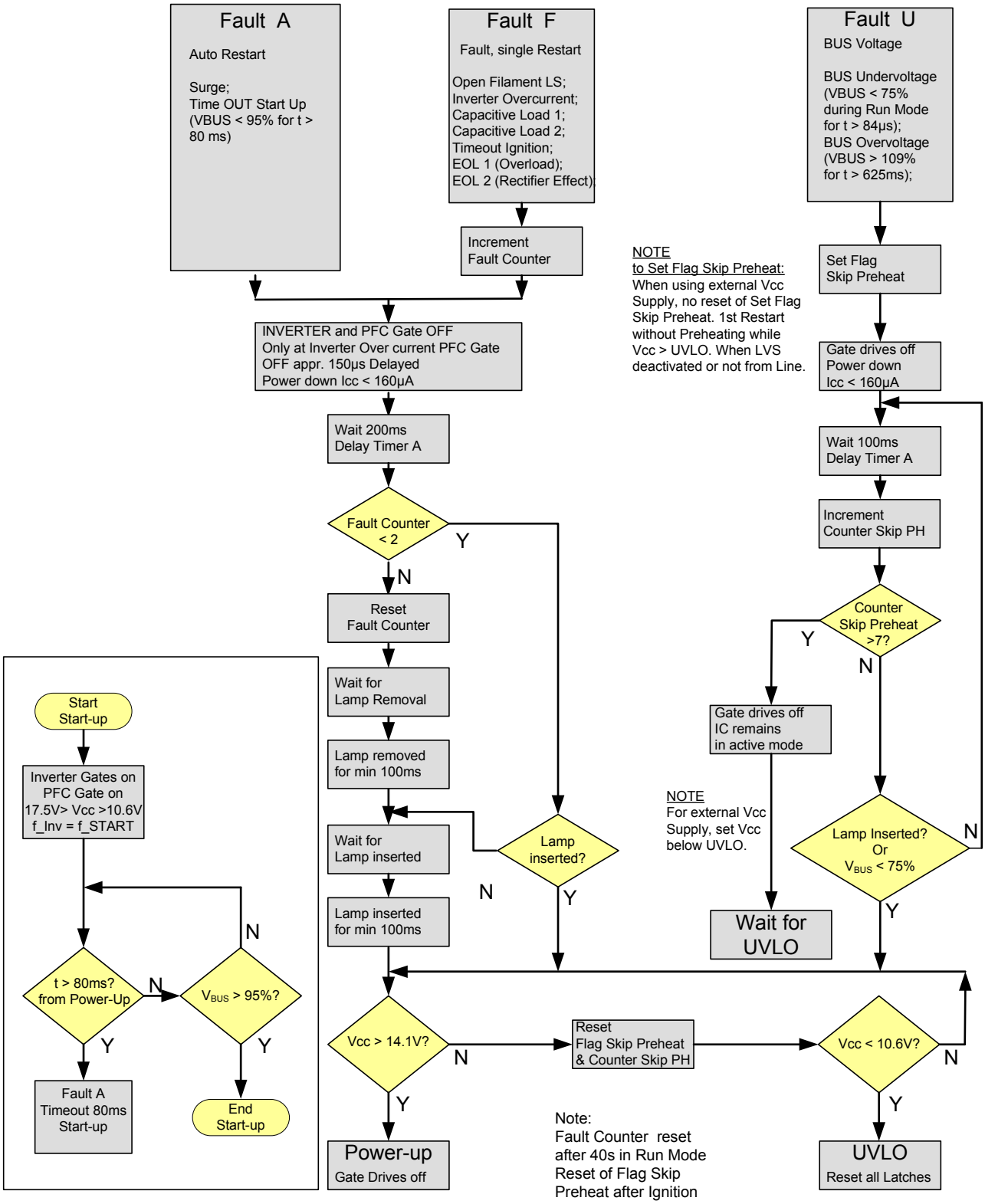


Figure 39: Operating Process during Start-up Mode and Handling of Fault Conditions

4 Protection Functions Matrix

Description of Fault	Characteristics of fault			Operating Mode Detection is active								Consequence
	Name of Fault	Type of fault	Minimum Duration of effect	Monitoring	Power-up 130µs	Start-up until VBUS > 95%	Softstart 10ms	Preheat Mode 0 – 2500ms	Ignition Mode 40 – 237ms	Pre-Run Mode 625ms	Run Mode	
Supply voltage Vcc < 14.1V before power up	Below start-up threshold	S	1µs	X								Prevents power up
Supply voltage Vcc < 10.6V after power up	Below UVLO threshold	S	5µs	X	X	X	X	X	X	X	X	Power down, Reset failure latch
Current into LVS1 pin < 18µA before power up	open filament HS	S	100µs	X								Prevents power up
Current into LVS2 pin < 18µA before power up	open filament HS	S	100µs	X								Prevents power up
Voltage at RES pin > 1.6V before power up	open filament LS	S	100µs	X								Prevents power up
Voltage at RES pin > 3.2V	open filament LS	F	620µs								X	Power down,latched Fault Mode, 1 Restart
Bus voltage < 12.5% of rated level 10µs after power up	Open Loop detection	S	1µs		X							Keep Gate drives off, re-start after Vcc hysteresis
Bus voltage < 12.5% of rated level	Open Loop detection	N	1µs			X	X	X	X	X	X	Stops PFC FET until VBUS > 12.5%
Bus voltage < 12.5% of rated level	Shut down option	U	625ms								X	Power down, restart when VBUS> 12.5%
Bus voltage < 75% of rated level add. shut down delay 120µs	Under-voltage	U	84µs								X	Power down, 100ms delay, restart, skip pre-heating max 7 times
Bus voltage < 95% of rated level during start-up	Timeout max start-up time	A	80ms			X						Power down, 200ms delay, restart
Bus voltage > 105% of rated level 10µs after power up	Over-voltage	S	5µs		X							Keep Gate drives off, re-start after Vcc hysteresis
Bus voltage > 109% of rated level in active operation	PFC Overvoltage	N	5µs			X	X	X	X	X	X	Stops PFC FET until VBUS< 105%
Bus voltage > 109% of rated level in active operation	Inverter Overvoltage	U	625ms								X	Power down, restart when VBUS<105%
+/- peak level of lamp voltage at Pin LVS above threshold	EOL 1 Overvoltage	F	620µs								X	Power down,latched Fault Mode, 1 Restart
DC level of lamp voltage above +/- threshold	EOL 2 Rect. Effect	F	2500ms								X	Power down,latched Fault Mode, 1 Restart
Capacitive Load 1	Cap Load 1 Idling	F	2500ms								X	Power down,latched Fault Mode, 1 Restart
Capacitive Load 2, operation below resonance	Cap.Load 2 Overload	F	620µs								X	Power down,latched Fault Mode, 1 Restart
Run frequency cannot be achieved	Timeout Ignition	F	237ms						X			Power down,latched Fault Mode, 1 Restart
Voltage at PFCCS pin > 1.0V	PFC Overcurrent	N	200ns			X	X	X	X	X	X	Stops on-time of PFC FET immediately
Voltage at LSCS pin > 0.8V	Inverter current lim	N	200ns						X			Activates Ignition control
Voltage at LSCS pin > 0.8V	Inverter overcurrent	F	500ns					X			X	Power down,latched Fault Mode, 1 Restart
Voltage at LSCS pin > 1.6V	Inverter overcurrent	F	500ns			X	X		X	X		Power down,latched Fault Mode, 1 Restart
Voltage at LSCS pin > 0.8V & VBUS > 109% (Surge)	Inverter overcurrent	A	500ns							X	X	Power down, restart when VBUS<109%
After jump into latched fault mode F wait			200ms	A single restart attempt after delay of internal timer								
Reset of failure latch in run mode after			40s	Reset of failure latch by UVLO or 40s in run mode								
S = Start-up condition, N = No Fault, A = Auto-Restart , U = Undervoltage												
F = Fault with a single Restart, a second F leads to a latched fault / **Note: all values @ typical 50 Hz mains frequency**												

5 Electrical Characteristics

Note: All voltages without the high side signals are measured with respect to ground (pin 4). The high side voltages are measured with respect to pin17. The voltage levels are valid if other ratings are not violated.

5.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 3 (VCC) and pin 18 (HSVCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
LSCS Voltage	V_{LSCS}	- 5	6	V	
LSCS Current	I_{LSCS}	- 3	3	mA	
LSGD Voltage	V_{LSGD}	- 0.3	V_{cc}+0.3	V	Internally clamped to 11V
LSGD Peak Source Current	$I_{LSGDsomax}$	- 75	5	mA	< 500ns
LSGD Peak Sink Current	$I_{LSGDsimax}$	- 50	400	mA	< 100ns
VCC Voltage	V_{VCC}	- 0.3	18.0	V	
VCC Zener Clamp Current	$I_{VCCzener}$	- 5	5	mA	IC in Power Down Mode
PFCGD Voltage	V_{PFCGD}	- 0.3	V_{cc}+0.3	V	
PFCGD Peak Source Current	$I_{PFCGDsomax}$	- 150	5	mA	< 500ns
PFCGD Peak Sink Current	$I_{PFCGDsimax}$	- 100	700	mA	< 100ns
PFCCS Voltage	V_{PFCCS}	- 5	6	V	
PFCCS Current	I_{PFCCS}	- 3	3	mA	
PFCZCD Voltage	V_{PFCZCD}	- 3	6	V	
PFCZCD Current	I_{PFCZCD}	- 5	5	mA	
PFCVS Voltage	V_{PFCVS}	- 0.3	5.3	V	
RFRUN Voltage	V_{RFRUN}	- 0.3	5.3	V	
RFPH Voltage	V_{RFPH}	- 0.3	5.3	V	
RTPH Voltage	V_{RTPH}	- 0.3	5.3	V	
RES Voltage	V_{RES}	- 0.3	5.3	V	
LVS1 Voltage	V_{LVS1}	- 6	7	V	
LVS1 Current1	I_{LVS1_1}	- 1	1	mA	IC in Power Down Mode
LVS1 Current2	I_{LVS1_2}	- 3	3	mA	IC in active Mode
LVS2 Voltage	V_{LVS2}	- 6	7	V	
LVS2 Current1	I_{LVS2_1}	- 1	1	mA	IC in Power Down Mode
LVS2 Current2	I_{LVS2_2}	- 3	3	mA	IC in active Mode

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
AUX Voltage	$\mathbf{V}_{AUX}$	- 0.3	5.3	V	
HSGND Voltage	$\mathbf{V}_{HSGND}$	- 900	900	V	Referring to GND
HSGND Voltage Transient	$d\mathbf{V}_{HSGND}/dt$	- 40	40	V/ns	
HSVCC Voltage	$\mathbf{V}_{HSVCC}$	- 0.3	18.0	V	Referring to HSGND
HSGD Voltage	$\mathbf{V}_{HSGD}$	- 0.3	$\mathbf{V}_{HSVCC}$+0.3	V	Internally clamped to 11V
HSGD Peak Source Current	$I_{HSGDsomax}$	- 75	0	mA	< 500ns
HSGD Peak Sink Current	$I_{HSGDsimax}$	0	400	mA	< 100ns
Junction Temperature	T_J	- 25	150	°C	
Storage Temperature	T_S	- 55	150	°C	
Maximum Power Dissipation	P_{TOT}	—	2	W	PG_DSO-19-1 T_{amb}=25°C
Thermal Resistance (2 Chips)	R_{thJA}	—	60	K/W	PG_DSO-19-1
Thermal Resistance (HS Chip)	R_{thJAHS}	—	120	K/W	PG_DSO-19-1
Thermal Resistance (LS Chip)	R_{thJALS}	—	120	K/W	PG_DSO-19-1
Soldering Temperature		—	260	°C	Wave Soldoldering[1)]
ESD Capability	V_{ESD}	—	2	kV	Human Body Model[2)]
Creepage Distance HS vs. LS		1.9	2.0	mm	
Rated Bus Voltage (95%)	$\mathbf{V}_{PFCVS95}$	2.33	2.43	V	

[1)] According to JESD22A111
[2)] According to EIA/JESD22-A114-B (discharging an 100 pF Capacitor through an 1.5kΩ series Resistor)

5.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	Max.		
HSVCC Supply Voltage	V_{HSVCC}	$V_{HSVCCOff}$	17.5	V	Referring to HSGND
HSGND Voltage	V_{HSGND}	- 900	900	V	Referring to GND
VCC Voltage @ 25°C	V_{VCC}	V_{VCCOff}	17.5	V	T_J = 25°C
VCC Voltage @ 125°C	V_{VCC}	V_{VCCOff}	18.0	V	T_J = 125°C
LSCS Voltage Range	V_{LSCS}	- 4	5	V	In active Mode
PFCVS Voltage Range	V_{PFCVS}	0	4	V	
PFCCS Voltage Range	V_{PFCCS}	- 4	5	V	In active Mode
PFZCD Current Range	I_{PFCZCD}	- 3	3	mA	In active Mode
LVS1, LVS2 Voltage Range	$V_{LVS1,LVS2}$	- 6	6 [1]	V	
LVS1, LVS2 Current Range	$I_{LVS1,LVS2}$	[2]	210	µA	IC Power Down Mode
LVS1, LVS2 Current Range	$I_{LVS1,LVS2}$	- 2.5	2.5	mA	IC active Mode
RFPH Frequency	$F_{RFPHrange}$	F_{RUN}	150	kHz	
RFPH Source Current Range	I_{RFPH}	- 500	0	µA	@ V_{RFPH} = 2.5V
RTPH Voltage Range	V_{RTPH}	0	2.5	V	
Junction Temperature	T_j	- 25	125	°C	
Adjustable Preheating Freq.	F_{RFPH}	F_{RFRUN}	150	kHz	Range set by RFPH
Adjustable Run Frequency	F_{RFRUN}	20	120	kHz	Range set by RFRUN
Adjustable Preheating Time	t_{RTPH}	0	2500	ms	Range set by RTPH
Set Resistor for Run Feq.	R_{RFRUN}	4	25	kΩ	
Set Resistor for Preheat Feq.	R_{RFPH}	4	—	kΩ	R_{RFRUN} parallel to R_{RFPH}
Set Resistor for Preheat Time	R_{RTPH}	0	25	kΩ	
Mains Frequency	f_{Mains}	45	65	Hz	NOTCH Filter Operation

[1] Limited by Maximum of Current Range at LVS1, LVS2
[2] Limited by Minimum of Voltage Range at LVS1, LVS2

5.3 Characteristics

5.3.1 Power Supply Section

Note: The electrical Characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from -25 °C to 125 °C. Typical values represent the median values, which are related to 25 °C. If not otherwise stated, a supply voltage of 15V and V_{HSVCC} = 15V is assumed and the IC operates in active mode. Furthermore, all voltages are referring to GND if not otherwise mentioned.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
VCC Quiescent Current1	$\mathbf{I}_{VCCqu1}$	—	90	130	µA	$\mathbf{V}_{VCC} = \mathbf{V}_{VCCOff} - 0.5V$
VCC Quiescent Current2	$\mathbf{I}_{VCCqu2}$	—	120	160	µA	$\mathbf{V}_{VCC} = \mathbf{V}_{VCCOn} - 0.5V$
VCC Supply Current [2]	$\mathbf{I}_{VCCSupply}$	—	4.2	6.0	mA	$\mathbf{V}_{PFCVS} > 2.725V$
VCC Supply Current in Latched Fault Mode	$\mathbf{I}_{VCCLatch}$	—	110	170	µA	$V_{RES} = 5V$
LSVCC Turn-On Threshold LSVCC Turn-Off Threshold LSVCC Turn-On/Off Hyst.	$\mathbf{V}_{VCCOn}$ $\mathbf{V}_{VCCOff}$ $\mathbf{V}_{VCCHys}$	13.6 10.0 3.2	14.1 10.6 3.6	14.6 11.0 4.0	V V V	 Hysteresis
VCC Zener Clamp Voltage	$\mathbf{V}_{VCCClamp}$	15.5	16.3	16.9	V	$\mathbf{I}_{VCC}$ = 2mA/V_{RES} = 5V
VCC Zener Clamp Current	$\mathbf{I}_{VCCZener}$	2.5	—	5	mA	$\mathbf{V}_{VCC}$ = 17.5V/V_{RES} = 5V
High Side Leakage Current	$\mathbf{I}_{HSGNDleak}$	—	0.01	2	µA	$\mathbf{V}_{HSGND}$ = 800V, $\mathbf{V}_{GND}$=0V
HSVCC Quiescent Current	$\mathbf{I}_{HSVCCqu1}$ [1]	—	170	250	µA	$\mathbf{V}_{HSVCC} = \mathbf{V}_{HSVCCOn} - 0.5V$
HSVCC Quiescent Current[2]	$\mathbf{I}_{HSVCCqu2}$ [1]	0.3	0.65	1.2	mA	$\mathbf{V}_{HSVCC} > \mathbf{V}_{HSVCCOn}$
HSVCC Turn-On Threshold HSVCC Turn-Off Threshold HSVCC Turn-On/Off Hyst.	$\mathbf{V}_{HSVCCOn}$ [1] $\mathbf{V}_{HSVCCOff}$ [1] $\mathbf{V}_{HSVCCHy}$ [1]	9.6 7.9 1.4	10.1 8.4 1.7	10.7 9.1 2.0	V V V	 Hysteresis
Low Side Ground	GND					

[1] Referring to High Side Ground (HSGND)
[2] With inactive Gate

5.3.2 PFC Section

5.3.2.1 PFC Current Sense (PFCCS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Turn – Off Threshold	$V_{PFCCSOff}$	0.95	1.0	1.05	V	
Over Current Blanking + Propagation Delay [1]	$t_{PFCCSOff}$	140	200	260	ns	
Leading Edge Blanking	$t_{Blanking}$	180	250	310	ns	Pulse Width when V_{PFCCS} > 1.0V
PFCCS Bias Current	$I_{PFCCSBias}$	- 0.5	—	0.5	µA	V_{PFCCS} = 1.5V

[1] Propagation Delay = 50ns

5.3.2.2 PFC Zero Current Detection (PFCZCD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Zero Crossing upper Thr. [1]	$V_{PFCZCDUp}$	1.4	1.5	1.6	V	
Zero Crossing lower Thr. [2]	$V_{PFCZCDLow}$	0.4	0.5	0.6	V	
Zero Crossing Hysteresis	$V_{PFCZCDHys}$	—	1.0	—	V	
Clamping of pos. Voltages	$V_{PFCZCDpclp}$	4.1	4.6	5.1	V	$I_{PFCZCDSink}$ = 2mA
Clamping of neg. Voltages	$V_{PFCZCDnclp}$	- 1.7	- 1.4	- 1.0	V	$I_{PFCZCDSource}$ = - 2mA
PFCZCD Bias Current	$I_{PFCZCDBias}$	- 0.5	—	5.0	µA	V_{PFCZCD} = 1.5V
PFCZCD Bias Current	$I_{PFCZCDBias}$	- 0.5	—	0.5	µA	V_{PFCZCD} = 0.5V
PFCZCD Ringing Su.[3] Time	$t_{Ringsup}$	350	500	650	ns	
Limit Value for ON Time Extension	$_{\Delta}t \times I_{ZCD}$	500	700	900	pAxs	

[1] Turn OFF Threshold
[2] Turn ON Threshold
[3] Ringing Suppression Time

5.3.2.3 PFC Bus Voltage Sense (PFCVS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
Trimmed Reference Voltage	$V_{PFCVSRef}$	2.47	2.50	2.53	V	± 1.2 %
Overvoltage turn Off (109%)	$V_{PFCVSRUp}$	2.68	2.73	2.78	V	
Overvoltage turn On (105%)	$V_{PFCVSLow}$	2.57	2.63	2.68	V	
Overvoltage Hysteresis	$V_{PFCVSHys}$	70	100	130	mV	4 % rated Bus Voltage
Under voltage (75%)	$V_{PFCVSUV}$	1.835	1.88	1.915	V	
Under voltage (12.5%)	$V_{PFCVSUV}$	0.237	0.31	0.387	V	
Rated Bus Voltage (95%)	$V_{PFCVS95}$	2.325	2.38	2.425	V	
PFCVS Bias Current	$I_{PFCVSBias}$	- 1.0	—	1.0	µA	V_{PFCVS} = 2.5V

5.3.2.4 PFC PWM Generation

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
Initial ON – Time [1]	$t_{PFCON_initial}$	—	4.0	—	µs	V_{PFCZCD} = 0V
Max. ON – Time [2]	t_{PFCON_max}	18	22.7	26	µs	0.45V < V_{PFCVS} < 2.45V
Switch Threshold from CritCM into DCM	t_{PFCON_min}	160	270	370	ns	
Repetition Time [1]	t_{PFCRep}	47	52	57	µs	V_{PFCZCD} = 0V
Off Time	t_{PFCOff}	42	47	52	µs	

[1] When missing Zero Crossing Signal
[2] At the Maxima of the AC Line Input Voltage

5.3.2.5 PFC Gate Drive (PFCGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	Typ.	max.		
PFCGD Low Voltage	$V_{PFCGDLow}$	0.4	0.7	0.9	V	I_{PFCGD} = 5mA
		0.4	0.75	1.1	V	I_{PFCGD} = 20mA
		- 0.2	0.3	0.6	V	I_{PFCGD} = -20mA
PFCGD High Voltage	$V_{PFCGDHigh}$	10.0	11.0	11.6	V	I_{PFCGD} = -20mA
		9.0	—	—	V	I_{PFCGD} = -1mA / V_{VCC} [1]
		8.5	—	—	V	I_{PFCGD} = -5mA / V_{VCC} [1]
PFCGD active Shut Down	$V_{PFCGASD}$	0.4	0.75	1.1	V	I_{PFCGD} = 20mA V_{VCC}=5V
PFCGD UVLO Shut Down	$V_{PFCGDuvlo}$	0.3	1.0	1.5	V	I_{PFCGD} = 5mA V_{VCC}=2V
PFCGD Peak Source Current	$I_{PFCGDSouce}$	—	- 100	—	mA	[2] + [3]
PFCGD Peak Sink Current	$I_{PFCGDSink}$	—	500	—	mA	[2] + [3]
PFCGD Voltage during sink Current	$V_{PFCGDHigh}$	11.0	11.7	12.3	V	$I_{PFCGDSinkH}$ = 3mA
PFC Rise Time	$V_{PFCGDRise}$	80	220	380	ns	2V > VLSGD > 8V [2]
PFC Fall Time	$V_{PFCGDFall}$	20	45	70	ns	8V > VLSGD > 2V [2]

[1] V_{VCC} = V_{VCCOff} + 0.3V
[2] R_{Load} = 4Ω and C_{Load} = 3.3nF
[3] The Parameter is not Subject to Production Test – verified by Design / Characterization

5.3.2.6 Auxiliary (AUX)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
AUX Voltage OFF Level	V_{AUXOff}	—	—	0.24	V	I_{AUX} = 1mA
AUX Voltage ON Level 1	V_{AUXOn1}	1.7	2.6	3.1	V	I_p = 0A [1]
AUX Voltage ON Level 2	V_{AUXOn2}	1.8	2.6	3.1	V	I_p = 1mA [1]
AUX Current	I_{AUX}	- 0.60	-0.45	- 0.3	mA	V_{AUX} = 1V / I_P = 0A

[1] I_P = the positive Current into PIN ZCD

5.3.3 Inverter Section

5.3.3.1 Low Side Current Sense (LSCS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Overcurrent Shut Down Volt.	$V_{LSCSOvC1}$	1.5	1.6	1.7	V	1)
Overcurrent Shut Down Volt.	$V_{LSCSOvC2}$	0.75	0.8	0.85	V	2)
Duration of Overcurrent	$t_{LSCSOvC}$	450	600	700	ns	
Capacitive Mode Det. Level 1	$V_{LSCSCap1}$	80	100	123	mV	During Run Mode
Capacitive Mode Duration 1	$t_{LSCSCap1}$	—	280	—	ns	3)
Capacitive Mode Det. Level 2	$V_{LSCSCap2}$	1.8	2.0	2.2	V	During Run Mode
Capacitive Mode Duration 2	$t_{LSCSCap2}$	—	50	—	ns	4)
Capacitive Mode Det. Level 3	$V_{LSCSCap3}$	- 120	- 100	- 77	mV	
Capacitive Mode Duration 3	$t_{LSCSCap3}$	—	280	—	ns	5)
LSCS Bias Current	$I_{LSCSBias}$	-1.0	—	1.0	µA	@ V_{LSCS} = 1.5V

1) Overcurrent Voltage Threshold active during: Start Up, Soft start, Ignition and Pre Run Mode
2) Overcurrent Voltage Threshold active during: Preheating and Run Mode
3) Active during 2nd 50% Duty Cycle of LSGD in Run Mode
4) Active during Turn ON of the HSGD in Run Mode
5) Active before Turn ON of the HSGD in Run Mode

5.3.3.2 Low Side Gate Drive (LSGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
LSGD Low Voltage	$V_{LSGDLow}$	0.4	0.7	1.0	V	I_{LSGD} = 5mA[5)]
		0.4	0.8	1.2	V	I_{LSGD} = 20mA[5)]
		- 0.3	0.2	0.5	V	I_{LSGD} = - 20mA (Source)
LSGD High Voltage	$V_{LSGDHigh}$	10.0	10.8	11.6	V	[1)]
		9.0	—	—	V	[2)]
		8.5	—	—	V	[3)]
LSGD active Shut Down	$V_{LSGDASD}$	0.4	0.75	1.1	V	V_{CC}=5V / I_{LSGD} = 20mA[5)]
LSGD UVLO Shut Down	$V_{LSGDUVLO}$	0.3	1.0	1.5	V	V_{CC}=2V / I_{LSGD} = 5mA[5)]
LSGD Peak Source Current	$I_{LSGDSource}$	—	- 50	—	mA	[4) + 6)]
LSGD Peak Sink Current	$I_{LSGDSink}$	—	300	—	mA	[4) + 6)]
LSGD Voltage during [5)]	$V_{LSGDHigh}$	—	11.7	—	V	$I_{LSGDsinkH}$ = 3mA
LSGD Rise Time	$t_{LSGDRise}$	80	220	380	ns	2V < V_{LSGD} < 8V[4)]
LSGD Fall Time	$t_{LSGDFall}$	20	35	60	ns	8V > V_{LSGD} > 2V[4)]

[1)] I_{LSGD} = - 20mA Source Current
[2)] V_{CCOFF} + 0.3V and I_{LSGD} = - 1mA Source Current
[3)] V_{CCOFF} + 0.3V and I_{LSGD} = - 5mA Source Current
[4)] Load: R_{Load} = 10Ω and C_{Load} = 1nF
[5)] Sink Current
[6)] The Parameter is not Subject to Production Test – verified by Design / Characterization

5.3.3.3 Inverter Control Run (RFRUN)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed Start – Up Frequency	$F_{StartUp}$	121.5	135	148.5	kHz	
Duration of Soft Start	$t_{SoftStart}$	9	11	13.5	ms	1)
RFRUN Voltage in Run Mode	V_{RFRUN}	—	2.5	—	V	@ 100µA<I_{RFRUN}<600µA
Run Frequency	F_{RFRUN}	49	50	51	kHz	R_{RFRUN} = 10kΩ
Adjustable Run Frequency	F_{RFRUN1}	—	20	—	kHz	I_{RFRUN}= - 100 µA
	F_{RFRUN2}	—	40	—	kHz	I_{RFRUN}= - 200 µA
	F_{RFRUN3}	—	100	—	kHz	I_{RFRUN}= - 500 µA
RFRUN max. Current Range	$I_{RFRUNmax}$	—	-1000	- 650	µA	@ V_{RFRUN} = 0V

1) Shift Start Up Frequency to Preheating Frequency

5.3.3.4 Inverter Control Preheating (RFPH, RTPH)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
RFPH Voltage Preheating	V_{RFPH}	—	2.5	—	V	V_{RFPH} = 0V in Run Mode
Preheating Frequency	F_{RFPH1}	97	100	103	kHz	R_{RFPH} = R_{RFRUN} = 10kΩ
RFPH max. Current Range	$I_{RFPHmax}$	—	-1000	- 550	µA	@ V_{RFPH} = 0V
Current for set Preh. Time	I_{RTPH}	—	- 100	—	µA	
Preheating Time	t_{RTPH1}	950	1000	1050	ms	R_{RTPH1} = 10kΩ
	t_{RTPH2}	50	100	150	ms	R_{RTPH2} = 1kΩ
	t_{RTPH3}	—	500	—	ms	R_{RTPH3} = 5kΩ
	t_{RTPH4}	—	2000	—	ms	R_{RTPH4} = 20kΩ
	t_{RTPH5}	—	2500	—	ms	R_{RTPH5} = 25kΩ

5.3.3.5 Restart after Lamp Removal (RES)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High Side Filament In Det.	V_{RES1}	1.55	1.60	1.65	V	UVLO, $V_{CC} < V_{CCON}$
	V_{RES2}	1.25	1.30	1.35	V	
	V_{RES3}	—	3.2	—	V	Run Mode
RES Current Source	I_{RES1}	- 53.2	-42.6	-32.0	µA	V_{RES} = 1V ; LVS1 = 5µA
	I_{RES2}	-44.2	-35.4	-26.6	µA	V_{RES} = 2V ; LVS1 = 5µA
	I_{RES3}	- 26.6	-21.3	- 16.0	µA	V_{RES} = 1V ; LVS1 = 30µA
	I_{RES4}	- 22.1	-17.7	-13.3	µA	V_{RES} = 2V ; LVS1 = 30µA

5.3.3.6 Lamp Voltage Sense (LVS1, LVS2)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Source Current before Startup	$I_{LVSSource}$	- 5.0	- 3.0	- 2.0	µA	V_{LVS} = 0V
Enable Lamp Monitoring	$V_{LVSEnable1}$	350	530	750	mV	[1]
Sink Current for Lamp Det.	$I_{LVSSink}$	8.0	12.0	18.0	µA	$V_{LVS} > V_{LVSClamp}$
Positive Clamping Voltage	$V_{LVSClamp}$	—	6.5	—	V	@ I_{LVS} = 300µA
AC EOLCurrent Threshold	$I_{LVSSourceAC}$	190	210	230	µApp	$I_{LVS} > I_{LVSEOLpp}$ EOL 1
Positive EOL Current Thr.	$I_{LVSDCPos}$	34	42	50	µA	$I_{LVS} > I_{LVSDCPos}$ EOL 2
Negative EOL Current Thr.	$I_{LVSDCNeg}$	- 50	- 42	- 34	µA	$I_{LVS} > I_{LVSDCNeg}$ EOL 2

[1] If $V_{LVS} < V_{LVS1Enable1}$ Monitoring is disabled

5.3.3.7 High Side Gate Drive (HSGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	typ.	max.		
HSGD Low Voltage	$V_{HSGDLow}$	0.02	0.05	0.1	V	I_{HSGD} = 5mA (sink)
		0.5	1.1	2.5	V	I_{HSGD} = 100mA (sink)
		- 0.4	- 0.2	- 0.05	V	I_{LSGD} = - 20mA (source)
HSGD High Voltage	$V_{HSGDHigh}$	9.7	10.5	11.2	V	V_{CCHS}=15V I_{HSGD} = - 20mA (source)
		7.8	—	—	V	$V_{CCHSOFF}$ + 0.3V I_{HSGD} = - 1mA (source)
HSGD active Shut Down	$V_{HSGDASD}$	0.05	0.22	0.5	V	V_{CCHS}=5V I_{HSGD} = 20mA (sink)
HSGD Peak Source Current	$I_{HSGDSource}$	—	- 50	—	mA	R_{Load} = 10Ω+C_{Load} = 1nF [1]
HSGD Peak Sink Current	$I_{HSGDSink}$	—	300	—	mA	R_{Load} = 10Ω+C_{Load} = 1nF [1]
HSGD Rise Time	$T_{HSGDRise}$	140	220	300	ns	2V < V_{LSGD} < 8V R_{Load} = 10Ω+C_{Load} = 1nF
HSGD Fall Time	$T_{HSGDFall}$	20	35	70	ns	8V > V_{LSGD} > 2V R_{Load} = 10Ω+C_{Load} = 1nF

[1] The Parameter is not Subject to Production Test – verified by Design / Characterization

5.3.3.8 Timer Section

Delay Timer 1	t_{TIMER1}	70	100	160	ms	For Lamp Detection
Delay Timer 2	t_{TIMER2}	74	84	94	ms	For V_{BUS} > 95%
Inverter Time	t_{Inv}	100	130	160	µs	
Inverter Dead Time Max	$t_{DeadMax}$	2.25	2.5	2.75	µs	
Inverter Dead Time Min	$t_{DeadMin}$	1.0	1.25	1.5	µs	
Δ Inverter Dead Time Max	$t_{DeadMax}$	- 200	—	200	ns	
Δ Inverter Dead Time Min	$t_{DeadMin}$	- 200	—	200	ns	
Min. Duration of Ignition	$t_{Ignition}$	34	40	48	ms	
Max. Duration of Ignition	$t_{NOIgnition}$	197	—	236	ms	
Duration of Pre – Run	t_{PRERUN}	565	625	685	ms	

5.3.3.9 Built in Customer Test Mode

Voltage at RTPH Pin	V_{RTPH}	0	V	Preheating Time = 0ms (Skipped Preheating)
Voltage at RTPH Pin	V_{RTPH}	5.0	V [1]	IC remains in Preheating
Voltage at LVS1 / LVS2 Pin	$V_{LVS1,2}$	0	V	Disables Lamp Voltage Sense
Voltage at RES Pin	V_{RES}	0	V	Disable the Filament Detection
Voltage at RFPH Pin	V_{RFPH}	5.0	V [1]	Built in Customer Test Mode - Clock Acceleration. Decreasing Time for the following Procedures. Preheating by Factor 4 Timeout Ignition by Factor 2 Pre RUN by Factor 15 EOL by 60
Voltage at RFRUN Pin	V_{RFRUN}	5.0	V [1]	
Voltage at V_{CC} Pin	V_{CC}	> 14.1	V	
Voltage at RES Pin	V_{RES}	0	V	

1) Tolerance for this voltage is: ± 5%

6 Application Example

6.1 Schematic Ballast 54W T5 Single Lamp

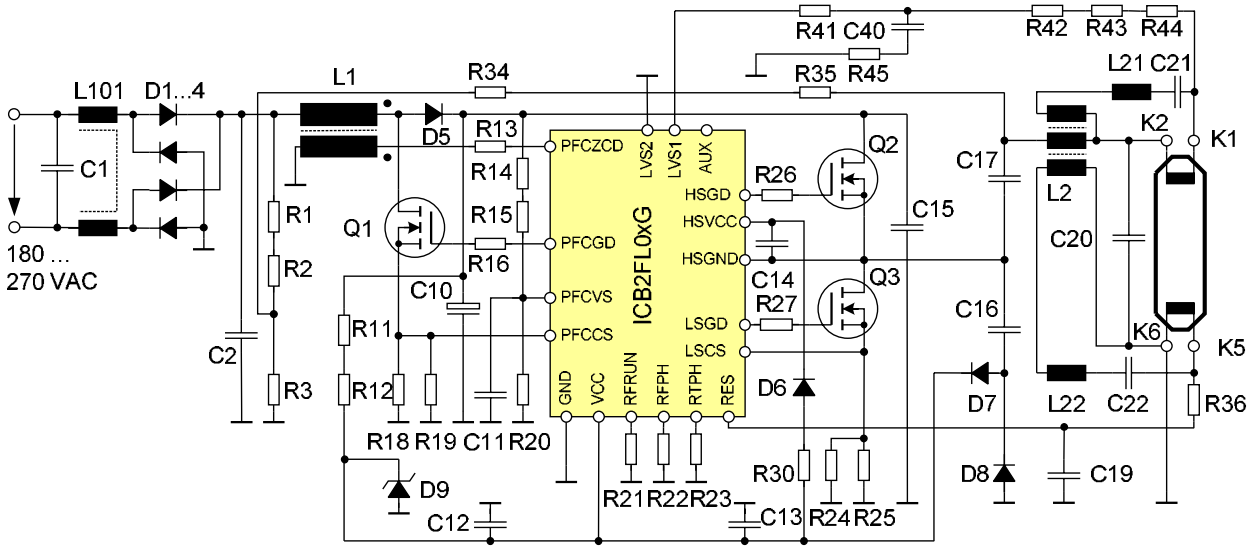


Figure 40: Application Circuit of Ballast for single Fluorescent Lamp Voltage Mode Preheating

6.2 Bill of Material

090402-1-L-54W-T5-FL2-VM **BOM**

54W T5, single Lamp, Voltage Mode Preheat				ICB2FL01G	Gen-2
Input Voltage 180VAC...270V AC				V_BUS= 412V	
					Package
F1	Fuse 1A fast	Wickmann	Typ 370		
	Fuse Holder				
K1/1	AC Input	B-Nr: 250-203			
K1/2	AC Input				
K1/3	PE				
K2/1	not connected	B-Nr: 250-203			
K2/2	High Side Filament				
K2/3	High Side Filament				
K3/1	Low Side Filament	B-Nr: 250-203			
K3/2	Low Side Filament				
K3/3	not connected				
IC1	ICB2FL01G	Infineon	>GE834	SO-20	
Q1	SPD03N60C3	Infineon		D-Pack	
Q2	SPD03N60C3	Infineon		D-Pack	
Q3	SPD03N60C3	Infineon		D-Pack	
Q4	not assembled	Infineon		SOT-223	
D1…4	S1M	Fairchild	(1000V/1A/2µs)	DO-214AC	
D5	MURS160T3	ON Semi	(600V/1A/75ns)	SMB	
D6	BYG26J	Philips	(600V/1A/30ns)	SOD124	
D7	BYG22D	Philips	(200V/1A/25ns)	DO214	
D8	BYG22D	Philips	(200V/1A/25ns)	DO214	
D9	BZX284C16	Philips		SOD110	
D10	not assembled				
D11	not assembled				
DR12	110kΩ				
D13	not assembled				
D61	not assembled	Philips		SOD110	
L101	2x68mH/0,6A	Epcos	B82732F2601B001		
L1 PFC	1,58mH	Epcos	105turns/10turns	EFD25/13/9	
	total gap= 1.1mm	2 pcs	B78326P7373A005	T1904	
L 2	1,46mH	Epcos	182turns	EFD25/13/9	
	total gap= 2mm	2 pcs	B78326P7374A005	T1905	
L 21	100µH	Epcos	B82144B1104J000	RM5	
L 22	100µH	Epcos	B82144B1104J000	RM5	
L 23	not assembled	Epcos	B82144B1104J000	RM5	
C1	220nF/X2/305V	Epcos	B32922C3224M000	RM15	
C2	33nF/630V/MKT	Epcos	B32521N8333K000	RM10	
C3	3,3nF/Y2-RM10	Epcos	B32021A3332	RM10/15	
C4	220nF/X2/305V	Epcos	B32922C3224M000	RM15	
C5	not assembled	Epcos	B32529C8102K000	RM5	
C10	10µF/450V	Epcos	B43888A5106M000	single ended	
C11	2,2nF/50V			.0805	
C12	100nF/50V			.0805	
C13	1µF/63V/MKT	Epcos	B32529C0105K000	RM5	
C14	68nF/50V	Epcos		.0805	
C15	33nF/630V/MKT	Epcos	B32521N8333K000	RM10	
C16	1nF/630V/MKT	Epcos	B32529C8102K000	RM5	
C17	100nF/630V	Epcos	B32612A6104K008	RM15	
C18	not assembled			RM7,5	
C19	22nF/50V			.0805	
C20	4,7nF/1600V/MKP	Epcos	B32612-J1472J008	RM15	
C21	22nF/400V/MKT	Epcos	B32620A4223J000	RM7,5/10	
C22	22nF/400V/MKT	Epcos	B32620A4223J000	RM7,5/10	
C23	not assembled	Epcos	B32620A4223J000	RM7,5/10	
C24	not assembled	Epcos	B32612-J1472J008	RM15	
C25	not assembled	Roederstein		RM7,5	
C40	220nF/25V			.0805	

		Package
R1	470kΩ	.1206
R2	470kΩ	.1206
R3	not assembled	.1206
R4	not assembled	.1206
R402	not assembled	.1206
R403	not assembled	.1206
R11	470kΩ	.1206
R12	470kΩ	.1206
R13	33kΩ	.1206
R14	820kΩ	.1206
R15	820kΩ	.1206
R16	22Ω	.0805
R18	1Ω	.1206
R19	not assembled	.1206
R20	10kΩ	.0805
R21	11kΩ (45,5kHz!)	.0805
R22	8,2kΩ (106,4kHz!)	.0805
R23	10kΩ (1000ms!)	.0805
R24	0,68Ω	.1206
R25	0,68Ω (Σ 0,34Ω)	.1206
R26	22Ω	.1206
R27	22Ω	.0805
R30	33Ω	.1206
R34	150kΩ	.1206
R35	150kΩ	.1206
R36	56kΩ	.1206
R36A	0Ω	.1206
R61	0Ω	.1206

connect LVS2 (pin14) to GND		
R41	68kΩ	.1206
R42	68kΩ	.1206
R43	68kΩ	.1206
R44	68kΩ	.1206
R45	6,8kΩ	.1206
R61	0Ω	.0805
	EOL1 threshold	
167Vpeak x 1.5=250V peak		
	5W	

6.3 Multi Lamp Ballast Topologies

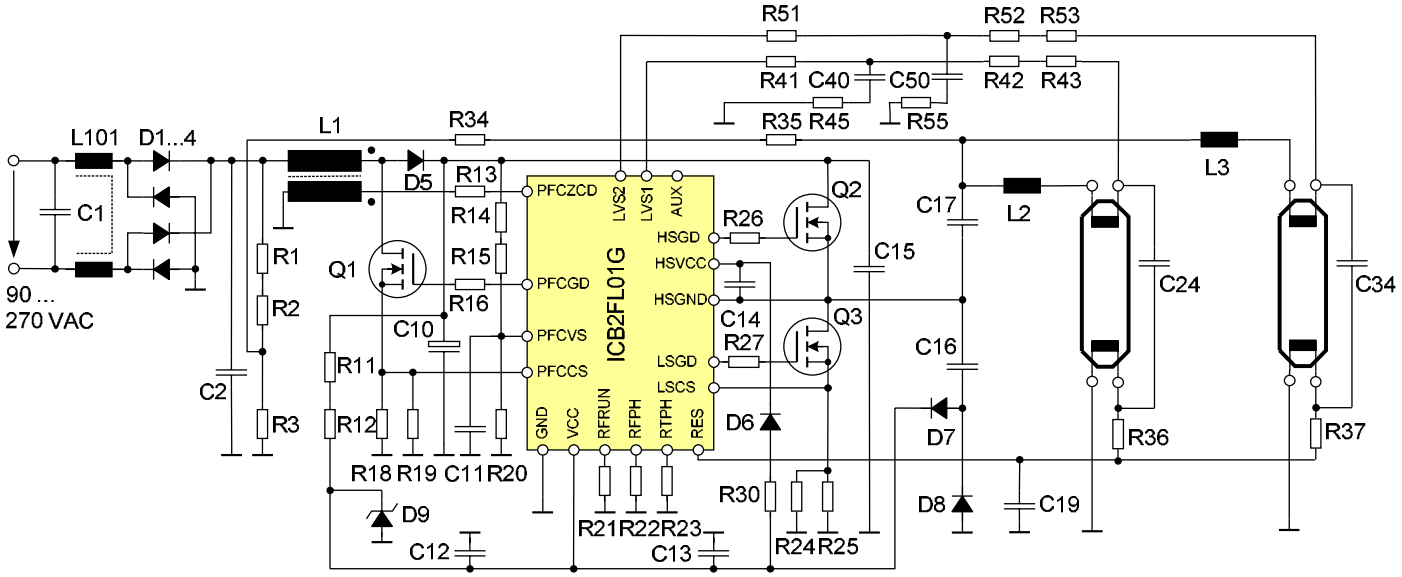


Figure 41: Parallel 2 Lamp Ballast Circuit with Current Mode Preheating

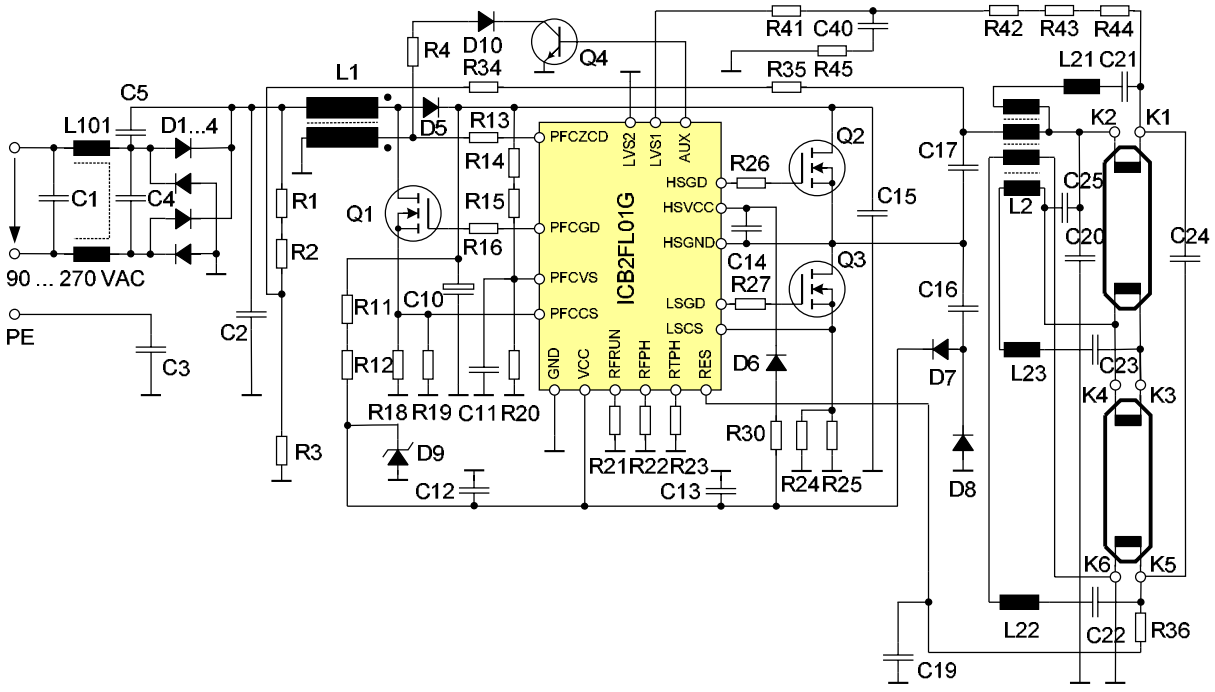


Figure 42: Serial 2 Lamp Ballast Circuit with Voltage Mode Preheating

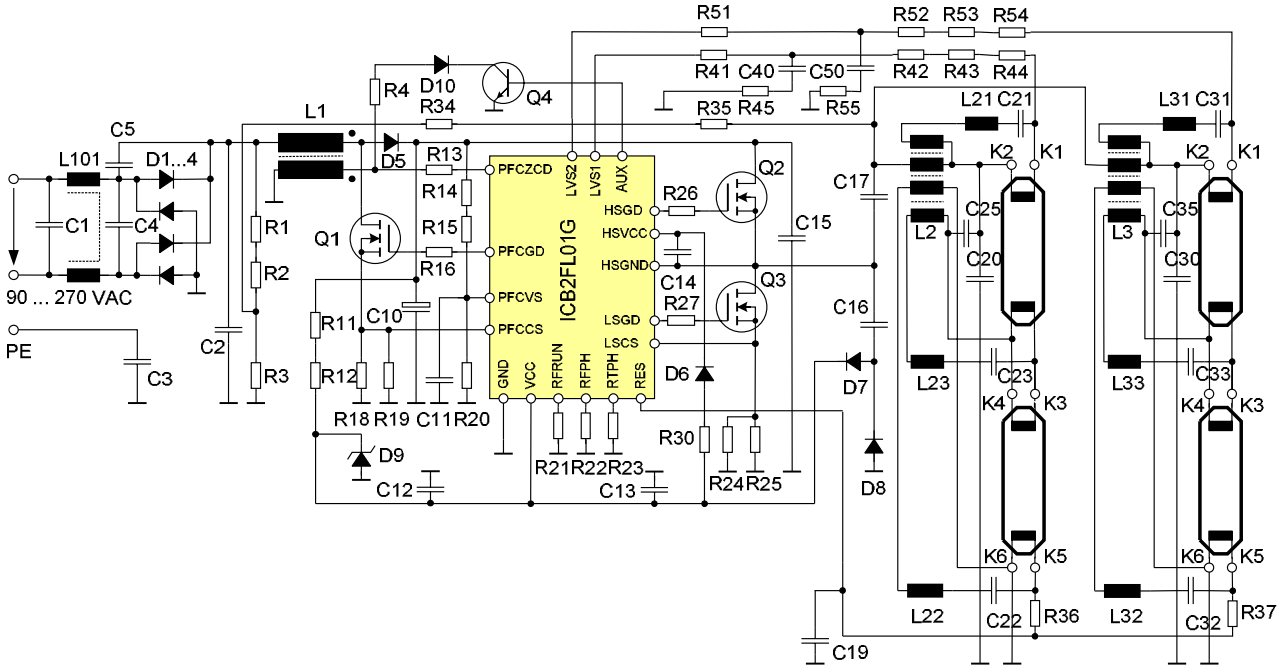
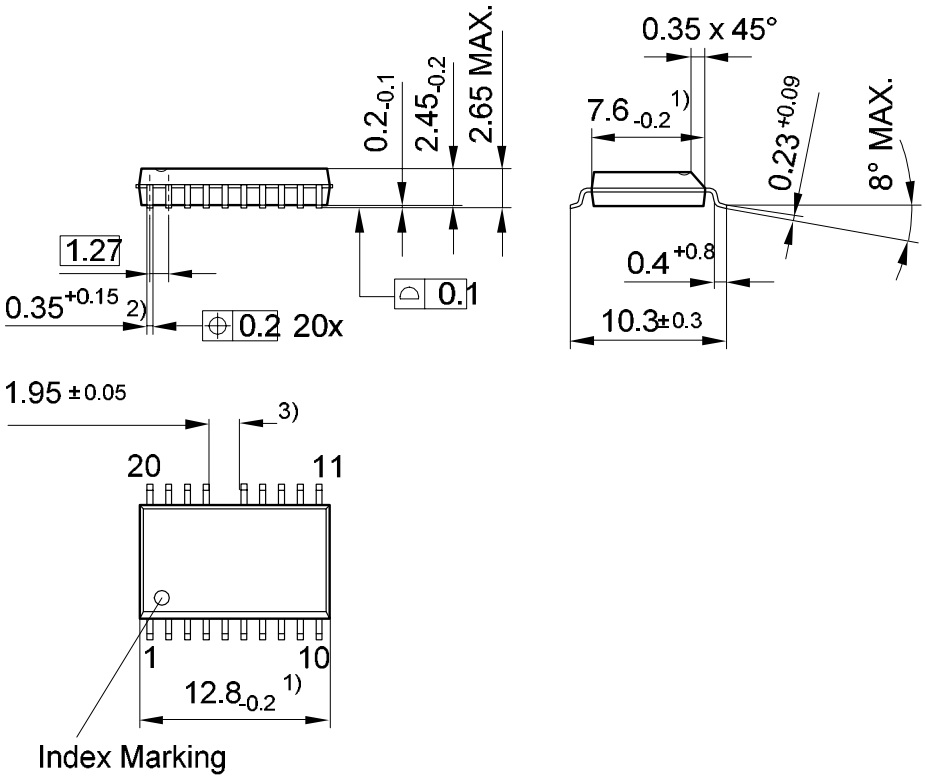


Figure 43: 4 Lamp Ballast Circuit with Voltage Mode Preheating

7 Package Outlines



1) Does not include plastic or metal protrusions of 0.15 max per side
2) Does not include dambar protrusion of 0.05 max per side
3) Creepage distance between High-Side and Low-Side - Pins

Figure 44: Package Outline with Creepage Distance