TEXAS INSTRUMENTS

TAS3001C

Digital Audio Processor

Data Manual

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DAV−Audio Products

SLAS226B

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

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1 Introduction

1.1 Description

The TAS3001 is a high-quality, fixed-function, 32-bit digital audio processor. This device contains a number of built-in processing functions including mixing/scaling of two digital inputs, bass and treble controls, six cascaded stereo high-precision, limit-cycle-free, second-order IIR filters, soft volume, and soft mute.

These functions can be controlled by specifying the desired operating parameters using the I^2C interface.

The TAS3001 architecture preserves high-quality audio by using a 32-bit data path, 24×32-bit multiplies, and up to 56 bits of precision for some internal calculations. By using 24-bit filter coefficients, the TAS3001 can implement practically any second-order IIR filter with outstanding fidelity.

1.2 Overview

The TAS3001 is a 32-bit audio signal processor that provides mixing of two digital inputs and digital parametric equalization. In addition, this device provides high-quality, soft digital volume, bass, and treble controls. All control parameters are uploaded through the I^2C port from an outside MCU.

The TAS3001 has four audio processing blocks as shown in Figure 1−1.

- Two digital stereo audio inputs that can be scaled and mixed prior to processing.
- Parametric EQ that consists of six cascaded independent second-order IIR filters for each of the left and right independent channels. Each filter has five 24-bit coefficients that can be configured into many different filter functions, such as band-pass, high-pass, low-pass, shelves, notch, all-pass, high-/low-pass with shelf, etc.
- Digital bass and treble controls
- Digital soft volume and mute

The TAS3001 device uses a system clock that is generated by the internal phase-locked loop (PLL). An external master clock (MCLK) of 256 times the sampling frequency provides the reference clock for the PLL.

The TAS3001 device supports several serial data formats (I^2S, left justified, right justified) with data word lengths of 16, 18, or 20. The sampling frequencies (f_S) that are supported include 32 kHz, 44.1 kHz, 48 kHz and 96 kHz.

1.3 Features

1.3.1 Stereo Digital Audio Processing

- Supports nine serial data formats. Receive and transmit serial data formats may be different.
- Programmable two-input digital mixer
- Programmable six-band digital parametric EQ
- Programmable digital bass and treble controls
- Programmable digital volume control with soft mute
- 108-dB dynamic range
- Sample rates from 32 kHz to 96 kHz

1.3.2 Interfaces

- Two serial digital input channels
- Single serial digital output channel
- Serial I^2C control channel

1.3.3 Electrical and Physical

- Single 3.3-V power supply
- 28-pin PW package
- Low-power standby

1.4 Applications

1.4.1 Digital Audio Controls

The TAS3001 can be used to provide a high-quality digital system control of volume, bass, treble, and parametric equalization.

1.4.2 Equalization

The TAS3001 can be used to perform parametric equalization to correct the frequency response of loudspeakers or microphones. The TAS3001 corrects the response by applying filters to compensate for the response irregularities of the transducers.

1.4.3 Loudspeaker Active Crossovers

The TAS3001 can be used to implement an active crossover for multi-way loudspeaker systems.

1.5 Functional Block Diagram

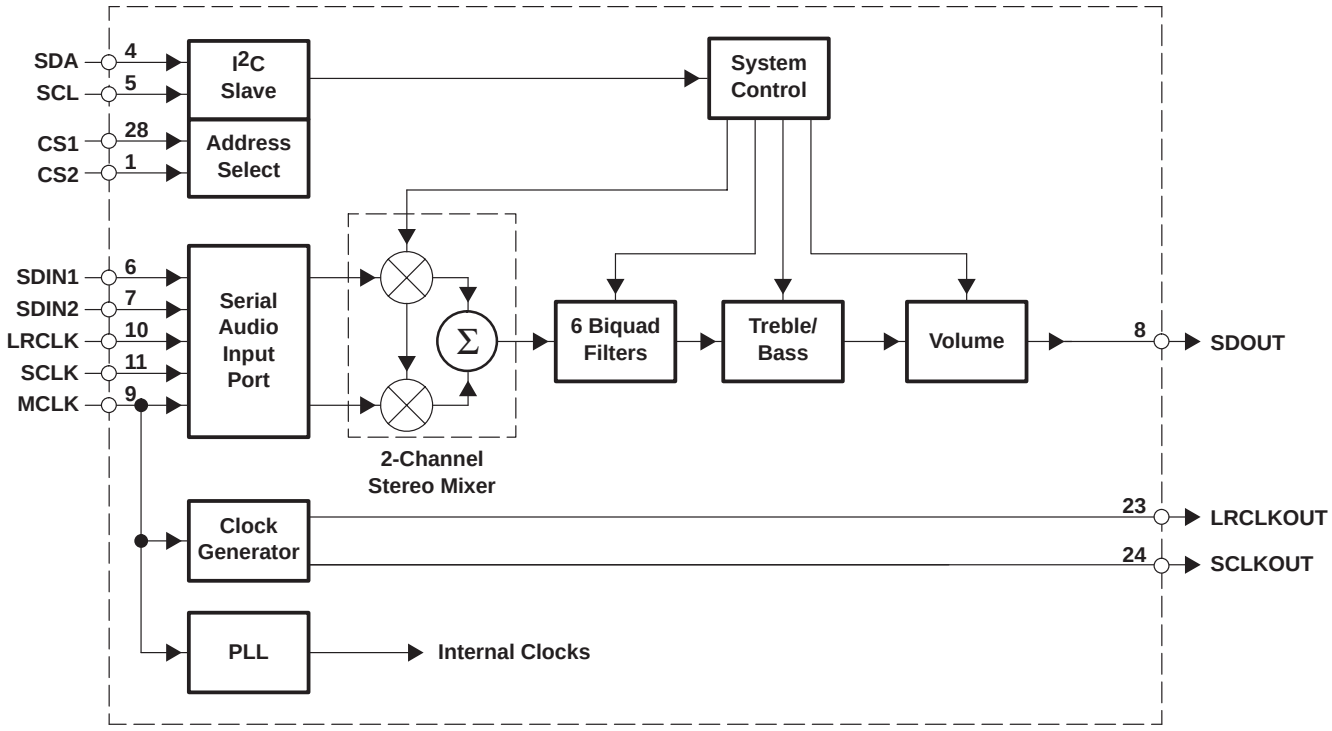


Figure 1−1. TAS3001 Signal Flow

Figure 1−1 shows the signal flow from the inputs (SDIN1 and SDIN2) though each processing stage to the output (SDOUT) where it is passed to an external DAC, digital amplifier, or other subsequent digital data processing stage.

Each of these audio processing functions is discussed in more detail in the following sections.

1.6 Mixing/Input Scaling

The TAS3001 is equipped with a dual-input stereo digital mixer. This mixer permits each input to scaled (−∞ to +18 dB) independently. A stereo sum of the scaled results is produced.

1.7 High-Precision, Second-Order Biquad Filter Structure

The TAS3001 has six cascaded biquad filters for the left and right channels to permit parametric equalization and filtering of the input signal. Each biquad is able to specify a wide variety of first- and second-order filter types, including high-pass, low-pass, band-pass, band-block, notch, and all-pass filter types. Examples of a few of the filters that can be implemented by the TAS3001 shapes are illustrated in Figure 1−2 though Figure 1−6.

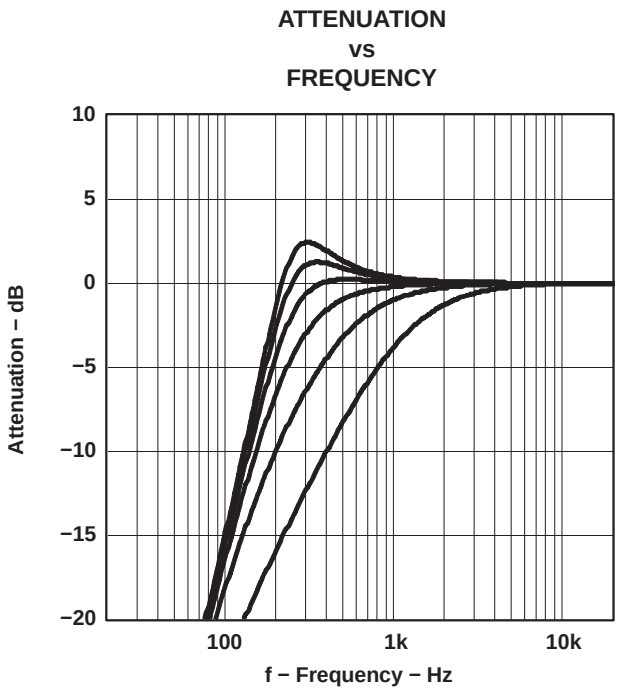


Figure 1−2. Examples of High-Pass Filters

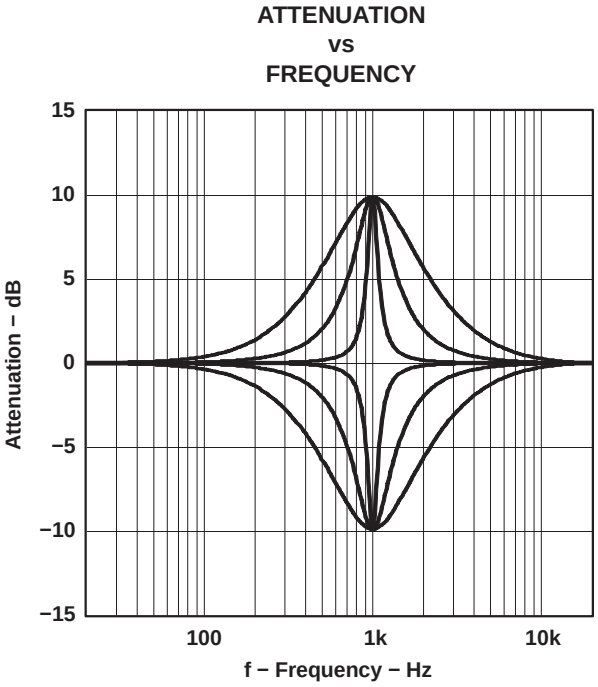


Figure 1−3. Examples of Equalization Filters

The biquad structure is of the form:

$$H(z) = \frac{b_0 + b_1 Z^{-1} + b_2 Z^{-2}}{1 + a_1 Z^{-1} + a_2 Z^{-2}}$$

Coefficients are downloaded to the TAS3001 registers in 4.20 format.

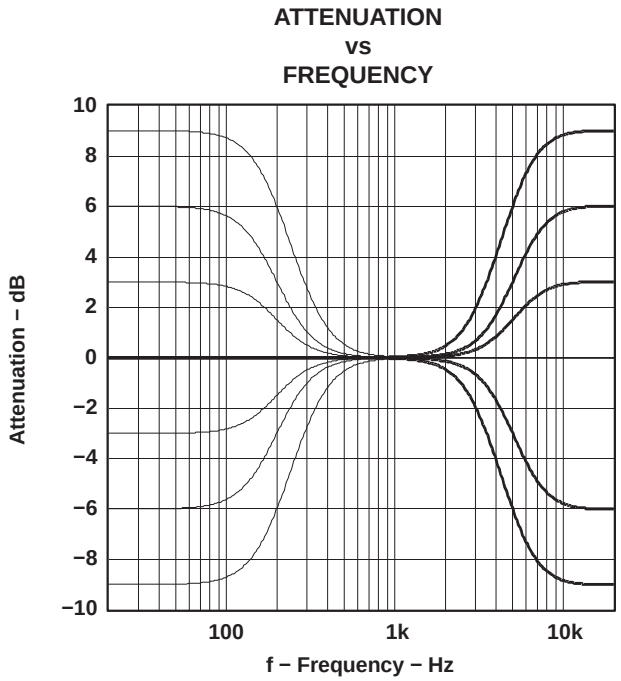


Figure 1−4. Bass and Treble Shelves

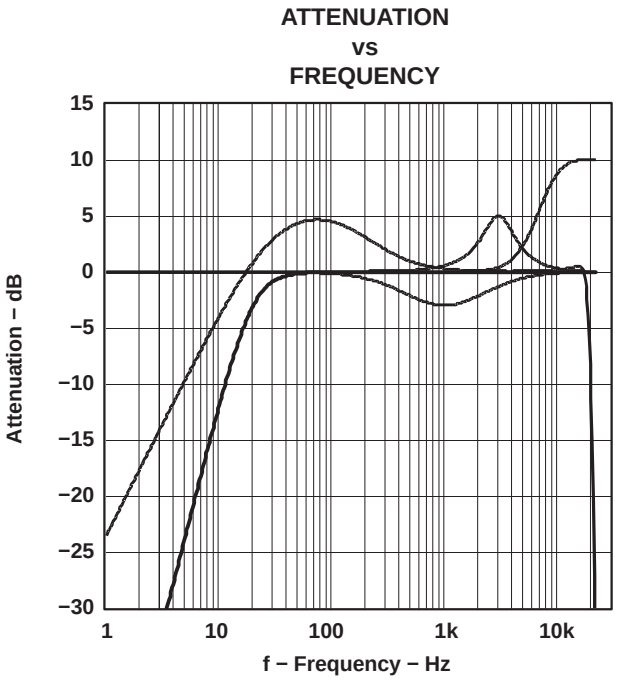


Figure 1−5. Multiple Filter Response

The TAS3001 provides a zero-input limit-cycle-free second-order IIR filtering structure that implements a direct form I filter structure. This architecture preserves high-quality audio by using a 32-bit data path, 24 × 32-bit multiplies, and 56 bits of precision for some internal calculations. By using 24-bit filter coefficients, the TAS3001 can implement practically any second-order IIR filter with outstanding fidelity.

Texas Instruments has several tools that provide a powerful and flexible means to develop applications using the TAS3001. Chapter 8 provides examples of how the TAS3001 can be used to meet various system needs.

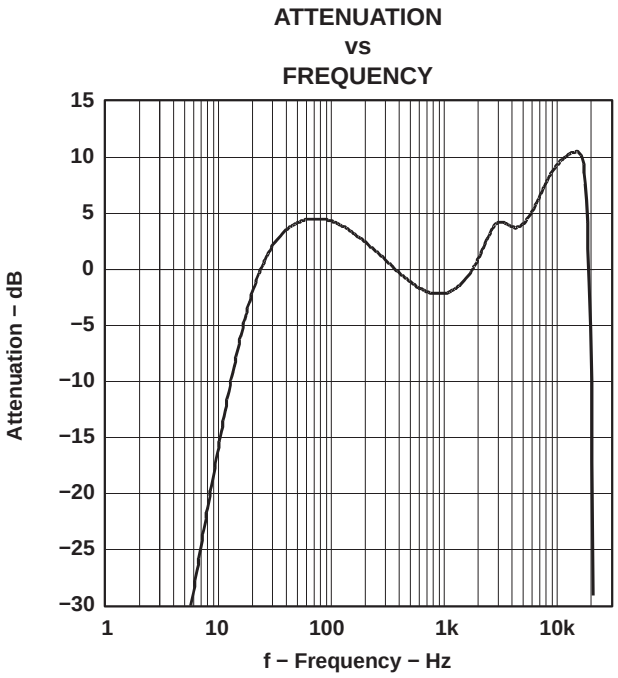


Figure 1−6. Combed Response of the Multiple Filters

1.8 Bass and Treble Controls

The TAS3001 has bass and treble controls that can be adjusted dynamically. These controls can be adjusted throughout their entire range of 18 dB to –18 dB without experiencing any pops, clicks, or other audible artifacts. This permits the user to have a listening experience much like what is experienced when adjusting high-quality analog controls.

Figure 1−7 shows the response for the bass and treble filters plotted at 3-dB intervals for 44.1-kHz sample-rate data.

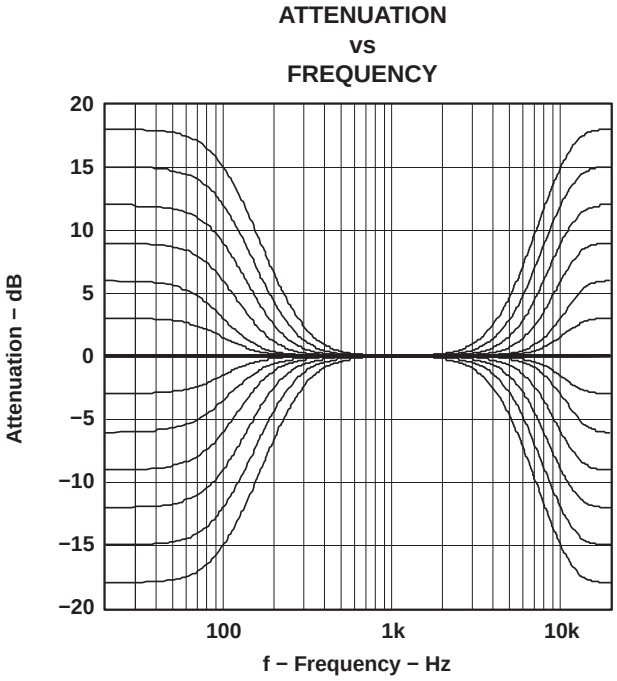


Figure 1−7. Bass and Treble Filters

1.9 Soft Volume and True Soft Mute

The TAS3001 contains a Texas Instruments proprietary soft volume update. This allows a smooth and pleasant-sounding change from one volume level to another over the entire range of volume (18 dB to mute). The volume is adjustable by downloading a 4.20 gain coefficient through the I^2C interface.

Mute is implemented by loading all zeros in the volume control register. This causes the volume to ramp down over 2048 samples to a final output of zero (−∞ dB).

1.10 Reliability and Flexibility of Digital Filtering

Digital filtering provides outstanding consistency, reliability, and flexibility. Once a digital filter is designed and tested in the system, it continues to perform in the same manner without change. Because digital filters are computed, their performance is exceedingly consistent and does not change due to variations in component matching, tolerances, environmental conditions, aging, or the effects of moisture and dust. Analog filters, however, are affected by all of these. The performance of analog filters can be improved, in part, by using high-quality precision components but this comes with a higher comparable cost.

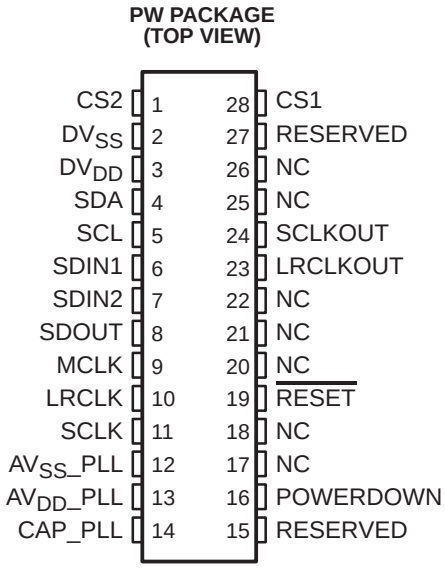
One of the greatest strengths of a digital filter is its flexibility. Each filter is completely specified by five 24-bit coefficients. By modifying the value of one or more of the filter coefficients, both the filter value and filter type are changed. In a system, these modifications produce different crossover curves, different equalization curves, different sound effects (by changing the relative phase of the left and right loudspeakers) or different user graphical equalization settings.

Attempting similar changes in an analog filter would require component changes and potentially a new circuit layout. The flexibility of digital filtering provides a particular advantage to digital equalization. Because of its programmability, a single design using digital filtering can provide a wide range of filtering functions. As a result, this one design can span a number of applications.

For a product that is in production, digital filtering can permit equalization changes with minimal cost impact because of this programmability.

One concern about digital filters is that some implementations have been prone to zero-input limit cycles. This is a condition where the filter oscillates at a low level when no signal is presented. In a digital audio system, this condition may present itself as a tone or low-level noise. The TAS3001 has a patent-pending technique to combat this problem.

1.11 Pin Assignments



NC − No internal connection

Figure 1−8. TAS3001 Pin Location Diagram

1.12 Pin Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
AV_{DD}_PLL	13	I	Analog power supply for the PLL
AV_{SS}_PLL	12	I	Analog ground for the PLL
CAP_PLL	14	I	C1 = 1500 pF // R1 = 27 Ω + C2 = 0.068 μF (recommended)
CS1	28	I	I^2C address bit A0; low = 0, high = 1
CS2	1	I	I^2C address bit A1; low = 0, high = 1
DV_{DD}	3	I	Digital power supply
DV_{SS}	2	I	Digital ground
LRCLK	10	I	I^2S left/right clock sampling frequency (f_S)
LRCLKOUT	23	O	LRCLK generated from input MCLK (usually 256 f_S) − normally routed on PCB to pin 10 (LRCLK) as input f_S sample clock.
MCLK	9	I	Master clock (256 x f_S)
NC	17, 18, 20−22, 25, 26		Reserved − No connection for normal operation
POWERDOWN	16	I	Powerdown input
$\overline{\text{RESET}}$	19	I	Reset, high = normal operation, low = reinitialize the device
RESERVED	15, 27		Reserved − digital ground for normal operation
SCL	5	I/O	Slave serial I^2C clock
SCLK	11	I	Shift clock (bit clock)
SCLKOUT	24	O	SCLK generated from input MCLK (usually 256 f_S) − normally routed on PCB to pin 11 (SCLK) as input 64 f_S bit clock.
SDA	4	I/O	Slave serial I^2C data
SDIN1	6	I	Serial audio data input one
SDIN2	7	I	Serial audio data input two
SDOUT	8	O	Serial audio data output

NOTE: Reset and other control functions require MCLK to be running. The system reset operation is a synchronous operation and requires a minimum of four MCLK cycles to reset the device.

1.13 Ordering Information

T_A	PACKAGE
	SMALL OUTLINE (PW)
0°C to 70°C	TAS3001CPW

1.14 Power Supply

- Digital supply voltage—DV_{DD}, DV_{SS} of 3.3 V
- Analog supply voltage—AV_{DD}_PLL, AV_{SS}_PLL of 3.3 V

NOTE: AV_{DD} and AV_{SS} for the PLL are derived from the digital supply and digital ground.

2 Audio Data Formats

2.1 Serial Audio Interface

The TAS3001 operates in digital audio slave mode only. The TAS3001 supports three serial audio data formats: I^2S, left-justified, and right-justified. Data word lengths of 16, 18, and 20 bits are supported.

Data is input into SDIN1 and SDIN2 under the influence of the master clock (MCLK), left/right clock (LRCLK), and shift clock (SCLK) inputs.

Data is output on the SDOUT pin under the influence of the master clock (MCLK) input plus the left/right clock (LRCLKOUT) and shift clock (SCLKOUT) outputs. LRCLKOUT and SCLKOUT are generated from the MCLK input (usually at $256 \times f_S$). Typically these are routed on the PCB to LRCLK (as the input f_S sample clock) and SCLK (as the input $64 \times f_S$ bit clock).

The TAS3001 device is compatible with 10 different serial interfaces. Available interface options are I^2S, right-justified, and left-justified. Table 2−1 and Table 2−2 indicate how the 10 options are selected using the I^2C bus and the main control register (MCR, I^2C address 01h). All serial interface options at either 16, 18, or 20 bits operate with SCLK at $64 \times f_S$. The 16-bit mode, left-justified, can operate at $32 \times f_S$ or $64 \times f_S$.

Table 2−1. Serial Interface Input Options

MODE	MCR BIT 6 SC	MCR BITS 3−2 F(1,0)	MCR BITS 1−0 W(1,0)	SERIAL INTERFACE SDIN1, SDIN2
0	0	00	00	16-bit, left-justified, $32 \times f_S$
1	1	00	00	16-bit, left-justified, $64 \times f_S$
2	1	01	00	16-bit, right-justified, $64 \times f_S$
3	1	10	00	16-bit, I^2S, $64 \times f_S$
4	1	00	01	18-bit, left-justified, $64 \times f_S$
5	1	01	01	18-bit, right-justified, $64 \times f_S$
6	1	10	01	18-bit, I^2S, $64 \times f_S$
7	1	00	10	20-bit, left-justified, $64 \times f_S$
8	1	01	10	20-bit, right-justified, $64 \times f_S$
9	1	10	10	20-bit, I^2S, $64 \times f_S$

Table 2−2. Serial Interface Output Options

MODE	MCR BIT 6 SC	MCR BITS 5−4 E(1,0)	MCR BITS 1−0 W(1,0)	SERIAL INTERFACE SDOUT
0	0	00	00	16-bit, left-justified, $32 \times f_S$
1	1	00	00	16-bit, left-justified, $64 \times f_S$
2	1	01	00	16-bit, right-justified, $64 \times f_S$
3	1	10	00	16-bit, I^2S, $64 \times f_S$
4	1	00	01	18-bit, left-justified, $64 \times f_S$
5	1	01	01	18-bit, right-justified, $64 \times f_S$
6	1	10	01	18-bit, I^2S, $64 \times f_S$
7	1	00	10	20-bit, left-justified, $64 \times f_S$
8	1	01	10	20-bit, right-justified, $64 \times f_S$
9	1	10	10	20-bit, I^2S, $64 \times f_S$

Figure 2−1 through Figure 2−4 illustrate the relationship between the SCLK, LRCLK, and the serial data input and output protocol options.

2.1.1 I²S Serial Format

The following are characteristics of this protocol:

- LRCLK is the left/right clock. The left channel is transmitted when LRCLK is low. The right channel is transmitted when LRCLK is high.
- SDIN is sampled with the rising edge of SCLK.
- SDOUT is transmitted on the falling edge of SCLK.
- LRCK must have a 50% duty cycle.

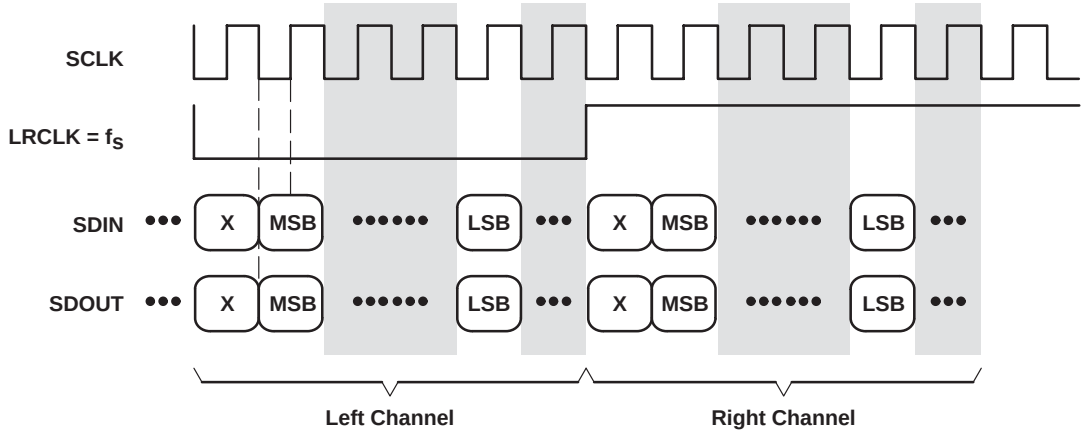


Figure 2–1. I²S-Compatible Serial Format

2.1.1.1 I²S Signal Timing

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(SCLK)}$	SCLK frequency			6.144	MHz
$t_{d(SLR)}$	SCLK rising to LRCLK edge	20			ns
$t_{d(SDOUT)}$	SDOUT valid from SCLK falling (see Note 1)			$1/(256 \times f_S)$ +10	ns
$t_{su(SDIN)}$	SDIN setup before SCLK rising edge	20			ns
$t_{h(SDIN)}$	SDIN hold after SCLK rising edge	100			ns
	LRCLK	32	44.1/48	96	kHz
	Duty cycle		50%		

NOTE 1: Maximum of 50-pF external load on SDOUT.

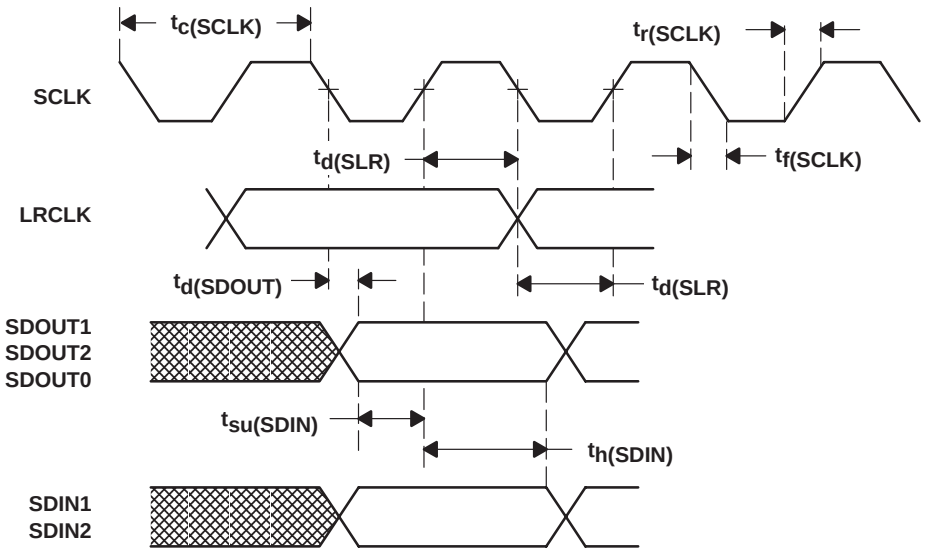


Figure 2−2. For Right/Left Justified, I²S, Left/Left Justified Serial Protocols

2.1.2 Left-Justified Serial Format

The following are characteristics of this protocol:

- LRCLK is the left/right clock. The left channel is transmitted when LRCLK is high. The right channel is transmitted when LRCLK is low.
- The SDIN data is justified to the leading edge of LRCLK.
- The MSBs are transmitted at the same time as the LRCLK edge and captured at the very next rising edge of SCLK.
- Serial data is sampled into the device on the rising edge of SCLK.
- Serial data is transmitted out of the device on the falling edge of SCLK.
- SCLK = 32 × LRCLK (32 × f_S SCLK is only supported for 16-bit data) or 64 × LRCLK
- In this mode, LRCLK does not have to be a 50% duty-cycle clock. The number of bits used in the interface sets the minimum duty cycle. There must be enough SCLK pulses to shift all of the data.

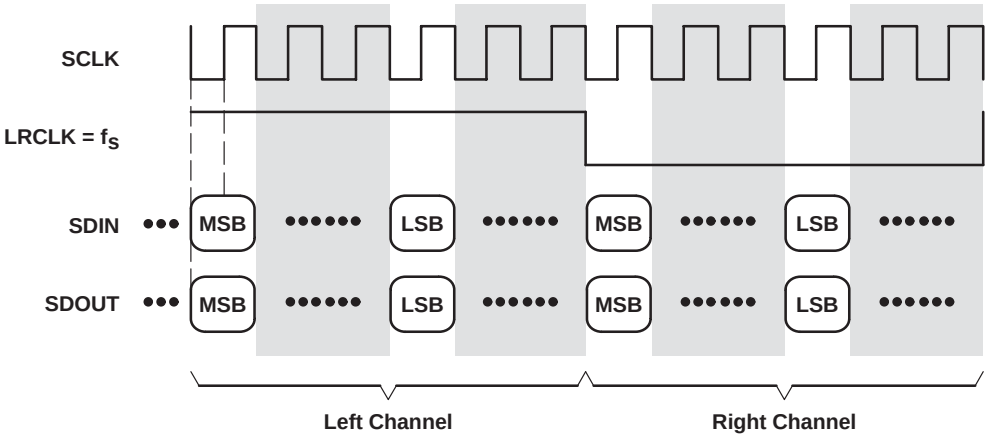


Figure 2−3. Left-Justified Serial Format

2.1.3 Right-Justified Serial Format

The following are characteristics of this protocol:

- LRCLK is the left/right clock. The left channel is transmitted when LRCLK is high. The right channel is transmitted when LRCLK is low.
- The SDIN data (recorded data) is justified to the trailing edge of the LRCLK.
- Serial data is sampled on the rising edge of SCLK.
- Serial data is transmitted on the falling edge of SCLK.
- In this mode, LRCLK does not have to be a 50% duty-cycle clock. The number of bits used in the interface sets the minimum duty cycle. There must be enough SCLK pulses to shift all of the data.

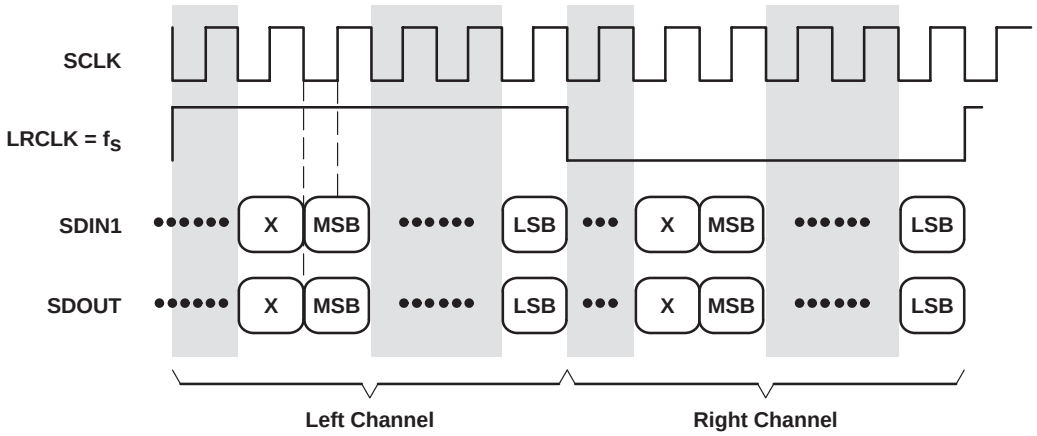


Figure 2−4. Right-Justified Serial Format

2.2 LRCLKOUT and SCLKOUT

The digital audio processor and on-chip logic are sequenced using an internal system clock that is derived from MCLK (master clock). Also derived from MCLK are the LRCLKOUT and SCLKOUT signals that provide clocks to the TAS3001 and other devices in the system.

The TAS3001 allows multiple system clocking schemes. In Figure 2−5, the TAS3001 provides system clocks (LRCLK and SCLK) to other parts of the system. In Figure 2−6, a system master other than the TAS3001, provides system clocks (LRCLK and SCLK) to the TAS3001.

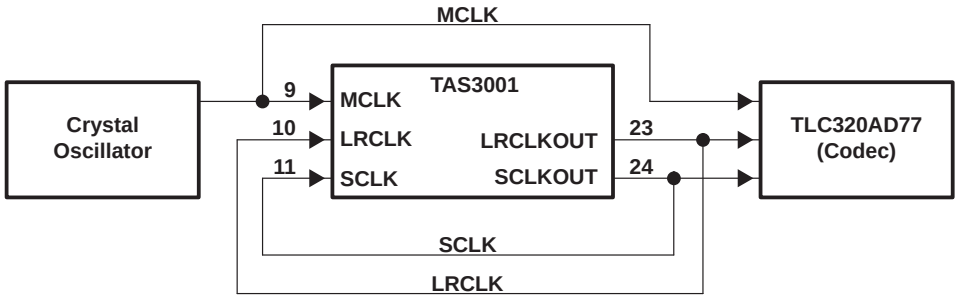


Figure 2−5. Master Mode

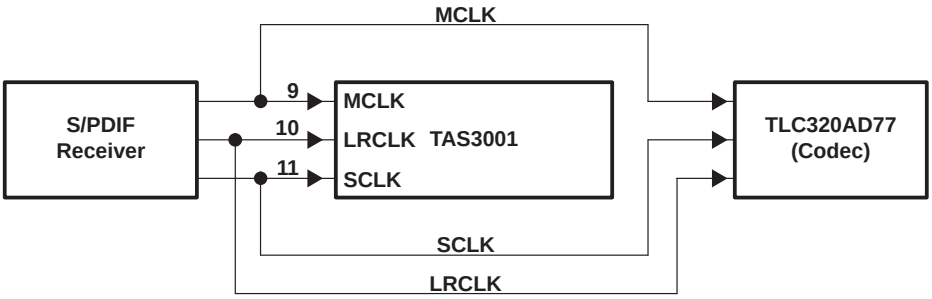


Figure 2−6. Slave Mode

3 Serial Control Interface (I²C)

The TAS3001 operation is controlled using the $\overline{\text{RESET}}$ signal and the serial control interface. Control information is downloaded into the TAS3001 control registers by an I²C master device, such as a microprocessor, microcontroller, or DSP. These registers control the settings for volume, bass, treble, mixing, and filtering. A description of the register addresses and control formats is given in Appendix A.

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system. Each device is addressed by sending a unique 7-bit slave address plus an R/$\overline{\text{W}}$ bit (1 byte).

All I²C compatible devices are controlled using the SDA and SCL signals using a wire-ANDed connection. A pullup resistor must be used to set the high level on the bus. The TAS3001 operates in standard I²C mode up to 100 kbps with as many devices on the bus as desired up to the capacitance load limit of 400 pF.

The TAS3001 is an I²C slave-only device; therefore, at least one device connected to the I²C bus with this device must operate in master mode. The pullup resistor is generally 4.99 kΩ. Upon power up, the I²C is in an unknown state until the master clock has been applied and the TAS3001 has been reset. Prior to reset, the TAS3001 may hold the SDA and/or SCL lines low. This creates I²C communication errors for any other device that attempts to use the bus.

3.1 I²C Protocol

The bus standard uses transitions on the data pin (SDA) while the clock is high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. These conditions are shown in Figure 3−1. These start and stop conditions for the I²C bus are required by standard protocol to be generated by the master. The master must also generate the 7-bit slave address and the read/write (R/$\overline{\text{W}}$) bit to open communication with another device and then wait for an acknowledge condition. The slave holds SDA low during acknowledge clock period to indicate an acknowledgment. When this occurs, the master transmits the next byte of the sequence.

After each 8-bit word, an acknowledgment must be transmitted by the receiving device. There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. A generic data transfer sequence is shown in Figure 3−1. Definitions for the I²C protocol terms are listed in Table 3−1.

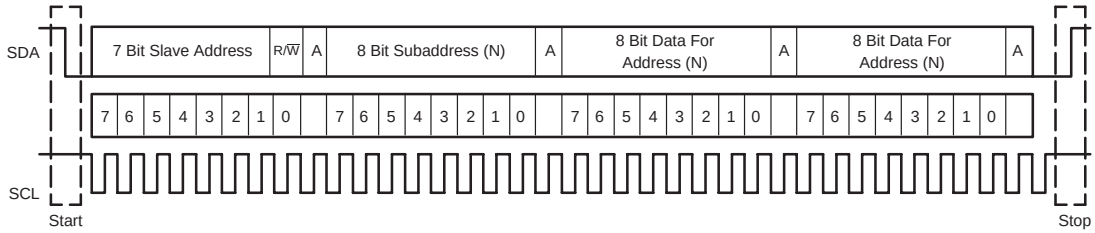


Figure 3−1. Typical I²C Data Transfer Sequence

Table 3−1. I²C Protocol Definitions

DEFINITION	DESCRIPTION
Master	The device that initiates a transfer, generates clock signals, and terminates the transfer
Receiver	The device that receives data
Slave	The device addressed by the master

3.2 Operation

To permit multiple devices to be controlled via the I^{2}C bus, each slave device has an address. The TAS3001 has been assigned four unique addresses to permit multiple TAS3001s to be used in a system. The addresses are selected using the CS1 and CS2 pins. These four addresses, listed in Table 3−2, are licensed I^{2}C addresses and do not conflict with other licensed I^{2}C audio devices. To communicate with the TAS3001, the I^{2}C master must use the address 01101XX. In addition to the 7-bit device address, subaddresses are used to direct communication to the proper memory location within the device. A complete table of subaddresses and control registers is provided in Appendix A, *Software Interface*.

Table 3−2. TAS3001 I^{2}C Address

I^{2}C ADDRESS BYTE	A6−A2	CS2(A1)	CS1(A0)	R/$\overline{W}$
68h	01101	0	0	0
6Ah	01101	0	1	0
6Ch	01101	1	0	0
6Eh	01101	1	1	0

3.2.1 Write Cycle Example

An example write cycle is demonstrated in Figure 3−2 and Table 3−3.

Start	Slave Address	R/W	A	Subaddress	A	Data Byte 1	A	Data Byte 1	A	Data Byte 2	A	Data Byte N	A	Stop

Figure 3−2. Write Cycle Example

Table 3−3. Write Cycle Example

FUNCTION	DESCRIPTION
Start	Start condition as defined in I^{2}C
Slave address	0110100 (CS1 = CS2 = 0)
R/$\overline{W}$	0 (write)
A	Acknowledgement as defined in I^{2}C (slave)
Subaddress	00000110 (see Appendix A, *Software Interface*)
Data	00011100 (see Appendix A, *Software Interface*)
Stop	Stop condition as defined in I^{2}C

Whenever writing to a subaddress, the correct number of data bytes must follow in order to complete the write cycle. For example, if the volume control register with subaddress 04h is written to, six bytes of data must follow; otherwise, the cycle will be incomplete and errors will occur.

3.2.2 I^{2}C Timing and Wait Cycles

The TAS3001 issues I^{2}C wait cycles to regulate the flow of command information. The TAS3001 can issue wait cycles for each instruction. For any instruction, the TAS3001 can issue up to a one sample (23 μs) wait between data bytes and between the last data byte and the I^{2}C stop. This wait is generated after the acknowledgement. The duration of this wait cycle is slightly longer than a sample interval, on the order of 1.1 x 1 ÷ F_S (or 25 μs at 44.1 kHz). This wait cycle is illustrated in Figure 3−3.

Start	Slave Address	R/W	A	Subaddress	A	Data Byte 1	A	Wait	Data Byte 1	A	Wait	Data Byte 2	A	Wait	Data Byte N	A	Wait	Stop

Figure 3−3. Wait Cycle Example

The TAS3001 can also issue an I^{2}C wait state after receiving an entire volume or tone command. The TAS3001 produces these wait cycles while it executes the interpolation algorithms from the present setting to the new setting. The volume command always takes the same amount of time to process for a given sample rate. The treble and bass commands vary depending upon the current index and the destination index. E.g., moving from −18 dB to 18 dB or vice versa produces the longest wait.

However, this wait cycle does not occur during the volume or tone change command, instead it occurs during the next command after the acknowledgement of the first data byte.

Table 3−4 gives typical values of the wait states of the TAS3001 commands.

Table 3−4. I²C Wait States

	SYSTEM SAMPLING FREQUENCY				COMMENT
	32 kHz	44.1 kHz	48 kHz	96 kHz	
Volume	62 ms	49 ms	41 ms	21 ms	Not dependent on size of change
Bass	231 ms	167 ms	153 ms	77 ms	18 dB to −18 dB (proportional to step change)
Treble	231 ms	167 ms	153 ms	77 ms	18 dB to −18 dB (proportional to step change)
Mixer	None	None	None	None	
Equalization	None	None	None	None	

The I²C operation sequence that the TAS3001 uses to assert an I²C wait cycle is:

1. The TAS3001 detects a valid start condition and correct device ID. At this point the TAS3001 issues an ACK.
2. The TAS3001 decodes the eight-bit subaddress and issues another ACK.
3. The TAS3001 decodes the first data byte and issues a third ACK.
4. At this point, the TAS3001 device can hold the SCL clock line low until the internal controller is ready to accept more data. This is an I²C slave wait state.

There are two ways a master can handle the I²C slave wait.

- The preferred way to handle wait states is to use an I²C master that recognizes wait states. During the wait-state period, the master stops sending data over I²C. In this case, when the master releases the clock to go high after a slave ACK (to latch in the next bit of data), the master monitors the SCL line and ensures that the slave has released SCL. Once SCL has been released the master can start the next transmission.
- Alternatively, if this function is not available on the system controller, fixed delays can be implemented in the system software to ensure that the TAS3001 is ready to receive additional data. Sending I²C data while the TAS3002 device is busy causes errors and the device locks up and have to be reset.

Issuing a stop command in the middle of an I²C transaction puts the TAS3001 I²C slave block into an unknown state, possibly locking up the controller or causing it to send incorrect data to the signal processing block.

3.2.3 Resetting the TAS3001 I²C Interface

To put the TAS3001 back into a known state, an I²C transaction with a subaddress of 00h and followed by 16 bytes of zeros clears out the I²C slave block buffer. Resetting the device also puts it into a known state.

During normal operation, the TAS3001 should never issue a NACK. If the TAS3001 issues a NACK, this is an indication of an I²C protocol discrepancy.

3.2.4 Power-Up Conditions

Upon system power up, the I²C bus SCL can initialize in a mode in which the line is held low. This prevents any I²C operations from being performed. To prevent this from occurring, always hold $\overline{\text{RESET}}$ low for a minimum of 10 MCLK clock cycles after applying power.

Upon reset, the TAS3001 goes through an initialization sequence with a duration of 5 ms.

Before a reset, the SDA and SCL lines may be held low by the device.

3.2.5 I²C Serial Port Timing

PARAMETER		MIN	MAX	UNIT
$f_{(scl)}$	SCL clock frequency	0	100	kHz
t_{BUF}	Bus free time between start and stop	4.7		µs
$t_{w(low)}$	Pulse duration, SCL clock low (see Note 1)	4.7		µs
$t_{w(high)}$	Pulse duration, SCL clock high (see Note 2)	4		µs
$t_{h(STA)}$	Hold time, repeated start	4		µs
$t_{su(STA)}$	Setup time, repeated start	4.7	20	µs
$t_{h(DAT)}$	Hold time, data	0†		µs
$t_{su(DAT)}$	Setup time, data	250		ns
t_r	Rise time for SDA and SCL		1000	ns
t_f	Fall time for SDA and SCL		300	ns
$t_{su(STO)}$	Setup time for stop condition	4		µs

† A device must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

NOTES: 1. $t_{w(low)}$ is measured from the end of t_f to the beginning of t_r.
2. $t_{w(high)}$ is measured from the end of t_r to the beginning of t_f.

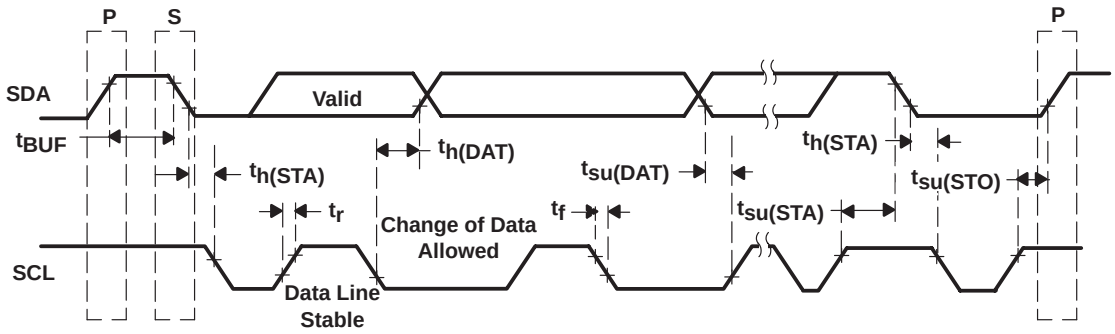


Figure 3–4. I²C Serial Port Timing

4 Digital Audio Processor

4.1 Input Mixer Control

The TAS3001 is capable of mixing two channels of serial audio data. The mixer permits each input to scaled (−∞ to +18 dB) independently and then a stereo summation is performed. One important function of this circuit is to scale the input signals down to compensate for gains in the equalization settings and the bass and treble controls. This prevents the system from exceeding the maximum digital signal output.

The mixer operation is controlled by loading values into the MIXER1 (07h) and MIXER2 (08h) control registers. The mixer control values are in 4.20 format—4 bits for the integer and 20 bits for the fraction. The formula for converting a 4.N number to dB is: dB = 20 log(X), where X is a positive 4.N number. To mute a mixer channel, 0s are loaded into its respective mixer control register.

In order to transmit mixer control values over I^2C, it is necessary to separate each value into three bytes. The first nibble of byte 2 is the integer; the second nibble of byte 2 and bytes 1 and 0 are the fraction.

Table A−7 contains dB converted into 4.20 numbers for the range –70 dB to 18 dB, although any positive 4.20 number can be used.

The mixer operation is updated instantly in response to a control register change. This may cause audible artifacts when changing mixer settings outside of fast load mode.

4.2 Biquad Block

The biquad block consists of six digital biquad filters per channel organized in a cascade structure as shown in Figure 4−1. Each of these biquad filters has five downloadable 24-bit (4.20) coefficients. Each stereo channel has independent coefficients.

Figure 4−1. Cascaded Biquad Filters

4.2.1 Filter Coefficients

The filter coefficients for the TAS3001 are downloaded through the I^2C port and loaded into the biquad memory space. Digital audio data coming into the device is processed by the biquad filters and then output from the device, usually to an external DAC. Any biquad filter may be downloaded and processed by the TAS3001. The biquad structure that is used for the parametric equalization filters is:

$$H(z) = \frac{b_0 + b_1 Z^{-1} + b_2 Z^{-2}}{1 + a_1 Z^{-1} + a_2 Z^{-2}}$$

The coefficients for these filters are quantized and represented in 4.20 format—4 bits for the integer part and 20 bits for the fractional part. Each biquad uses five coefficients to define the operation.

4.3 Volume Control Functions

4.3.1 Soft Volume Update

The TAS3001 implements a Texas Instruments proprietary soft volume update. This update allows a smooth and pleasant-sounding change from one volume level to another over the entire range of volume (18 dB to mute).

The volume is adjustable by downloading a 4.20 gain coefficient through the I^2C interface to register (04h). Table A−4 in the Appendix lists the 4.20 coefficient values for 0.5-dB volume steps for the range of –70 dB to 18 dB. However, positive 4.20 values other than those listed in Table A−4 are allowed.

Right and left channel volumes can be unganged and set to different values to implement balance control.

4.3.2 Software Soft Mute

Mute is implemented by loading all zeros in the volume control register. This causes the volume to ramp down automatically over a maximum of 2048 samples to a final output of zero (–∞ dB).

4.4 Tone Controls

4.4.1 Treble Control

The treble gain level may be adjusted within the range of 18 dB to –18 dB with 0.5 dB step resolution. The level changes are accomplished by downloading the one byte treble control codes into the treble control register (05h). The bass control codes are shown in Table A−5.

4.4.2 Bass Control

The bass gain level may be adjusted within the range of 18 dB to –18 dB with 0.5 dB step resolution. The level changes are accomplished by downloading the one byte bass control codes into the bass control register (06h). The treble control codes are shown in Table A−6.

4.4.3 Frequency Dependence of Treble and Bass Controls

The bass and treble controls are based upon fixed filter coefficients. The coefficients define a response that is a based upon the data sample rate. As a result, if the sample rate is increased or decreased by a factor, the filter frequency response will increase or decrease in frequency by an equal factor. Table 4−1 and Table 4−2 show the relationship between the sample frequency and corner frequency for the bass and treble controls.

Table 4−1. Bass Control Corner Frequencies

Sampling Rate	32,000	44,100	48,000	96,000
Corner Frequency	72.6	100.0	108.8	217.7

Table 4−2. Treble Control Corner Frequencies

Sampling Rate	32,000	44,100	48,000	96,000
Corner Frequency	7,256	10,000	10,884	21,769

5 Device Operation

5.1 Device Initialization

5.1.1 Reset

The reset pin allows the device to be reset. The reset operation is a synchronous operation requiring MCLK to perform the sequence of reset operations. During reset, the TAS3001 returns to the default state as described in this section and goes through the initialization process. The TAS3001 does not reset automatically when power is applied to the device.

A reset is required after power is applied to any of the power pins.

Required conditions for a successful reset:

- MCLK is running.
- $\overline{\text{RESET}}$ is low for a minimum of 10 MCLK cycles.

The reset operation typically takes 5 ms to complete.

Once reset has completed, the master control register (MCR) should be set. The MCR sets the serial mode and fast load. It is recommended that the MCR be set only once, following reset.

5.1.2 Device Power On and System Reset

When power is applied to the TAS3001, the device powers up in an unknown state. It must be reset before the device will be in a known state. It is recommended that $\overline{\text{RESET}}$ be applied following power up. The TAS3001 performs its internal reset operations in 5 ms and is then ready for operation. Following the reset, the TAS3001 initializes to its default state (fast load mode). The main control register is configured to 1XXX XXXX, where X is not initialized, as shown in Figure 5−1 (see Appendix A for a complete description of the MCR). Only the fast load bit set to a 1 in the main control register. This puts the device into fast load mode (see the *Initialization* section). All random access memory (RAM) will be initialized (previous data will be overwritten).

Bit 7							Bit 0
1	X	X	X	X	X	X	X

Figure 5−1. Main Control Register (MCR)

The I^2C address pins (CS1 and CS2) should be driven or biased to set the TAS3001 to a known I^2C address. This also ensures the I^2C port is active immediately after the reset initialization phase. Furthermore, when implementing a three- or six-speaker system, the CS1 and CS2 pins must always be driven or set to unique addresses on all devices. The I^2C port is powered up but does not acknowledge any I^2C bus activity until the entire device has been initialized. This initialization typically takes 5 ms.

5.1.3 Initialization

After reset, the system enters fast-load mode and the following occur as part of initialization:

- All of the parametric EQ is initialized to 0 dB (all-pass).
- The tone (bass/treble) is set to 0 dB.
- The mix function sets SDIN1 to 0 dB and SDIN2 to mute (no-pass).
- The volume is set to mute.

While in fast-load mode, it is possible to update the parametric EQ without any audio processing delay. The audio processor pauses while the RAM is being updated in this mode. It is recommended that parametric EQ be downloaded in this mode. Bass and treble cannot be downloaded in this mode. Mixer1 and Mixer2 registers can be downloaded in this mode or normal mode (FL bit = 0). It is not recommended to download the volume control register and mixer registers in this mode. Once the download is complete, the fast-load bit needs to be cleared by writing a 0 into bit 7 of the main control register. This puts the TAS3001 into normal mode.

> **NOTE:** While in the fast-load mode, the TAS3001 does not accept audio. The device must be set to the normal mode before it can accept and process audio data.

When coming out of fast-load mode, it is good practice to be sure that the system is muted. This prevents the system from producing spurious pops and clicks. Once back in normal mode, treble, bass, and volume controls can be downloaded to complete device setup.

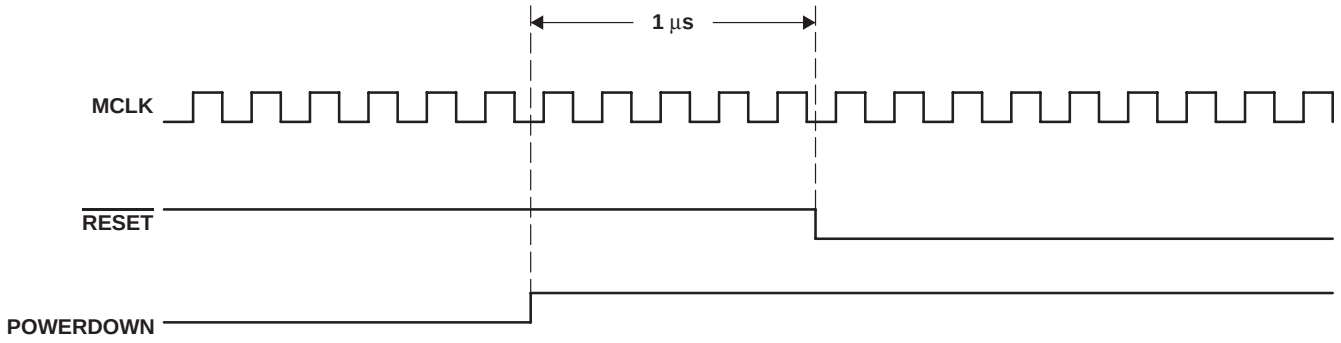
5.2 Power Consumption

During normal operation the average power consumption is 20 mA.

When $\overline{\text{RESET}}$ is held low, asserted, the TAS3001 draws an average current of 35 mA.

5.3 Power Down and Restart

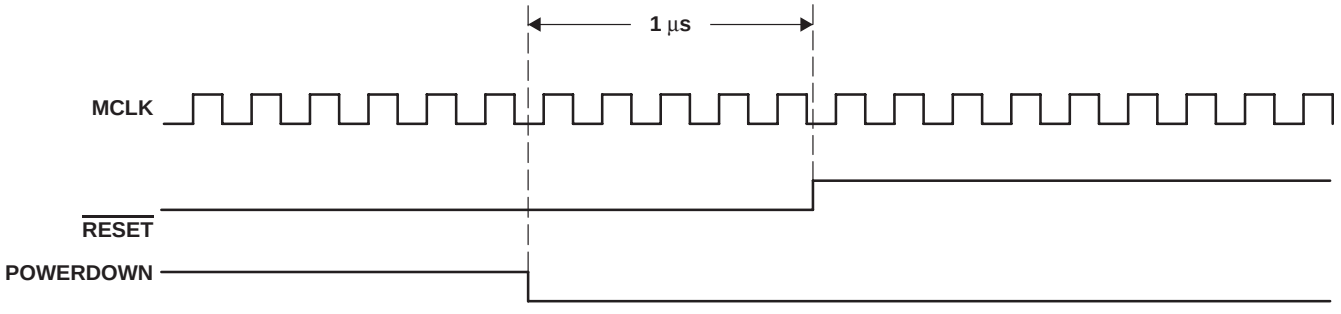
The TAS3001 can be placed in a low-power mode. It is entered synchronously by asserting the POWERDOWN pin high, logic 1, followed by asserting the $\overline{\text{RESET}}$ pin low, logic 1, 1 µs later. Figure 5−2 illustrates the timing for power down. MCLK must be present for the TAS3001 to enter the power-down mode.



NOTE: $\overline{\text{RESET}}$ and POWERDOWN do not have to be synchronized with MCLK.

Figure 5−2. Power-Down Timing

To recover from the power-down state, the POWERDOWN pin is set low, logic 0, followed by asserting the $\overline{\text{RESET}}$ pin high, logic 0, 1 µs later. Figure 5−3 illustrates the timing for start-up. MCLK must be present for the TAS3001 to exit the power-down mode.



NOTE: $\overline{\text{RESET}}$ and POWERDOWN do not have to be synchronized with MCLK.

Figure 5−3. Start-Up Timing

6 Electrical Characteristics

6.1 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage range, AV_{DD}_PLL, DV_{DD} . . . . . −0.3 V to 4.2 V
Digital input voltage range . . . . . −0.3 V to V_{DD} + 0.3 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C
Case temperature for 10 seconds, T_C . . . . . 122.3°C
Lead temperature from case for 10 seconds . . . . . 97.8°C
ESD tolerance‡ . . . . . 2000 V

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
‡ Human body model per method 3015.2 of MIL-STD-883B.

6.2 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
PLL supply voltage, AV_{DD}	3	3.3	3.6	V
Digital IC supply voltage, DV_{DD}	3	3.3	3.6	V
Capacitive load for each bus line $C_{L(bus)}$ (SDA, SCL)			400	pF
Operating free-air temperature, T_A	0	25	70	°C

6.3 Power Consumption

PARAMETER	TEST CONDITIONS	32−48 kHz SAMPLE RATE	96 kHz SAMPLE RATE	UNIT
		TYP	TYP	
PLL and digital IC supply current, I_{DD}	V_{DD} = 3.3 V, No load	20	40	mA
	V_{DD} = 3.3 V, No load, Reset active	35	70	
	V_{DD} = 3.3 V, No load, Standby	2	4	

6.4 Static Digital Specifications

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2		V_{DD} +0.3	V
V_{IL}	Low-level input voltage		−0.3		0.8	V
V_{OH}	High-level output voltage	I_O = −1 mA	2.4		V_{DD}	V
V_{OL}	Low-level output voltage	I_O = 4 mA			0.4	V
I_{IH}	High-level input leakage current		−10		10	µA
I_{IL}	Low-level input leakage current		−10		10	µA
$I_{OZ(H)}$	High-level output leakage current	SCL, SDA	−10		10	µA
$I_{OZ(L)}$	Low-level output leakage current	SCL, SDA	−10		10	µA

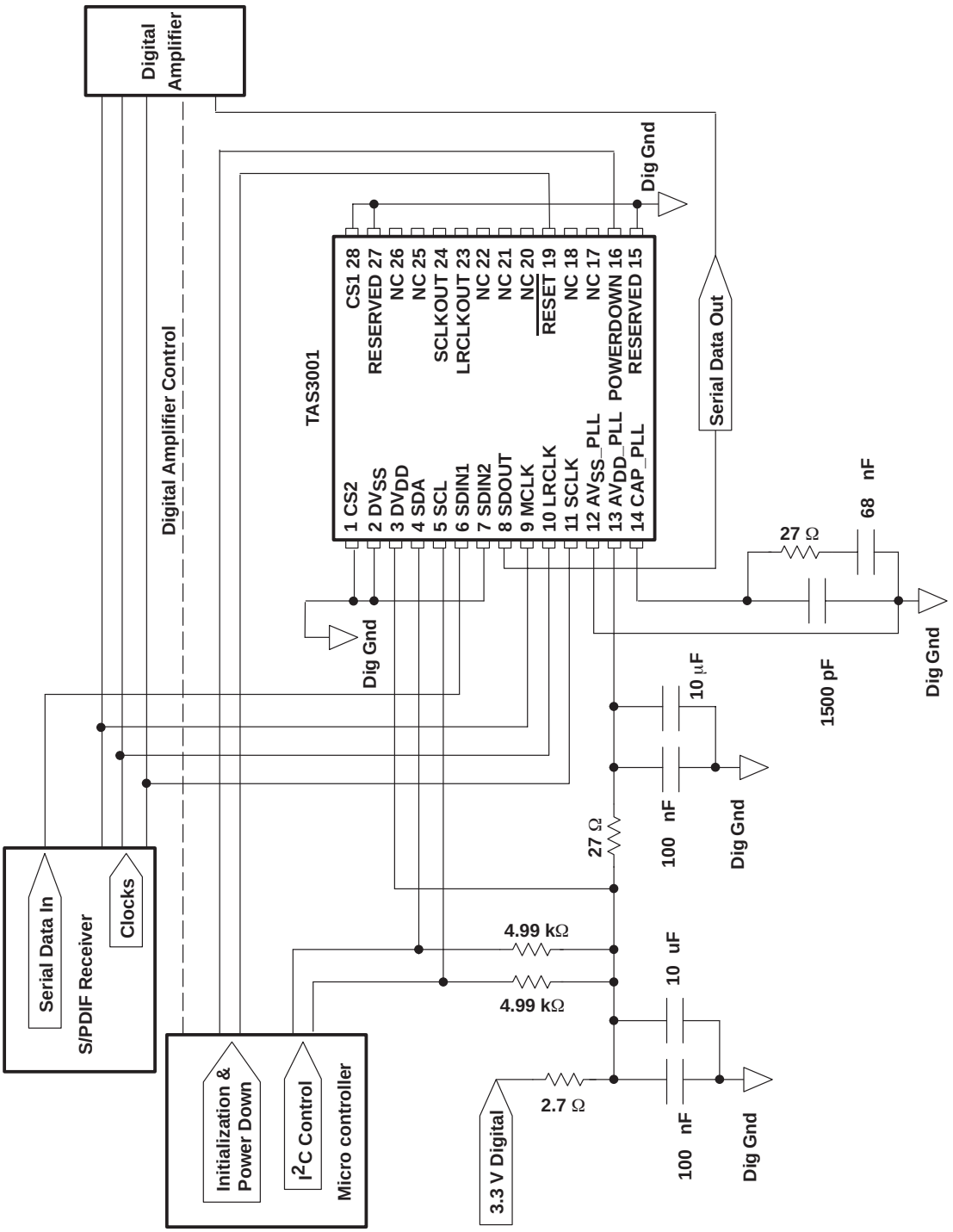


Figure 6−1. Typical TAS3001 Connection

7 Measured Audio Performance for Some Typical Examples

To illustrate the performance of the TAS3001, a series of measurements was performed on a system shown in Figure 7−1.

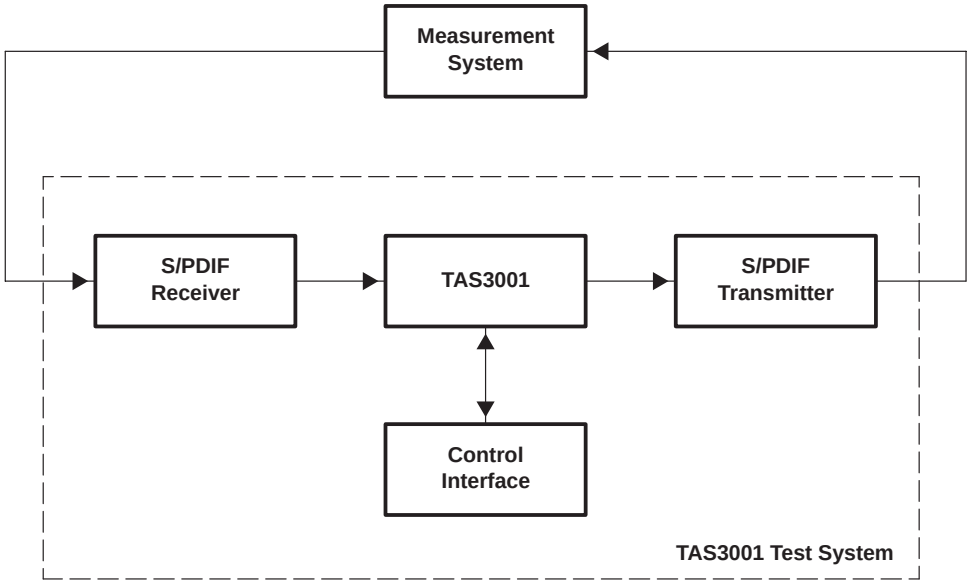


Figure 7−1. Audio Performance Measurement System

The system performance was measured for three filter types at 48 kHz.

- Butterworth high-pass filter at 1 kHz
- Butterworth low-pass filter at 1 kHz
- EQ filter at 1 kHz with a gain of 8 dB and a bandwidth of 500 Hz

The audio performance that was measured is shown in Table 7−1. The response shapes of the three test filters are shown in Figure 7−2.

Table 7−1. Audio Filter Performance

PARAMETER	FILTER	CONDITIONS	MEASURED
THD+N	All-pass	Vol = 0, mixer –0 dB, 48-kHz f_S	< −110 dB < 0.0003%
	1-kHz second-order Butterworth high- and low-pass filters	Vol = 0, mixer –0 dB, 48-kHz f_S	< −106 dB < 0.0005%
	1-kHz EQ +8 dB, 500-Hz bandwidth	Vol = 0, mixer –8 dB, 48 kHz f_S	< −108 dB < 0.0004%
SNR	All filters		> 110 dB
IM	All filters		< −98 dB < 0.001%

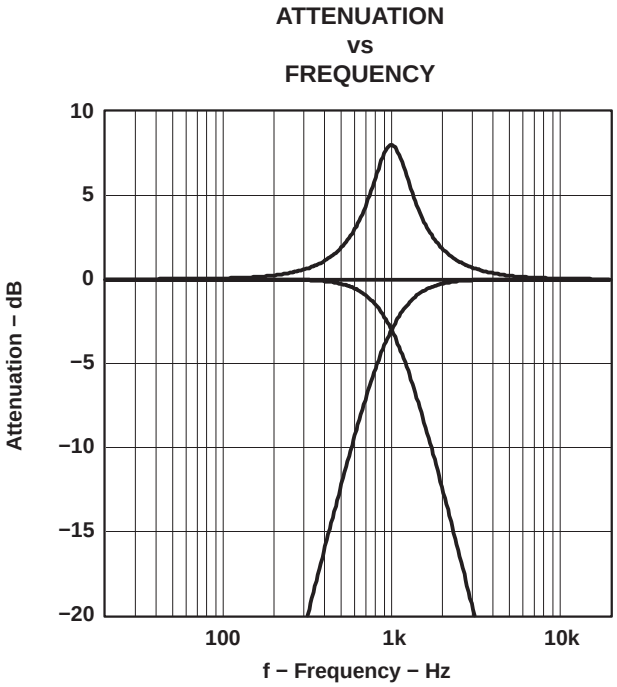


Figure 7−2. Audio Performance Test Filters

8 Using the TAS3001 in a System

8.1 TAS3001 Applications

The TAS3001 can be used to perform a number of audio processing functions.

The TAS3001 can be used to perform parametric equalization to correct the frequency response of a pair of loudspeakers and microphones as shown in Figure 8−1. In this case, the TAS3001 is used to shape the frequency response of the transducers by applying filters to compensate for the response irregularities of each transducer (peaks and valleys of the microphone and loudspeaker response).

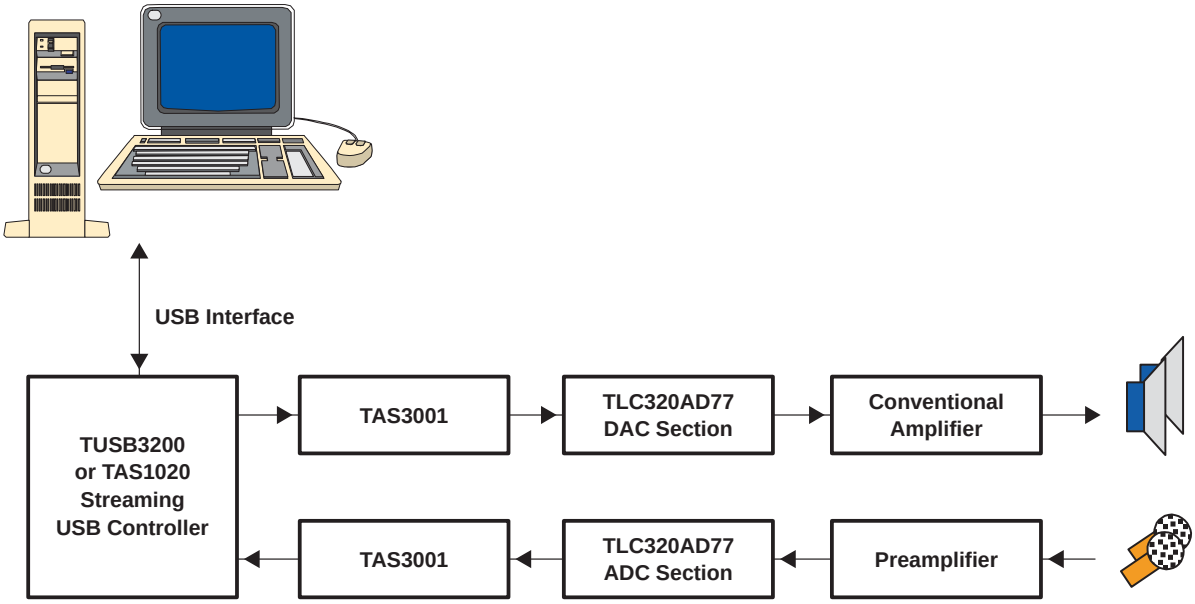


Figure 8−1. TAS3001 as a System Equalizer

The filters can be developed and evaluated using a personal computer, the TAS3001 EVM, a speaker analysis package, and the automatic loudspeaker equalization program. The next section demonstrates the use of the Texas Instruments automatic loudspeaker equalization program that automates many of the steps in developing filters for loudspeaker equalization.

A second application of the TAS3001 is to perform both the crossover and frequency equalization of individual loudspeaker drivers in a two- or multi-way loudspeaker design as in Figure 8−2. In this case, the TAS3001 provides two functions: the crossover band-pass and band-limiting functions for each speaker and the compensation for the response irregularities of each loudspeaker driver.

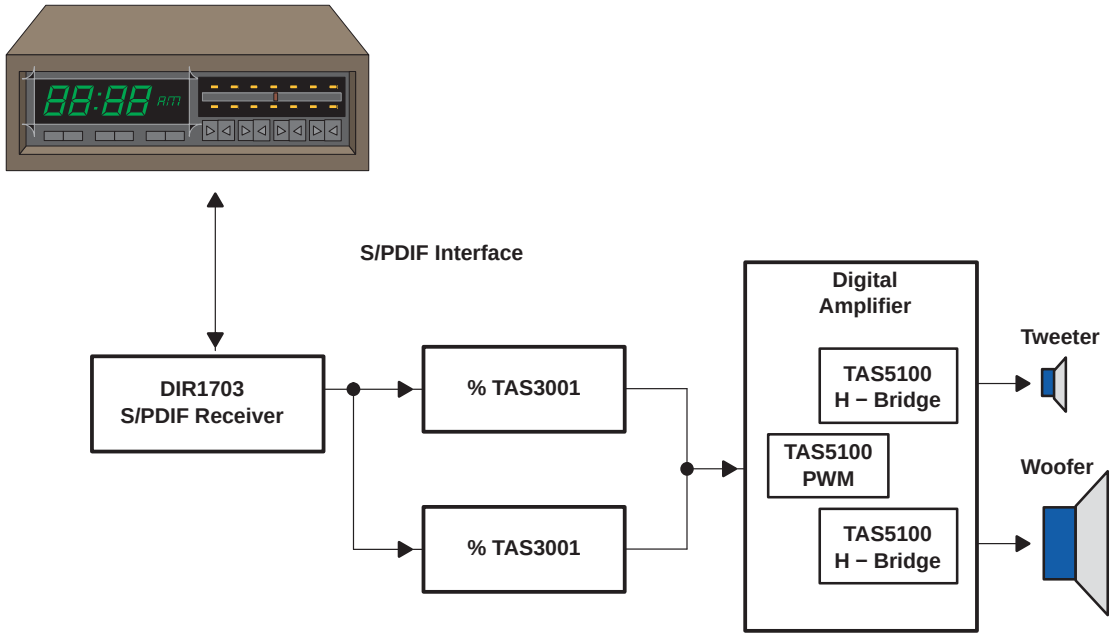


Figure 8−2. TAS3001 as a Crossover and Equalizer

8.2 Measurement-Based Speaker Correction

Although loudspeakers ideally should be designed for a uniform sound pressure response as a function of frequency, cost and physical constraints usually result in speakers that are less than ideal. To correct large nonlinearities in the response or to shape the response to listener preferences, speaker equalization can be performed.

In the example speaker response shown in Figure 8−3, it is seen that the sound pressure level (y-axis) varies significantly as a function of frequency (x-axis). For speakers such as this typical loudspeaker, equalization can improve performance and enhance the listening experience.

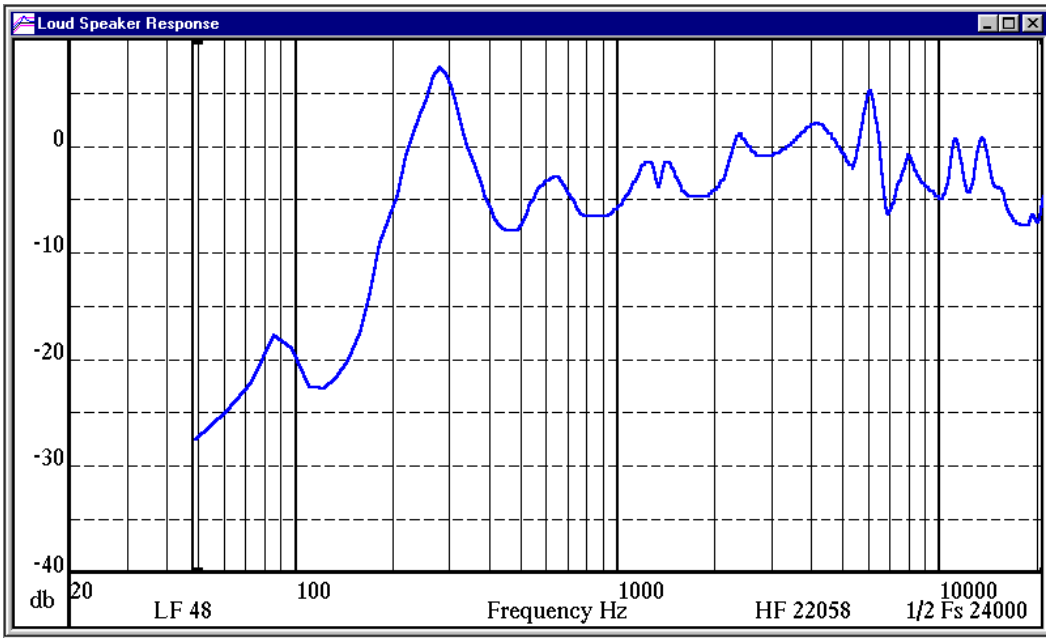


Figure 8−3. Typical Small Loudspeaker Response

In addition to equalization of the frequency response, the TAS3001 can be used to notch out specific frequencies that excite mechanical resonances in the speaker. The removal of mechanical resonances improves the temporal response of the loudspeaker, so that it more accurately reproduces a recorded signal. For small and ported loudspeakers, a high-pass filter eliminates signal energy that is lower than the speaker can reproduce. This filtering improves the loudspeaker power handling and intelligibility by eliminating large cone excursions produced by signals that are below the loudspeaker resonant frequency.

The kinds of corrections being discussed here begin with a thorough understanding of the inherent operation of the particular loudspeaker. This information can best be obtained by means of a measurement such as that shown in Figure 8−3. The measurement information allows the equalization designer to find the resonances and other problems associated with the speaker and to correct them.

8.3 Sound-Based Speaker Correction

While a high-quality speaker measurement can be extremely valuable to the equalization designer, many good equalization designers also rely upon their own perception of the sound from the speaker. Based upon what they measure and hear, designers are able to design filters to achieve a specific frequency response and desired sonic character. Digital filters can be used to provide these corrections and shape the produced sound.

8.4 Loudspeaker Equalization Example

An example of loudspeaker equalization follows. In Figure 8−3, a loudspeaker has the frequency response shown. In Figure 8−5 the designer specifies the desired response that is the center of the three new lines. The lines above and below the center line are the + and − tolerances. The tolerances can be adjusted.

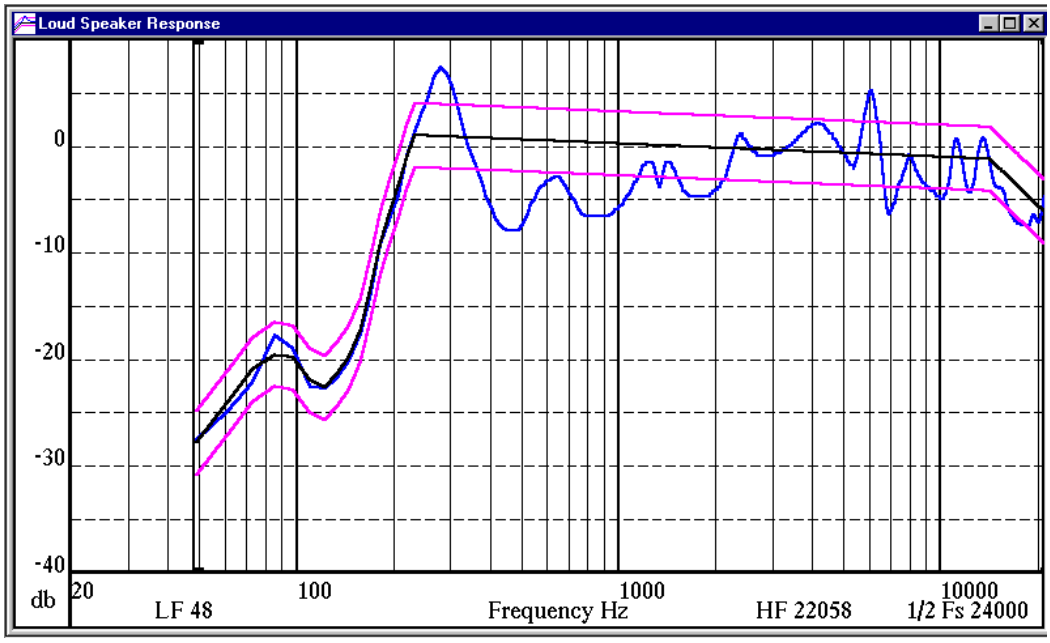


Figure 8−4. Preparation for Equalization

Figure 8−5 shows the corrected loudspeaker response that has been developed by the ALE program.

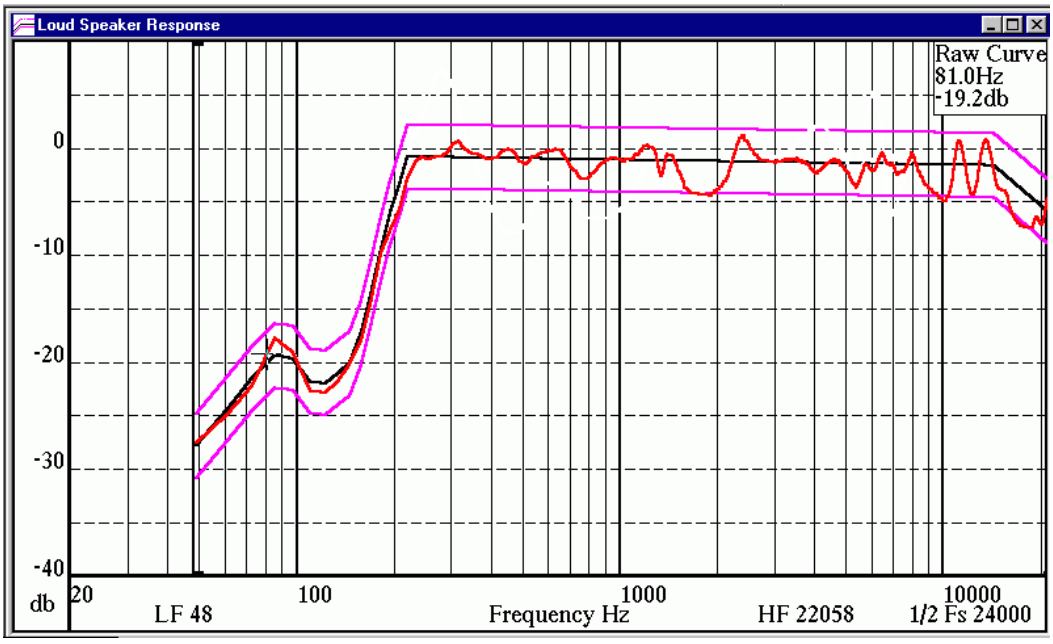


Figure 8−5. After Equalization

Figure 8−6 shows the filters that were used to equalize the loudspeaker response.

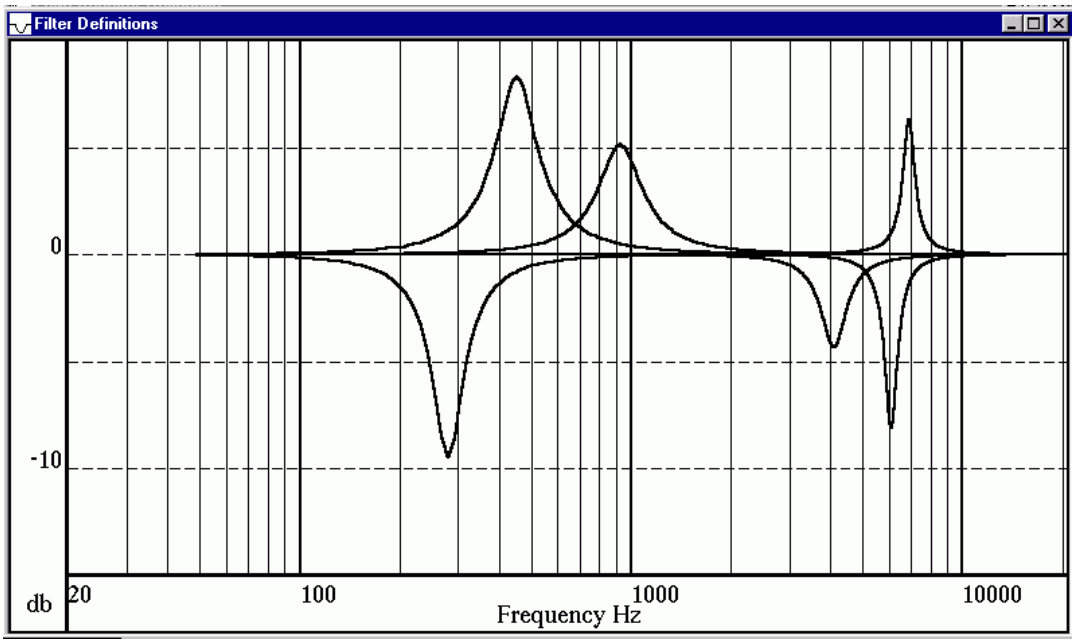


Figure 8−6. Equalization Filters

8.5 Speaker Correction and Equalization

Digital filters are able to provide a fairly broad range of filter types and responses.

The TAS3001 contains six programmable filters. The system designer has the choice of using one to all six of these filters. The filters can be used to equalize response peaks and dips from a desired response. They can also be used to shape the loudspeaker phase response. Because of their available precision and temperature insensitivity, not only can the filters be used to equalize the frequency and phase response of a loudspeaker closely, but they also can be used to remove resonances or other small deviations in the response of a loudspeaker surgically. This permits the system designer a greater degree of flexibility in the design of both the individual loudspeaker drivers and the cabinet. If additional filtering is needed, multiple TAS3001s can be cascaded.

This enables greater freedom in the design of acoustical systems. The TAS3001 permits additional flexibility in transducer design. Overall flatness of a transducer response is no longer an overriding concern with the low-cost/high-performance frequency correction of the TAS3001. The constraints on the transducer design can be relaxed so that they provide optimum performance after correction. This, in turn, allows the transducer and its equalization to be designed as a system, providing wide flexibility in the design and achieving outstanding sound presentation.

8.6 The TAS3001 Can Implement Nearly Any Second-Order IIR Filter

Filter designs can tax computational resources, so it is not uncommon to see simplified filter implementations that must limit either the number of or the nature of the filters that can be implemented. For example, a particular architecture might impose limits on the gains, Qs, and/or center frequencies that can be implemented. This, however, is not the case with the TAS3001. Its high-precision, patent-pending structure allows implementation of almost any second-order IIR filter. These are implemented in an almost limitless range of filter functions without fear of degradation due to limit cycles or increased system noise.

Additionally, higher order filters can be developed by factoring the desired filter into consecutive multiple second-order sections. Similarly, any filter that has been designed in analog can be converted and implemented as a digital filter.

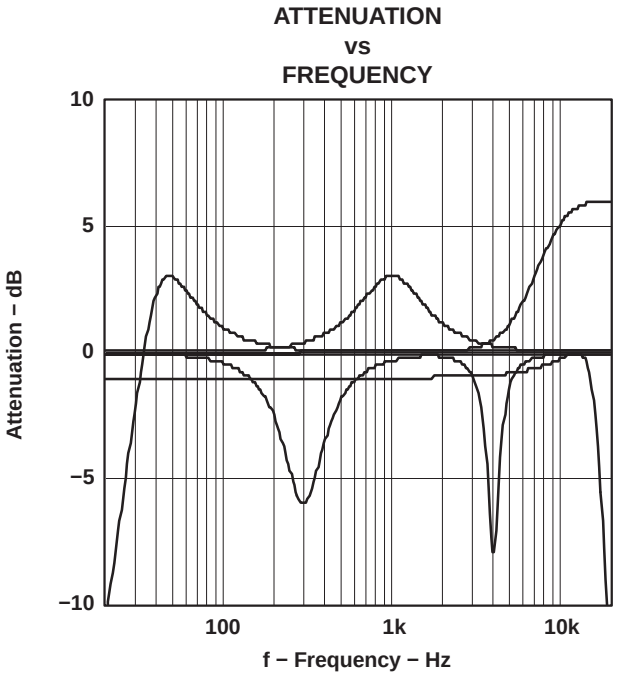


Figure 8−7. Individual Filters

From left to right the filters that are shown in Figure 8−7 are:

- Variable Q high-pass filter with a Q = 1.3 to emphasize the bass and prevent distortion by cutting of frequencies below the cabinet resonance
- Equalization filters of various amplitudes, center frequencies, and bandwidths
- A treble shelf
- A Chebychev low-pass filter with a ripple of 1 dB to attenuate high frequencies

The combined response of these filters is shown in Figure 8−8.

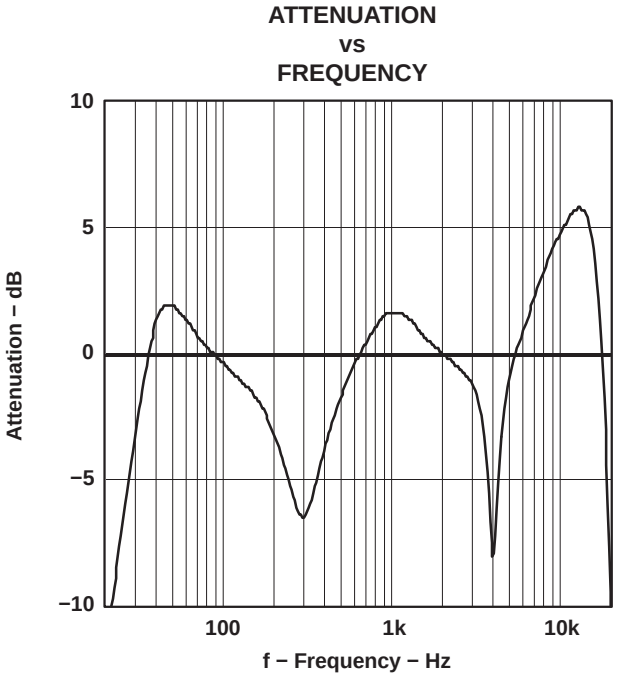


Figure 8−8. Combined Response

8.7 Converting Analog Filters to Digital

Many audio engineers may already be using analog equalization. If a satisfactory set of analog filters has already been defined, the user can convert those analog filters to digital. This is perhaps the easiest way to get started. For converting analog filters to digital, refer to *Digital Signal Processing*, A. V. Oppenheim, R. W. Schafer, Prentice-Hall, 1975, pp. 197–211. This information is also available in almost any digital signal processing textbook. Users of Matlab can perform these manipulations easily using the BILINEAR or IMPINVAR commands available in the Matlab signal processing toolbox.

9 Automatic Loudspeaker Equalizer

To simplify the process of designing digital filters for implementation in the TAS3001, Texas Instruments provides a filter design tool called the *Automatic Loudspeaker Equalizer* or ALE. Details of this tool are provided in this section.

9.1 Automatic Generation of Equalization Filters Given a Measurement

ALE has the capability of reading in a speaker or environment measurement. The user can then provide the desired speaker response. From these two inputs, ALE can automatically produce an optimized set of filters to equalize the speaker. The patent-pending optimization algorithm was developed at Texas Instruments. An example of its operation is shown in Figure 8−3 through Figure 8−6.

9.2 Automatic Approximation of an Equalization Curve

When the desired equalization transfer function is known, the problem becomes one of finding a set of digital second-order IIR filters to implement it. In the case where H(s) is known, it can be converted to a digital filter using a bilinear or impulse invariant method. The resulting transfer function (H(z) can then be factored and implemented as a combination of second- and first-order sections using the TAS3001. (This factoring capability is not included in ALE, but can be accomplished simply in Matlab.) However, in many cases the desired transfer function can be specified as a curve. In this case, the curve can be read by ALE. Then an approximation to it can be generated manually (see the *Manual Filter Generation* section below) or automatically. In the automatic mode, ALE again uses the patent-pending optimization technique developed at Texas Instruments.

9.3 Manual Filter Design

In many cases, the user already has filter specifications and just needs a way of designing such filters. In such cases, ordinary filter parameters, such as gain, bandwidth, and center frequency can be entered into ALE, which then provides coefficients for the desired filters. As filters are generated, ALE displays the responses of individual filters and the composite filter response. In addition, the manual filter generation capability can be used in conjunction with the automatic capability (see Section 9.2, *Automatic Approximation of an Equalization Curve*). The user can specify filters manually and allow ALE to optimize them and generate additional filters automatically as needed. The user can also specify manual filters and let ALE automatically generate additional filters as needed but without disturbing the manually-generated filters. In addition, the user can manually modify the filters created by ALE. A graphical user interface allows easy manipulation of filters and movement between automatic and manual filter generation modes.

9.4 Conversion of Decimal Filter Coefficients to the TAS3001 Format

The filters generated in ALE can be saved in the TAS3001 hexadecimal format (4 integer bits, 20 fraction bits, 2's complement). ALE can read in filters in decimal and convert them to the hexadecimal format needed for implementation in the TAS3001.

9.5 Editing of TAS3001 File Format

ALE can read and write filter files in the TAS3001 format. This allows the filters generated to be stored in the format used by the TAS3001 control software. In addition, ALE can read TAS3001 filter files and display the filters.

9.6 Examples of the Filter Types Available From ALE 2.1

At the current time the following filter types can be designed by ALE:

Equalization (bell-shaped) filters with a variety of center frequencies (Qs) and gains, as shown in Figure 9−1.

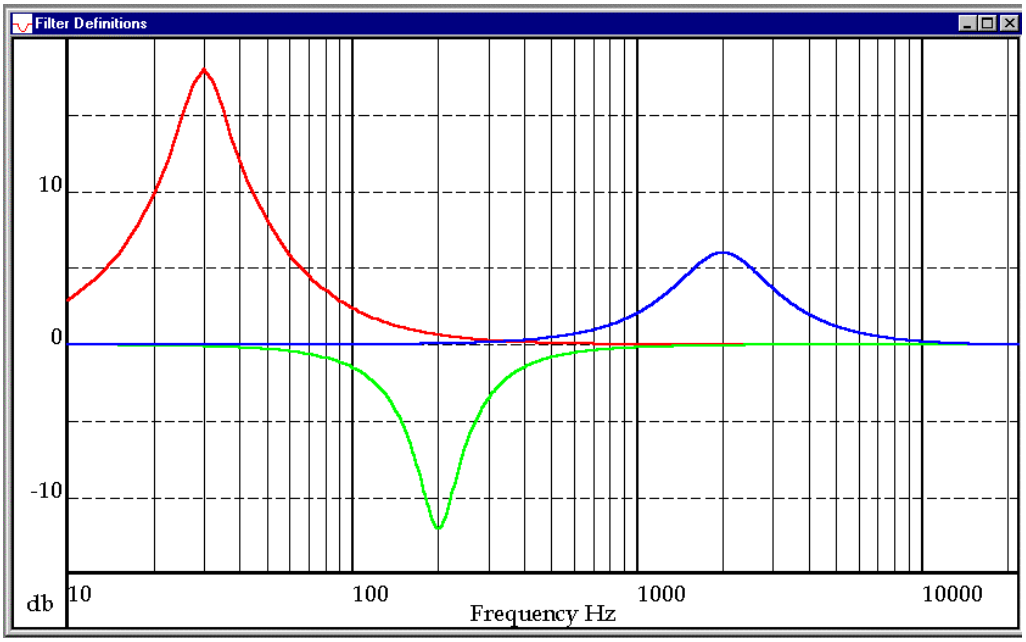


Figure 9−1. Equalization Filters

Similarly, the system can design a variety of high- and low-pass filters such as Butterworth, Linkwitz-Riley, and Type 1 Chebychev. Examples of Butterworth, Linkwitz-Riley, high- and low-pass filters with equal cut frequencies (and a pass-band ripple specification of 1 dB for the Chebychev filters), are shown in Figure 9−2.

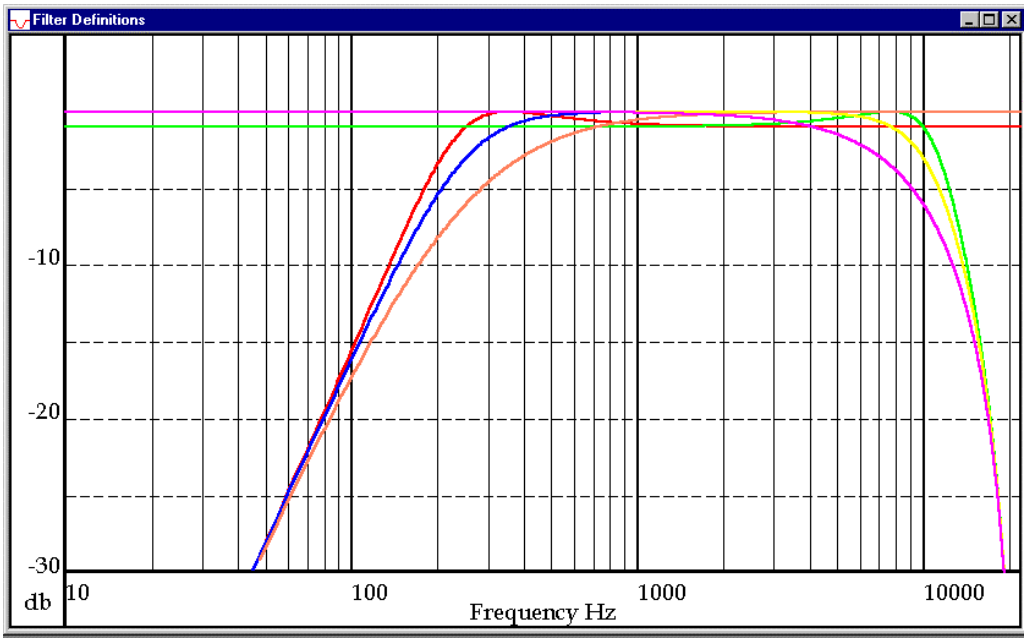


Figure 9−2. High- and Low-Pass Filters

Treble and bass shelf filters can be employed with various gains and corner frequencies as shown in Figure 9−3.

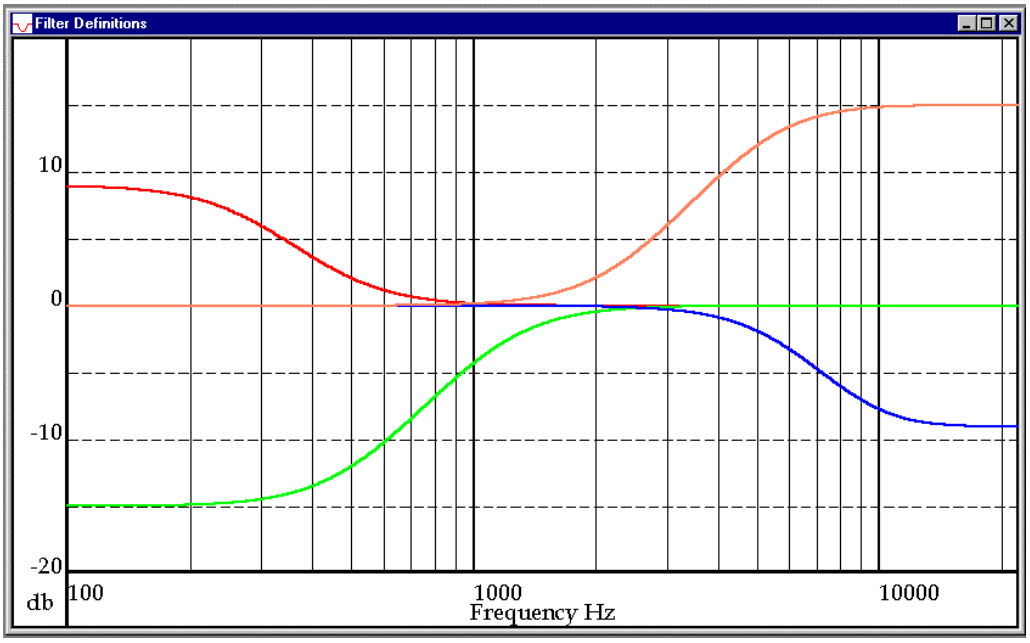


Figure 9−3. Treble and Bass Shelf Filters

Notch filters can be employed to remove energy that excites mechanical resonances in loudspeakers as shown in Figure 9−4.

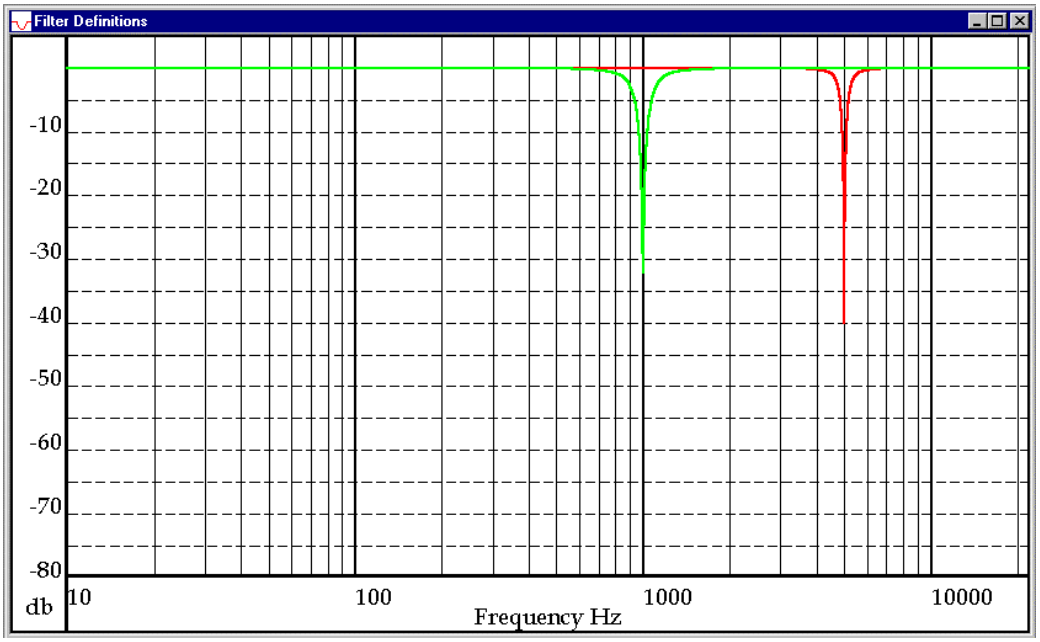


Figure 9−4. Notch Filters

ALE 3.2 also supports a number of filters which are not shown here, including Chebychev I, high/low plateau, Linkwitz-Riley, and variable Q. As new versions of ALE are developed, more filter types will be added. In addition, Texas Instruments filtering engineers are available to help TAS3001 users design any needed filter type.

10 FilterBuilder and FilterMaker

To make filter creation as simple as possible for everyone, Texas Instruments can provide two tools in addition to ALE (previous section). FilterBuilder is an Excel spreadsheet based manual filter creation tool. While not nearly as capable as ALE, it is a simple and effective way to get started quickly with filter creation.

FilterMaker is another manual filter creation tool created by Texas Instruments. It runs in the Matlab environment. This might be the choice of those who prefer to work in Matlab or who would like to add additional capabilities to their filter generation tool. In addition, Texas Instruments engineers can add additional filter types in either one of these two tools.

Appendix A
Software Interface

Table A−1. Register Map

REGISTER	ADDRESS	NO. OF BYTES	BYTE DESCRIPTION
Reserved	00h		
MCR	01h	1	C(7−0)
Reserved	02h	2	Reserved
Reserved	03h		
Volume†	04h	6	VL(23−16), VL(15−8), VL(7−0), VR(23−16), VR(15−8), VR(7−0)
Treble	05h	1	T(7−0)
Bass	06h	1	B(7−0)
Mixer 1‡	07h	3	S(23−16), S(15−8), S(7−0)
Mixer 2‡	08h	3	S(23−16), S(15−8), S(7−0)
Reserved	09h		
Left Biquad 0	0Ah	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Left Biquad 1‡	0Bh	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Left Biquad 2‡	0Ch	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Left Biquad 3‡	0Dh	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Left Biquad 4‡	0Eh	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Left Biquad 5‡	0Fh	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0) A_2(23−16), A_2(15−8), A_2(7−0)
Reserved	10h−12h		
Right Biquad 0‡	13h	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Right Biquad 1‡	14h	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Right Biquad 2‡	15h	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Right Biquad 3‡	16h	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Right Biquad 4‡	17h	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Right Biquad 5‡	18h	15	B_0(23−16), B_0(15−8), B_0(7−0), B_1(23−16), B_1(15−8), B_1(7−0), B_2(23−16), B_2(15−8), B_2(7−0), A_1(23−16), A_1(15−8), A_1(7−0), A_2(23−16), A_2(15−8), A_2(7−0)
Reserved	19h−FFh		

† The volume value is a 4.16 coefficient. In order to transmit it over I^2C, it is necessary to separate the value into three bytes. Byte 2 (MSB) is the integer part and bytes 1 and 0 are the fractional part.

‡ The mixer gain values and biquad coefficients are 4.20 coefficients. In order to transmit them over I^2C, it is necessary to separate the value into three bytes. The first nibble of byte 2 (MSB) is the integer part; the second nibble of byte 2 and bytes 1 and 0 are the fractional part.

A.1 Main Control Register (MCR)

Configuration of the digital serial audio interface is set up through the main control register as shown in Table A−2 and Table A−3. Bits F0 and F1 allow selection between three different serial data formats (left justified = 00, right justified = 01, and I^2S standard = 10). The output serial port mode set by E0 and E1 must be set to the same value as the input serial port mode set by F0 and F1. Bits W0 and W1 allow selection between three different word widths (16-bit word = 00, 18-bit word = 01, and 20-bit word = 10). The SC bit selects $32f_S$ (0) or $64f_S$ (1) bit clock. The FL bit is primarily for use during initialization and is defined in *Device Initialization* (see Section 5.1). See Section 3, *Serial Control Interface*, for additional information on how to address the main control register.

Table A−2. Main Control Register (MCR)

C7	C6	C5	C4	C3	C2	C1	C0
FL	SC	E1	E0	F1	F0	W1	W0
1	x	x	x	x	x	x	x

Table A−3. Main Control Register (MCR) Description

BIT	DESCRIPTOR	FUNCTION	VALUE	FUNCTION
C(7)	FL	Fast load	0	Normal operating mode
			1 (default)	Fast load mode
C(6)	SC	SCLK frequency	0	SCLK = 32 × f_S
			1	SCLK = 64 × f_S
C(5,4)	E(1,0)	Output serial port mode	00	Left justified
			01	Right justified
			10	I^2S
			11	Reserved
C(3,2)	F(1,0)	Input serial port mode	00	Left justified
			01	Right justified
			10	I^2S
			11	Reserved
C(1,0)	W(1,0)	Serial port word length	00	16 bit
			01	18 bit
			10	20 bit
			11	Reserved

Table A−4. Volume Gain Values
[The gain error is less than 0.12 dB (excluding mute)]

GAIN (dB)	VOLUME V(23−16), V(15−8), V(7−0)
18.0	07, F1, 7B
17.5	07, 7F, BB
17.0	07, 14, 57
16.5	06, AE, F6
16.0	06, 4F, 40
15.5	05, F4, E5
15.0	05, 9F, 98
14.5	05, 4F, 10
14.0	05, 03, 0A
13.5	04, BB, 44
13.0	04, 77, 83
12.5	04, 37, 8B
12.0	03, FB, 28
11.5	03, C2, 25
11.0	03, 8C, 53
10.5	03, 59, 83
10.0	03, 29, 8B
9.5	02, FC, 42
9.0	02, D1, 82
8.5	02, A9, 25
8.0	02, 83, 0B
7.5	02, 5F, 12
7.0	02, 3D, 1D
6.5	02, 1D, 0E
6.0	01, FE, CA
5.5	01, E2, 37
5.0	01, C7, 3D
4.5	01, AD, C6
4.0	01, 95, BC
3.5	01, 7F, 09
3.0	01, 69, 9C
2.5	01, 55, 62
2.0	01, 42, 49
1.5	01, 30, 42
1.0	01, 1F, 3D
0.5	01, 0F, 2B

GAIN (dB)	VOLUME V(23−16), V(15−8), V(7−0)
0.0	01, 00, 00
−0.5	00, F1, AE
−1.0	00, E4, 29
−1.5	00, D7, 66
−2.0	00, CB, 59
−2.5	00, BF, F9
−3.0	00, B5, 3C
−3.5	00, AB, 19
−4.0	00, A1, 86
−4.5	00, 98, 7D
−5.0	00, 8F, F6
−5.5	00, 87, E8
−6.0	00, 80, 4E
−6.5	00, 79, 20
−7.0	00, 72, 5A
−7.5	00, 6B, F4
−8.0	00, 65, EA
−8.5	00, 60, 37
−9.0	00, 5A, D5
−9.5	00, 55, C0
−10.0	00, 50, F4
−10.5	00, 4C, 6D
−11.0	00, 48, 27
−11.5	00, 44, 1D
−12.0	00, 40, 4E
−12.5	00, 3C, B5
−13.0	00, 39, 50
−13.5	00, 36, 1B
−14.0	00, 33, 14
−14.5	00, 30, 39
−15.0	00, 2D, 86
−15.5	00, 2A, FA
−16.0	00, 28, 93
−16.5	00, 26, 4E
−17.0	00, 24, 29
−17.5	00, 22, 23

GAIN (dB)	VOLUME V(23−16), V(15−8), V(7−0)
−18.0	00, 20, 3A
−18.5	00, 1E, 6D
−19.0	00, 1C, B9
−19.5	00, 1B, 1E
−20.0	00, 19, 9A
−20.5	00, 18, 2B
−21.0	00, 16, D1
−21.5	00, 15, 8A
−22.0	00, 14, 56
−22.5	00, 13, 33
−23.0	00, 12, 20
−23.5	00, 11, 1C
−24.0	00, 10, 27
−24.5	00, 0F, 40
−25.0	00, 0E, 65
−25.5	00, 0D, 97
−26.0	00, 0C, D5
−26.5	00, 0C, 1D
−27.0	00, 0B, 6F
−27.5	00, 0A, CC
−28.0	00, 0A, 31
−28.5	00, 09, 9F
−29.0	00, 09, 15
−29.5	00, 08, 93
−30.0	00, 08, 18
−30.5	00, 07, A5
−31.0	00, 07, 37
−31.5	00, 06, D0
−32.0	00, 06, 6E
−32.5	00, 06, 12
−33.0	00, 05, BB
−33.5	00, 05, 69
−34.0	00, 05, 1C
−34.5	00, 04, D2
−35.0	00, 04, 8D
−35.5	00, 04, 4C

GAIN (dB)	VOLUME V(23−16), V(15−8), V(7−0)
−36.0	00, 04, 0F
−36.5	00, 03, D5
−37.0	00, 03, 9E
−37.5	00, 03, 6A
−38.0	00, 03, 39
−38.5	00, 03, 0B
−39.0	00, 02, DF
−39.5	00, 02, B6
−40.0	00, 02, 8F
−40.5	00, 02, 6B
−41.0	00, 02, 48
−41.5	00, 02, 27
−42.0	00, 02, 09
−42.5	00, 01, EB
−43.0	00, 01, D0
−43.5	00, 01, B6
−44.0	00, 01, 9E
−44.5	00, 01, 86
−45.0	00, 01, 71
−45.5	00, 01, 5C
−46.0	00, 01, 48
−46.5	00, 01, 36
−47.0	00, 01, 25
−47.5	00, 01, 14
−48.0	00, 01, 05
−48.5	00, 00, F6
−49.0	00, 00, E9
−49.5	00, 00, DC
−50.0	00, 00, CF
−50.5	00, 00, C4
−51.0	00, 00, B9
−51.5	00, 00, AE
−52.0	00, 00, A5
−52.5	00, 00, 9B
−53.0	00, 00, 93
−53.5	00, 00, 8B

GAIN (dB)	VOLUME V(23−16), V(15−8), V(7−0)
−54.0	00, 00, 83
−54.5	00, 00, 7B
−55.0	00, 00, 75
−55.5	00, 00, 6E
−56.0	00, 00, 68
−56.5	00, 00, 62
−57.0	00, 00, 5D
−57.5	00, 00, 57
−58.0	00, 00, 53
−58.5	00, 00, 4E
−59.0	00, 00, 4A
−59.5	00, 00, 45
−60.0	00, 00, 42
−60.5	00, 00, 3E
−61.0	00, 00, 3A
−61.5	00, 00, 37
−62.0	00, 00, 34
−62.5	00, 00, 31
−63.0	00, 00, 2E
−63.5	00, 00, 2C
−64.0	00, 00, 29
−64.5	00, 00, 27
−65.0	00, 00, 25
−65.5	00, 00, 23
−66.0	00, 00, 21
−66.5	00, 00, 1F
−67.0	00, 00, 1D
−67.5	00, 00, 1C
−68.0	00, 00, 1A
−68.5	00, 00, 19
−69.0	00, 00, 17
−69.5	00, 00, 16
−70.0	00, 00, 15
Mute	00, 00, 00

Table A−5. Treble Control Register
(Both left and right channel will be given the same treble gain setting)

Gain (dB)	T(7−0) (hex)	Gain (dB)	T(7−0) (hex)	Gain (dB)	T(7−0) (hex)	Gain (dB)	T(7−0) (hex)	Gain (dB)	T(7−0) (hex)
18.0	01h	10.5	4Ch	3.0	6Bh	−4.5	7Bh	−12.0	8Ah
17.5	09h	10.0	4Fh	2.5	6Ch	−5.0	7Ch	−12.5	8Bh
17.0	10h	9.5	52h	2.0	6Dh	−5.5	7Dh	−13.0	8Ch
16.5	16h	9.0	55h	1.5	6Eh	−6.0	7Eh	−13.5	8Dh
16.0	1Ch	8.5	57h	1.0	70h	−6.5	7Fh	−14.0	8Eh
15.5	22h	8.0	5Ah	0.5	71h	−7.0	80h	−14.5	8Fh
15.0	28h	7.5	5Ch	0.0	72h	−7.5	81h	−15.0	90h
14.5	2Dh	7.0	5Eh	−0.5	73h	−8.0	82h	−15.5	91h
14.0	32h	6.5	60h	−1.0	74h	−8.5	83h	−16.0	92h
13.5	36h	6.0	62h	−1.5	75h	−9.0	84h	−16.5	93h
13.0	3Ah	5.5	63h	−2.0	76h	−9.5	85h	−17.0	94h
12.5	3Eh	5.0	65h	−2.5	77h	−10.0	86h	−17.5	95h
12.0	42h	4.5	66h	−3.0	78h	−10.5	87h	−18.0	96h
11.5	45h	4.0	68h	−3.5	79h	−11.0	88h		
11.0	49h	3.5	69h	−4.0	7Ah	−11.5	89h		

Table A−6. Bass Control Register
(Both left and right channel will be given the same bass setting)

Gain (dB)	B(7−0) (hex)	Gain (dB)	B(7−0) (hex)	Gain (dB)	B(7−0) (hex)	Gain (dB)	B(7−0) (hex)	Gain (dB)	B(7−0) (hex)
18.0	01h	10.5	19h	3.0	35h	−4.5	51h	−12.0	6Bh
17.5	03h	10.0	1Ch	2.5	36h	−5.0	53h	−12.5	6Dh
17.0	06h	9.5	1Fh	2.0	38h	−5.5	54h	−13.0	6Eh
16.5	08h	9.0	21h	1.5	39h	−6.0	55h	−13.5	70h
16.0	0Ah	8.5	23h	1.0	3Bh	−6.5	56h	−14.0	72h
15.5	0Bh	8.0	25h	0.5	3Ch	−7.0	58h	−14.5	74h
15.0	0Dh	7.5	26h	0.0	3E	−7.5	59h	−15.0	76h
14.5	0Fh	7.0	28h	−0.5	40h	−8.0	5Ah	−15.5	78h
14.0	10h	6.5	29h	−1.0	42h	−8.5	5Ch	−16.0	7Ah
13.5	12h	6.0	2Bh	−1.5	44h	−9.0	5Dh	−16.5	7Dh
13.0	13h	5.5	2Ch	−2.0	46h	−9.5	5Fh	−17.0	7Fh
12.5	14h	5.0	2Eh	−2.5	49h	−10.0	61h	−17.5	82h
12.0	16h	4.5	30h	−3.0	4Bh	−10.5	64h	−18.0	86h
11.5	17h	4.0	31h	−3.5	4Dh	−11.0	66h		
11.0	18h	3.5	33h	−4.0	4Fh	−11.5	69h		

Table A−7. Mixer1 and Mixer2 Gain Values
[The gain error is less than 0.12 dB (excluding mute)]

Gain (dB)	Gain S(23−16), S(15−8), S(7−0)
18.0	7F, 17, AF
17.5	77, FB, AA
17.0	71, 45, 75
16.5	6A, EF, 5D
16.0	64, F4, 03
15.5	5F, 4E, 52
15.0	59, F9, 80
14.5	54, F1, 06
14.0	50, 30, A1
13.5	4B, B4, 46
13.0	47, 78, 28
12.5	43, 78, B0
12.0	3F, B2, 78
11.5	3C, 22, 4C
11.0	38, C5, 28
10.5	35, 98, 2F
10.0	32, 98, B0
9.5	2F, C4, 20
9.0	2D, 18, 18
8.5	2A, 92, 54
8.0	28, 30, AF
7.5	25, F1, 25
7.0	23, D1, CD
6.5	21, D0, D9
6.0	1F, EC, 98
5.5	1E, 23, 6D
5.0	1C, 73, D5
4.5	1A, DC, 61
4.0	19, 5B, B8
3.5	17, F0, 94
3.0	16, 99, C0
2.5	15, 56, 1A
2.0	14, 24, 8E
1.5	13, 04, 1A
1.0	11, F3, C9
0.5	10, F2, B4

Gain (dB)	Gain S(23−16), S(15−8), S(7−0)
0.0	10, 00, 00
−0.5	0F, 1A, DF
−1.0	0E, 42, 90
−1.5	0D, 76, 5A
−2.0	0C, B5, 91
−2.5	0B, FF, 91
−3.0	0B, 53, BE
−3.5	0A, B1, 89
−4.0	0A, 18, 66
−4.5	09, 87, D5
−5.0	08, FF, 59
−5.5	08, 7E, 80
−6.0	08, 04, DC
−6.5	07, 92, 07
−7.0	07, 25, 9D
−7.5	06, BF, 44
−8.0	06, 5E, A5
−8.5	06, 03, 6E
−9.0	05, AD, 50
−9.5	05, 5C, 04
−10.0	05, 0F, 44
−10.5	04, C6, D0
−11.0	04, 82, 68
−11.5	04, 41, D5
−12.0	04, 04, DE
−12.5	03, CB, 50
−13.0	03, 94, FA
−13.5	03, 61, AF
−14.0	03, 31, 42
−14.5	03, 03, 8A
−15.0	02, D8, 62
−15.5	02, AF, A3
−16.0	02, 89, 2C
−16.5	02, 64, DB
−17.0	02, 42, 93
−17.5	02, 22, 35

Gain (dB)	Gain S(23−16), S(15−8), S(7−0)
−18.0	02, 03, A7
−18.5	01, E6, CF
−19.0	01, CB, 94
−19.5	01, B1, DE
−20.0	01, 99, 99
−20.5	01, 82, AF
−21.0	01, 6D, 0E
−21.5	01, 58, A2
−22.0	01, 45, 5B
−22.5	01, 33, 28
−23.0	01, 21, F9
−23.5	01, 11, C0
−24.0	01, 02, 70
−24.5	00, F3, FB
−25.0	00, E6, 55
−25.5	00, D9, 73
−26.0	00, CD, 49
−26.5	00, C1, CD
−27.0	00, B6, F6
−27.5	00, AC, BA
−28.0	00, A3, 10
−28.5	00, 99, F1
−29.0	00, 91, 54
−29.5	00, 89, 33
−30.0	00, 81, 86
−30.5	00, 7A, 48
−31.0	00, 73, 70
−31.5	00, 6C, FB
−32.0	00, 66, E3
−32.5	00, 61, 21
−33.0	00, 5B, B2
−33.5	00, 56, 91
−34.0	00, 51, B9
−34.5	00, 4D, 27
−35.0	00, 48, D6
−35.5	00, 44, C3

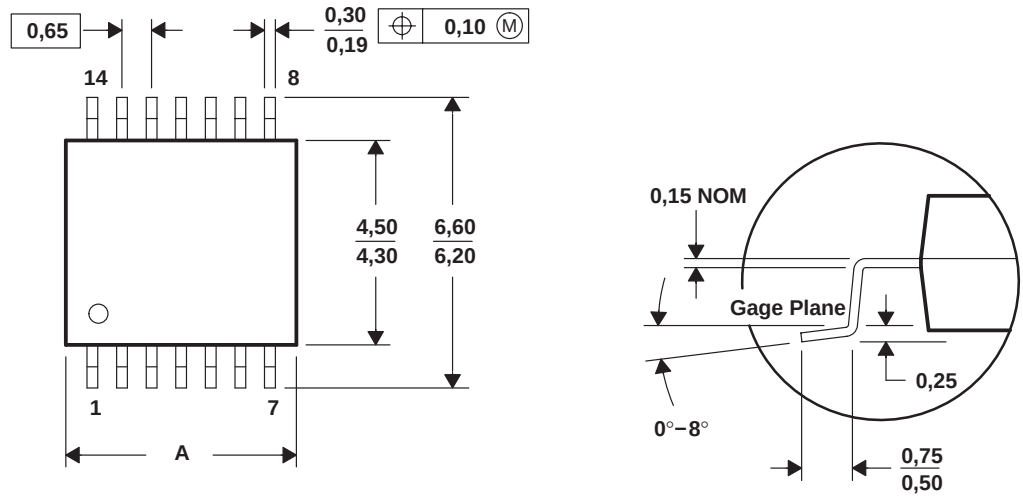
Gain (dB)	Gain S(23−16), S(15−8), S(7−0)
−36.0	00, 40, EA
−36.5	00, 3D, 49
−37.0	00, 39, DB
−37.5	00, 36, 9E
−38.0	00, 33, 90
−38.5	00, 30, AE
−39.0	00, 2D, F5
−39.5	00, 2B, 63
−40.0	00, 28, F5
−40.5	00, 26, AB
−41.0	00, 24, 81
−41.5	00, 22, 76
−42.0	00, 20, 89
−42.5	00, 1E, B7
−43.0	00, 1C, FF
−43.5	00, 1B, 60
−44.0	00, 19, D8
−44.5	00, 18, 65
−45.0	00, 17, 08
−45.5	00, 15, BE
−46.0	00, 14, 87
−46.5	00, 13, 61
−47.0	00, 12, 4B
−47.5	00, 11, 45
−48.0	00, 10, 4E
−48.5	00, 0F, 64
−49.0	00, 0E, 88
−49.5	00, 0D, B8
−50.0	00, 0C, F3
−50.5	00, 0C, 3A
−51.0	00, 0B, 8B
−51.5	00, 0A, E5
−52.0	00, 0A, 49
−52.5	00, 09, B6
−53.0	00, 09, 2B
−53.5	00, 08, A8

Gain (dB)	Gain S(23−16), S(15−8), S(7−0)
−54.0	00, 08, 2C
−54.5	00, 07, B7
−55.0	00, 07, 48
−55.5	00, 06, E0
−56.0	00, 06, 7D
−56.5	00, 06, 20
−57.0	00, 05, C9
−57.5	00, 05, 76
−58.0	00, 05, 28
−58.5	00, 04, DE
−59.0	00, 04, 98
−59.5	00, 04, 56
−60.0	00, 04, 18
−60.5	00, 03, DD
−61.0	00, 03, A6
−61.5	00, 03, 72
−62.0	00, 03, 40
−62.5	00, 03, 12
−63.0	00, 02, E6
−63.5	00, 02, BC
−64.0	00, 02, 95
−64.5	00, 02, 70
−65.0	00, 02, 4D
−65.5	00, 02, 2C
−66.0	00, 02, 0D
−66.5	00, 01, F0
−67.0	00, 01, D4
−67.5	00, 01, BA
−68.0	00, 01, A1
−68.5	00, 01, 8A
−69.0	00, 01, 74
−69.5	00, 01, 5F
−70.0	00, 01, 4B
Mute	00, 00, 00

Appendix B
Mechanical Information

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TAS3001CPW	NRND	TSSOP	PW	28	50	None	CU NIPDAU	Level-2-220C-1 YEAR
TAS3001CPWR	NRND	TSSOP	PW	28	2000	None	CU NIPDAU	Level-2-220C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
None: Not yet available Lead (Pb-Free).
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

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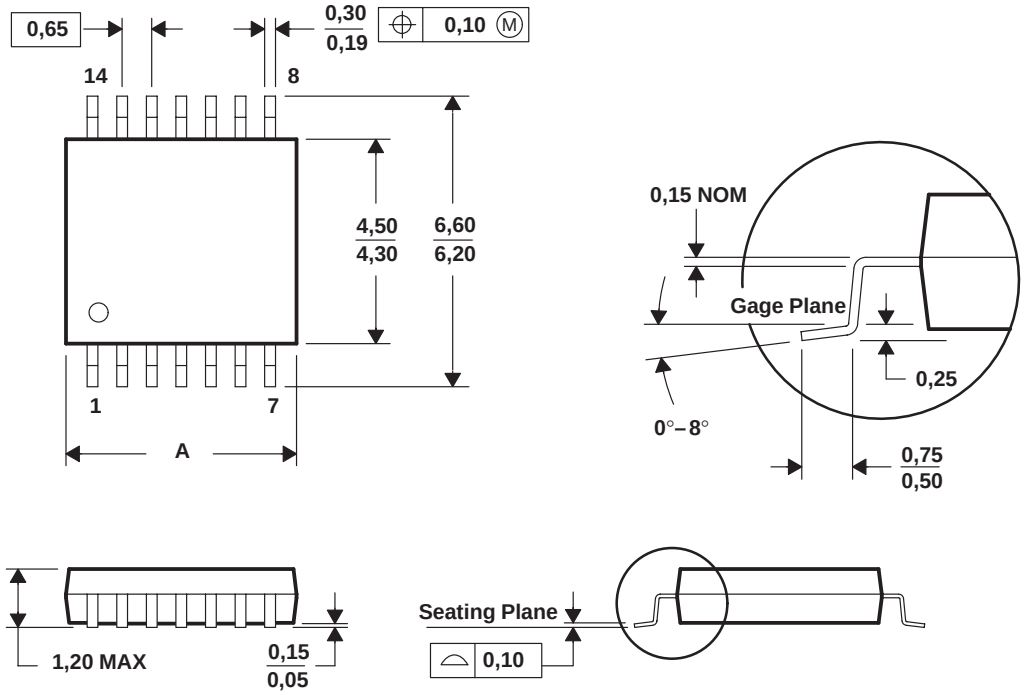
PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153