Reinforced, Fast, Low-Power, Four-Channel Digital Isolators

MAX22444–MAX22446

General Description

The MAX22444–MAX22446 are reinforced, fast, low-power 4-channel digital galvanic isolators using Maxim's proprietary process technology. These devices transfer digital signals between circuits with different power domains, using as little as 0.74mW per channel at 1Mbps (1.8V supply). All of the devices in the family feature reinforced isolation for a withstand voltage rating of $5kV_{RMS}$ for 60 seconds.

The MAX22444–MAX22446 family offers all possible unidirectional channel configurations to accommodate any 4-channel design, including SPI, RS-485, and digital I/O applications. Output enable for the A side of the MAX22445R/S/U/V is active-low, making them ideal for isolating a port on a shared SPI bus since the $\overline{CS}$ signal can directly enable the MISO signal on the isolator. All other output enables in the MAX22444-MAX22446 family are the traditional active-high.

All channels on the MAX22444–MAX22446M/N are always enabled, however, the default state of the outputs of these devices is selectable.

Devices are available with a maximum data rate of either 25Mbps or 200Mbps, and with outputs that are either default-high or default-low. The default is the state the output assumes when the input is either not powered or is open-circuit. See the Ordering Information and Product Selector Guide for suffixes associated with each option. Independent 1.71V to 5.5V supplies on each side of the isolator also make the devices suitable for use as level translators.

All of the devices in the MAX22444–MAX22446 family are available in a 16-pin wide-body SOIC package with 8mm of creepage and clearance. The package material has a minimum comparative tracking index (CTI) of 400, which gives it a group II rating in creepage tables. All devices are rated for operation at ambient temperatures of -40°C to +125°C.

Benefits and Features

- Reinforced Galvanic Isolation for Fast Digital Signals
  - Up to 200Mbps Maximum Data Rate
  - Withstands $5kV_{RMS}$ for 60s (V_{ISO})
  - Continuously Withstands $1500V_{RMS}$ (V_{IOWM})
  - Withstands ±12.8kV Surge Between GNDA and GNDB with 1.2/50µs waveform
  - High CMTI (50kV/µs, Typical)
- Low Power Consumption
  - 0.74mW per Channel at 1Mbps with V_{DD} = 1.8V
  - 1.4mW per Channel at 1Mbps with V_{DD} = 3.3V
  - 3.2mW per Channel at 100Mbps with V_{DD} = 1.8V
- Options to Support a Broad Range of Applications
  - 2 Maximum Data Rates (200Mbps, 25Mbps)
  - 3 Direction Configurations
  - Active-High or Active-Low Enable Inputs
  - 2 Fixed Output Default States (High/Low) or Pin-Selectable (M/N Versions)

Applications

- Isolated SPI Interface
- Fieldbus Communications for Industrial Automation
- Isolated RS-485/RS-422, CAN
- Battery Management
- Medical Systems

Safety Regulatory Approvals

- UL According to UL1577
- cUL According to CSA Bulletin 5A
- VDE 0884-11 Reinforced Isolation

***Ordering Information* and *Product Selector Guide* appear at end of data sheet.**

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Absolute Maximum Ratings

V_{DDA} to GNDA ..... -0.3V to +6V
V_{DDB} to GNDB ..... -0.3V to +6V
IN_ on Side A, ENA, $\overline{ENA}$, DEFA to GNDA ..... -0.3V to +6V
IN_ on Side B, ENB, DEFB to GNDB ..... -0.3V to +6V
OUT_ on Side A to GNDA ..... -0.3V to (V_{DDA} + 0.3V)
OUT_ on Side B to GNDB ..... -0.3V to (V_{DDB} + 0.3V)
Short-Circuit Continuous Current
OUT_ on Side A to GNDA,
OUT_ on Side B to GNDB ..... ±30mA

Continuous Power Dissipation (T_A = +70°C)
Wide SOIC (derate 14.1mW/°C above +70°C) 1126.8mW
Operating Temperature Range ..... -40°C to +125°C
Maximum Junction Temperature ..... +150°C
Storage Temperature Range ..... -60°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 16 Wide SOIC	
Package Code	W16MS+12
Outline Number	**21-0042**
Land Pattern Number	**90-0107**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	71°C/W
Junction to Case (θ_{JC})	24°C/W

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

DC Electrical Characteristics

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage	V_{DDA}	Relative to GNDA	1.71		5.5	V
	V_{DDB}	Relative to GNDB	1.71		5.5	
Undervoltage-Lockout Threshold	$V_{UVLO_}$	$V_{DD_}$ rising	1.5	1.6	1.66	V
Undervoltage-Lockout Threshold Hysteresis	V_{UVLO_HYST}			45		mV

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Side A Supply Current (MAX22444_) (Note 2)	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.54	1.00	mA
			V_{DDA} = 3.3V		0.53	0.97	
			V_{DDA} = 2.5V		0.52	0.96	
			V_{DDA} = 1.8V		0.50	0.68	
		12.5MHz square wave, C_L = 0pF	V_{DDA} = 5V		1.67	2.50	
			V_{DDA} = 3.3V		1.64	2.43	
			V_{DDA} = 2.5V		1.62	2.41	
			V_{DDA} = 1.8V		1.58	2.07	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		4.63	6.31	
			V_{DDA} = 3.3V		4.53	6.17	
			V_{DDA} = 2.5V		4.48	6.11	
			V_{DDA} = 1.8V		4.34	5.60	
Side B Supply Current (MAX22444_) (Note 2)	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.19	2.06	mA
			V_{DDB} = 3.3V		1.17	2.02	
			V_{DDB} = 2.5V		1.17	2.01	
			V_{DDB} = 1.8V		1.14	1.92	
		12.5MHz square wave, C_L = 0pF	V_{DDB} = 5V		2.28	3.29	
			V_{DDB} = 3.3V		1.85	2.79	
			V_{DDB} = 2.5V		1.68	2.58	
			V_{DDB} = 1.8V		1.51	2.33	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		5.66	7.07	
			V_{DDB} = 3.3V		3.98	5.16	
			V_{DDB} = 2.5V		3.28	4.34	
			V_{DDB} = 1.8V		2.69	3.59	
Side A Supply Current (MAX22445_) (Note 2)	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.70	1.26	mA
			V_{DDA} = 3.3V		0.69	1.23	
			V_{DDA} = 2.5V		0.68	1.22	
			V_{DDA} = 1.8V		0.66	0.99	
		12.5MHz square wave, C_L = 0pF	V_{DDA} = 5V		1.83	2.70	
			V_{DDA} = 3.3V		1.70	2.53	
			V_{DDA} = 2.5V		1.63	2.45	
			V_{DDA} = 1.8V		1.56	2.14	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		4.89	6.51	
			V_{DDA} = 3.3V		4.39	5.93	
			V_{DDA} = 2.5V		4.18	5.67	
			V_{DDA} = 1.8V		3.93	5.11	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Side B Supply Current (MAX22445_) (Note 2)	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		1.03	1.80	mA
			V_{DDB} = 3.3V		1.01	1.76	
			V_{DDB} = 2.5V		1.01	1.75	
			V_{DDB} = 1.8V		0.98	1.61	
		12.5MHz square wave, C_L = 0pF	V_{DDB} = 5V		2.13	3.09	
			V_{DDB} = 3.3V		1.80	2.70	
			V_{DDB} = 2.5V		1.66	2.54	
			V_{DDB} = 1.8V		1.53	2.27	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		5.41	6.88	
			V_{DDB} = 3.3V		4.11	5.41	
			V_{DDB} = 2.5V		3.58	4.78	
			V_{DDB} = 1.8V		3.11	4.11	
Side A Supply Current (MAX22446_) (Note 2)	I_{DDA}	500kHz square wave, C_L = 0pF	V_{DDA} = 5V		0.87	1.53	mA
			V_{DDA} = 3.3V		0.85	1.49	
			V_{DDA} = 2.5V		0.84	1.49	
			V_{DDA} = 1.8V		0.82	1.30	
		12.5MHz square wave, C_L = 0pF	V_{DDA} = 5V		1.98	2.89	
			V_{DDA} = 3.3V		1.75	2.61	
			V_{DDA} = 2.5V		1.65	2.49	
			V_{DDA} = 1.8V		1.55	2.20	
		50MHz square wave, C_L = 0pF	V_{DDA} = 5V		5.15	6.69	
			V_{DDA} = 3.3V		4.25	5.66	
			V_{DDA} = 2.5V		3.88	5.22	
			V_{DDA} = 1.8V		3.52	4.60	
Side B Supply Current (MAX22446_) (Note 2)	I_{DDB}	500kHz square wave, C_L = 0pF	V_{DDB} = 5V		0.87	1.53	mA
			V_{DDB} = 3.3V		0.85	1.49	
			V_{DDB} = 2.5V		0.84	1.49	
			V_{DDB} = 1.8V		0.82	1.30	
		12.5MHz square wave, C_L = 0pF	V_{DDB} = 5V		1.98	2.89	
			V_{DDB} = 3.3V		1.75	2.61	
			V_{DDB} = 2.5V		1.65	2.49	
			V_{DDB} = 1.8V		1.55	2.20	
		50MHz square wave, C_L = 0pF	V_{DDB} = 5V		5.15	6.69	
			V_{DDB} = 3.3V		4.25	5.66	
			V_{DDB} = 2.5V		3.88	5.22	
			V_{DDB} = 1.8V		3.52	4.60	

DC Electrical Characteristics (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 1, 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
LOGIC INTERFACE (IN_, EN_, $\overline{ENA}$, DEF_, OUT_)							
Input High Voltage	V_{IH}	EN_, $\overline{ENA}$, IN_	2.25V ≤ $V_{DD_}$ ≤ 5.5V	0.7 x $V_{DD_}$			V
			1.71V ≤ $V_{DD_}$ < 2.25V	0.75 x $V_{DD_}$			
		DEF_ (Note 2)	2.25V ≤ $V_{DD_}$ ≤ 5.5V	0.7 x $V_{DD_}$			
			1.71V ≤ $V_{DD_}$ < 2.25V	0.75 x $V_{DD_}$			
Input Low Voltage	V_{IL}	EN_, $\overline{ENA}$, IN_	2.25V ≤ $V_{DD_}$ ≤ 5.5V			0.8	V
			1.71V ≤ $V_{DD_}$ < 2.25V			0.7	
		DEF_ (Note 2)	2.25V ≤ $V_{DD_}$ ≤ 5.5V			0.8	
			1.71V ≤ $V_{DD_}$ < 2.25V			0.7	
Input Hysteresis	V_{HYS}	EN_, $\overline{ENA}$, DEF_, IN_	MAX2244_B/E/M/R/U		410		mV
			MAX2244_C/F/N/S/V		80		
IN_ Input Pullup Current	I_{PU}	MAX2244_B/C/R/S		-10	-5	-1.5	µA
		MAX2244_M/N, DEFA = DEFB = high		-10	-5	-1.5	
IN_ Input Pulldown Current	I_{PD}	MAX2244_E/F/U/V		1.5	5	10	µA
		MAX2244_M/N, DEFA = DEFB = low		1.5	5	10	
IN_ Input Capacitance	C_{IN}	f_{SW} = 1MHz			2		pF
ENA Pullup Current	I_{PU_ENA}	MAX2244_B/C/E/F		-10	-5	-1.5	µA
ENB Pullup Current	I_{PU_ENB}	MAX2244_B/C/E/F/R/S/U/V		-10	-5	-1.5	µA
$\overline{ENA}$ Pulldown Current	I_{PD_EN}	MAX22445R/S/U/V		1.5	5	10	µA
DEF_ Pullup Current	I_{PU_DEF}	MAX2244_M/N		-10	-5	-1.5	µA
OUT_ Output Voltage High	V_{OH}	$I_{OUT_}$ = -4mA source		$V_{DD_}$ - 0.4			V
OUT_ Output Voltage Low	V_{OL}	$I_{OUT_}$ = 4mA sink				0.4	V

Dynamic Characteristics MAX2244_C/F/N/S/V

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or $V_{DD_}$ (Note 5)			50		kV/µs
Maximum Data Rate	DR_{MAX}	2.25V ≤ $V_{DD_}$ ≤ 5.5V		200			Mbps
		1.71V ≤ $V_{DD_}$ < 2.25V		150			
Minimum Pulse Width	PW_{MIN}	IN_ to OUT_	2.25V ≤ $V_{DD_}$ ≤ 5.5V			5.00	ns
			1.71V ≤ $V_{DD_}$ < 2.25V			6.67	
Propagation Delay (Figure 3)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V	4.1	5.7	9.2	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V	4.2	6.5	10.2	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V	4.9	7.9	13.4	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V	7.1	12.0	20.3	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V	4.3	6.1	9.4	
			3.0V ≤ $V_{DD_}$ ≤ 3.6V	4.4	6.9	10.5	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V	5.1	8.2	14.1	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V	7.2	12.1	21.7	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ $V_{DD_}$ ≤ 5.5V		0.4	2.0	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V		0.4	2.0	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V		0.3	2.0	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V		0.0	2.0	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD_}$ ≤ 5.5V				3.7	ns
		3.0V ≤ $V_{DD_}$ ≤ 3.6V				4.3	
		2.25V ≤ $V_{DD_}$ ≤ 2.75V				6.0	
		1.71V ≤ $V_{DD_}$ ≤ 1.89V				10.3	
	t_{SPHL}	4.5V ≤ $V_{DD_}$ ≤ 5.5V				3.8	
		3.0V ≤ $V_{DD_}$ ≤ 3.6V				4.7	
		2.25V ≤ $V_{DD_}$ ≤ 2.75V				6.5	
		1.71V ≤ $V_{DD_}$ ≤ 1.89V				11.5	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	1.71V ≤ $V_{DD_}$ ≤ 5.5V				2.0	ns
	t_{SCSHL}	1.71V ≤ $V_{DD_}$ ≤ 5.5V				2.0	

Dynamic Characteristics MAX2244_C/F/N/S/V (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	4.5V ≤ $V_{DD_}$ ≤ 5.5V				2.9	ns
		3.0V ≤ $V_{DD_}$ ≤ 3.6V				3.4	
		2.25V ≤ $V_{DD_}$ ≤ 2.75V				4.9	
		1.71V ≤ $V_{DD_}$ ≤ 1.89V				10.2	
	t_{SCOHL}	4.5V ≤ $V_{DD_}$ ≤ 5.5V				3.2	
		3.0V ≤ $V_{DD_}$ ≤ 3.6V				3.8	
		2.25V ≤ $V_{DD_}$ ≤ 2.75V				5.3	
		1.71V ≤ $V_{DD_}$ ≤ 1.89V				10.9	
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	200Mbps			100		ps
Clock Jitter RMS	$T_{JCLK(RMS)}$	500kHz clock input, rising/falling edges			7.5		ps
Rise Time (Figure 3)	t_R	C_L = 5pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V			0.8	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V			1.1	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V			1.5	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V			2.4	
Fall Time (Figure 3)	t_F	C_L = 5pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V			1.0	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V			1.4	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V			1.9	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V			3.0	
Enable to Data Valid (MAX2244_C/F/S/V only, Figure 4)	t_{EN}	$\overline{ENA}$ to OUT_, EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V			3.9	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V			6.4	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V			10.1	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V			18.4	
Enable to Tristate (MAX2244_C/F/S/V only, Figure 4)	t_{TRI}	$\overline{ENA}$ to OUT_, EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V			6.3	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V			9.0	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V			12.6	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V			19.2	

Dynamic Characteristics MAX2244_B/E/M/R/U

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Transient Immunity	CMTI	IN_ = GND_ or VDD_ (Note 5)			50		kV/µs
Maximum Data Rate	DR_{MAX}			25			Mbps
Minimum Pulse Width	PW_{MIN}	IN_ to OUT_				40	ns
Glitch Rejection		IN_ to OUT_		10	17	29	ns
Propagation Delay (Figure 3)	t_{PLH}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V	17.4	24.2	32.5	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V	17.6	25.0	33.7	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V	18.3	26.4	36.7	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V	20.7	30.6	43.5	
	t_{PHL}	IN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V	16.9	24.0	33.6	
			3.0V ≤ $V_{DD_}$ ≤ 3.6V	17.2	24.8	35.1	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V	17.8	26.1	38.2	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V	19.8	30.0	45.8	
Pulse Width Distortion	PWD	$\lvert t_{PLH} - t_{PHL} \rvert$	4.5V ≤ $V_{DD_}$ ≤ 5.5V		0.2	4.0	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V		0.2	4.0	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V		0.3	4.0	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V		0.6	4.0	
Propagation Delay Skew Part-to-Part (Same Channel)	t_{SPLH}	4.5V ≤ $V_{DD_}$ ≤ 5.5V				15.1	ns
		3.0V ≤ $V_{DD_}$ ≤ 3.6V				15.0	
		2.25V ≤ $V_{DD_}$ ≤ 2.75V				15.4	
		1.71V ≤ $V_{DD_}$ ≤ 1.89V				20.5	
	t_{SPHL}	4.5V ≤ $V_{DD_}$ ≤ 5.5V				13.9	
		3.0V ≤ $V_{DD_}$ ≤ 3.6V				14.2	
		2.25V ≤ $V_{DD_}$ ≤ 2.75V				16.0	
		1.71V ≤ $V_{DD_}$ ≤ 1.89V				21.8	
Propagation Delay Skew Channel-to-Channel (Same Direction)	t_{SCSLH}	1.71V ≤ $V_{DD_}$ ≤ 5.5V				2.0	ns
	t_{SCSHL}	1.71V ≤ $V_{DD_}$ ≤ 5.5V				2.0	
Propagation Delay Skew Channel-to-Channel (Opposite Direction)	t_{SCOLH}	4.5V ≤ $V_{DD_}$ ≤ 5.5V				13.9	ns
		3.0V ≤ $V_{DD_}$ ≤ 3.6V				13.7	
		2.25V ≤ $V_{DD_}$ ≤ 2.75V				14.2	
		1.71V ≤ $V_{DD_}$ ≤ 1.89V				19.4	
	t_{SCOHL}	4.5V ≤ $V_{DD_}$ ≤ 5.5V				13.0	
		3.0V ≤ $V_{DD_}$ ≤ 3.6V				12.9	
		2.25V ≤ $V_{DD_}$ ≤ 2.75V				14.4	
		1.71V ≤ $V_{DD_}$ ≤ 1.89V				20.1	

Dynamic Characteristics MAX2244_B/E/M/R/U (continued)

(V_{DDA} - V_{GNDA} = 1.71V to 5.5V, V_{DDB} - V_{GNDB} = 1.71V to 5.5V, C_L = 15pF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{DDA} - V_{GNDA} = 3.3V, V_{DDB} - V_{GNDB} = 3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.) (Notes 2, 4)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Peak Eye Diagram Jitter	$T_{JIT(PK)}$	25Mbps			250		ps
Rise Time (Figure 3)	t_R	C_L = 5pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V			0.8	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V			1.1	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V			1.5	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V			2.4	
Fall Time (Figure 3)	t_F	C_L = 5pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V			1.0	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V			1.4	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V			1.9	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V			3.0	
Enable to Data Valid (MAX2244_B/E/R/U only, Figure 4)	t_{EN}	$\overline{ENA}$ to OUT_, EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V			3.9	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V			6.4	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V			10.1	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V			18.4	
Enable to Tristate (MAX2244_B/E/R/U only, Figure 4)	t_{TRI}	$\overline{ENA}$ to OUT_, EN_ to OUT_, C_L = 15pF	4.5V ≤ $V_{DD_}$ ≤ 5.5V			6.3	ns
			3.0V ≤ $V_{DD_}$ ≤ 3.6V			9.0	
			2.25V ≤ $V_{DD_}$ ≤ 2.75V			12.6	
			1.71V ≤ $V_{DD_}$ ≤ 1.89V			19.2	

Note 1: All devices are 100% production tested at T_A = +125°C. Specifications over temperature are guaranteed by design and characterization.

Note 2: Not production tested. Guaranteed by design and characterization.

Note 3: All currents into the device are positive. All currents out of the device are negative. All voltages are referenced to their respective ground (GNDA or GNDB), unless otherwise noted.

Note 4: All measurements taken with V_{DDA} = V_{DDB}, unless otherwise noted.

Note 5: CMTI is the maximum sustainable common-mode voltage slew rate while maintaining the correct output. CMTI applies to both rising and falling common-mode voltage edges. Tested with the transient generator connected between GNDA and GNDB (V_{CM} = 1000V).

ESD Protection

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD		Human Body Model, All Pins		±4		kV

Table 1. Insulation Characteristics

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNITS
Partial Discharge Test Voltage	V_{PR}	Method B1 = V_{IORM} x 1.875 (t = 1s, partial discharge < 5pC)	3977	V_P
Maximum Repetitive Peak Isolation Voltage	V_{IORM}	(Note 6)	2121	V_P
Maximum Working Isolation Voltage	V_{IOWM}	Continuous RMS voltage (Note 6)	1500	V_{RMS}
Maximum Transient Isolation Voltage	V_{IOTM}	t = 1s (Note 6)	8000	V_P
Maximum Withstand Isolation Voltage	V_{ISO}	f_{SW} = 60Hz, duration = 60s (Notes 6, 7)	5000	V_{RMS}
Maximum Surge Isolation Voltage	V_{IOSM}	Reinforced Insulation, test method per IEC 60065, V_{TEST} = 1.6 × V_{IOSM} = 12800V_{PEAK} (Notes 6, 9)	8000	V_P
Insulation Resistance	R_{IO}	V_{IO} = 500V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500V at T_S = 150°C	$>10^9$	
Barrier Capacitance Side A to Side B	CIO	f_{SW} = 1MHz (Note 8)	1.5	pF
Minimum Creepage Distance	CPG		8	mm
Minimum Clearance Distance	CLR		8	mm
Internal Clearance		Distance through insulation	0.021	mm
Comparative Tracking Index	CTI	Material Group II (IEC 60112)	>400	
Climate Category			40/125/21	
Pollution Degree (DIN VDE 0110, Table 1)			2	

Note 6: V_{ISO}, V_{IOTM}, V_{IOSM}, V_{IOWM}, and V_{IORM} are defined by the IEC 60747-5-5 standard.
Note 7: Product is qualified at V_{ISO} for 60s and 100% production tested at 120% of V_{ISO} for 1s.
Note 8: Capacitance is measured with all pins on field-side and logic-side tied together.
Note 9: Devices are submerged in oil during surge characterization.

Safety Regulatory Approvals

UL
The MAX22444–MAX22446 are certified under UL1577. For more details, refer to File E351759.
Rated up to 5000V_{RMS} isolation voltage for single protection.
cUL (Equivalent to CSA notice 5A)
The MAX22444–MAX22446 are certified up to 5000V_{RMS} for single protection. For more details, refer to File E351759.
VDE
The MAX22444–MAX22446 are certified to DIN VDE V 0884-11: 2017-1. For details, see file reference 5015017-4880-0002/265080/TL7/SCT; Certificate Number 40049143. Reinforced Insulation, Maximum Transient Isolation Voltage 8000V_{PK}, Maximum Repetitive Peak Isolation Voltage 2121V_{PK}

These couplers are suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Safety Limits

Damage to the IC can result in a low-resistance path to ground or to the supply and, without current limiting, the MAX22444-MAX22446 could dissipate excessive amounts of power. Excessive power dissipation can damage the die and result in damage to the isolation barrier, potentially causing downstream issues. Table 2 shows the safety limits for the MAX22444-MAX22446.

The maximum safety temperature (T_S) for the device is the 150°C maximum junction temperature specified in the Absolute Maximum Ratings. The power dissipation (P_D) and junction-to-ambient thermal impedance (θ_{JA}) determine the junction temperature. Thermal impedance values (θ_{JA} and θ_{JC}) are available in the Package Thermal Characteristics section of the datasheet and power dissipation calculations are discussed in the Calculating Power Dissipation section. Calculate the junction temperature (T_J) as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

Figure 1 and Figure 2 show the thermal derating curve for safety limiting the power and the current of the device. Ensure that the junction temperature does not exceed 150°C.

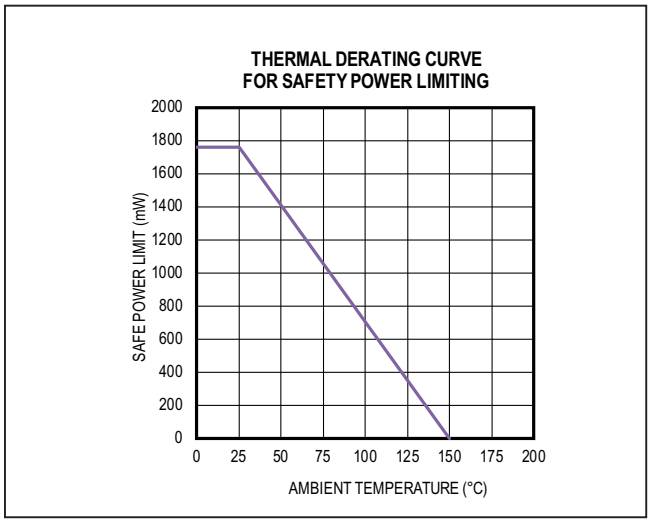


Figure 1. Thermal Derating Curve for Safety Power Limiting

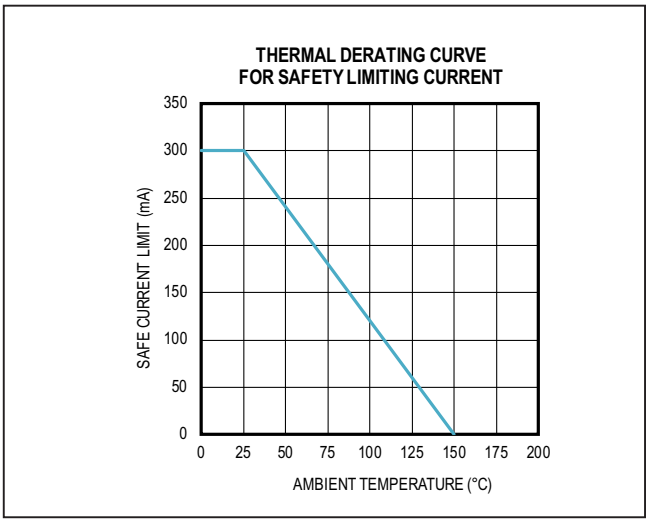


Figure 2. Thermal Derating Curve for Safety Current Limiting

Table 2. Safety Limiting Values for the MAX22444-MAX22446

PARAMETER	SYMBOL	TEST CONDITIONS	MAX	UNIT
Safety Current on Any Pin (No Damage to Isolation Barrier)	I_S	T_J = 150°C, T_A = 25°C	300	mA
Total Safety Power Dissipation	P_S	T_J = 150°C, T_A = 25°C	1760	mW
Maximum Safety Temperature	T_S		150	°C

Test Circuits and Timing Diagrams

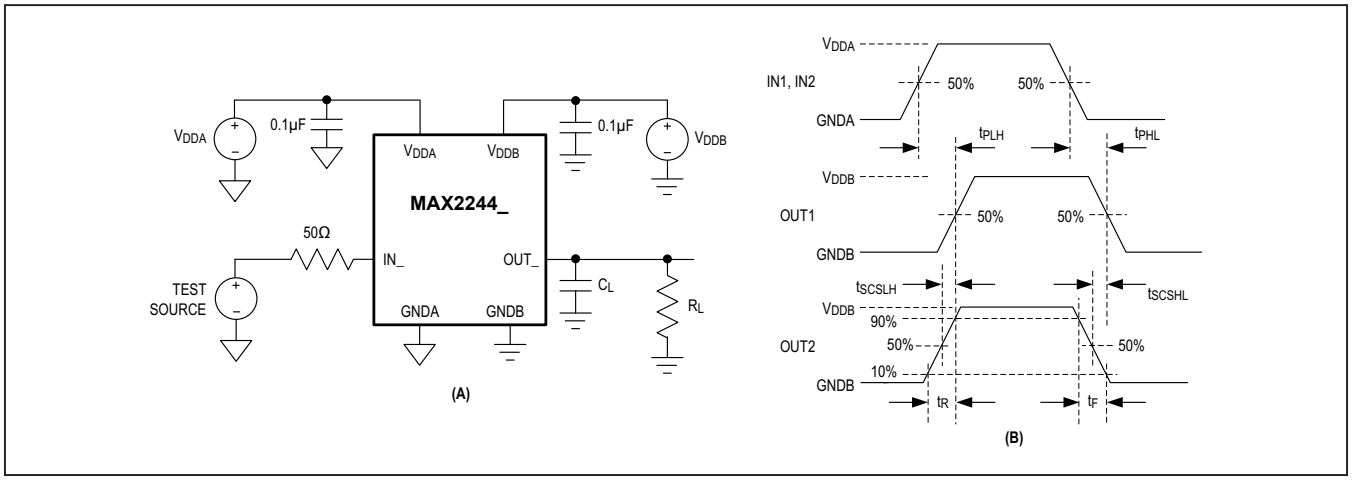


Figure 3. Test Circuit (A) and Timing Diagram (B)

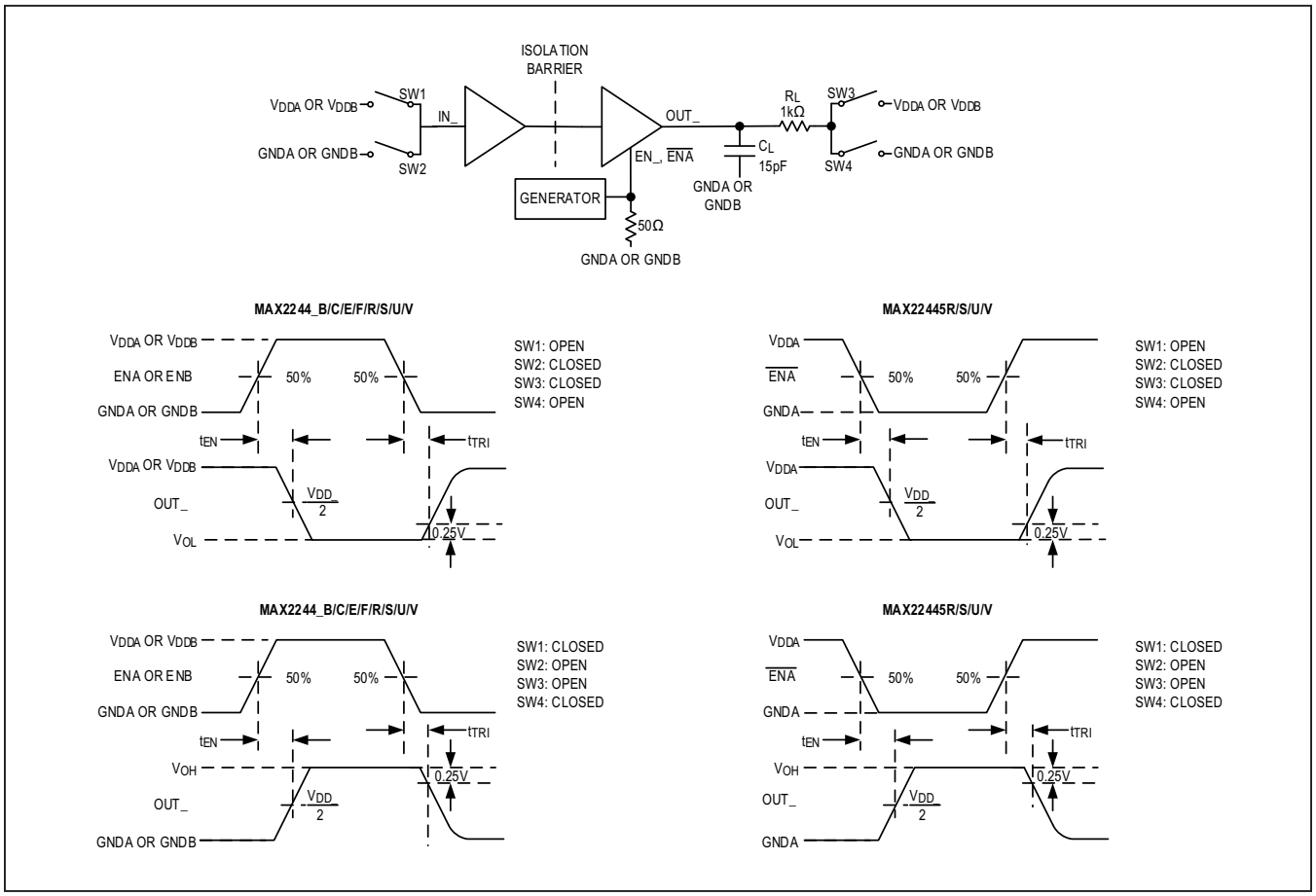
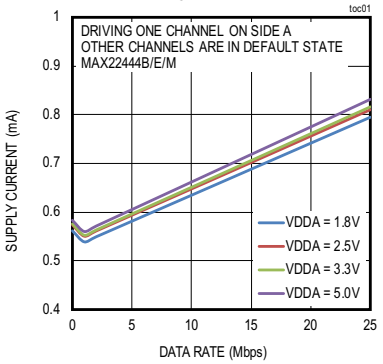


Figure 4. Enable to Output Timing (t_{EN}, t_{TRI})

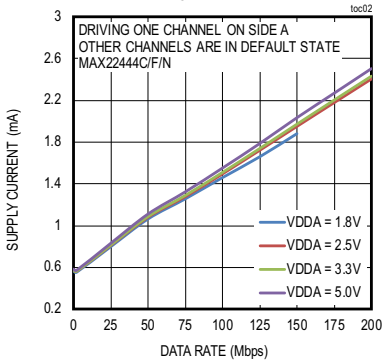
Typical Operating Characteristics

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

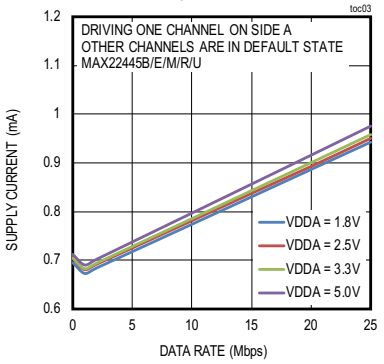
SIDE A SUPPLY CURRENT vs. DATA RATE



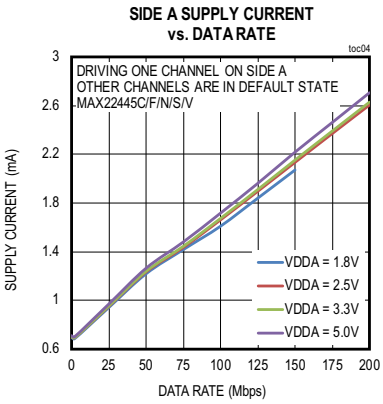
SIDE A SUPPLY CURRENT vs. DATA RATE



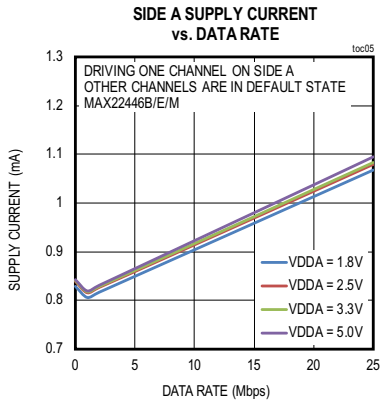
SIDE A SUPPLY CURRENT vs. DATA RATE



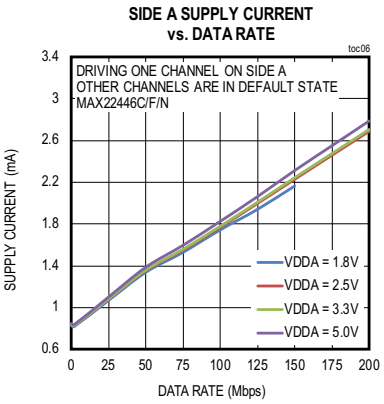
SIDE A SUPPLY CURRENT vs. DATA RATE



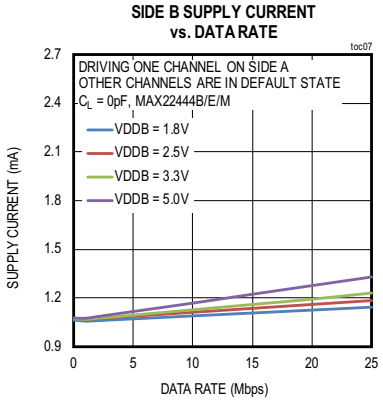
SIDE A SUPPLY CURRENT vs. DATA RATE



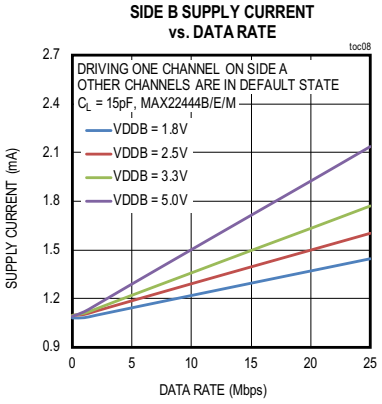
SIDE A SUPPLY CURRENT vs. DATA RATE



SIDE B SUPPLY CURRENT vs. DATA RATE



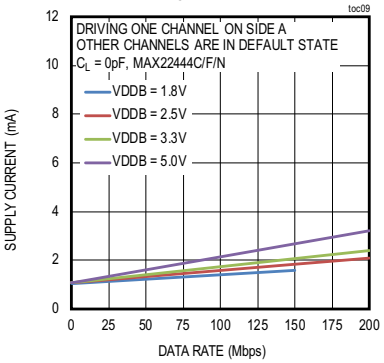
SIDE B SUPPLY CURRENT vs. DATA RATE



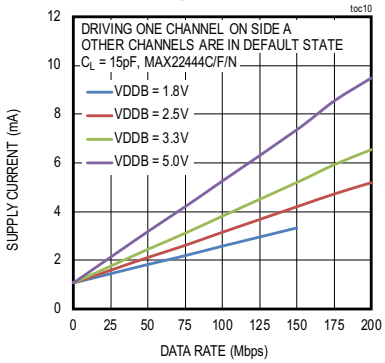
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

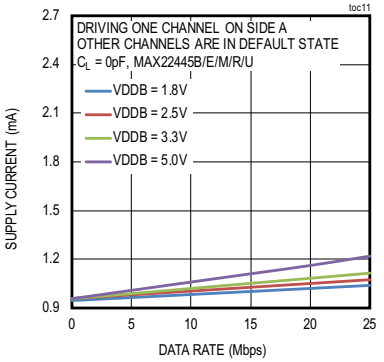
SIDE B SUPPLY CURRENT vs. DATA RATE



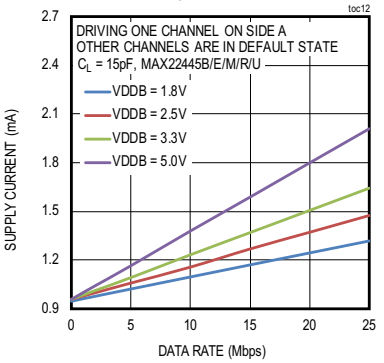
SIDE B SUPPLY CURRENT vs. DATA RATE



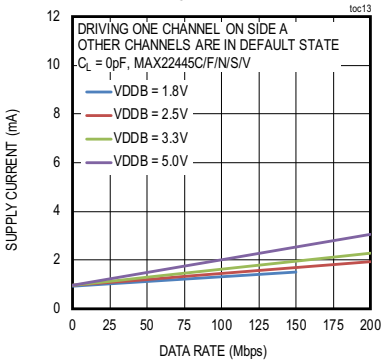
SIDE B SUPPLY CURRENT vs. DATA RATE



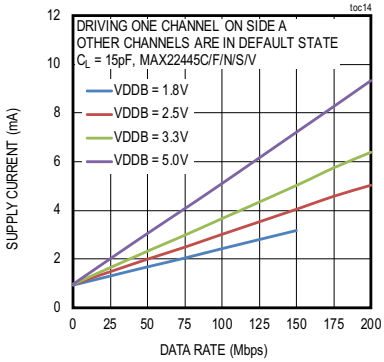
SIDE B SUPPLY CURRENT vs. DATA RATE



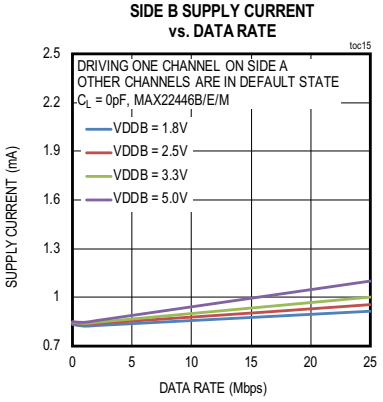
SIDE B SUPPLY CURRENT vs. DATA RATE



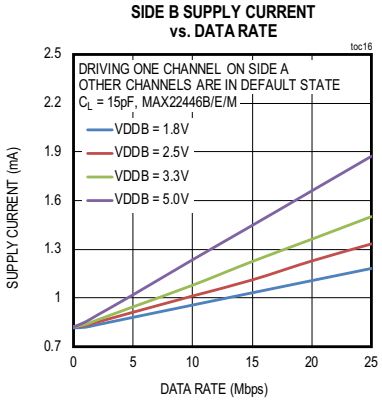
SIDE B SUPPLY CURRENT vs. DATA RATE



SIDE B SUPPLY CURRENT vs. DATA RATE



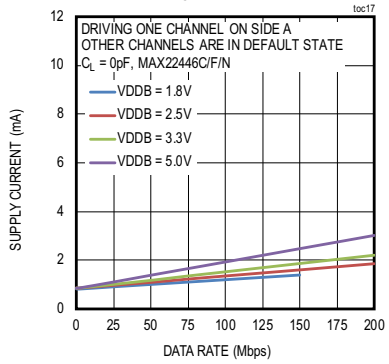
SIDE B SUPPLY CURRENT vs. DATA RATE



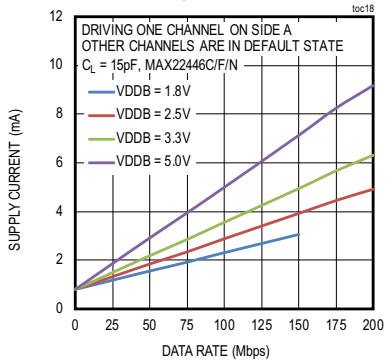
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

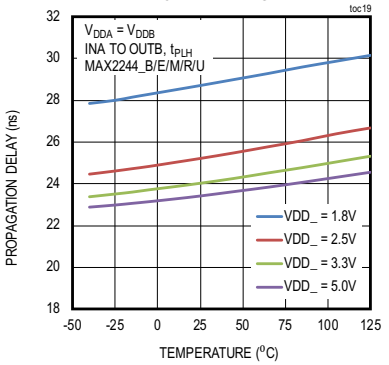
SIDE B SUPPLY CURRENT vs. DATA RATE



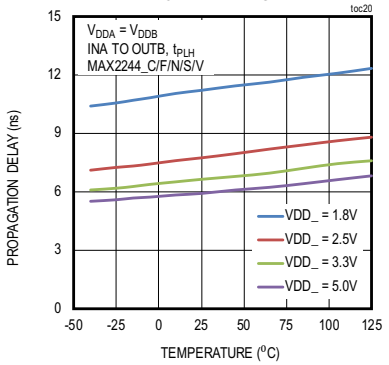
SIDE B SUPPLY CURRENT vs. DATA RATE



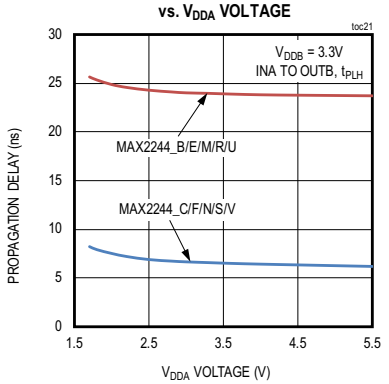
PROPAGATION DELAY vs. TEMPERATURE



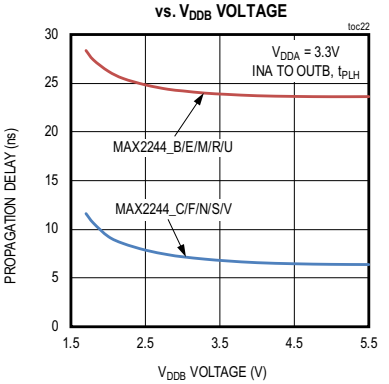
PROPAGATION DELAY vs. TEMPERATURE



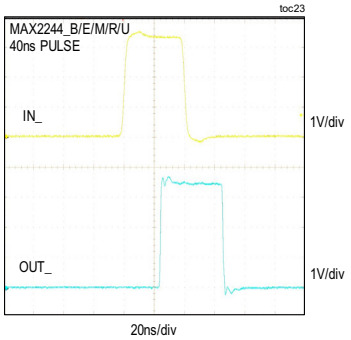
PROPAGATION DELAY vs. V_{DDA} VOLTAGE



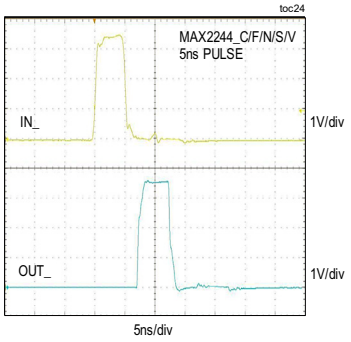
PROPAGATION DELAY vs. V_{DDB} VOLTAGE



MINIMUM PULSE WIDTH



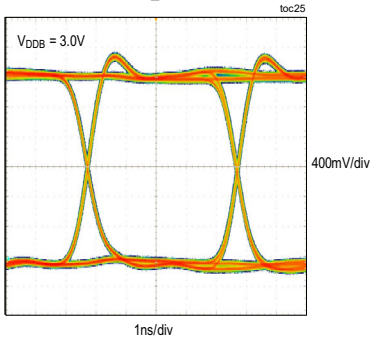
MINIMUM PULSE WIDTH



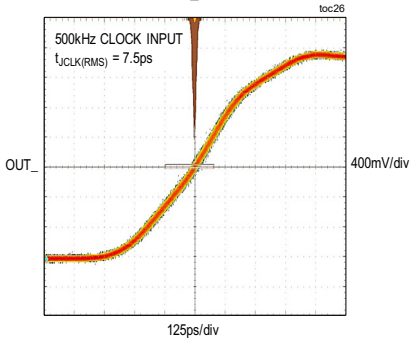
Typical Operating Characteristics (continued)

(V_{DDA} - V_{GNDA} = +3.3V, V_{DDB} - V_{GNDB} = +3.3V, V_{GNDA} = V_{GNDB}, T_A = +25°C, unless otherwise noted.)

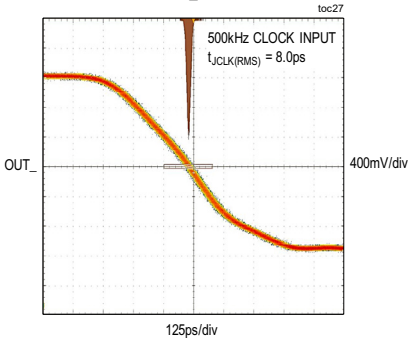
EYE DIAGRAM AT 200MBPS
MAX2244_C/F/N/S/V



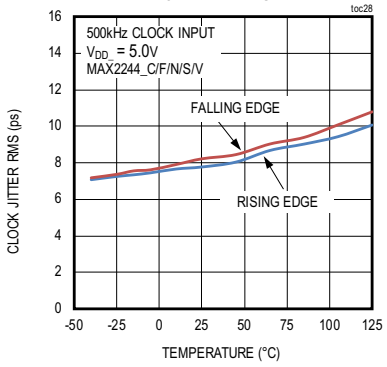
CLOCK JITTER RMS ON RISING EDGE
MAX2244_C/F/N/S/V



CLOCK JITTER RMS ON FALLING EDGE
MAX2244_C/F/N/S/V

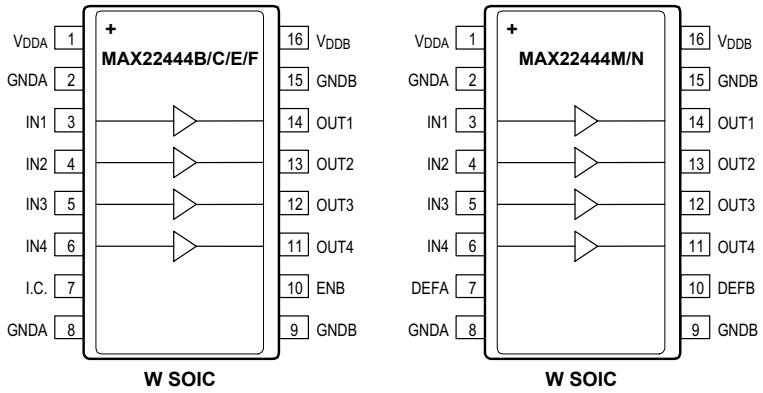


CLOCK JITTER RMS
vs. TEMPERATURE

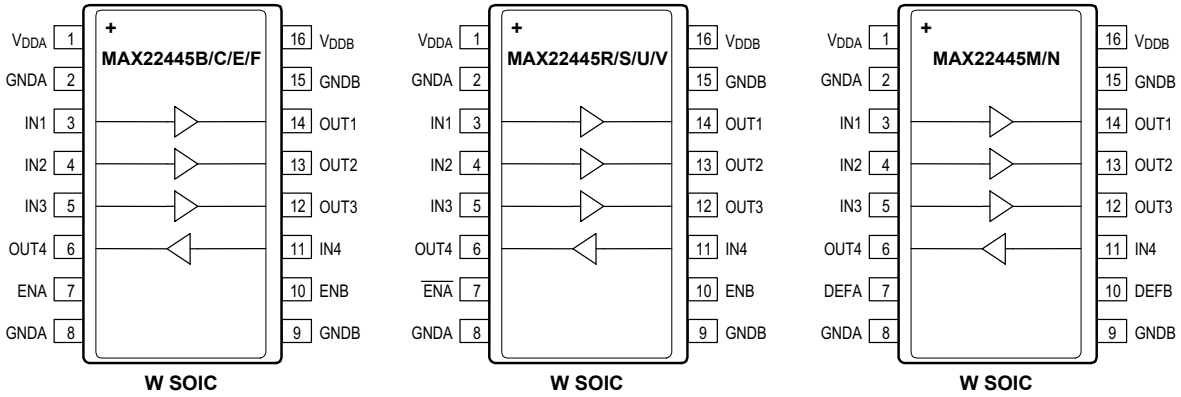


Pin Configurations

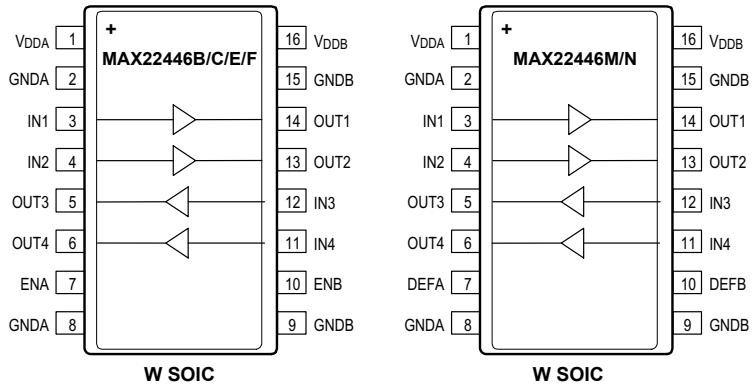
TOP VIEW



TOP VIEW



TOP VIEW



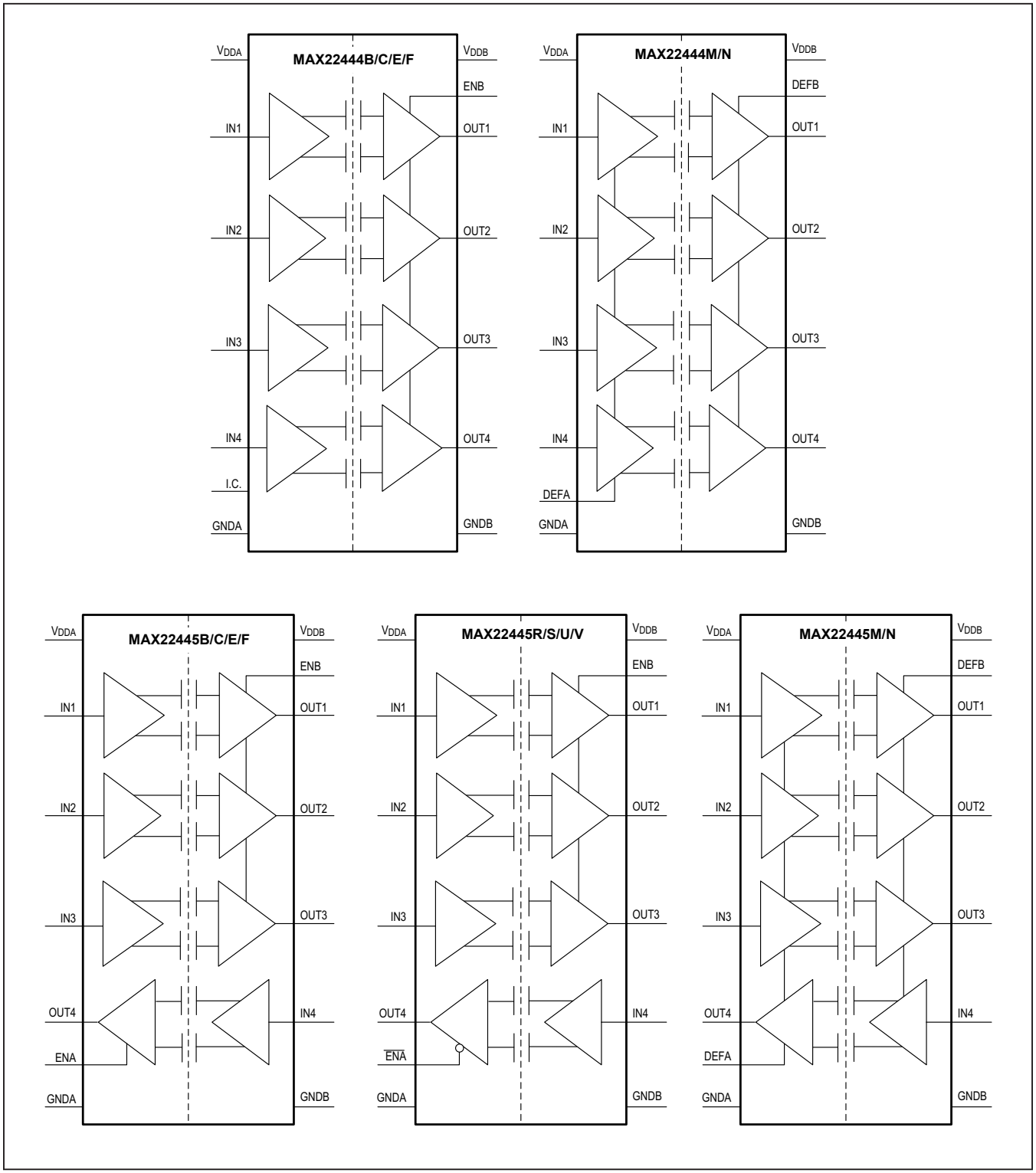
Pin Description

NAME	PIN						
	MAX22444 B/C/E/F	MAX22444 M/N	MAX22445 B/C/E/F	MAX22445 R/S/U/V	MAX22445 M/N	MAX22446 B/C/E/F	MAX22446 M/N
V_{DDA}	1	1	1	1	1	1	1
GNDA	2, 8	2, 8	2, 8	2, 8	2, 8	2, 8	2, 8
IN1	3	3	3	3	3	3	3
IN2	4	4	4	4	4	4	4
IN3	5	5	5	5	5	12	12
IN4	6	6	11	11	11	11	11
I.C.	7	—	—	—	—	—	—
DEFA	—	7	—	—	7	—	7
ENA	—	—	7	—	—	7	—
$\overline{ENA}$	—	—	—	7	—	—	—
GNDB	9, 15	9, 15	9, 15	9, 15	9, 15	9, 15	9, 15
ENB	10	—	10	10	—	10	—
DEFB	—	10	—	—	10	—	10
OUT4	11	11	6	6	6	6	6
OUT3	12	12	12	12	12	5	5
OUT2	13	13	13	13	13	13	13
OUT1	14	14	14	14	14	14	14
V_{DDB}	16	16	16	16	16	16	16

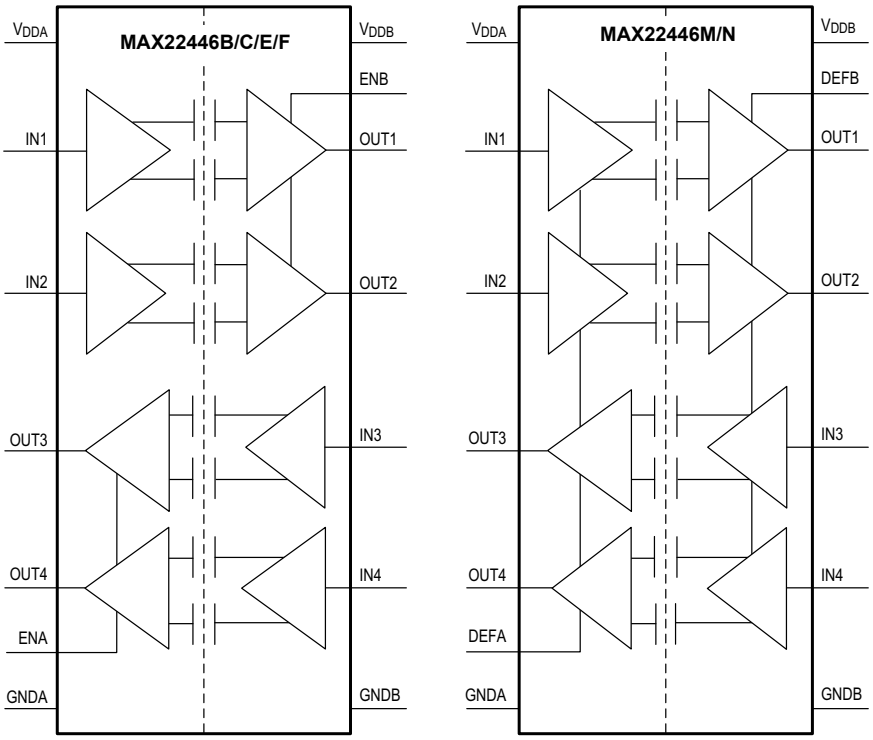
Pin Description (continued)

NAME	FUNCTION
POWER	
V_{DDA}	Power Supply Input for Side A. Bypass V_{DDA} to GNDA with a 0.1µF ceramic capacitor as close as possible to the pin.
GNDA	Ground Reference for Side A.
V_{DDB}	Power Supply Input for Side B. Bypass V_{DDB} to GNDB with a 0.1µF ceramic capacitor as close as possible to the pin.
GNDB	Ground Reference for Side B.
INPUTS	
IN1	Logic Input 1 on Side A. Corresponds to Logic Output 1 on Side B.
IN2	Logic Input 2 on Side A. Corresponds to Logic Output 2 on Side B.
IN3	Logic Input 3 on Side A/B. Corresponds to Logic Output 3 on Side B/A.
IN4	Logic Input 4 on Side A/B. Corresponds to Logic Output 4 on Side B/A.
OUTPUTS	
OUT1	Logic Output 1 on Side B. OUT1 is the logic output for the IN1 input on Side A.
OUT2	Logic Output 2 on Side B. OUT2 is the logic output for the IN2 input on Side A.
OUT3	Logic Output 3 on Side B/A. OUT3 is the logic output for the IN3 input on Side A/B.
OUT4	Logic Output 4 on Side B/A. OUT4 is the logic output for the IN4 input on Side A/B.
ENABLE INPUTS	
ENA	Active-High Enable for Side A. ENA has an internal 5µA pull-up to V_{DDA}.
$\overline{ENA}$	Active-Low Enable for Side A. $\overline{ENA}$ has an internal 5µA pull-down to GNDA.
ENB	Active-High Enable for Side B. ENB has an internal 5µA pull-up to V_{DDB}.
DEFAULT CONTROL	
DEFA	Default Control Input for Side A. Connect DEFA to V_{DDA} to set side A outputs to a default-high state and to enable the pullup current on side A inputs. Connect DEFA to GNDA to set side A outputs to a default-low state and enable the pulldown current on side A inputs. DEFA must be tied to the same state (high or low) as DEFB.
DEFB	Default Control Input for Side B. Connect DEFB to V_{DDB} to set side B outputs to a default-high state and to enable the pullup current on side B inputs. Connect DEFB to GNDB to set side B outputs to a default-low state and enable the pulldown current on side B inputs. DEFB must be tied to the same state (high or low) as DEFA.
INTERNALLY CONNECTED	
I.C.	Internally Connected. Leave unconnected or connect to GNDA or V_{DDA}.

Functional Diagrams



Functional Diagrams (continued)



Detailed Description

The MAX22444–MAX22446 are a family of 4-channel reinforced digital isolators. The MAX22444–MAX22446 have an isolation rating of $5kV_{RMS}$. The MAX22444-MAX22446 family offers all possible unidirectional channel configurations to accommodate any 4-channel design, including SPI, RS-232, RS-485, and digital I/O applications. For applications requiring bidirectional channels, such as I^2C, see the MAX14933 and MAX14937.

The MAX22444 features four channels transferring digital signals in one direction for applications such as isolated digital I/O. The MAX22445 has three channels transmitting data in one direction and one channel transmitting in the opposite direction, making them ideal for applications such as isolated SPI and RS-485 communication. The MAX22446 provides further design flexibility with two channels in each direction for isolated RS-232 or other applications.

Devices are available in a 16-pin wide-body SOIC package and are rated for up to $5kV_{RMS}$. This family of digital isolators offers low-power operation, high electromagnetic interference (EMI) immunity, and stable temperature performance through Maxim's proprietary process technology. The devices isolate different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry.

Devices are available with a maximum data rate of either 25Mbps (B/E/M/R/U versions) or 200Mbps (C/F/N/S/V versions). The MAX2244_B/C/R/S feature default-high outputs. The MAX2244_E/F/U/V feature default-low outputs. The MAX2244_M/N feature user-selectable default-high or default-low outputs. The default is the state the output assumes when the input is not powered or if the input is open-circuit. The devices have two supply inputs (V_{DDA} and V_{DDB}) that independently set the logic levels on either side of the device. V_{DDA} and V_{DDB} are referenced to GNDA and GNDB, respectively. The MAX22444-MAX22446 also feature a refresh circuit to ensure output accuracy when an input remains in the same state indefinitely.

Digital Isolation

The MAX22444-MAX22446 provide reinforced galvanic isolation for digital signals that are transmitted between two ground domains. The devices withstand differences of up to $5kV_{RMS}$ for up to 60 seconds, and up to $2121V_{PEAK}$ of continuous isolation.

Level-Shifting

The wide supply voltage range of both V_{DDA} and V_{DDB} allows the MAX22444-MAX22446 to be used for level translation in addition to isolation. V_{DDA} and V_{DDB} can be independently set to any voltage from 1.71V to 5.5V. The supply voltage sets the logic level on the corresponding side of the isolator.

Unidirectional Channels

Each channel of the MAX22444-MAX22446 is unidirectional; it only passes data in one direction, as indicated in the functional diagram. Each device features four unidirectional channels that operate independently with guaranteed data rates from DC up to 25Mbps (B/E/M/R/U versions), or from DC to 200Mbps (C/F/N/S/V versions). The output driver of each channel is push-pull, eliminating the need for pullup resistors. The outputs are able to drive both TTL and CMOS logic inputs.

Startup and Undervoltage-Lockout

The V_{DDA} and V_{DDB} supplies are both internally monitored for undervoltage conditions. Undervoltage events can occur during power-up, power-down, or during normal operation due to a sagging supply voltage. When an undervoltage condition is detected on either supply while the outputs are enabled, all outputs go to their default states regardless of the state of the inputs (Table 3, Table 4, Table 5). Figure 5 through Figure 8 show the behavior of the outputs during power-up and power-down.

Table 3. MAX2244_B/C/E/F Output Behavior During Undervoltage Conditions

$V_{IN_}$	V_{DDA}	V_{DDB}	ENA	ENB	V_{OUTA}	V_{OUTB}
1	Powered	Powered	1	1	High	High
			0	0	Hi-Z	Hi-Z
0	Powered	Powered	1	1	Low	Low
			0	0	Hi-Z	Hi-Z
X	Undervoltage	Powered	1	1	Default	Default
			0	0	Hi-Z	Hi-Z
X	Powered	Undervoltage	1	1	Default	Default
			0	0	Hi-Z	Hi-Z

Table 4. MAX22445R/S/U/V Output Behavior During Undervoltage Conditions

$V_{IN_}$	V_{DDA}	V_{DDB}	$\overline{ENA}$	ENB	V_{OUTA}	V_{OUTB}
1	Powered	Powered	0	1	High	High
			1	0	Hi-Z	Hi-Z
0	Powered	Powered	0	1	Low	Low
			1	0	Hi-Z	Hi-Z
X	Undervoltage	Powered	0	1	Default	Default
			1	0	Hi-Z	Hi-Z
X	Powered	Undervoltage	0	1	Default	Default
			1	0	Hi-Z	Hi-Z

Table 5. MAX2244_M/N Output Behavior During Undervoltage Conditions

$V_{IN_}$	V_{DDA}	V_{DDB}	DEFA = DEFB	V_{OUTA}	V_{OUTB}
1	Powered	Powered	1	High	High
			0	High	High
0	Powered	Powered	1	Low	Low
			0	Low	Low
X	Undervoltage	Powered	1	Default (High)	Default (High)
			0	Default (Low)	Default (Low)
X	Powered	Undervoltage	1	Default (High)	Default (High)
			0	Default (Low)	Default (Low)

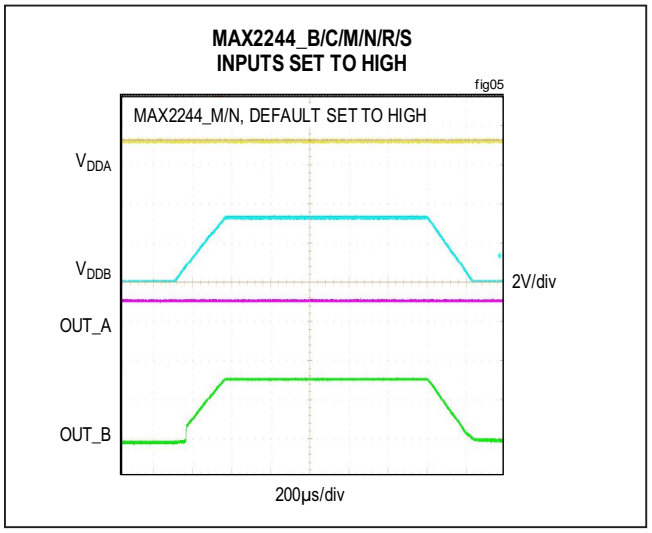


Figure 5. Undervoltage Lockout Behavior (MAX2244_ High)

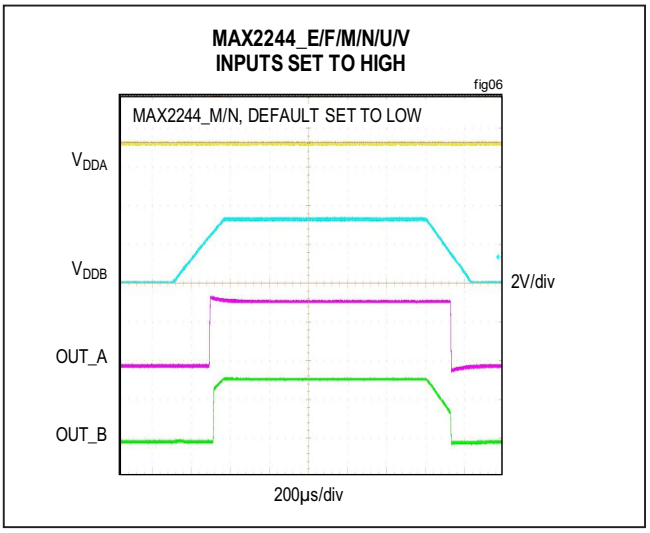


Figure 6. Undervoltage Lockout Behavior (MAX2244_ High)

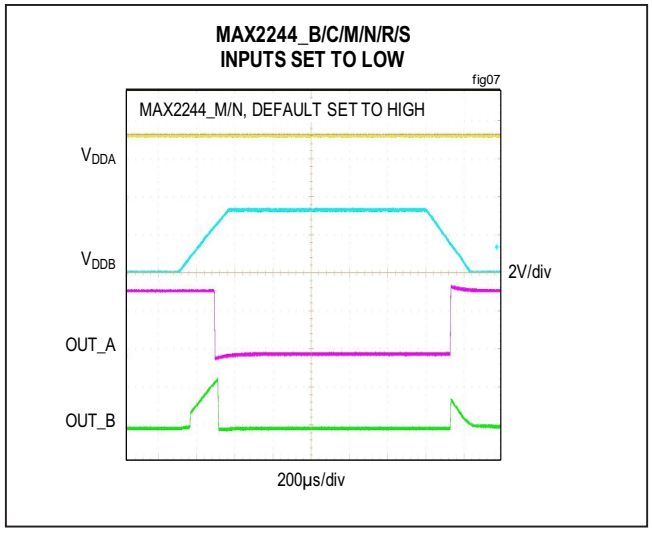


Figure 7. Undervoltage Lockout Behavior (MAX2244_ Low)

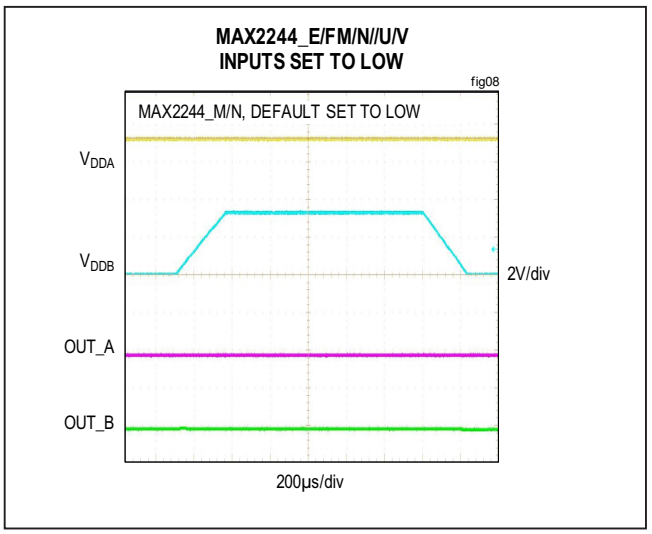


Figure 8. Undervoltage Lockout Behavior (MAX2244_ Low)

Selectable Output Default (DEFA, DEFB) (MAX2244_M/N Only)

The default is the state the output assumes when the input is not powered or if the input is open circuit. The MAX2244_M/N feature user-selectable default-high or default-low outputs. Set both DEFA and DEFB high to set all channels to default-high, or set both DEFA and DEFB low to set all channels to default-low.

Ensure the logic state (high or low) of DEFA is the same as that for DEFB. Do not toggle DEFA or DEFB during normal operation.

Applications Information

Power-Supply Sequencing

The MAX22444-MAX22446 do not require special power supply sequencing. The logic levels are set independently on either side by V_{DDA} and V_{DDB}. Each supply can be present over the entire specified range regardless of the level or presence of the other supply.

Power-Supply Decoupling

To reduce ripple and the chance of introducing data errors, bypass V_{DDA} and V_{DDB} with 0.1µF low-ESR ceramic capacitors to GNDA and GNDB, respectively. Place the bypass capacitors as close to the power supply input pins as possible.

Layout Considerations

The PCB designer should follow some critical recommendations in order to get the best performance from the design.

- Keep the input/output traces as short as possible. To keep signal paths low-inductance, avoid using vias.
- Have a solid ground plane underneath the high-speed signal layer.
- Keep the area underneath the MAX22444-MAX22446 free from ground and signal planes. Any galvanic or metallic connection between the Side A and Side B defeats the isolation.

Calculating Power Dissipation

The required current for a given supply (V_{DDA} or V_{DDB}) can be estimated by summing the current required for each channel. The supply current for a channel depends on whether the channel is an input or an output, the channel's data rate, and the capacitive or resistive load if it is an output. The typical current for an input or output at any data rate can be estimated from the graphs in Figure 9 and Figure 10. Please note that the data in Figure 9 and Figure 10 are extrapolated from the supply current measurements in a typical operating condition.

The total current for a single channel is the sum of the "no load" current (shown in Figure 9 and Figure 10) which is a function of Voltage and Data Rate, and the "load current," which depends on the type of load. Current into a capacitive load is a function of the load capacitance, the switching frequency, and the supply voltage.

$$I_{CL} = C_L \times f_{SW} \times V_{DD}$$

where

I_{CL} is the current required to drive the capacitive load.

C_L is the load capacitance on the isolator's output pin.

f_{SW} is the switching frequency (bits per second / 2).

V_{DD} is the supply voltage on the output side of the isolator.

Current into a resistive load depends on the load resistance, the supply voltage and the average duty cycle of the data waveform. The DC load current can be conservatively estimated by assuming the output is always high.

$$I_{RL} = V_{DD} \div R_L$$

where

I_{RL} is the current required to drive the resistive load.

V_{DD} is the supply voltage on the output side of the isolator.

R_L is the load resistance on the isolator's output pin.

Example (shown in Figure 11): A MAX22445 is operating with V_{DDA} = 2.5V, V_{DDB} = 3.3V, channel 1 operating at 20Mbps with a 10pF capacitive load, channel 2 held high with a 10kΩ resistive load, and channel 4 operating at 100Mbps with a 15pF capacitive load. Channel 3 is not in use and the resistive load is negligible since the isolator is driving a CMOS input. Refer to Table 6 and Table 7 for V_{DDA} and V_{DDB} supply current calculation worksheets.

V_{DDA} must supply:

- Channel 1 is an input channel operating at 2.5V and 20Mbps, consuming 0.33mA, estimated from Figure 9.
- Channel 2 and 3 are input channels operating at 2.5V with DC signal, consuming 0.14mA, estimated from Figure 9.
- Channel 4 is an output channel operating at 2.5V and 100Mbps, consuming 0.77mA, estimated from Figure 10.
- I_{CL} on channel 4 for 15pF capacitor at 2.5V and 100Mbps is 1.875mA.

Total current for side A = 0.33 + 0.14 × 2 + 0.77 + 1.875 = 3.255mA, typical

V_{DDB} must supply:

- Channel 1 is an output channel operating at 3.3V and 20Mbps, consuming 0.40mA, estimated from Figure 10.
- Channel 2 and 3 are output channels operating at 3.3V with DC signal, consuming 0.27mA, estimated from Figure 10.
- Channel 4 is an input channel operating at 3.3V and 100Mbps, consuming 1.11mA, estimated from Figure 9.
- I_{CL} on channel 1 for 10pF capacitor at 3.3V and 20Mbps is 0.33mA.
- I_{RL} on channel 2 for 10kΩ resistor held at 3.3V is 0.33mA.

Total current for side B = 0.40 + 0.27 × 2 + 1.11 + 0.33 + 0.33 = 2.71mA, typical

Table 6. Side A Supply Current Calculation Worksheet

SIDE A	V_{DDA} = 2.5V					
Channel	**IN/ OUT**	**Data Rate (Mbps)**	**Load Type**	**Load**	**"No Load" Current (mA)**	**Load Current (mA)**
1	IN	20			0.33	
2	IN	0			0.14	
3	IN	0			0.14	
4	OUT	100	Capacitive	15pF	0.77	2.5V x 50MHz x 15pF = 1.875mA
Total: 3.26mA						

Table 7. Side B Supply Current Calculation Worksheet

SIDE B	V_{DDB} = 3.3V					
Channel	**IN/ OUT**	**Data Rate (Mbps)**	**Load Type**	**Load**	**"No Load" Current (mA)**	**Load Current (mA)**
1	OUT	20	Capacitive	10pF	0.40	3.3V x 10MHz x 10pF = 0.33mA
2	OUT	0	Resistive	10kΩ	0.27	3.3V / 10kΩ = 0.33mA
3	OUT	0			0.27	
4	IN	100			1.11	
Total: 2.71mA						

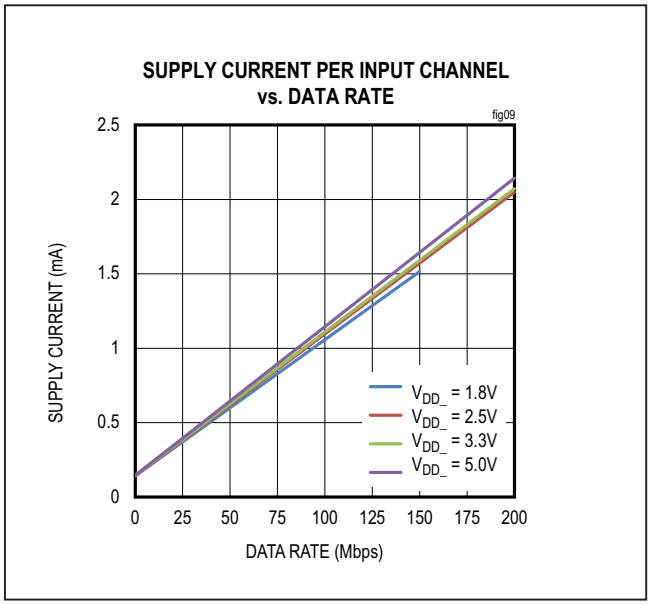


Figure 9. Supply Current Per Input Channel (Estimated)

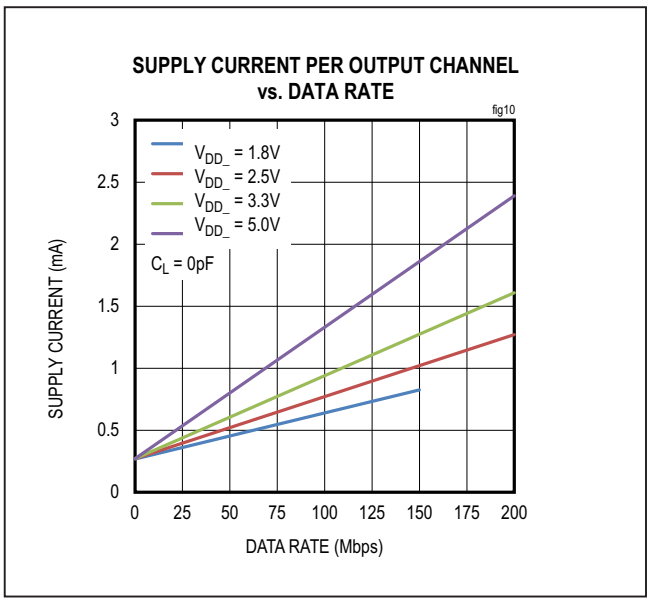


Figure 10. Supply Current Per Output Channel (Estimated)

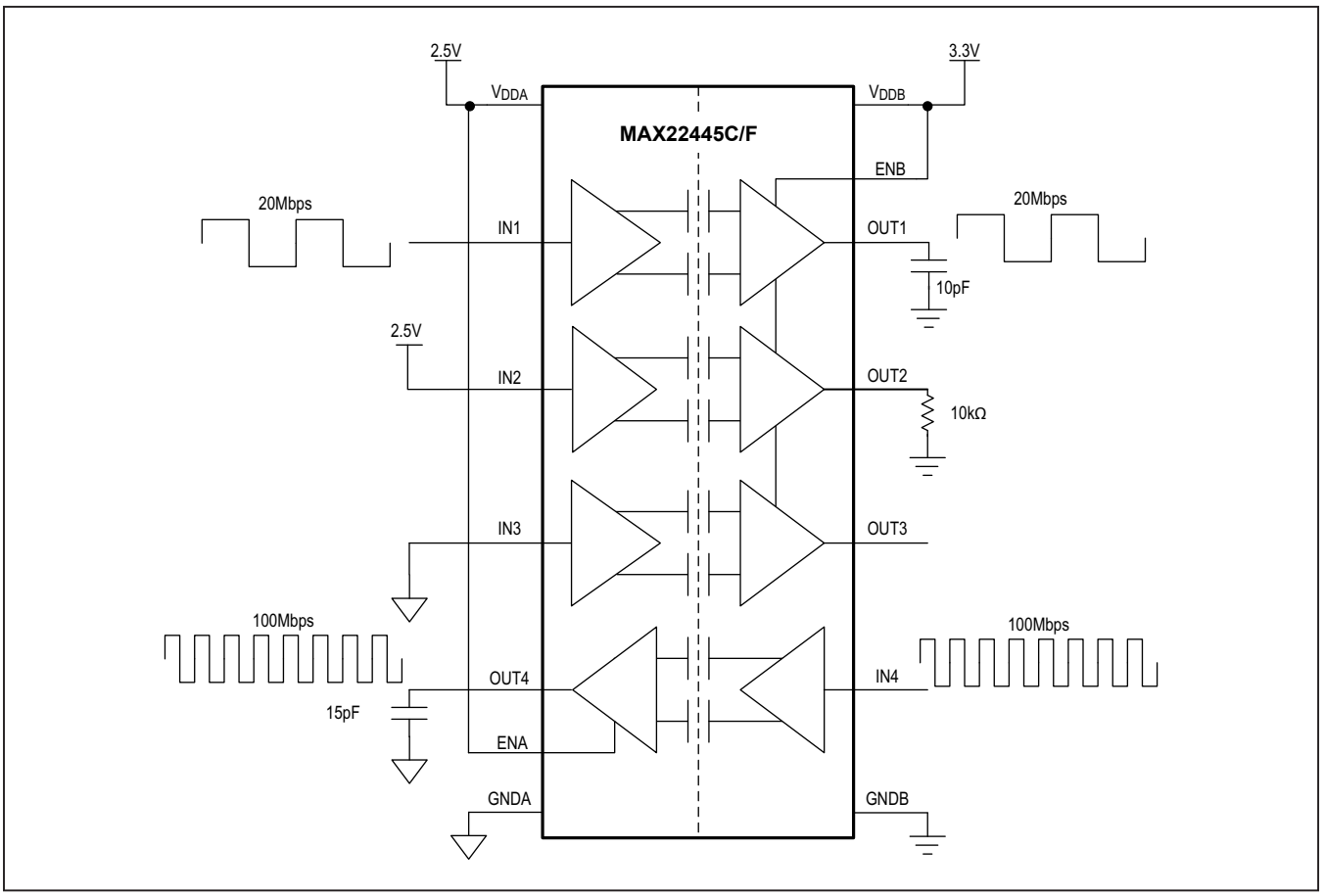
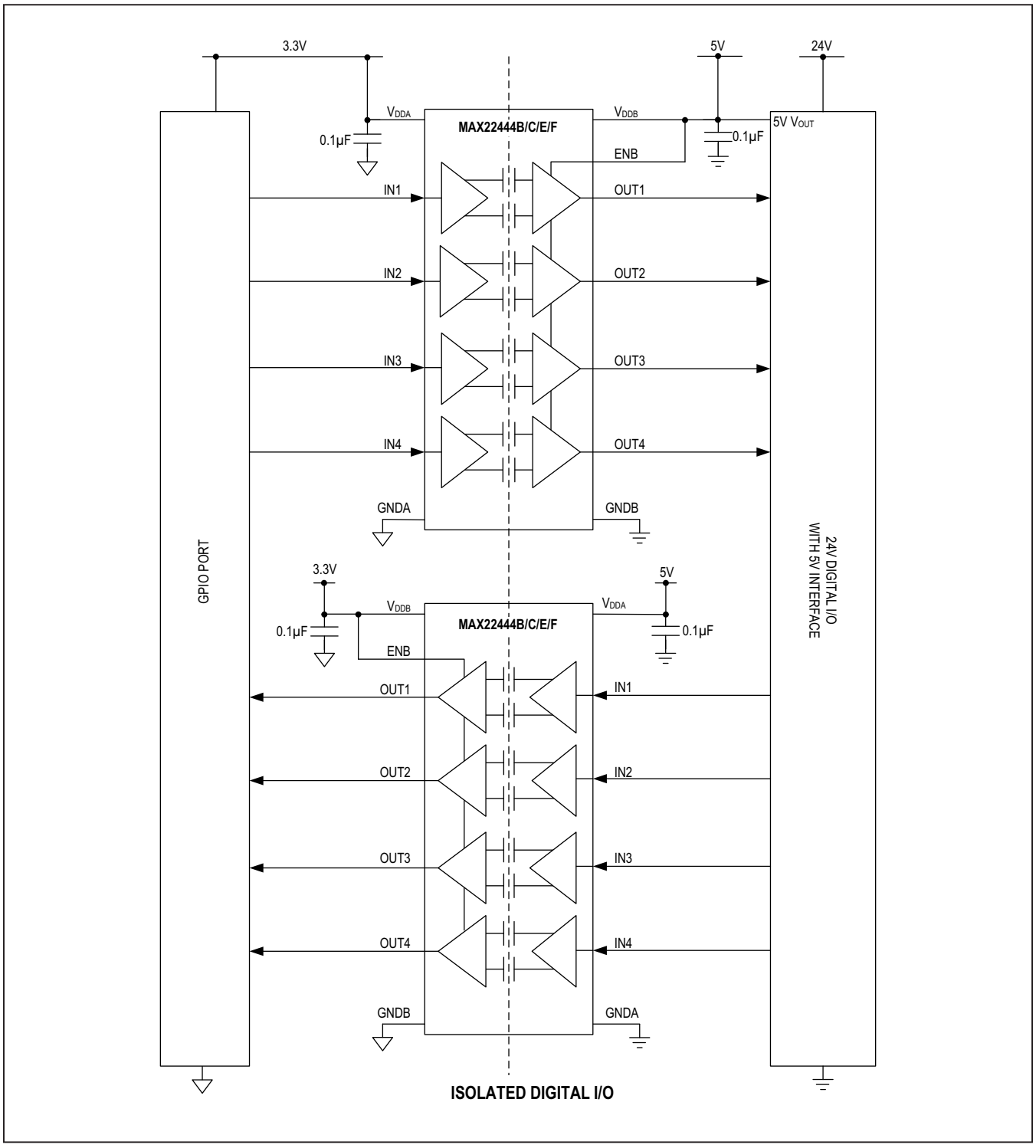
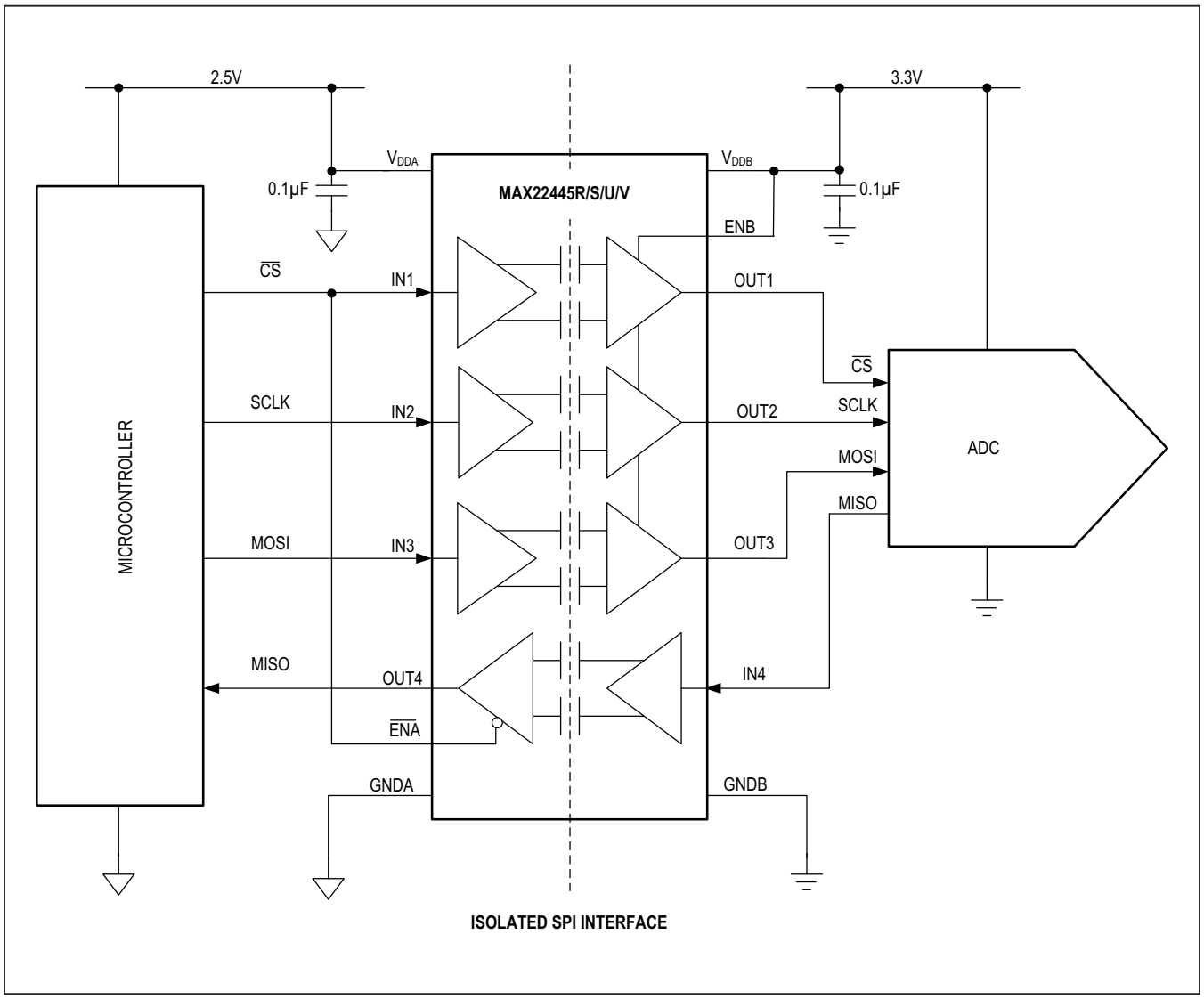


Figure 11. Example Circuit for Supply Current Calculation

Typical Application Circuits

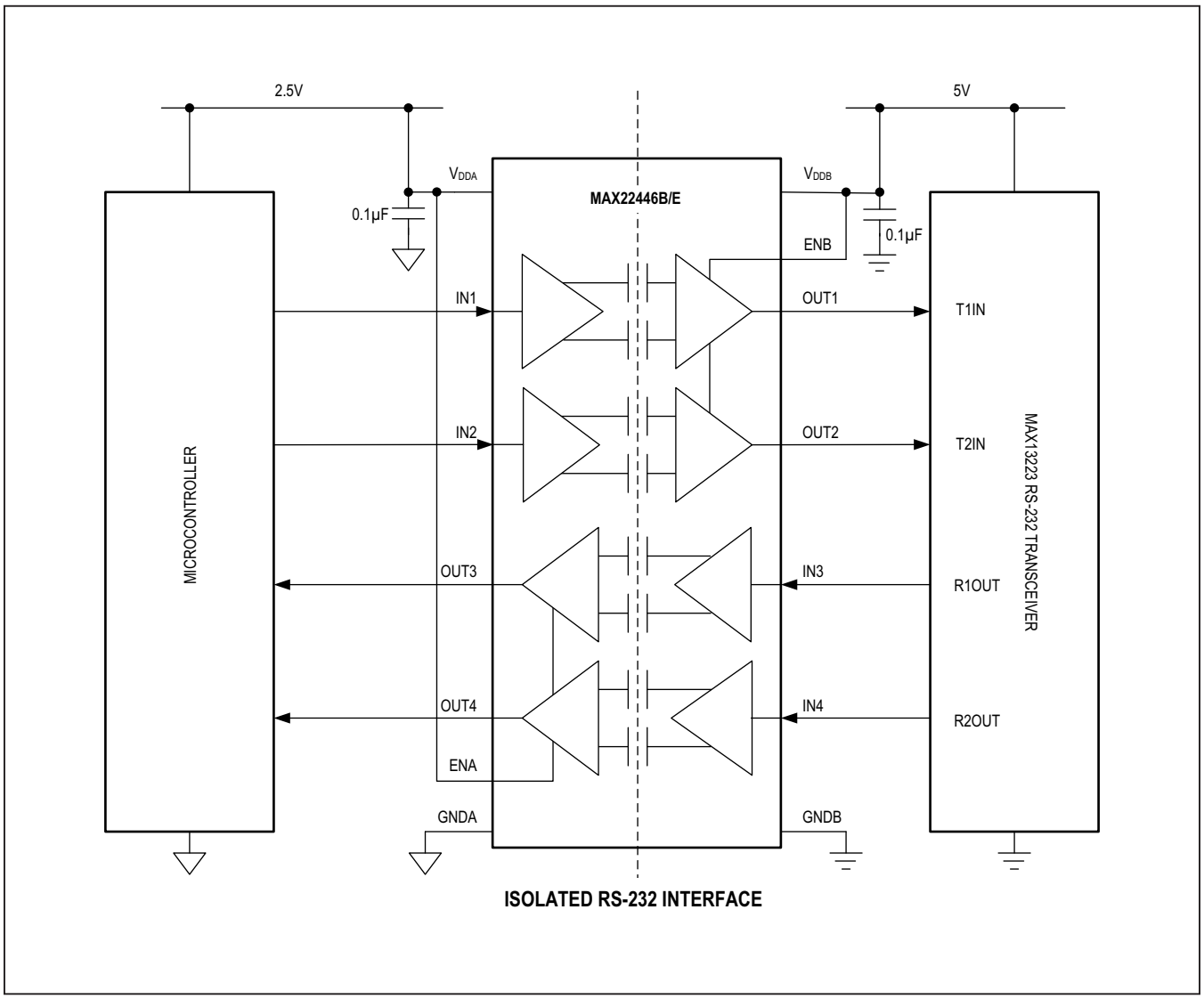


Typical Application Circuits (continued)

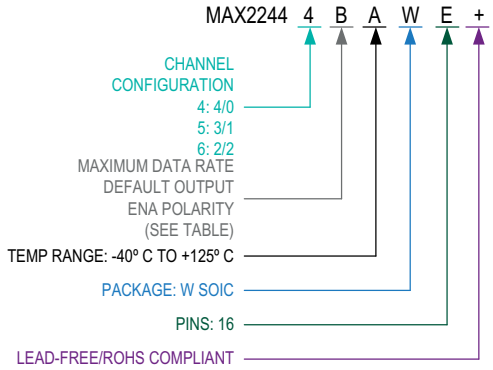


ISOLATED SPI INTERFACE

Typical Application Circuits (continued)



Product Selector Guide



DEVICE CONFIGURATION	ACTIVE-HIGH EN_		ACTIVE-LOW ENA	
	MAX DATA RATE		MAX DATA RATE	
	25Mbps	200Mbps	25Mbps	200Mbps
DEFAULT-HIGH OUTPUT	B	C	R	S
DEFAULT-LOW OUTPUT	E	F	U	V
SELECTABLE DEFAULT OUTPUT STATE	M	N	—	—

Ordering Information

PART	CHANNEL CONFIGU-RATION	DATA RATE (Mbps)	DEFAULT OUTPUT	ENA POLARITY	ISOLATION VOLTAGE (kV_{RMS})	TEMP RANGE (°C)	PIN-PACKAGE
MAX22444BAWE+*	4/0	25	Default High	Active-High	5	-40 to +125	16 Wide SOIC
MAX22444CAWE+	4/0	200	Default High	Active-High	5	-40 to +125	16 Wide SOIC
MAX22444EAWE+*	4/0	25	Default Low	Active-High	5	-40 to +125	16 Wide SOIC
MAX22444FAWE+	4/0	200	Default Low	Active-High	5	-40 to +125	16 Wide SOIC
MAX22444MAWE+*	4/0	25	Selectable	—	5	-40 to +125	16 Wide SOIC
MAX22444NAWE+*	4/0	200	Selectable	—	5	-40 to +125	16 Wide SOIC
MAX22445BAWE+*	3/1	25	Default High	Active-High	5	-40 to +125	16 Wide SOIC
MAX22445CAWE+*	3/1	200	Default High	Active-High	5	-40 to +125	16 Wide SOIC
MAX22445EAWE+	3/1	25	Default Low	Active-High	5	-40 to +125	16 Wide SOIC
MAX22445FAWE+	3/1	200	Default Low	Active-High	5	-40 to +125	16 Wide SOIC
MAX22445MAWE+*	3/1	25	Selectable	—	5	-40 to +125	16 Wide SOIC
MAX22445NAWE+*	3/1	200	Selectable	—	5	-40 to +125	16 Wide SOIC
MAX22445RAWE+	3/1	25	Default High	Active-Low	5	-40 to +125	16 Wide SOIC
MAX22445SAWE+*	3/1	200	Default High	Active-Low	5	-40 to +125	16 Wide SOIC
MAX22445UAWE+*	3/1	25	Default Low	Active-Low	5	-40 to +125	16 Wide SOIC
MAX22445VAWE+*	3/1	200	Default Low	Active-Low	5	-40 to +125	16 Wide SOIC
MAX22446BAWE+*	2/2	25	Default High	Active-High	5	-40 to +125	16 Wide SOIC
MAX22446CAWE+	2/2	200	Default High	Active-High	5	-40 to +125	16 Wide SOIC
MAX22446EAWE+	2/2	25	Default Low	Active-High	5	-40 to +125	16 Wide SOIC
MAX22446FAWE+*	2/2	200	Default Low	Active-High	5	-40 to +125	16 Wide SOIC
MAX22446MAWE+*	2/2	25	Selectable	—	5	-40 to +125	16 Wide SOIC
MAX22446NAWE+*	2/2	200	Selectable	—	5	-40 to +125	16 Wide SOIC

**Future Product—Contact Maxim for availability.*

+Denotes a lead(Pb)-free/RoHS-compliant package.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/18	Initial release	—
1	10/18	Removed Future Product designation from MAX22446CAWE+	30
2	1/19	Updated *Safety Regulatory Approvals* section and added a *Safety Regulatory Approvals* table	1, 10
3	3/19	Updated *General Description* and Table 1	1, 10
4	9/19	Updated *Safety Regulatory Approvals* section and added a *Safety Regulatory Approvals* table; Corrected typo in Revision History table	1, 10, 31
5	10/19	Updated the *General Description* section and the *Safety Regulatory Approvals* table	1, 10
6	1/20	Removed future product designation from MAX2245EAWE+	30
7	3/20	Removed future product designation from MAX22445RAWE+	30
8	1/21	Updated the *Benefits and Features, Electrical Characteristics* and *Typical Operating Circuits* section, and removed future product designation from MAX22444CAWE+ and MAX22446EAWE+ in the *Ordering Information*	1, 10, 27–30
9	9/21	Updated *General Description*, *Safety Regulatory Approvals*, Table 2, Figures 9 and 10, and Ordering Information table	1, 10, 11, 26, 30

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