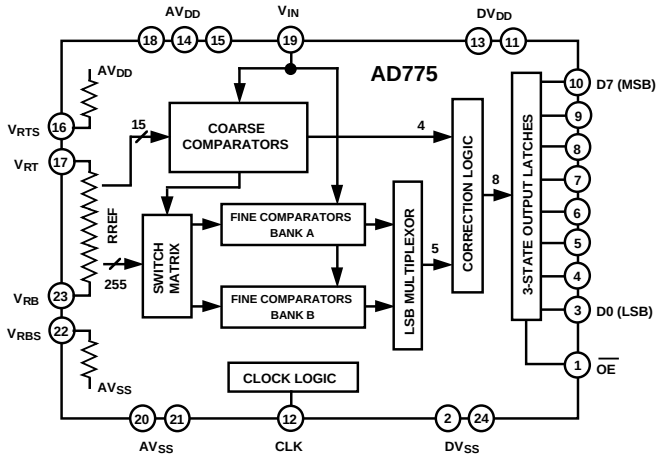
8-Bit 20 MSPS, 60 mW Sampling A/D Converter

AD775

FEATURES

CMOS 8-Bit 20 MSPS Sampling A/D Converter
Low Power Dissipation: 60 mW
+5 V Single Supply Operation
Differential Nonlinearity: 0.3 LSB
Differential Gain: 1%
Differential Phase: 0.5 Degrees
Three-State Outputs
On-Chip Reference Bias Resistors
Adjustable Reference Input
Video Industry Standard Pinout
Small Packages:
24-Pin 300 Mil SOIC Surface Mount
24-Pin 400 Mil Plastic DIP

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD775 is a CMOS, low power, 8-bit, 20 MSPS sampling analog-to-digital converter (ADC). The AD775 features a built-in sampling function and on-chip reference bias resistors to provide a complete 8-bit ADC solution. The AD775 utilizes a pipelined/ping pong two-step flash architecture to provide high sampling rates (up to 35 MHz) while maintaining very low power consumption (60 mW).

Its combination of excellent DNL, fast sampling rate, low differential gain and phase errors, extremely low power dissipation, and single +5 V supply operation make it ideally suited for a variety of video and image acquisition applications, including portable equipment. The AD775's reference ladder may be connected in a variety of configurations to accommodate different input ranges. The low input capacitance (11 pF typical) provides an easy-to-drive input load compared to conventional flash converters.

The AD775 is offered in both 300 mil SOIC and 400 mil DIP plastic packages, and is designed to operate over an extended commercial temperature range (–20°C to +75°C).

PRODUCT HIGHLIGHTS

Low Power: The AD775 has a typical supply current of 12 mA, for a power consumption of 60 mW. Reference ladder current is also low: 6.6 mA typical, minimizing the reference power consumption.

Complete Solution: The AD775's switched capacitor design features an inherent sample/hold function: no external SHA is required. On-chip reference bias resistors are included to allow a supply-based reference to be generated without any external resistors.

Excellent Differential Nonlinearity: The AD775 features a typical DNL of 0.3 LSBs, with a maximum limit of 0.5 LSBs. No missing codes is guaranteed.

Single +5 V Supply Operation: The AD775 is designed to operate on a single +5 V supply, and the reference ladder may be configured to accommodate analog inputs inclusive of ground.

Low Input Capacitance: The 11 pF input capacitance of the AD775 can significantly decrease the cost and complexity of input driving circuitry, compared with conventional 8-bit flash ADCs.

REV. 0

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AD775—SPECIFICATIONS (T_A = +25°C with AV_{DD}, DV_{DD} = +5 V, AV_{SS}, DV_{SS} = 0 V, V_{RT} = 2.6 V, V_{RB} = +0.6 V, CLOCK = 20 MHz unless otherwise noted)

Parameter	AD775J Min	AD775J Typ	AD775J Max	Units
RESOLUTION	8			Bits
DC ACCURACY				
Integral Nonlinearity (INL)		+0.5	1.3	LSB
Differential Nonlinearity (DNL)		±0.3	±0.5	LSB
No Missing Codes		GUARANTEED		
Offset				
To Top of Ladder V_{RT}	–10	–35	–60	mV
To Bottom of Ladder V_{RB}	0	+15	+45	mV
VIDEO ACCURACY[1]				
Differential Gain Error		1.0		%
Differential Phase Error		0.5		Degrees
ANALOG INPUT				
Input Range (V_{RT}–V_{RB})		2.0		V p-p
Input Capacitance		11		pF
AC SPECIFICATIONS[2]				
Signal-to-Noise and Distortion (S/(N + D))				
f_{IN} = 1 MHz		47		dB
f_{IN} = 5 MHz		41		dB
Total Harmonic Distortion (THD)				
f_{IN} = 1 MHz		–51		dB
f_{IN} = 5 MHz		–42		dB
REFERENCE INPUT				
Reference Input Resistance (R_{REF})	230	300	450	Ω
Case 1: V_{RT} = V_{RTS}, V_{RB} = V_{RBS}				
Reference Bottom Voltage (V_{RB})	0.60	0.64	0.68	V
Reference Span (V_{RT}–V_{RB})	1.96	2.09	2.21	V
Reference Ladder Current (I_{REF})	4.4	7.0	9.6	mA
Case 2: V_{RT} = V_{RTS}, V_{RB} = AV_{SS}				
Reference Span (V_{RT}–V_{RB})	2.25	2.39	2.53	V
Reference Ladder Current (I_{REF})	5	8	11	mA
POWER SUPPLIES				
Operating Voltages				
AV_{DD}	+4.75		+5.25	Volts
DV_{DD}	+4.75		+5.25	Volts
Operating Current				
IAV_{DD}		9.5		mA
IDV_{DD}		2.5		mA
IAV_{DD} + IDV_{DD}		12	17	mA
POWER CONSUMPTION		60	85	mW
TEMPERATURE RANGE				
Operating	–20		+75	°C

NOTES
[1]NSTC 40 IRE modulation ramp, CLOCK = 14.3 MSPS.
[2]f_{IN} amplitude = 0.3 dB full scale.

Specifications subject to change without notice. See Definition of Specifications for additional information.

DIGITAL SPECIFICATIONS

(T_A = +25°C with AV_{DD}, DV_{DD} = +5 V, AV_{SS}, DV_{SS} = 0 V, V_{RT} = 2.6 V, V_{RB} = +0.6 V, CLOCK = 20 MHz unless otherwise noted)

Parameter	Symbol	DV_{DD}	AD775J Min	AD775J Typ	AD775J Max	Units
LOGIC INPUT						
High Level Input Voltage	V_{IH}	5.0	4.0			V
Low Level Input Voltage	V_{IL}	5.0			1.0	V
High Level Input Current (V_{IH} = DV_{DD})	I_{IH}	5.25			5	µA
Low Level Input Current (V_{IL} = 0 V)	I_{IL}	5.25	–5			µA
Logic Input Capacitance	C_{IN}			5		pF
LOGIC OUTPUTS						
High Level Output Current						
$\overline{OE}$ = DV_{SS}, V_{OH} = DV_{DD}–0.5 V	I_{OH}	4.75			–1.1	mA
$\overline{OE}$ = DV_{DD}, V_{OH} = DV_{DD}	I_{OZ}	5.25			16	µA
Low Level Output Current						
$\overline{OE}$ = DV_{SS}, V_{OL} = 0.4 V	I_{OL}	4.75	3.7			mA
$\overline{OE}$ = DV_{DD}, V_{OL} = 0 V	I_{OZ}	5.25			16	µA

TIMING SPECIFICATIONS

	Symbol	Min	Typ	Max	Units
Maximum Conversion Rate		20	35		MHz
Clock Period	t_C	50			ns
Clock High	t_{CH}	25			ns
Clock Low	t_{CL}	25			ns
Output Delay	t_{OD}		18	30	ns
Pipeline Delay (Latency)				2.5	Clock Cycles
Sampling Delay	t_{DS}		4		ns
Aperture Jitter			30		ps

Specifications subject to change without notice.

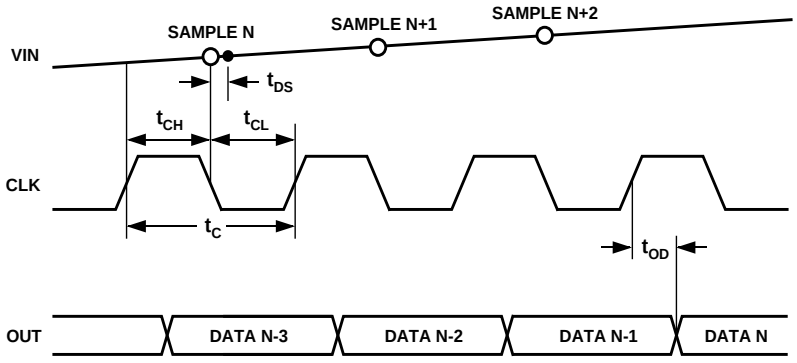


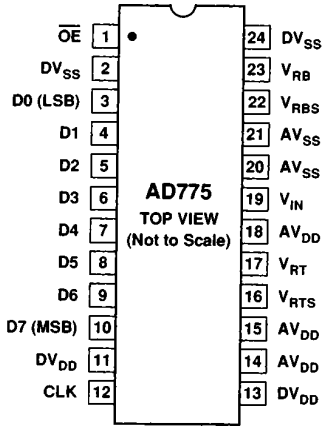
Figure 1. AD775 Timing Diagram

PIN DESCRIPTION

Pin No.	Symbol	Type	Name and Function
1	$\overline{OE}$	DI	$\overline{OE}$ = Low Normal Operating Mode. $\overline{OE}$ = High High Impedance Outputs.
2, 24	DV_{SS}	P	Digital Ground. Note: DV_{SS} and AV_{SS} pins should share a common ground plane on the circuit board.
3	D0 (LSB)	DO	Least Significant Bit, Data Bit 0.
4–9	D1–D6	DO	Data Bits 1 Through 6.
10	D7 (MSB)	DO	Most Significant Bit, Data Bit 7.
11, 13	DV_{DD}	P	+5 V Digital Supply. Note: DV_{DD} and AV_{DD} pins should share a common supply on the circuit board.
12	CLK	DI	Clock Input.
16	V_{RTS}	AI	Reference Top Bias. Short to V_{RT} for Self-Bias.
17	V_{RT}	AI	Reference Ladder Top.
23	V_{RB}	AI	Reference Ladder Bottom.
22	V_{RBS}	AI	Reference Bottom Bias. Short to V_{RB} for Self-Bias.
14, 15, 18	AV_{DD}	P	+5 V Analog Supply. Note: DV_{DD} and AV_{DD} pins should share a common supply within 0.5 inches of the AD775.
19	V_{IN}	AI	Analog Input. Input Span = V_{RT}–V_{RB}.
20, 21	AV_{SS}	P	Analog Ground. Note: DV_{SS} and AV_{SS} pins should share a common ground within 0.5 inches of the AD775.

NOTE
Type: AI = Analog Input; DI = Digital Input; DO = Digital Output; P = Power.

PIN CONFIGURATION (DIP and SOIC)



MAXIMUM RATINGS*

Supply Voltage (AV_{DD}, DV_{DD}) . . . . . 7 V
Supply Difference (AV_{DD}–DV_{DD}) . . . . . 0 V
Ground Difference (AV_{SS}–DV_{SS}) . . . . . 0 V
Reference Voltage (V_{RT}, V_{RB}) . . . . . V_{DD} to V_{SS}
Analog Input Voltage (V_{IN}) . . . . . V_{DD} to V_{SS}
Digital Input Voltage (CLK) . . . . . V_{DD} to V_{SS}
Digital Output Voltage (V_{OH}, V_{OL}) . . . . . V_{DD} to V_{SS}
Storage Temperature . . . . . –55°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD775JN	–20°C to +75°C	24-Pin 400 Mil Plastic DIP	N-24B
AD775JR	–20°C to +75°C	24-Pin 300 Mil SOIC	R-24A

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD775 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



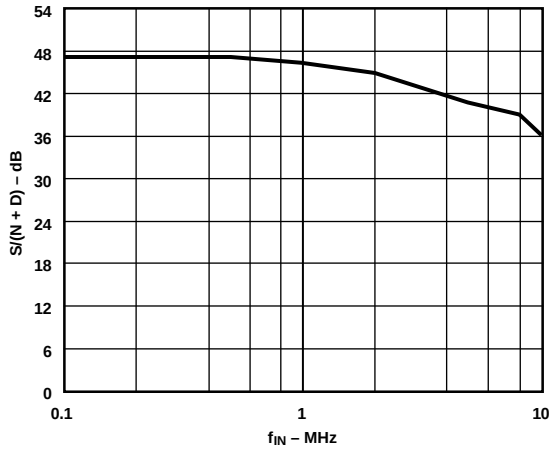


Figure 2. S/(N + D) vs. Input Frequency at 20 MSPS Clock Rate (V_{IN} = –0.3 dB)

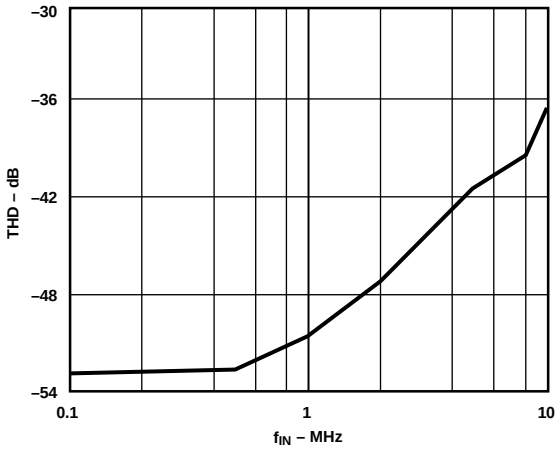


Figure 5. THD vs. Input Frequency at 20 MSPS Clock Rate (V_{IN} = –0.3 dB)

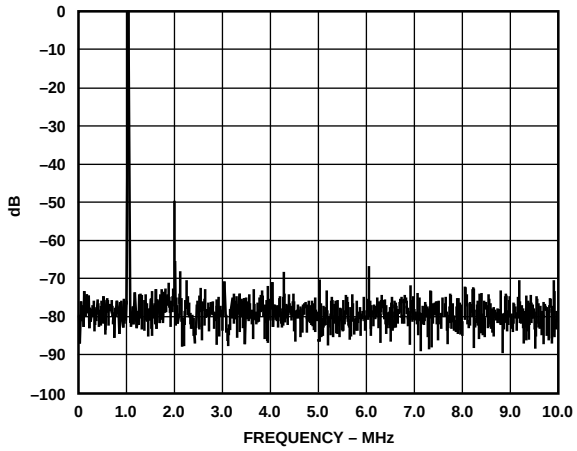


Figure 3. Typical FFT at 1 MHz Input, 20 MSPS Clock Rate (V_{IN} = –0.5 dB)

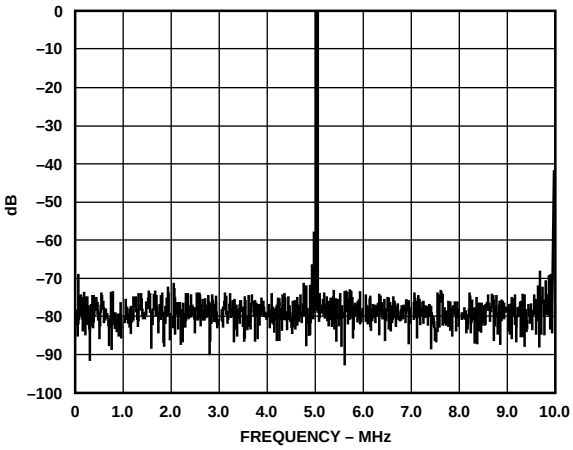


Figure 6. Typical FFT at 5 MHz Input, 20 MSPS Clock Rate (V_{IN} = –0.5 dB)

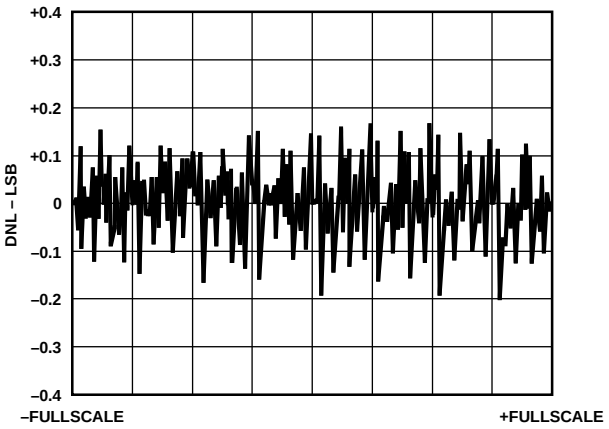


Figure 4. Typical Differential Nonlinearity (DNL)

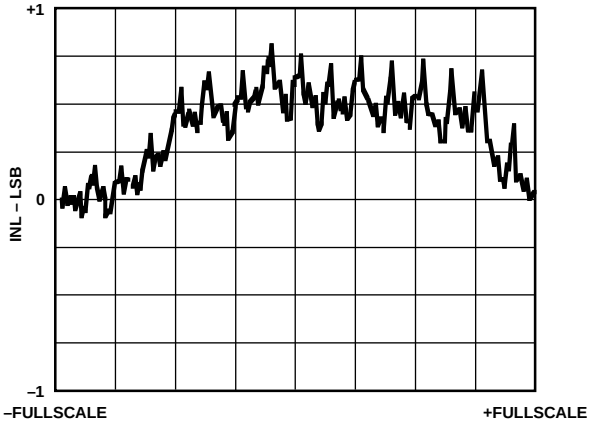


Figure 7. Typical Integral Nonlinearity (INL)

DEFINITIONS OF SPECIFICATIONS

Integral Nonlinearity (INL)
Integral nonlinearity refers to the deviation of each individual code from a line drawn from "zero" through "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line.

Differential Nonlinearity (DNL, No Missing Codes)
An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. It is often specified in terms of the resolution for which no missing codes (NMC) is guaranteed.

Offset Error
The first code transition should occur at a level 1/2 LSB above nominal negative full scale. Offset referred to the Bottom of Ladder V_{RB} is defined as the deviation from this ideal. The last code transition should occur 1 1/2 LSB below the nominal positive full scale. Offset referred to the Top of Ladder V_{RT} is defined as the deviation from this ideal.

Differential Gain
The percentage difference between the output amplitudes of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

Differential Phase
The difference in the output phase of a small high frequency sine wave at two stated levels of a low frequency signal on which it is superimposed.

Pipeline Delay (Latency)
The number of clock cycles between conversion initiation and the associated output data being made available. New output data is provided every clock cycle.

Signal-to-Noise Plus Distortion Ratio (S/N+D)
S/N+D is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components including harmonics but excluding dc. The value for S/N+D is expressed in decibels.

Total Harmonic Distortion (THD)
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

THEORY OF OPERATION

The AD775 uses a pipelined two-step (subranging) flash architecture to achieve significantly lower power and lower input capacitance than conventional full flash converters while still maintaining high throughput. The analog input is sampled by the switched capacitor comparators on the falling edge of the input clock: no external sample and hold is required. The coarse comparators determine the top four bits (MSBs), and select the appropriate reference ladder taps for the fine comparators. With the next falling edge of the clock, the fine comparators determine the bottom four bits (LSBs). Since the LSB comparators require a full clock cycle between their sampling instant and their decision, the converter alternates between two sets of fine comparators in a "ping-pong" fashion. This multiplexing allows a new input sample to be taken on every falling clock edge, thereby providing 20 MSPS operation. The data is accumulated in the correction logic and output through a three-state output latch on the rising edge of the clock. The latency between input sampling and the corresponding converted output is 2.5 clock cycles.

All three comparator banks utilize the same resistive ladder for their reference input. The analog input range is determined by the voltages applied to the bottom and top of the ladder, and the AD775 can digitize inputs down to 0 V using a single supply. On-chip application resistors are provided to allow the ladder to be conveniently biased by the supply voltage.

The AD775 uses switched capacitor autozeroing techniques to cancel the comparators' offsets and achieve excellent differential nonlinearity performance: typically ±0.3 LSB. The integral nonlinearity is determined by the linearity of the reference ladder and is typically +0.5 LSB.

APPLYING THE AD775

REFERENCE INPUT

The AD775 features a resistive reference ladder similar to that found in most conventional flash converters. The analog input range of the converter falls between the top (V_{RT}) and bottom (V_{RB}) voltages of this ladder. The nominal resistance of the ladder is 300 ohms, though this may vary from 230 ohms to 450 ohms. The minimum recommended voltage for V_{RB} is 0 V; the linearity performance of the converter may deteriorate for input spans (V_{RB}–V_{RB}) below 1.8 V. While 2.8 V is the recommended maximum ladder top voltage (V_{RT}), the top of the ladder may be as high as the positive supply voltage (AV_{DD}) with minimal linearity degradation.

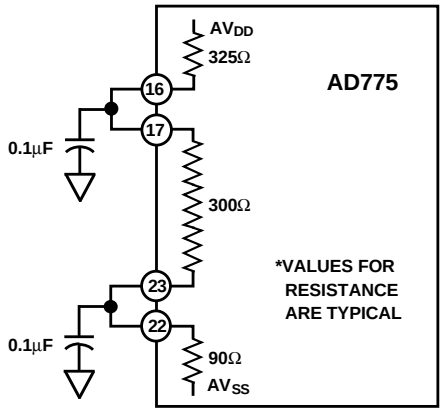


Figure 8. Reference Configuration: 0.64 V to 2.73 V

To simplify biasing of the AD775, on-chip reference bias resistors are provided on Pins 16 and 22. The two recommended configurations for these resistors are shown in Figures 8 and 9.

In the topology shown in Figure 8, the top of the ladder (V_{RT}) is shorted to the top bias resistor (V_{RTS}) (Pin 17 shorted to Pin 16), while the bottom of the ladder (V_{RB}) is shorted to the bottom bias resistor (V_{RBS}) (Pin 23 shorted to Pin 22). This creates a resistive path (nominally 725 ohms) between AV_{DD} and AV_{SS}. For nominal supply voltages (5 V and 0 V respectively), this creates an input range of 0.64 V to 2.73 V.

Both top and bottom of the reference ladder should be decoupled, preferably with a chip capacitor to ground to minimize reference noise.

The topology shown in Figure 9 provides a ground-inclusive input range. The bottom of the ladder (V_{RB}) is shorted to AV_{SS}. (0 V), while the top of the ladder (V_{RT}) is connected to the onboard bias resistor (V_{RTS}). This provides a nominal input range of 0 V to +2.4 V for AV_{DD} of 5 V. The V_{RBS} pin may be left floating, or shorted to AV_{SS}.

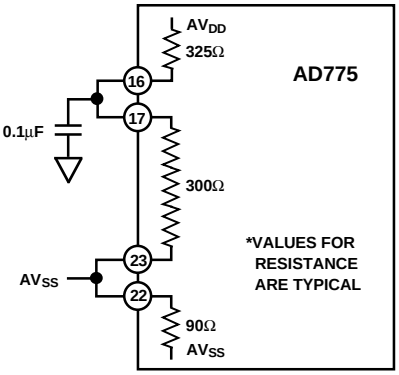


Figure 9. Reference Configuration: 0 V to +2.4 V

More elaborate topologies can be used for those wishing to provide an input span based on an external reference voltage. The circuit in Figure 10 uses the AD780 2.5 V reference to drive the top of the ladder (V_{RT}), with the bottom (V_{RB}) of the ladder grounded to provide an input span of 0 V to +2.5 V. This is modified in Figure 11 to shift the 2.5 V span up 700 mV.

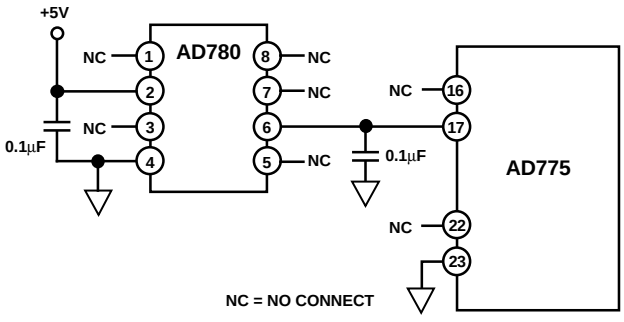


Figure 10. Reference Configuration: 0 V to 2.5 V

The AD775 can accommodate dynamic changes in the reference voltage for gain or offset adjustment. However, conversions that are in progress, including those in the converter pipeline, while the reference voltages are changing will be invalid.

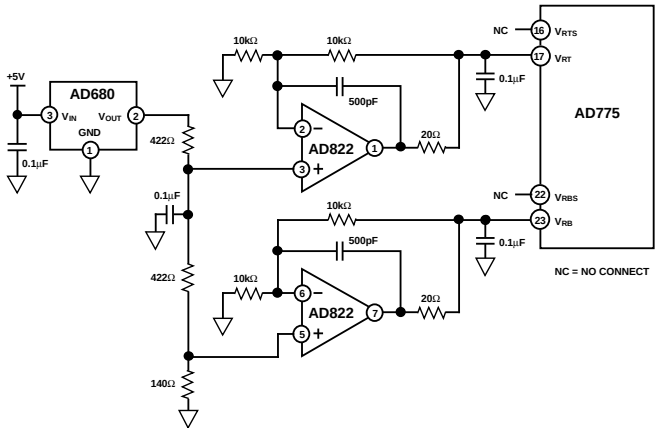


Figure 11. Reference Configuration: 0.7 V to 3.2 V

ANALOG INPUT

The impedance looking into the analog input is essentially capacitive, as shown in the equivalent circuit of Figure 12, typically totalling around 11 pF. A portion of this capacitance is parasitic; the remainder is part of the switched capacitor structure of the comparator arrays. The switches close on the rising edge of the clock, acquire the input voltage, and open on the clock's falling edge (the sampling instant). The charge that must be moved onto the capacitors during acquisition will be a function of the converter's previous two samples, but there should be no sample-to-sample crosstalk so long as ample driving impedance and acquisition time are provided.

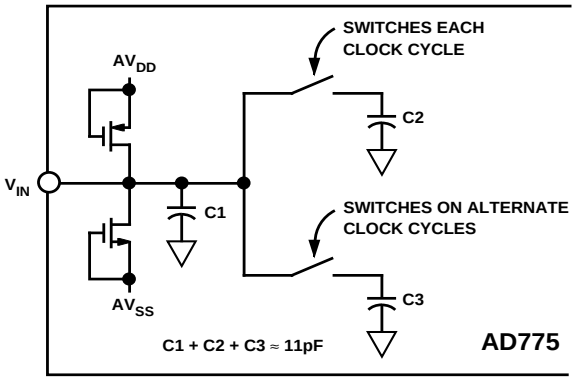


Figure 12. Equivalent Analog Input Circuit (V_{IN})

For example, to ensure accurate acquisition (to 1/4 bit accuracy) of a full-scale input step in less than 20 ns, a source impedance of less than 100 ohms is recommended. Figure 13 shows one option of input buffer circuitry using the AD817. The AD817 acts as both an inverting buffer and level shifting circuit. In order to level shift the ground-based input signal to the dc level required by the input of the AD775, the supply voltage is resistively divided to produce the appropriate voltage at the noninverting input of the AD817. For most applications, the AD817 provides a low cost, high performance level shifter. The AD811 is recommended for systems which require faster settling times.

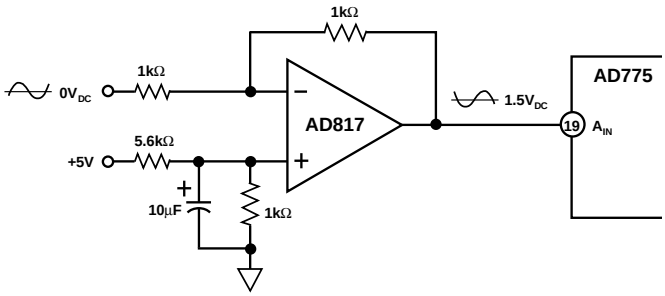


Figure 13. Level Shifting Input Buffer

The analog input range is set by the voltage at the top and bottom of the reference ladder. In general, the larger the span (V_{RT}–V_{RB}), the better the differential nonlinearity (DNL) of the converter; a 1.8 V span is suggested as a minimum to realize good linearity performance. AS the input voltage exceeds 2.8 V (for AV_{DD} = 4.75 V), the input circuitry may start to slightly degrade the acquisition performance.

CLOCK INPUT

The AD775's internal control circuitry makes use of both clock edges to generate on-chip timing signals. To ensure proper settling and linearity performance, both t_{CH} and t_{CL} times should be 25 ns or greater. For sampling frequencies at or near 20 MSPS, a 50% duty cycle clock is recommended. For slower sampling applications, the AD775 can accommodate a wider range of duty cycles, provided each clock phase is as least 25 ns.

Under certain conditions, the AD775 can be operated at sampling rates above 20 MSPS. Figure 14 shows the signal-to-noise plus distortion (S/(N+D)) performance of a typical AD775 versus clock frequency. It is extremely important to note that *the maximum clock rate will be a strong function of both temperature and supply voltage*. In general, the part slows down with increasing temperature and decreasing supply voltage.

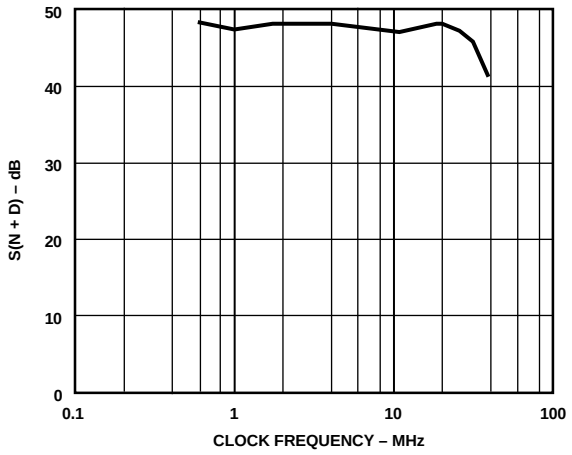


Figure 14. S(N + D) vs. Clock Frequency (Temperature = +25°C)

A significant portion of the AD775's power dissipation is proportional to the clock frequency: Figure 15 illustrates this tradeoff for a typical part.

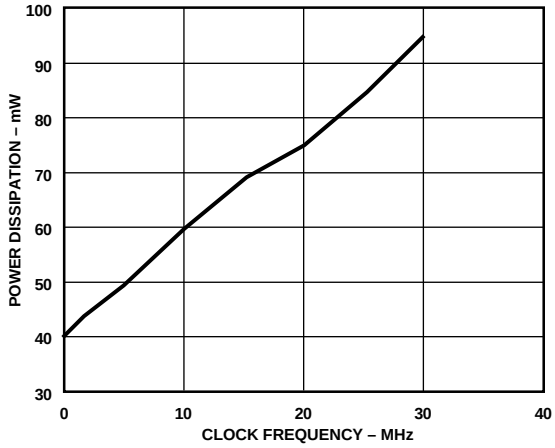


Figure 15. Power Dissipation vs. Clock Frequency

In applications sensitive to aperture jitter, the clock signal should have a fall time of less than 3 ns. High speed CMOS logic families (HC/HCT) are recommended for their symmetrical swing and fast rise/fall times. Care should be taken to minimize the fanout and capacitive loading of the clock input line.

DIGITAL INPUTS AND OUTPUTS

The AD775's digital interface uses standard CMOS, with logic thresholds roughly midway between the supplies (DV_{SS}, DV_{DD}). The digital output is presented in straight binary format, with full scale (1111 1111) corresponding to V_{IN} = V_{RT}, and zero (0000 0000) corresponding to V_{IN} = V_{RB}. Excessive capacitive loading of the digital output lines will increase the dynamic power dissipation as well as the on-chip digital noise. Logic fanout and parasitic capacitance on these lines should be minimized for optimum noise performance.

The data output lines may be placed in a high output impedance state by bringing $\overline{OE}$ (Pin 1) to a logic high. Figure 16 indicates typical timing for access and float delay times (t_{HL} and t_{DD} respectively). Note that even when the outputs are in a high impedance state, activity on the digital bus can couple back to the sensitive analog portions of the AD775 and corrupt conversions in progress.

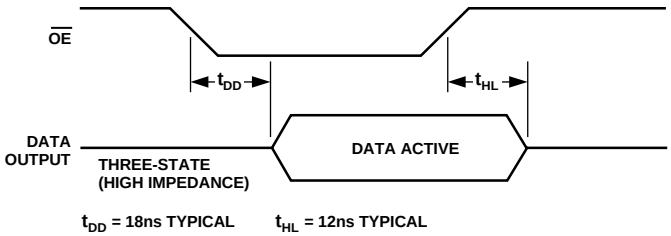


Figure 16. High Impedance Output Timing

POWER SUPPLY CONNECTIONS AND DECOUPLING

The analog and digital supplies of the AD775 have been separate to prevent the typically large transients associated with the on-chip digital circuitry from coupling into the analog supplies (AV_{DD}, AV_{SS}). However, in order to avoid possible latch-up conditions, AV_{DD} and DV_{DD} must share a common supply external to the part, preferably a common source somewhere on the PC board.

Each supply should be decoupled by a 0.1 µF capacitor located as close to the device pin as possible. Surface-mount capacitors, by virtue of their low parasitic inductance, are preferable to through-hole types. A larger capacitor (10 µF electrolytic) should be located somewhere on the board to help decouple large, low frequency supply noise. For specific layout information, refer to the AD775 Evaluation Board section of the data sheet.

APPLICATIONS

AD775 EVALUATION BOARD

Figures 17 through 22 show the schematic and printed circuit board (PCB) layout for the AD775 evaluation board. Referring to Figure 17, the input signal is buffered by U3, an AD817 op amp configured as a unity-gain follower. The signal is then ac-coupled and dc-biased by adjusting potentiometer R14. Video and imaging applications would typically use a dc-restoration circuit instead of the manual potentiometer adjustment. Q1, an emitter-follower, buffers the input signal and provides ample current to drive a simple low-pass filter. The filtering is included to limit wideband noise and highlight the fact that the AD775 can be driven from a nonzero source impedance.

The reference circuit is similar to the one shown in Figure 11 with the exception that R1 and R2 allow precise adjustment of

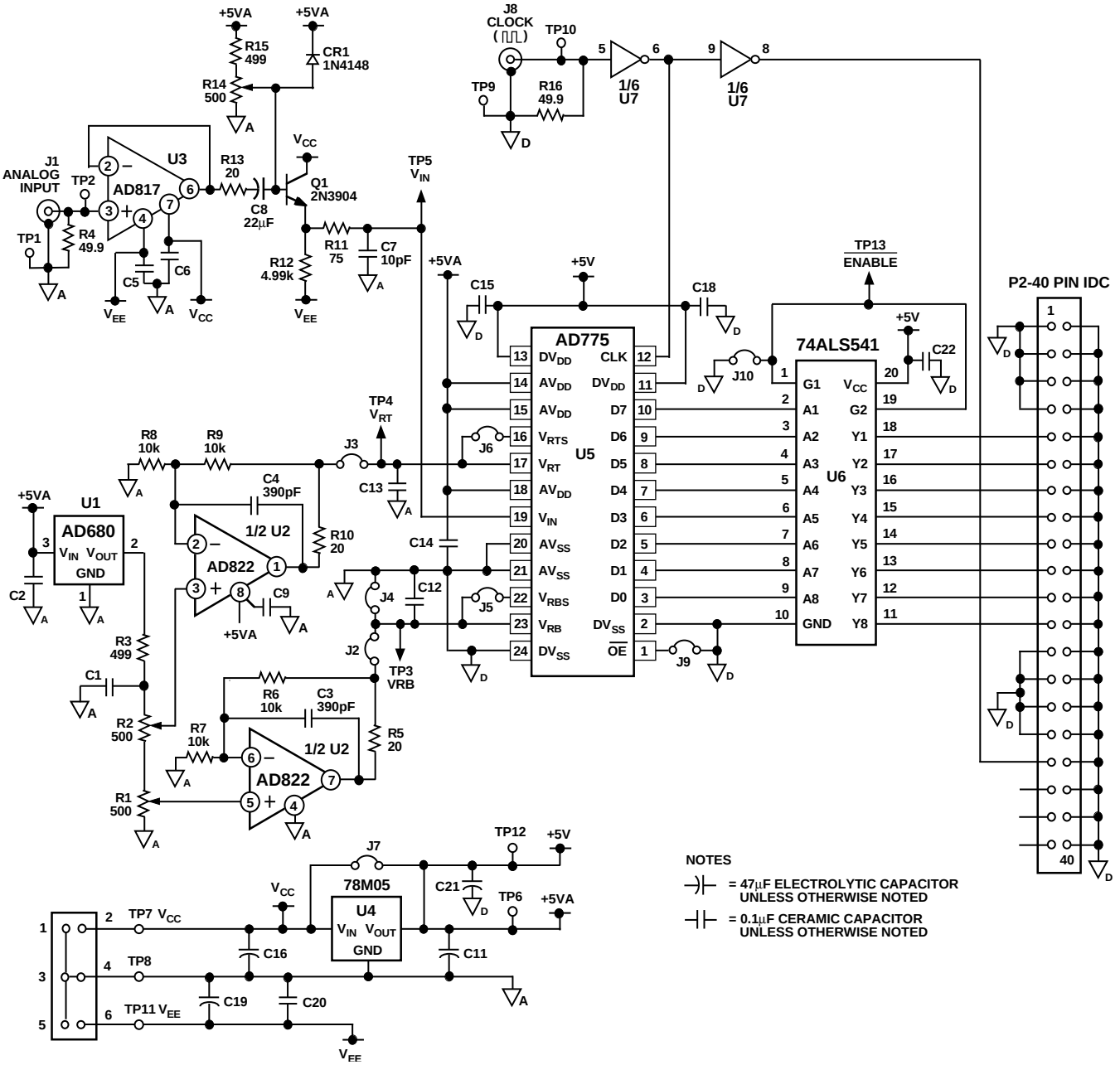


Figure 17. AD775 Evaluation Board Schematic

V_{RT} and V_{RB}. Note that the V_{RT} and V_{RB} traces (see Figures 19 and 20) are run in parallel and in the same proximity. Any noise coupling is likely to be common mode to both signals and would result in an offset error but not a gain error. The entire reference circuit is powered by a single +5 V supply. The minimum voltage for V_{RB} is determined by the impedance of the AD822 output stage and the amount of current flowing through the internal resistor ladder of the AD775.

The sampling clock is buffered by U7, a 74HC04 inverter. It is recommended that the output loading of the inverter is minimized in order to maintain fast transition times on the clock. An additional inverter is used to provide a buffered clock signal whose rising edges indicate that data is valid. A 74ALS541 buffers the eight digital data outputs of the AD775 to improve the load driving capability.

The multilayer PCB board layout shows some of the important design guidelines recommended for the AD775. The most important aspect is the power and ground distribution. While the AD775 has separate analog and digital power and ground pins, the AD775 should be treated as an entirely analog component. The ground plane is joined close to the ADC in order to maintain a low potential difference across the analog and digital ground pins. Because the power and grounds are derived from a common point, a slit in the ground plane is used to minimize any interaction between the analog and digital return currents.

The power for the AD775, AV_{DD} and DV_{DD}, are derived from the same supply. Separate traces are run to AV_{DD} and DV_{DD} and joined together at the source. While not used on the evaluation board, a ferrite bead or inductor can effectively isolate noise generated by digital circuitry such as the output buffers. In cases where only a single supply is available, the inductor should not be placed between AV_{DD} and DV_{DD}. Instead, both supplies of the AD775 should be connected together and isolated from entirely digital components.

Table I. Components List

Reference Designator	Description	Quantity
R1, R2, R14	Potentiometer	3
R3, R15	Resistor, 1%, 499 Ω	2
R4, R13, R16	Resistor, 1%, 49.9 Ω	3
R5, R10	Resistor, 1%, 20 Ω	2
R6–R9	Resistor, 1%, 10 kΩ	4
R11	Resistor, 1%, 75 Ω	1
R12	Resistor, 1%, 4.99 kΩ	1
CR1	Diode, 1N4148	1
C1, C2, C5, C6, C9, C12–C15, C18		
C20, C22, C23	Ceramic Cap, Z5U, 0.1 µF	13
C3, C4	Capacitor, Mica, 390 pF	2
C7	Capacitor, Mica, 10 pF	1
C8	Capacitor, Tantalum, 22 µF, 16 V	1
C11, C16, C19, C21	Capacitor, Alum. Electrolytic, 47 µF, 16 V	4
Q1	Transistor, 2N3904	1
U1	AD680JT	1
U2	AD822AN	1
U3	AD817AN	1
U4	78M05	1
U5	AD775	1
U6	74ALS541N	1
U7	74HC04N	1
J1, J8	BNC Jack	2

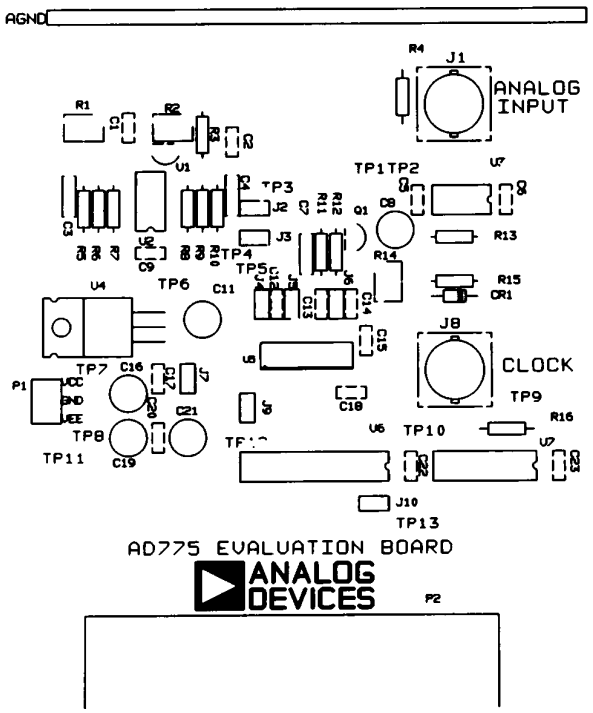


Figure 18. Silkscreen Layer (Not to Scale)

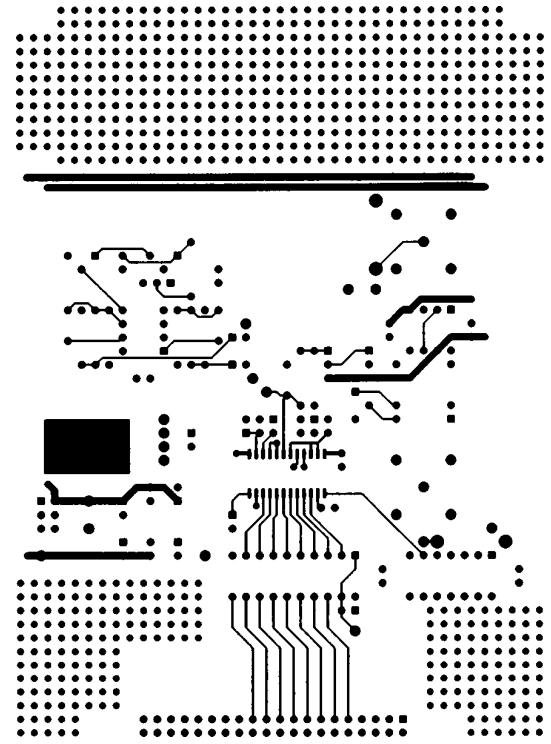


Figure 19. Component Side PCB Layout (Not to Scale)

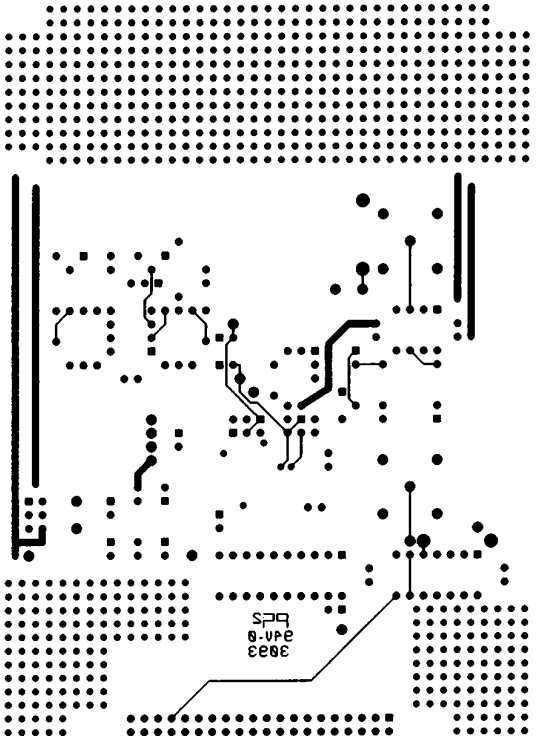


Figure 20. Solder Side PCB Layout (Not to Scale)

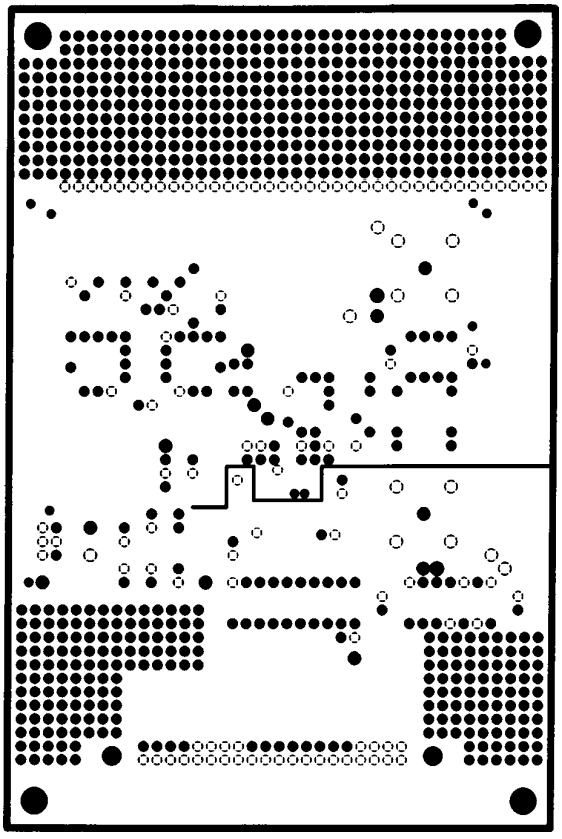


Figure 21. Ground Plane PCB Layout (Not to Scale)

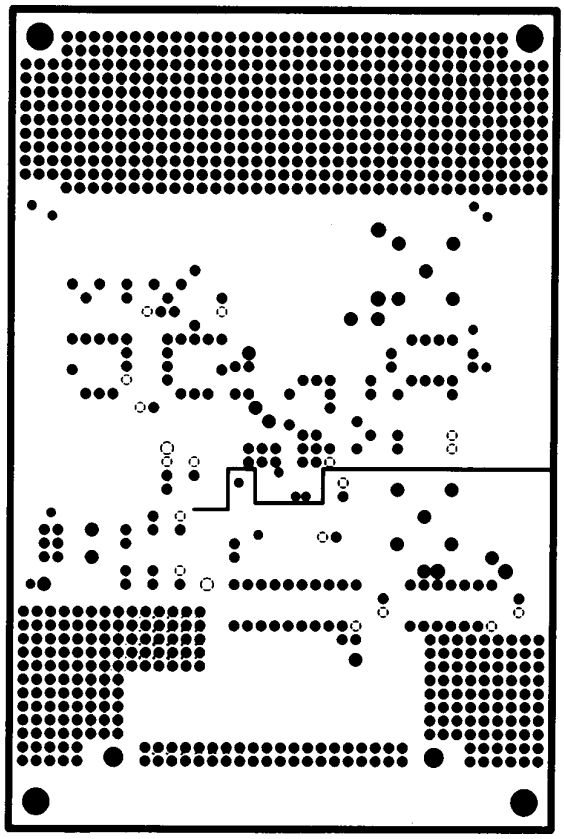


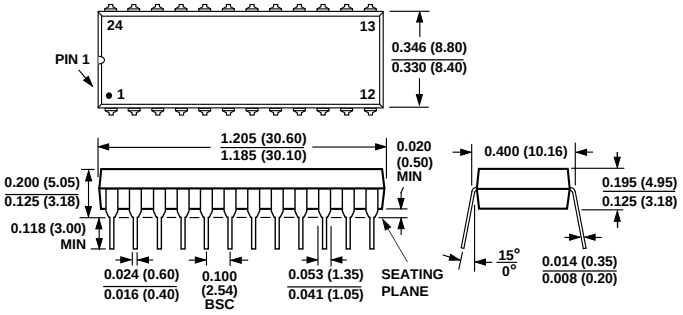
Figure 22. Power Plane PCB Layout (Not to Scale)

C1830–18–8/93

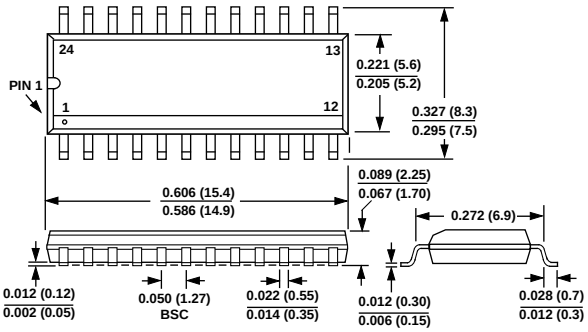
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

Plastic DIP (N-24B)



SOIC (R-24A)



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