1/13-Inch System-On-A-Chip (SOC) CMOS Digital Image Sensor

MT9V115 Datasheet, Rev. E

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Features

- Superior low-light performance
- Ultra-low-power
- VGA video at 30fps
- Internal master clock generated by on-chip phase locked loop (PLL) oscillator
- Electronic rolling shutter (ERS), progressive scan
- Integrated image flow processor (IFP) for single-die camera module
- One-time programmable memory (OTPM)
- Automatic image correction and enhancement, including four-channel lens shading correction
- Arbitrary image scaling with anti-aliasing
- Supports ITU.R.656 format (progressive scan version)
- Two-wire serial interface providing access to registers and microcontroller memory
- Selectable output data format: YCbCr, 565RGB, processed Bayer, RAW8- and RAW8+2-bit, BT656*
- Parallel data output
- Programmable I/O slew rate
- MIPI serial mode supporting 8-bit and 10-bit data streams
- Independently configurable gamma correction
- Direct XDMA access (reducing serial commands)
- Integrated hue rotation

Applications

- Mobile phones
- PC and notebook cameras
- Gaming systems

General Description

ON Semiconductor's MT9V115 is a 1/13-inch CMOS digital image sensor with an active-pixel array of 648H x 488V. It includes sophisticated camera functions such as auto exposure control, auto white balance, black level control, flicker detection and avoidance, and defect correction. It is designed for low light performance. It is programmable through a simple two-wire serial interface. The MT9V115 produces extraordinarily clear, sharp digital pictures that make it the perfect choice for a wide range of applications, including mobile phones, PC and notebook cameras, and gaming systems.

*Supports ITU-R BT.656 format with odd timing code. BT656 is used on interlaced output but this is a progressive scan output

Table 1: Key Parameters

Parameter		Typical Value
Optical format		1/13-inch
Active pixels		648 x 488= 0.3 Mp (VGA)
Pixel size		1.75µm
Color filter array		RGB Bayer
Shutter type		Electronic rolling shutter (ERS)
Input clock range		4 – 44 MHz
Output clock maximum	Parallel	22 MHz
	MIPI	176 Mbps
Output	Parallel	8 bit
	MIPI	8 bit, 10 bit
Frame rate, full resolution		30 fps
Responsivity		1.88 V/lux*sec
SNR_{MAX} (temporal)		34.1 dB
Dynamic range		64 dB
Supply voltage	Digital	1.8 V
	Analog	2.8 V
	MIPI	2.8 V
Power consumption		55 mW(Est.)
Operating temperature (ambient) -T_A		–30°C to +70° C
Chief ray angle		24°
Package options		Wafer, CSP

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Ordering Information

Table 2: Available Part Numbers

Part Number	Product Description	Orderable Product Attribute Description
MT9V115D00STCK22EC1-200	VGA 1/13"SOC	Die Sales, 200μm Thickness
MT9V115EBKSTC-CR	VGA 1/13"CIS SOC	Chip Tray without Protective Film
MT9V115W00STCK22EC1-750	VGA 1/4" SOC	Wafer Sales, 750μm Thickness

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Table of Contents

Features 1
Applications 1
General Description 1
Ordering Information 2
Functional Description 6
Register and Variable Description 32
Slave Address Selection in Dual Camera Application (Only for Parallel Not Supported in Serial) 37
One-Time Programming Memory (OTPM) 37
Spectral Characteristics 38
Electrical Specifications 40
Power Sequence 48
Revision History 51

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List of Figures

Figure 1: MT9V115 Block Diagram . . . 6
Figure 2: Typical Configuration (Connection) . . . 8
Figure 3: Hard Standby Mode Operation . . . 12
Figure 4: Soft Standby Mode Operation . . . 13
Figure 5: Pixel Data Timing Example: 8+2 Bayer format . . . 14
Figure 6: Frame Timing, FV, and LV Structure . . . 14
Figure 7: Sensor Core Block Diagram . . . 16
Figure 8: Pixel Color Pattern Detail . . . 17
Figure 10: Six Pixels in Normal and Column Mirror Readout Mode . . . 18
Figure 11: Eight Pixels in Normal and Column Skip 2X Readout Mode . . . 19
Figure 12: Pixel Readout (no skipping) . . . 19
Figure 13: Pixel Readout (x_odd_inc = 3, y_odd_inc = 1) . . . 20
Figure 14: Image Flow Processor . . . 21
Figure 16: Gamma Correction Curve . . . 25
Figure 17: 0° Hue . . . 26
Figure 18: –22° Hue . . . 27
Figure 19: +22° Hue . . . 27
Figure 20: BT656 Image Data with Odd SAV/EAV Codes . . . 31
Figure 21: Single READ from Random Location . . . 34
Figure 22: Single Read from Current Location . . . 35
Figure 23: Sequential READ, Start from Random Location . . . 35
Figure 24: Sequential READ, Start from Current Location . . . 35
Figure 25: Single WRITE to Random Location . . . 36
Figure 26: Sequential WRITE, Start at Random Location . . . 36
Figure 27: Dual Camera . . . 37
Figure 28: Chief Ray Angle (CRA) vs. Image Height . . . 38
Figure 29: Quantum Efficiency . . . 39
Figure 31: MIPI Clock Timing . . . 44
Figure 32: MIPI Data Timing . . . 46
Figure 33: Two-Wire Serial Bus Timing Parameters . . . 47
Figure 34: Power-Up Sequence . . . 49
Figure 35: Power-Down Sequence . . . 49

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List of Tables

Table 1: Key Parameters . . . 1
Table 2: Available Part Numbers . . . 2
Table 3: Signal Descriptions . . . 10
Table 4: Pad Functionality Based on Output Modes . . . 10
Table 5: Status of Output Signals During Reset and Standby . . . 11
Table 6: Hard Standby Signal Timing . . . 12
Table 7: Soft Standby Signal Timing . . . 13
Table 8: YCbCr Output Data Ordering . . . 30
Table 9: RGB Ordering in Default Mode . . . 30
Table 10: 2-Byte Bayer Format . . . 30
Table 11: Data Formats Supported by MIPI Interface . . . 31
Table 12: Summary of MT9V115 Variables . . . 32
Table 13: Absolute Maximum Ratings . . . 40
Table 14: Operating Conditions . . . 40
Table 15: DC Electrical Characteristics . . . 41
Table 16: Operating/Standby Current Consumption . . . 41
Table 17: AC Electrical Characteristics . . . 42
Table 18: MIPI Timing Measurements: Clock . . . 43
Table 19: MIPI Timing Measurements: Data . . . 44
Table 20: MIPI High Speed (HS) . . . 45
Table 21: MIPI Low Power (LP) . . . 46
Table 22: Two-Wire Serial Interface Timing Data . . . 47
Table 23: Power- Up Signal Timing . . . 49
Table 24: Power-Down Supply Rail Timing . . . 50

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Functional Description

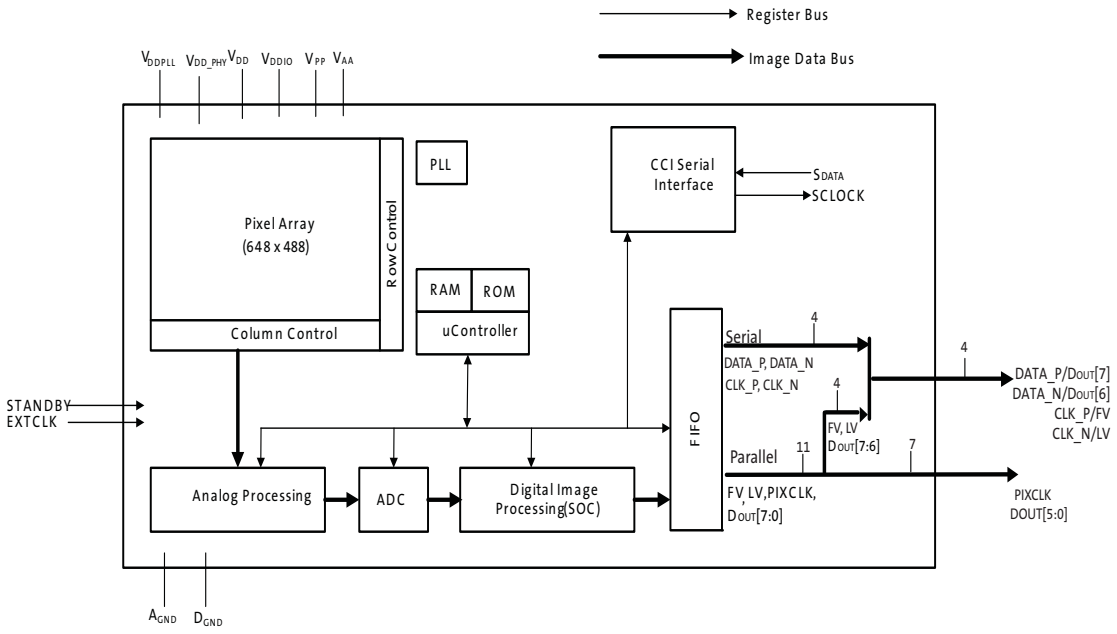
ON Semiconductor's MT9V115 is a 1/13-inch VGA CMOS digital image sensor with an integrated advanced camera system. This camera system features a microcontroller (MCU), a sophisticated image flow processor (IFP), a serial port, and a parallel port. The microcontroller manages all functions of the camera system and sets key operating parameters for the sensor core to optimize the quality of raw image data entering the IFP. The sensor core consists of an active pixel array of 648 x 488 pixels with programmable timing and control circuitry. It also includes an analog signal chain with automatic offset correction, programmable gain, and a 10-bit analog-to-digital converter (ADC).

The entire system-on-a-chip (SOC) has an ultra-low power operational mode and a superior low-light performance that is particularly suitable for mobile applications. The MT9V115 features ON Semiconductor's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost, and integration advantages of CMOS.

Architecture Overview

The MT9V115 combines a VGA sensor core with an IFP to form a stand-alone solution for both image acquisition and processing. Both the sensor core and the IFP have internal registers that can be controlled by the user. In normal operation, an integrated microcontroller autonomously controls most aspects of operation. The processed image data is transmitted to the host system through the serial or parallel bus. Figure 1 shows the major functional blocks of the MT9V115.

Figure 1: MT9V115 Block Diagram



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Sensor Core

The MT9V115 has a color image sensor with a Bayer color filter arrangement and a VGA active-pixel array with electronic rolling shutter (ERS). The sensor core readout is 10 bits. The sensor core also supports separate analog and digital gain for all four color channels (R, Gr, Gb, B).

Image Flow Processor (IFP)

The advanced IFP features and flexible programmability of the MT9V115 can enhance and optimize the image sensor performance. Built-in optimization algorithms enable the MT9V115 to operate with factory settings as a fully automatic and highly adaptable system-on-a-chip (SOC) for most camera systems.

These algorithms include shading correction, defect correction, color interpolation, edge detection, color correction, aperture correction, and image formatting with cropping and scaling.

Microcontroller Unit (MCU)

The MCU communicates with all functional blocks by way of an internal ON Semiconductor proprietary bus interface. The MCU firmware executes the automatic control algorithms for exposure and white balance.

System Control

The MT9V115 has a phase-locked loop (PLL) oscillator that can generate the internal sensor clock from the common system clock. The PLL adjusts the incoming clock frequency up, allowing the MT9V115 to run at almost any desired resolution and frame rate within the sensor's capabilities.

Low-power consumption is a very important requirement for all components of wireless devices. The MT9V115 provides power-conserving features, including an internal soft standby mode and a hard standby mode.

A two-wire serial interface bus enables read and write access to the MT9V115's internal registers and variables. The internal registers control the sensor core, the color pipeline flow, the output interface, auto white balance (AWB) and auto exposure (AE).

Output Interface

The output interface block can select either raw data or processed data. Image data is provided to the host system by an 8-bit parallel port (up to 22MB/sec) or by a serial MIPI port (up tp 176Mbps with 8-bit and 10-bit support). The parallel output port provides 8-bit YCbCr, YUV, 565 RGB, BT656, processed Bayer data or extended 10-bit Bayer data achieved using 8+2 format.

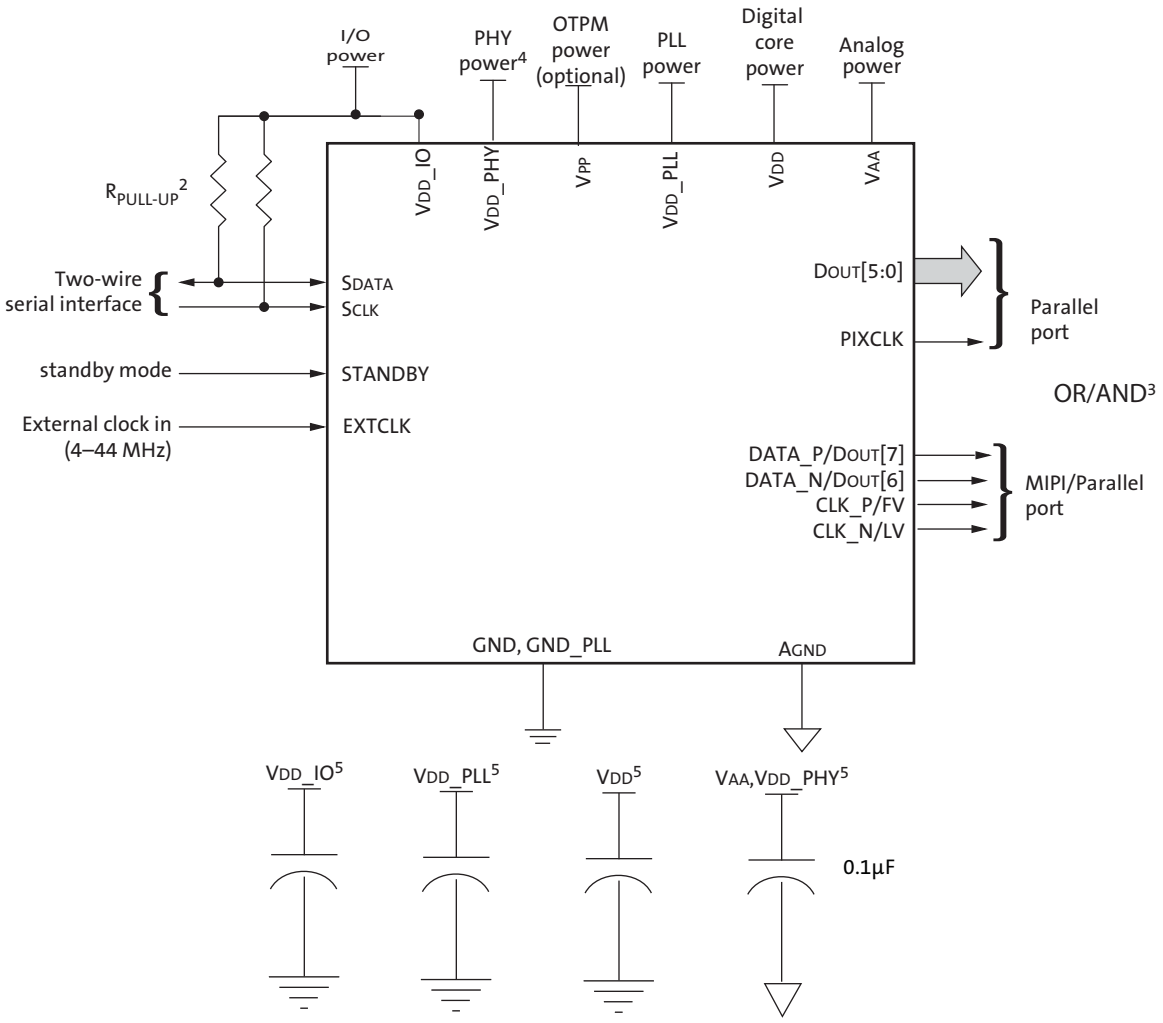
System Interfaces

Figure 2 on page 8 shows typical MT9V115 device connections. For low-noise operation, the MT9V115 requires separate power supplies for analog and digital sections of the die. Both power supply rails should be decoupled from ground using capacitors as close as possible to the die. The use of inductance filters is not recommended on the power supplies or output signals.

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The MT9V115 provides dedicated signals for digital core and I/O power domains that can be at different voltages. The PLL and analog circuitry require clean power sources. Table 3, "Signal Descriptions," on page 10 provides the signal descriptions for the MT9V115.

Figure 2: Typical Configuration (Connection)



Notes:
1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. ON Semiconductor recommends a minimum 1.5kΩ resistor value for the two-wire serial interface RPULL-UP; however, greater values may be used for slower transmission speed.
3. Only one mode, MIPI or Parallel can be used at one time
4. VDD_PHY requires 2.8v nominal in MIPI mode, but can take VDD_IO setting in parallel mode.
5. As a minimum, ON Semiconductor recommends that a 0.1µF decoupling capacitor for each power supply is mounted as close as possible to the pad inside the module. Actual values and numbers may vary depending on layout and design considerations.

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Decoupling Capacitor Recommendations

The minimum recommended decoupling capacitor recommendation is 0.1µF per supply in the module.

It is important to provide clean, well regulated power to each power supply. The ON Semiconductor recommendation for capacitor placement and values are based on our internal demo camera design and verified in hardware.

Note: Since hardware design is influenced by many factors, such as layout, operating conditions, and component selection, the customer is ultimately responsible to ensure that clean power is provided for their own designs.

In order of preference, ON Semiconductor recommends:

1. Mount 0.1µF and 1µF decoupling capacitors for each power supply as close as possible to the pad and place a 10 µF capacitor nearby off-module.
2. If module limitations allow for only six decoupling capacitors for a three-regulator design (V_{DD}_PLL tied to V_{AA}), use a 0.1µF and 1µF capacitor for each of the three regulated supplies. ON Semiconductor also recommends placing a 10µF capacitor for each supply off-module, but close to each supply.
3. If module limitations allow for only three decoupling capacitors, a 1µF capacitor for each of the three regulated supplies is preferred. ON Semiconductor recommends placing a 10µF capacitor for each supply off-module but closed to each supply.
4. If module limitations allow for only three decoupling capacitors, a 0.1µF capacitor for each of the three regulated supplies is preferred. ON Semiconductor recommends placing a 10µF capacitor for each supply off-module but close to each supply.
5. Priority should be given to the V_{AA} supply for additional decoupling capacitors.
6. Inductive filtering components are not recommended.
7. Follow best practices when performing physical layout. Refer to technical notes TN-09-131 and TN-09-214.

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Signal Descriptions

Table 3: Signal Descriptions

Name	Type	Description
EXTCLK	Input	Input clock signal
STANDBY	Input	Controls sensor's standby mode, active HIGH
SCLK	Input	Two-wire serial interface clock
SDATA	I/O	Two-wire serial interface data
FRAME_VALID (FV)	Output	Identifies rows in the active image
LINE_VALID (LV)	Output	Identifies pixels in the active line
PIXCLK	Output	Pixel clock
DOUT[7:0]	Output	DOUT[7:0] for 8-bit image data output
CLK_N	Output	Differential MIPI clock
CLK_P	Output	Differential MIPI clock
DATA_N	Output	DATA_N Output Differential MIPI data
DATA_P	Output	DATA_P Output Differential MIPI data
VDD	Supply	Digital power
DGND	Supply	Digital ground
VDD_IO	Supply	I/O power supply
VPP	Supply	OTPM power supply
VDD_PLL	Supply	PLL power
VDD_PHY	Supply	MIPI power supply
GND_PLL	Supply	PLL ground
VAA	Supply	Analog power
AGND	Supply	Analog ground

Table 4: Pad Functionality Based on Output Modes

Parallel Output	MIPI Output
DOUT[6]	DATA_N
DOUT[7]	DATA_P
FRAME_VALID	CLK_P
LINE_VALID	CLK_N

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Power-On Reset

The MT9V115 includes a power-on reset feature that initiates a reset upon power-up. A soft reset is issued by writing commands through the two-wire serial interface.

Two types of reset are available:

- A soft reset is issued by writing commands (SYSCTL R0x001A[0] = 1)through the two-wire serial interface register 0x1A bit[4:6] during normal operation.
- An internal power-on reset

The output states after hard reset are shown in Table 5 on page 11.

A soft reset sequence to the sensor has the same effect as the hard reset and can be activated by writing to a register through the two-wire serial interface. On-chip power-onreset circuitry can generate an internal reset signal in case an external reset is not provided. The RESET_BAR signal has an internal pull-up resistor and can be left floating.

Standby

The MT9V115 supports two different standby modes:

1. Hard standby mode
2. Soft standby mode

The hard standby mode is invoked by asserting the STANDBY pin. It then disables all of the digital logic within the image sensor, and only supports being awoken by de-asserting the STANDBY pin. The soft standby mode is enabled by a single register access, which then disables the sensor core and most of the digital logic. However, the serial interface is kept alive, which allows the image sensor to be awoken via a serial register access.

All output signal status during standby are shown in Table 5.

Table 5: Status of Output Signals During Reset and Standby

Signal	Reset	Post-Reset	Standby
DOUT[7:0]	High-Z	High-Z	High-Z
PIXCLK	High-Z	High-Z	High-Z
LV	High-Z	High-Z	High-Z
FV	High-Z	High-Z	High-Z
CLK_N	High-Z	0	0
CLK_P	High-Z	0	0
DATA_N	High-Z	0	0
DATA_P	High-Z	0	0

Hard Standby Mode

The MT9V115 can enter hard standby mode by using external STANDBY signal, as shown in Figure 3. The two-wire serial interface and IFP block shut down even when EXTCLK is running during hard standby mode.

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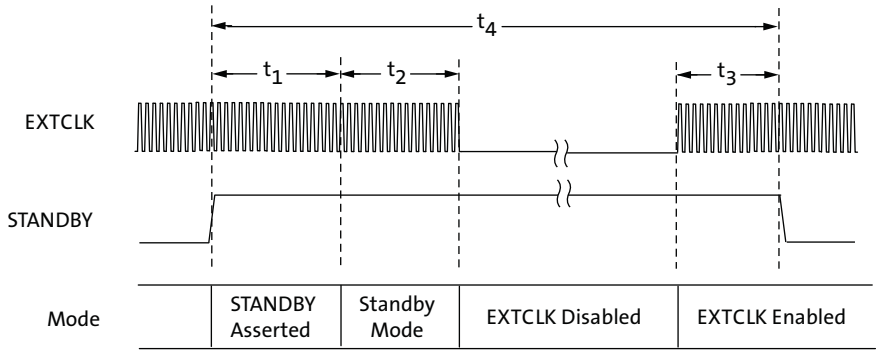
Entering Standby Mode

1. Assert STANDBY signal (HIGH).

Exiting Standby Mode

1. De-assert STANDBY signal (LOW).
2. Part is now ready for streaming.

Figure 3: Hard Standby Mode Operation



Note: In hard standby mode, EXTCLK is automatically gated off, and the two-wire serial interface is not active.

Table 6: Hard Standby Signal Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_1	Standby entry complete (EOF hard standby)	1 Frame + 16742	–	1 Frame + 17032	EXTCLKs
t_2	Active EXTCLK required after STANDBY asserted	10	–	–	EXTCLKs
t_3	Active EXTCLK required before STANDBY de-asserted	10	–	–	EXTCLKs
t_4	STANDBY pulse width	1 Frame + 16762	–	–	EXTCLKs

Soft Standby Mode

The MT9V115 can enter soft standby mode by writing to a SYSCTL register through the two-wire serial interface, as shown in Figure 4. EXTCLK can be stopped to reduce the power consumption during soft standby mode. However, since two-wire serial interface requires EXTCLK to operate, ON Semiconductor recommends that EXTCLK run continuously.

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Entering Standby Mode

1. Set SYSCTL 0x0018[0] to "1" to initiate standby mode.
2. Check until SYSCTL 0x0018[14] changes to "1" to indicate MT9V115 is in standby mode.
3. Turn EXTCLK off.

Exiting Standby Mode

1. Turn EXTCLK on.
2. Reset SYSCTL register 0x0018[0] to "0."
3. Check until SYSCTL register 0x0018[14] changes to "0".

Note: Steps 1 is only necessary in soft standby mode if EXTCLK is turned off.

Figure 4: Soft Standby Mode Operation

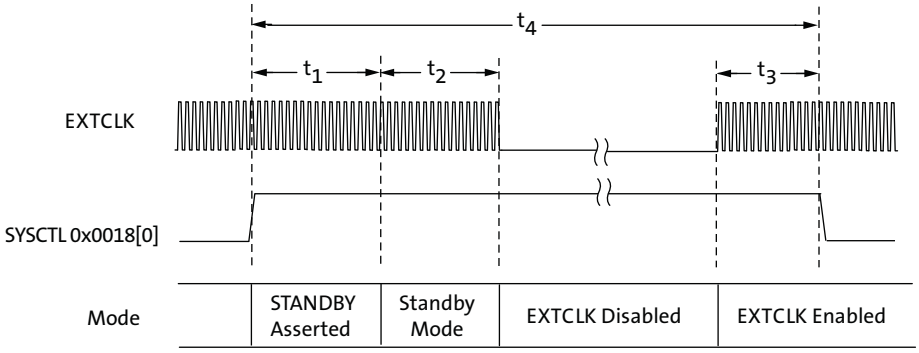


Table 7: Soft Standby Signal Timing

Symbol	Parameter	Min	Typ	Max	Unit
t_1	Standby entry complete (0x301A[4] = 1)	1 Frame + 16742	–	1 Frame + 17032	EXTCLKs
t_2	Active EXTCLK required after soft standby activates	10	–	–	EXTCLKs
t_3	Active EXTCLK required before soft standby de-activates	10	–	–	EXTCLKs
t_4	Minimum standby time	1 Frame + 16762	–	–	EXTCLKs

Module ID

The MT9V115 provides 4 bits of module ID that can be read by the host processor from register 0x001A[15:12]. The module ID is programmed through the OTPM.

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Parallel Image Data Output Interface

The user can use the 8-bit parallel output (DOUT[7:0])to transmit the sensor image data in 8-bit YUV or in 8+2 Bayer formats to the host system as shown in Figure 5 for pixel data timing within a line and in Figure 6 for frame and line timing structures.

The MT9V115 has an output FIFO to retain a constant pixel output clock independent from the data output rate variations due to scaling factor (used only in 8-bit YUV).

The MT9V115 image data is read out in a progressive scan mode. Valid image data is surrounded by horizontal blanking and vertical blanking. The amount of horizontal blanking and vertical blanking are programmable.

MT9V115 output data is synchronized with the PIXCLK output. When LINE_VALID(LV) is HIGH, one pixel value (10-bit bayer data) is output through PIXCLK period as shown in Figure 5. PIXCLK is continuously running as default even during the blanking period.The MT9V115 can be programmed to delay the PIXCLK edge relative to the DOUT transitions. Also, PIXCLK phase can be programmed by the user.

Figure 5: Pixel Data Timing Example: 8+2 Bayer format

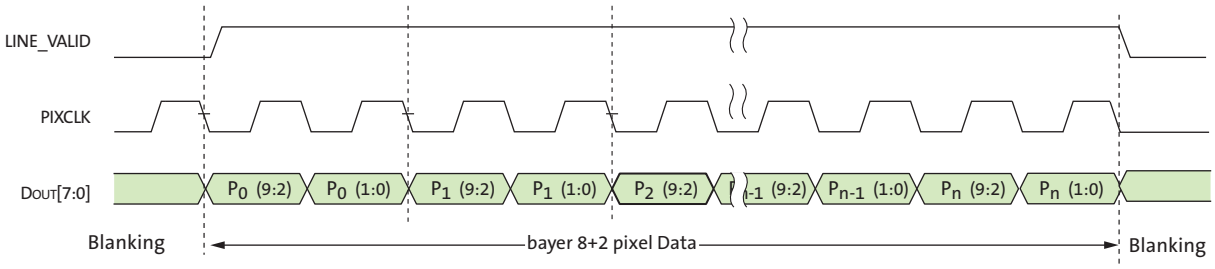
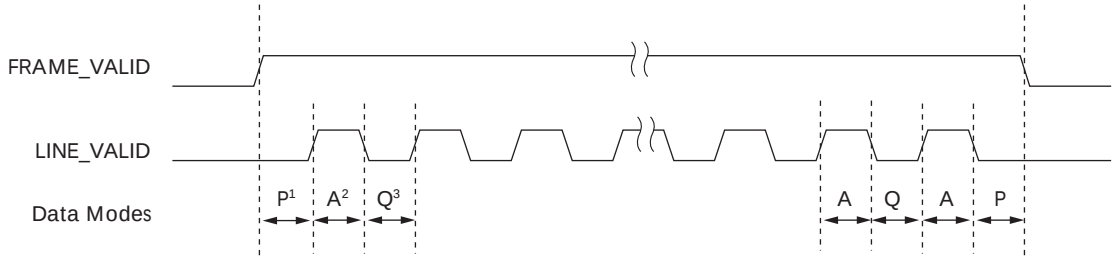


Figure 6: Frame Timing, FV, and LV Structure



Note:
1. P: Frame start and end blanking time.
2. A: Active data time.
3. Q: Horizontal blanking time

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Serial Port

This section describes how frames of pixel data are represented on the high-speed MIPI serial interface. The MIPI output transmitter implements a serial differential sub-LVDS transmitter capable of up to 176 Mb/s. It supports multiple formats, error checking, and custom short packets.

When the sensor is in the hard standby system state or in the soft standby system state, the MIPI signals (CLK_P, CLK_N, DATA_P, DATA_N) indicate ultra low power state (ULPS) corresponding to (nominal) 0V levels being driven on CLK_P, CLK_N, DATA_P, and DATA_N. This is equivalent to signaling code LP-00.

When the sensor enters the streaming state, the interface goes through the following transitions:

1. After the PLL has locked and the bias generator for the MIPI drivers has stabilized, the MIPI interface transitions from the ULPS state to the ULPS-exit state (signaling code LP–10).
2. After a delay (TWAKEUP), the MIPI interface transitions from the ULPS-exit state to the TX-stop state (signaling code LP–11).
3. After a short period of time (the programmed integration time plus a fixed overhead), frames of pixel data start to be transmitted on the MIPI interface. Each frame of pixel data is transmitted as a number of high-speed packets. The transition from the TXstop state to the high-speed signaling states occurs in accordance with the MIPI specifications.
   Between high-speed packets and between frames, the MIPI interface idles in the TX-stop state. The transition from the high-speed signaling states and the TX-stop state takes place in accordance with the MIPI specifications.
4. If the sensor is reset, any frame in progress is aborted immediately and the MIPI signals switch to indicate the ULPS.
5. If the sensor is taken out of the streaming system state and SYSCTL R0x0042[0] = 1 (standby end-of-frame), any frame in progress is completed and the MIPI signals switch to indicate the ULPS.

If the sensor is taken out of the streaming system state and SYSCTL R0x0042[0] = 0 (standby end-of-line), any frame in progress is aborted as follows:

1. Any long packet in transmission is completed.
2. The end of frame short packet is transmitted.

After the frame has been aborted, the MIPI signals switch to indicate the ULPS.

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Sensor Control

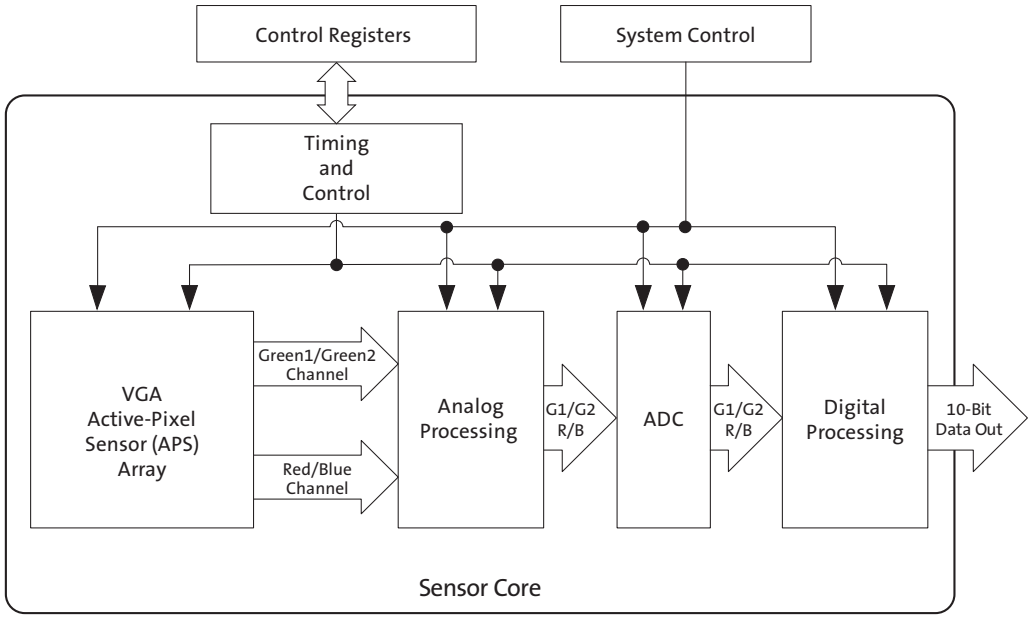
The sensor core of the MT9V115 is a progressive-scan sensor that generates a stream of pixel data at a constant frame rate. Figure 7 shows a block diagram of the sensor core. It includes the VGA active-pixel array. The timing and control circuitry sequences through the rows of the array, resetting and then reading each row in turn. In the time interval between resetting a row and reading that row, the pixels in the row integrate incident light. The exposure is controlled by varying the time interval between reset and readout. Once a row has been selected, the data from each column is sequenced through an analog signal chain, including offset correction, gain adjustment, and ADC. The final stage of the sensor core converts the output of the ADC into 10-bit data for each pixel in the array.

The pixel array contains optically active and light-shielded (dark) pixels. The dark pixels are used to provide data for the offset-correction algorithms (black level control).

The sensor core contains a set of control and status registers that can be used to control many aspects of the sensor behavior including the frame size, exposure, and gain setting. These registers are controlled by the MCU firmware and are also accessible by the host processor through the two-wire serial interface.

The output from the sensor core is a Bayer pattern; alternate rows are a sequence of either red and green pixels or blue and green pixels. The offset and gain stages of the analog signal chain provide per-color control of the pixel data.

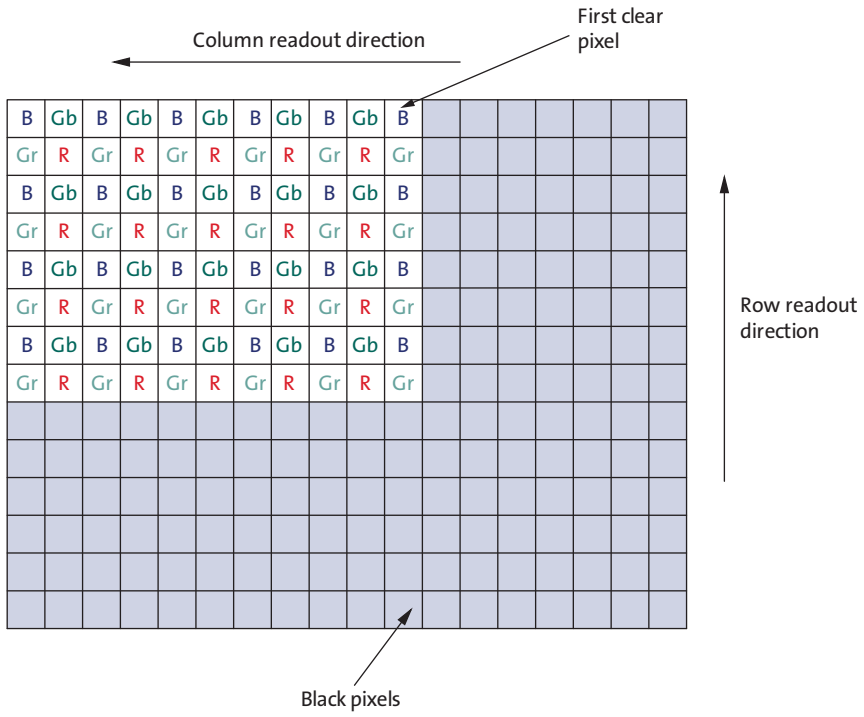
Figure 7: Sensor Core Block Diagram



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The sensor core uses a Bayer color pattern, as shown in Figure 8. The even-numbered rows contain green and red pixels; odd-numbered rows contain blue and green pixels. Even-numbered columns contain green and blue pixels; odd-numbered columns contain red and green pixels.

Figure 8: Pixel Color Pattern Detail

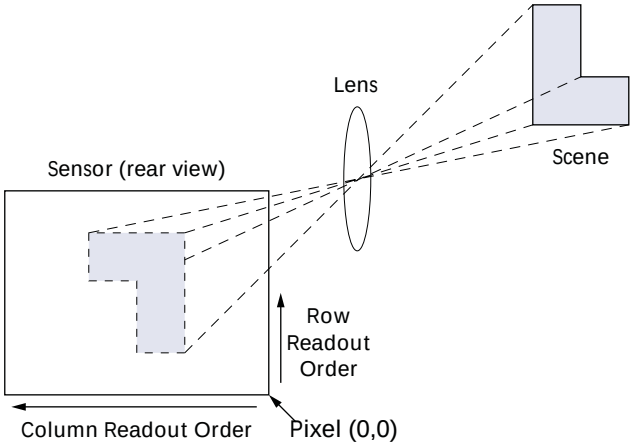


The MT9V115 sensor core pixel array is shown which reflects the layout of the array on the die. Figure 9 on page 18 shows the image shown in the sensor during normal operation.

When the image is read out of the sensor, it is read one row at a time, with the rows and columns sequenced.

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Figure 9: Imaging a Scene



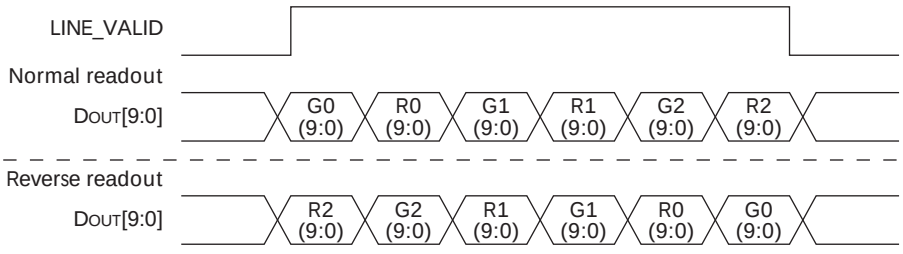
The sensor core supports different readout options to modify the image before it is sent to the IFP. The readout can be limited to a specific window size of the original pixel array.

By changing the readout order, the image can be mirrored in the horizontal direction.

The image output size is set by programming row and column start and end address registers. The four edge pixels in the 648 x 488 array are present to avoid edge effects and are not included in the visible window.

When the sensor is configured to mirror the image horizontally, the order of pixel readout within a row is reversed, so that readout starts from the last column address and ends at the first column address. Figure 10 shows a sequence of 6 pixels being read out with normal readout and reverse readout. This change in sensor core output is corrected by the IFP.

Figure 10: Six Pixels in Normal and Column Mirror Readout Mode



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Figure 11: Eight Pixels in Normal and Column Skip 2X Readout Mode

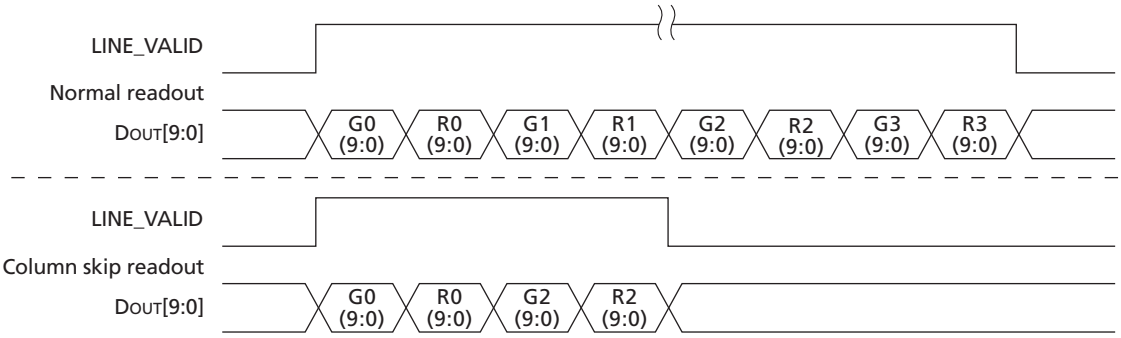
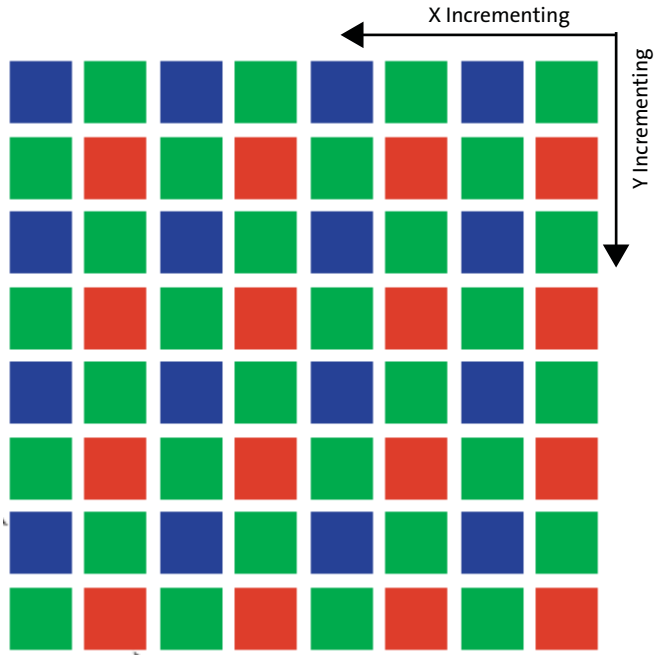


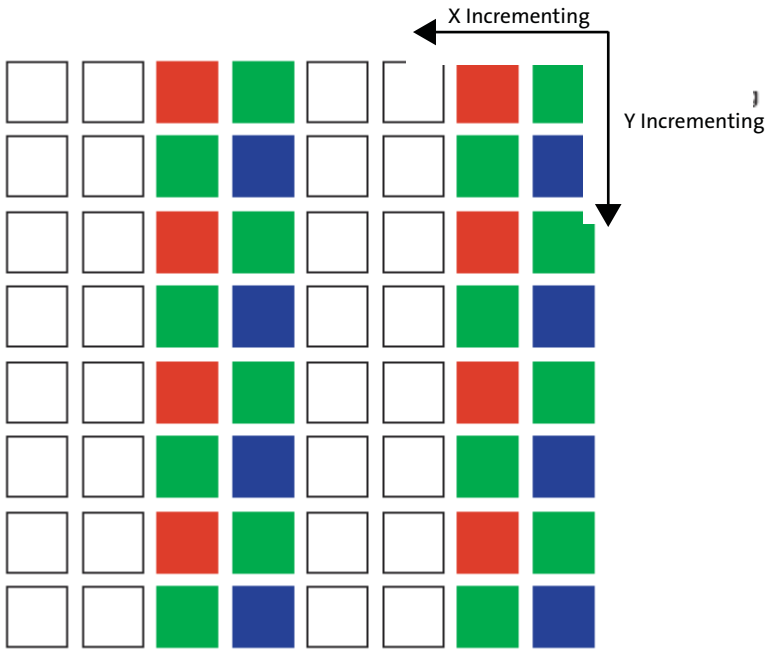
Figure 12 on page 19 through Figure on page 21 show the different skipping modes supported in MT9V115.

Figure 12: Pixel Readout (no skipping)



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Figure 13: Pixel Readout (x_odd_inc = 3, y_odd_inc = 1)

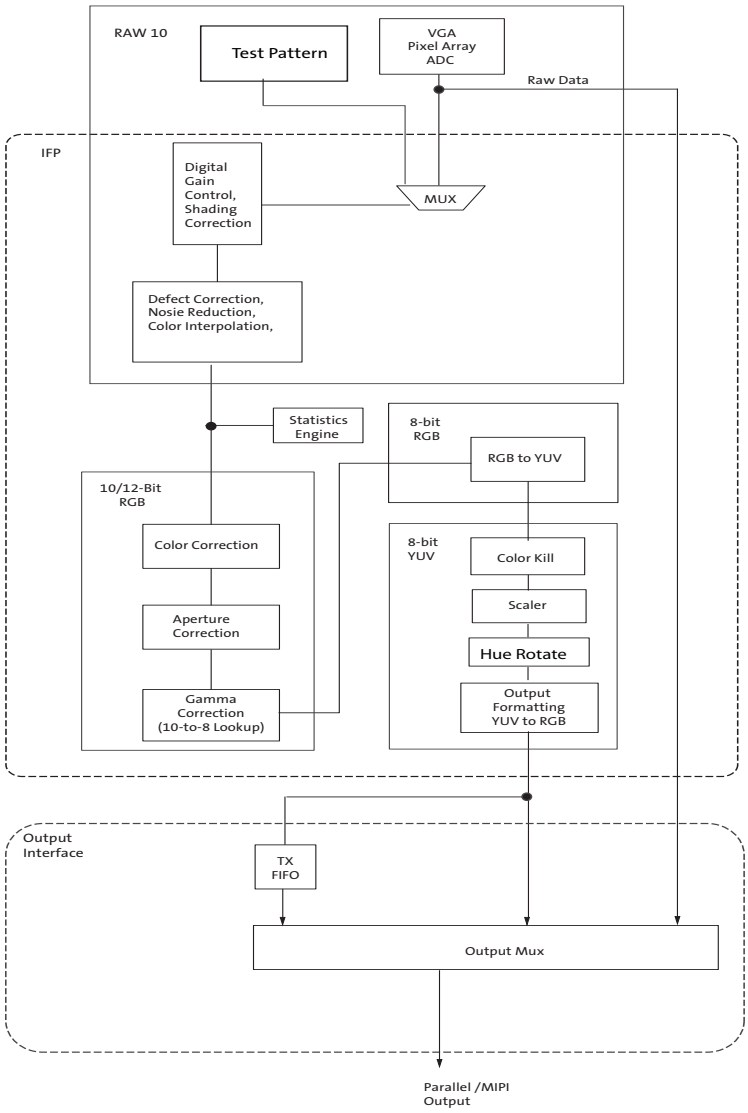


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Image Flow Processor

Image control processing in the MT9V115 is implemented in the IFP hardware logic. The IFP registers can be programmed by the host processor. For normal operation, the microcontroller automatically adjusts the operational parameters of the IFP. Figure 14 shows the image data processing flow within the IFP.

Figure 14: Image Flow Processor



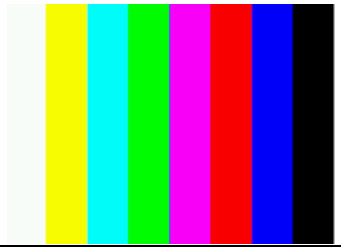
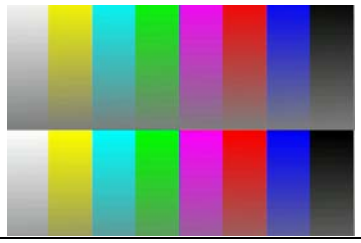
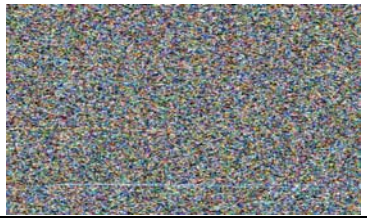
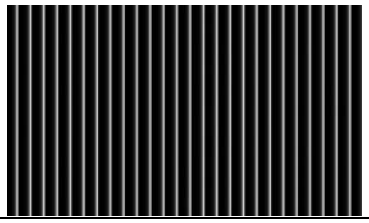
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For normal operation of the MT9V115, streams of raw image data from the sensor core are continuously fed into the color pipeline. The MT9V115 features an automatic color bar test pattern generation function to emulate sensor images as shown in Figure 15 on page 23.

Figure 15: Color Bar Test Pattern

Test Pattern	Example

FIELD_WR= SEQ_CMD, 0x15 // solid color
REG=0x3072, 0x0200 // RED
REG=0x3074, 0x0200 // GREEN RED
REG=0x3076, 0x0200 // BLUE
REG=0x3078, 0x0200 // GREEN BLUE
	

FIELD_WR= SEQ_CMD, 0x16 //100% color bar	
FIELD_WR= SEQ_CMD, 0x17 //fade to gray	
FIELD_WR= SEQ_CMD, 0x18 // pseudo random	
FIELD_WR= SEQ_CMD, 0x19 // marching ones	

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Image Corrections

Image stream processing starts with the multiplication of all pixel values by a programmable digital gain. This can be independently set to separate values for each color channel (R, Gr, Gb, B). Independent color channel digital gain can be adjusted with variables.

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The MT9V115 has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

The IFP performs continuous defect correction that can mask pixel array defects such as high dark-current (hot) pixels and pixels that are darker or brighter than their neighbors due to photoresponse nonuniformity. The module is edge-aware with exposure that is based on configurable thresholds. The thresholds are changed continuously based on the brightness of the current scene. Enabling and disabling noise reduction, and setting thresholds can be defined through variable settings.

Color Interpolation and Edge Detection

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 10-bit integer, which can be considered proportional to the pixel's response to a one-color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including the defect correction, preserve the one-color-per-pixel nature of the data stream, but after the defect correction it must be converted to a three-colors-per-pixel stream appropriate for standard color processing. The conversion is done by an edge-sensitive color interpolation module. The module adds the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high-frequency noise in flat field areas. The edge threshold can be set through variable settings.

Color Correction and Aperture Correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The color correction matrix can either be programmed by the user or automatically selected by the AWB algorithm implemented in the IFP. Color correction should ideally produce output colors that are independent of the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics. The color correction variables can be adjusted through variable settings.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to color-corrected image data. The gain and threshold for 2D correction can be defined through variable settings.

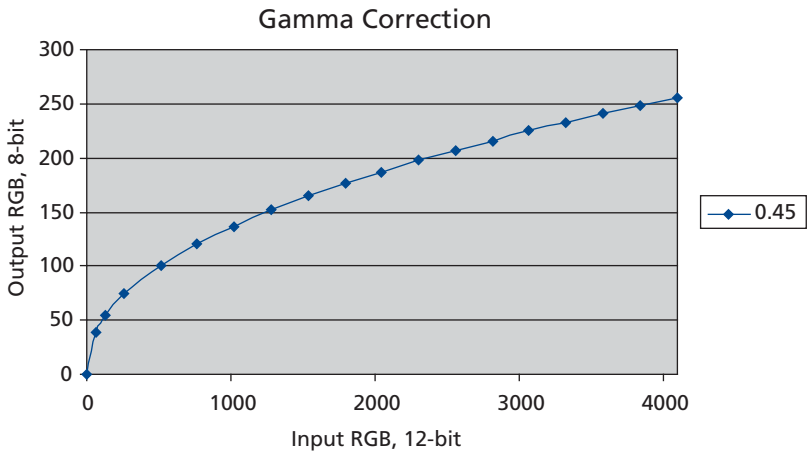
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Gamma Correction

The gamma correction curve (as shown in Figure 16) is implemented as a piecewise linear function with 19 knee points, taking 12-bit arguments and mapping them to 8-bit output. The abscissas of the knee points are fixed at 0, 64, 128, 256, 512, 768, 1024, 1280, 1536, 1792, 2048, 2304, 2560, 2816, 3072, 3328, 3584, 3840, and 4096.

The MT9V115 IFP includes a block for gamma correction that has the capability to adjust its shape, based on brightness, to enhance the performance under certain lighting conditions. Two custom gamma correction tables may be uploaded, one corresponding to a high lighting condition, the other one corresponding to a low lighting condition. The final gamma correction table used depends on the brightness of the scene and can take the form of either uploaded tables or an interpolated version of the two tables. A single (non-adjusting) table for all conditions can also be used.

Figure 16: Gamma Correction Curve



Special effects like negative image, sepia solarization, or B/W can be applied to the data stream at this point. These effects can be enabled and selected by cam_select_fx variable.

To remove high- or low-light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

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Image Scaling and Cropping

To ensure that the size of images output by the MT9V115 can be tailored to the needs of all users, the IFP includes a scaler module. When enabled, this module performs rescaling of incoming images—shrinks them to selected width and height without reducing the field of view and without discarding any pixel values. The scaler ratios are automatically computed from image output size and the FOV. The scaled output must not be greater than 352. Output widths greater than this must not use the scaler but instead must reduce the field of view.

By configuring the cropped and output windows to various sizes, different zooming levels such as 4X, 2X, and 1X can be achieved. The height and width definitions for the output window must be equal to or smaller than the cropped image. The image cropping and scaler module can be used together to implement a digital zoom.

Hue Rotate

The MT9V115 has integrated hue rotate. This feature will help for improving the color image quality and give customers the flexibility for fine color adjustment and special color effects.

Figure 17: 0° Hue



CAM VAR8= 0xA00F, 0x00 // CAM_HUE_ANGLE

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Figure 18: –22° Hue



CAM VAR8= 0xA00F, 0xEA // CAM_HUE_ANGLE

Figure 19: +22° Hue



CAM VAR8= 0xA00F, 0x16 // CAM_HUE_ANGLE

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Auto Exposure

The AE algorithm performs automatic adjustments of the image brightness by controlling exposure time, and analog gains of the sensor core as well as digital gains applied to the image.

The AE algorithm analyzes image statistics collected by the exposure measurement engine, and then programs the sensor core and color pipeline to achieve the desired exposure. AE uses 4 x 4 exposure statistics windows, which can be scaled in size to cover any portion of the image.

The MT9V115 uses Average Brightness Tracking (Average Y), which uses a constant average tracking algorithm where a target brightness value is compared to a current brightness value, and the gain and integration time are adjusted accordingly to meet the target requirement. The MT9V115 also has a weighted AE algorithm that allows the sensor to be configured to respond to scene illuminance based on each of the weights in the 4 x 4 exposure statistics windows.

The auto exposure can be configured to respond to scene illuminance based on certain criteria by adjusting gains and integration time based on scene brightness.

Auto White Balance

The MT9V115 has a built-in AWB algorithm designed to compensate for the effects of changing spectra of the scene illumination on the quality of the color rendition. The algorithm consists of two major parts: a measurement engine performing statistical analysis of the image and a module performing the selection of the optimal color correction matrix, digital, and sensor core analog gains. While default settings of these algorithms are adequate in most situations, the user can reprogram base color correction matrices and place limits on color channel gains.

The AWB algorithm estimates the dominant color temperature of a light source in a scene and adjusts the B/G, R/G gain ratios accordingly to produce an image for sRGB display in which grey and white surfaces are reproduced faithfully. This usually means that R,G,B are roughly equal for these surfaces hence the word “balance”.

The AWB algorithm uses statistics collected from the last frame to calculate the required B/G and R/G ratios and set the blue and red analog sensor gains and digital SOC gains to reproduce the most accurate grey and white surfaces in future frames.

Flicker Detection and Avoidance

Flicker occurs when the integration time is not an integer multiple of the period of the light intensity. The automatic flicker detection module does not compensate for the flicker, but rather avoids it by detecting the flicker frequency and adjusting the integration time. For integration times below the light intensity period (10ms for 50Hz environment, 8.33ms for 60Hz environment), flicker cannot be avoided.

While this fast flickering is marginally detectable by the human eye, it is very noticeable in digital images because the flicker period of the light source is very close to the range of digital images’ exposure times.

Many CMOS sensors use a “rolling shutter” readout mechanism that greatly improves sensor data readout times. This allows pixel data to be read out much sooner than other methods that wait until the entire exposure is complete before reading out the first pixel data. The rolling shutter mechanism exposes a range of pixel rows at a time. This range of exposed pixels starts at the top of the image and then “rolls” down to the bottom

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during the exposure period of the frame. As each pixel row completes its exposure, it is ready to be read out. If the light source oscillates (flickers) during this rolling shutter exposure period, the image appears to have alternating light and dark horizontal bands.

If the sensor uses the traditional snapshot readout mechanism, in which all pixels are exposed at the same time and then the pixel data is read out, then the image may appear overexposed or underexposed due to light fluctuations from the flickering light source. Lights operating on AC electric systems produce light flickering at a frequency of 100Hz or 120Hz, twice the frequency of the power line.

To avoid this flicker effect, the exposure times must be multiples of the light source flicker periods. For example, in a scene lit by 60Hz AC power source, the available exposure times are 8.33ms (1/120), 16.67ms, 25ms, 33.33ms, and so on.

In this case, the AE algorithm must limit the integration time to an integer multiple of the light's flicker period.

By default, the MT9V115 does all of this automatically, ensuring that all exposure times avoid any noticeable light flicker in the scene. The MT9V115 AE algorithm is always setting exposure times to be integer multipliers of either 100Hz (for 50Hz AC power source) or 120Hz (for 60Hz AC power source). The flicker detection module keeps monitoring the incoming frames to detect whether the scene's lighting has changed to the other of the two light source frequencies. A 50Hz/60Hz Tungsten lamp can be used to calibrate the flicker detect settings.

Output Conversion and Formatting

The YUV data stream can either exit the color pipeline as is or be converted before exit to an alternative YUV or RGB data format.

Color Conversion Formulas

Y'U'V'

This conversion is BT 601 scaled to make YUV range from 0 through 255. This setting is recommended for JPEG encoding and is the most popular, although it is not well defined and often misused in various operating systems.

$$Y' = 0.299 \times R' + 0.587 \times G' + 0.114 \times B' \quad \text{(EQ 1)}$$

$$U' = 0.564 \times (B' - Y') + 128 \quad \text{(EQ 2)}$$

$$V' = 0.713 \times (R' - Y') + 128 \quad \text{(EQ 3)}$$

There is an option where 128 is not added to U'V'.

Y'Cb'Cr' Using sRGB Formulas

The MT9V115 implements the sRGB standard. This option provides YCbCr coefficients for a correct 4:2:2 transmission.

Note: 16 < Y601< 235; 16 < Cb < 240; 16 < Cr < 240; and 0 < = RGB < = 255

$$Y' = (0.2126 \times R' + 0.7152 \times G' + 0.0722 \times B') \times (219/256) + 16 \quad \text{(EQ 4)}$$

$$Cb' = 0.5389 \times (B' - Y') \times (224/256) + 128 \quad \text{(EQ 5)}$$

$$Cr' = 0.635 \times (R' - Y') \times (224/256) + 128 \quad \text{(EQ 6)}$$

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Y'U'V' Using sRGB Formulas

These are similar to the previous set of formulas, but have YUV spanning a range of 0 through 255.

$$Y' = 0.2126 \times R' + 0.7152 \times G' + 0.0722 \times B' \quad \text{(EQ 7)}$$

$$U' = 0.5389 \times (B' - Y') + 128 = -0.1146 \times R' - 0.3854 \times G' + 0.5 \times B' + 128 \quad \text{(EQ 8)}$$

$$V' = 0.635 \times (R' - Y') + 128 = 0.5 \times R' - 0.4542 \times G' - 0.0458 \times B' + 128 \quad \text{(EQ 9)}$$

There is an option to disable adding 128 to U'V'. The reverse transform is as follows:

$$R' = Y + 1.5748 \times V - 128 \quad \text{(EQ 10)}$$

$$G' = Y - 0.1873 \times (U - 128) - 0.4681 \times (V - 128) \quad \text{(EQ 11)}$$

$$B' = Y + 1.8556 \times (U - 128) \quad \text{(EQ 12)}$$

Uncompressed YUV/RGB Data Ordering

The MT9V115 supports swapping YCbCr mode, as illustrated in Table 8.

Table 8: YCbCr Output Data Ordering

Mode	Data Sequence			
Default (no swap)	Cb_i	Y_i	Cr_i	Y_{i+1}
Swapped CrCb	Cr_i	Y_i	Cb_i	Y_{i+1}
Swapped YC	Y_i	Cb_i	Y_{i+1}	Cr_i
Swapped CrCb, YC	Y_i	Cr_i	Y_{i+1}	Cb_i

The RGB output data ordering in default mode is shown in Table 9. The odd and even bytes are swapped when luma/chroma swap is enabled. R and B channels are bitwise swapped when chroma swap is enabled.

Table 9: RGB Ordering in Default Mode

Mode (Swap Disabled)	Byte	$D_7D_6D_5D_4D_3D_2D_1D_0$
565RGB	Odd	$R_7R_6R_5R_4R_3G_7G_6G_5$
	Even	$G_4G_3G_2B_7B_6B_5B_4B_3$

Uncompressed 10-Bit Bypass Output

Raw 10-bit Bayer data from the sensor core can be output in bypass mode by using DOUT[7:0] with a special 8 + 2 data format, shown in Table 10.

Table 10: 2-Byte Bayer Format

Byte	Bits Used	Bit Sequence
Odd bytes	8 data bits	$D_9D_8D_7D_6D_5D_4D_3D_2$
Even bytes	2 data bits + 6 unused bits	0 0 0 0 0 0 D_1D_0

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Table 11: Data Formats Supported by MIPI Interface

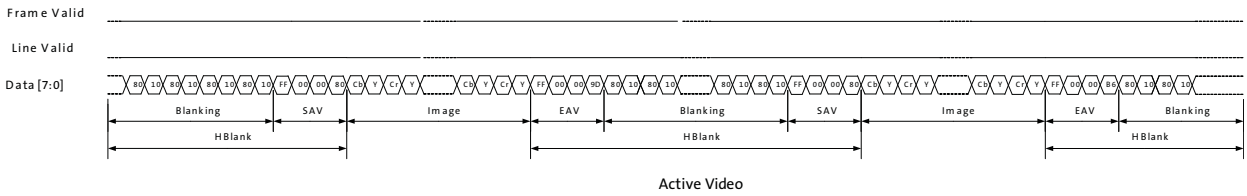
Data Format	Data Type
YUV 422 8-bit	0x1E
565RGB	0x22
RAW8	0x2A
RAW10	0x2B

Note: Data will be packed as RAW8 if the data type specified does not match any of the above data types.

BT656

YUV data can also be output in BT656 format with odd SAV/EAV codes. The BT656 data output will be progressive data and not interlaced (R0x3C00[5] = 1).

Figure 20: BT656 Image Data with Odd SAV/EAV Codes



Defect Correction(DC) and Noise Reduction(NR)

There is also a third output conversion format DCNR which is available in both MIPI and parallel mode. DCNR mode allows the image to be either defect corrected or noise corrected. In MIPI mode it is available as 10 bit output and in Parallel as 8+2 bit output. There is a restriction on the number of lines as four are removed for the process resulting in a maximum 648 x484 output.

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Register and Variable Description

To change internal registers and RAM variables of MT9V115, use the two-wire serial interface through the external host device.

Note: For more detailed information on MT9V115 registers and variables, see the MT9V115 Register and Variable Reference.

The sequencer is responsible for coordinating all events triggered by the user.

The sequencer provides the high-level control of the MT9V115. Commands are written to the command variable to start streaming, stop streaming, and to select test pattern modes. Command execution is confirmed by reading back the command variable with a value of zero. The sequencer state variable can also be checked for transition to the desired state. All configuration of the sensor (start/stop row/column, mirror, skipping) and the SOC (image size, format) and automatic algorithms for AE, AWB, low light, are performed when the sequencer is in the stopped state.

When the sequencer is in the idle or test pattern state the algorithms and register updates are not performed, allowing the host complete manual control.

Table 12: Summary of MT9V115 Variables

Name	Variable Description
Monitor Variables	General information
Sequencer Variables	Programming control interface
Advanced Control Variables	Advanced Control Variables Information
FD Variables	Flicker Detect
AE_Track Variables	Auto Exposure
AWB Variables	Auto White Balance
Stat Variables	Statistics
Low Light Variables	Low Light
Cam Variables	Camera Controls

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Two-Wire Serial Interface

The two-wire serial interface bus enables read and write access to control and status registers within the MT9V115.

The interface protocol uses a master/slave model in which a master controls one or more slave devices. The MT9V115 always operates in slave mode. The host (master) generates a clock (SCLK) that is an input to the MT9V115 and is used to synchronize transfers. Data is transferred between the master and the slave on a bidirectional signal (SDATA).

Protocol

Data transfers on the two-wire serial interface bus are performed by a sequence of low-level protocol elements, as follows:

1. a (repeated) start condition
2. a slave address/data direction byte
3. a 16-bit register address (8-bit addresses are not supported)
4. an (a no) acknowledge bit
5. a 16-bit data transfer (8-bit data transfers are supported using XDMA byte access)
6. a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

A start condition is defined as a HIGH-to-LOW transition on SDATA while SCLK is HIGH.

At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a repeated start or restart condition.

A stop condition is defined as a LOW-to-HIGH transition on SDATA while SCLK is HIGH.

Data is transferred serially, 8 bits at a time, with the most significant bit (MSB) transmitted first. Each byte of data is followed by an acknowledge bit or a no-acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes. One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

MT9V115 Slave Address

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a WRITE, and a “1” indicates a READ. The slave address default is 0x7A.

Messages

Message bytes are used for sending MT9V115 internal register addresses and data. The host should always use 16-bit address (two bytes) and 16-bit data to access internal registers. Refer to READ and WRITE cycles in Figure 21 on page 34 through Figure 25 on page 36.

Each 8-bit data transfer is followed by an acknowledge bit or a no-acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. For data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

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The no-acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no-acknowledge bit is used to terminate a read sequence.

Typical Operation

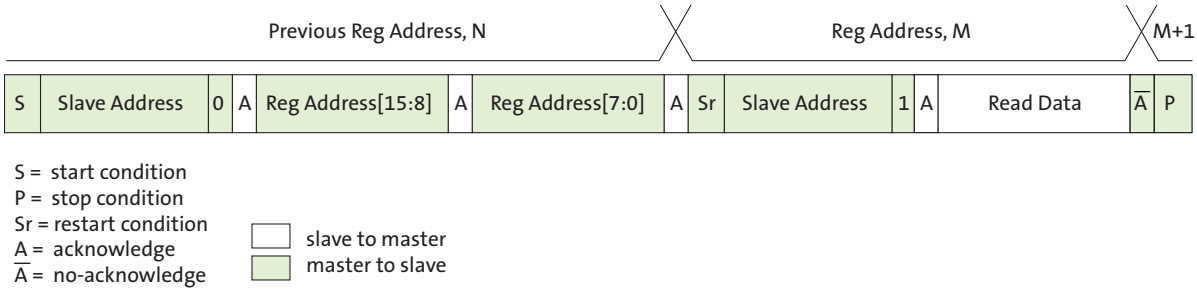
A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8-bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a "0" indicates a WRITE and a "1" indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16-bit register address to which a WRITE will take place. This transfer takes place as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 16-bit data, as two 8-bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8-bit write slave address/data direction byte and 16-bit register address, just as in the WRITE request. The master then generates a (re)start condition and the 8-bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8-bit transfer. The data transfer is stopped when the master sends a no-acknowledge bit.

Single READ from Random Location

Figure 21 shows the typical READ cycle of the host to MT9V115. The first 2 bytes sent by the host are an internal 16-bit register address. The following 2-byte READ cycle sends the contents of the registers to host.

Figure 21: Single READ from Random Location

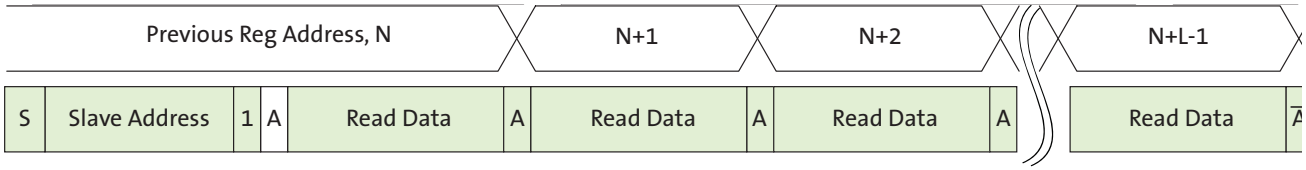


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Single READ from Current Location

Figure 22 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

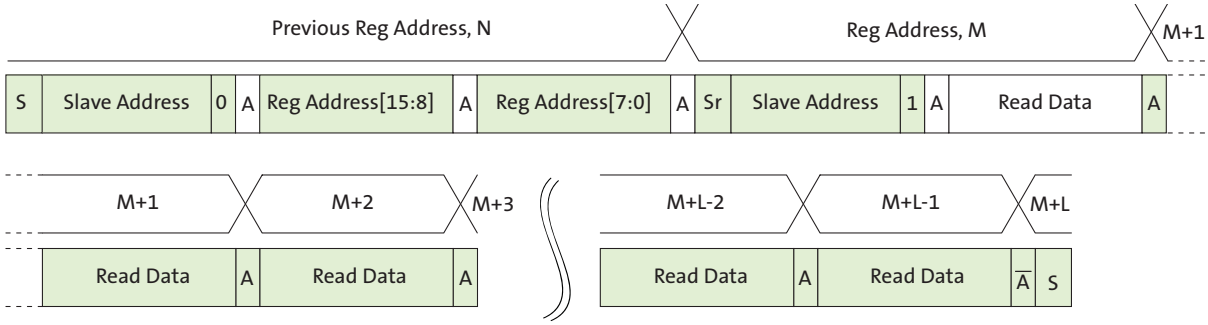
Figure 22: Single Read from Current Location



Sequential READ, Start from Random Location

This sequence (Figure 23) starts in the same way as the single READ from random location (Figure 21 on page 34). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until "L" bytes have been read.

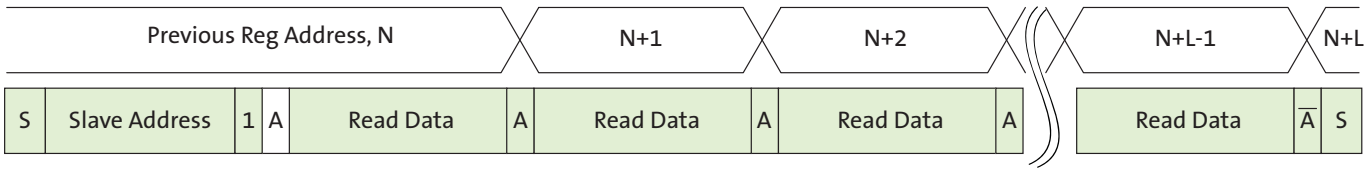
Figure 23: Sequential READ, Start from Random Location



Sequential READ, Start from Current Location

This sequence (Figure 24) starts in the same way as the single READ from current location (Figure 22). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until "L" bytes have been read.

Figure 24: Sequential READ, Start from Current Location

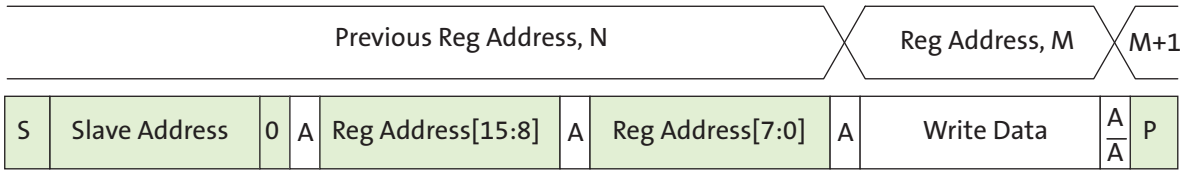


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Single Write to Random Location

Figure 25 shows the typical WRITE cycle from the host to the MT9V115. The first 2 bytes indicate a 16-bit address of the internal registers with most-significant byte first. The following 2 bytes indicate the 16-bit data.

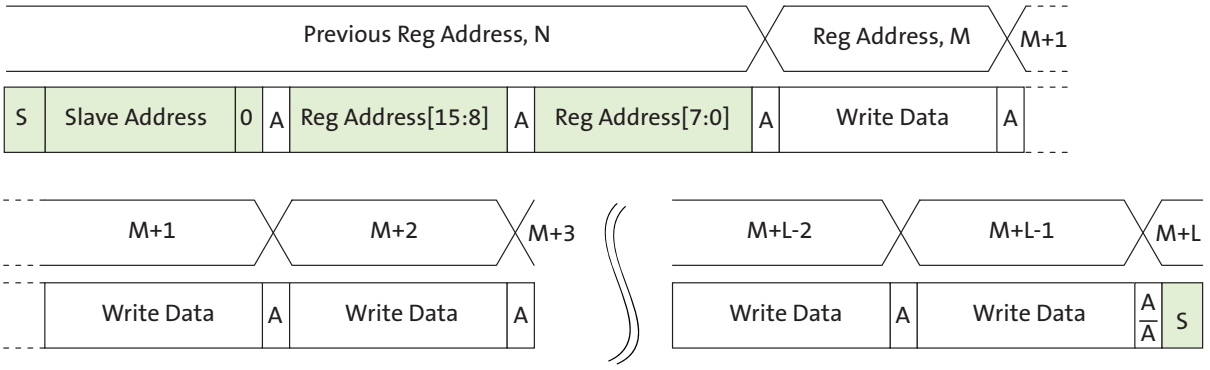
Figure 25: Single WRITE to Random Location



Sequential WRITE, Start at Random Location

This sequence (Figure 26) starts in the same way as the single WRITE to random location (Figure 25). Instead of generating a no-acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

Figure 26: Sequential WRITE, Start at Random Location

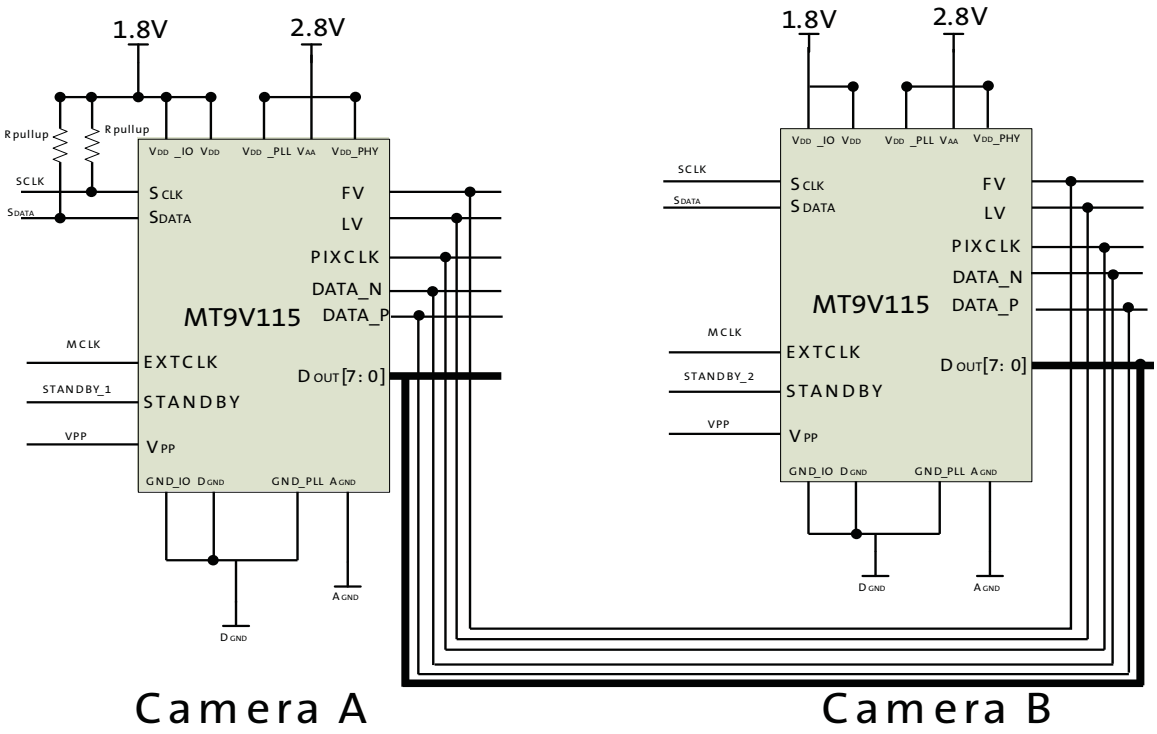


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Slave Address Selection in Dual Camera Application (Only for Parallel Not Supported in Serial)

The MT9V115 offers a special function specifically for mobile phone applications. This is the ability to connect two image sensors in a dual-camera configuration. A block diagram of this mode is shown in Figure 27. By toggling between the two STANDBY pins, the image data can be taken off either image sensor.

Figure 27: Dual Camera



The process for changing the slave address for Camera B is set out below:

1. Power up Camera A (0x7A) and B (0x7A). with HARD STANDBY asserted. (Both Camera A and B are in HARD STANDBY)
2. Take camera B out of HARD STANDBY
3. Change the address of Camera B (0x78) by writing to a register.
4. Put Camera B back to HARD STANDBY
5. Take Camera A out of HARD STANDBY.
   Camera A (0x7A) and Camera B (0x78) now have different slave addresses.

One-Time Programming Memory (OTPM)

The MT9V115 has one-time programmable memory (OTPM) for supporting defect correction, module ID, and other customer-related information. There are 2784 bits of OTPM available for these listed features. The OTPM can be programmed when the VPP voltage is applied.

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Spectral Characteristics

Figure 28: Chief Ray Angle (CRA) vs. Image Height

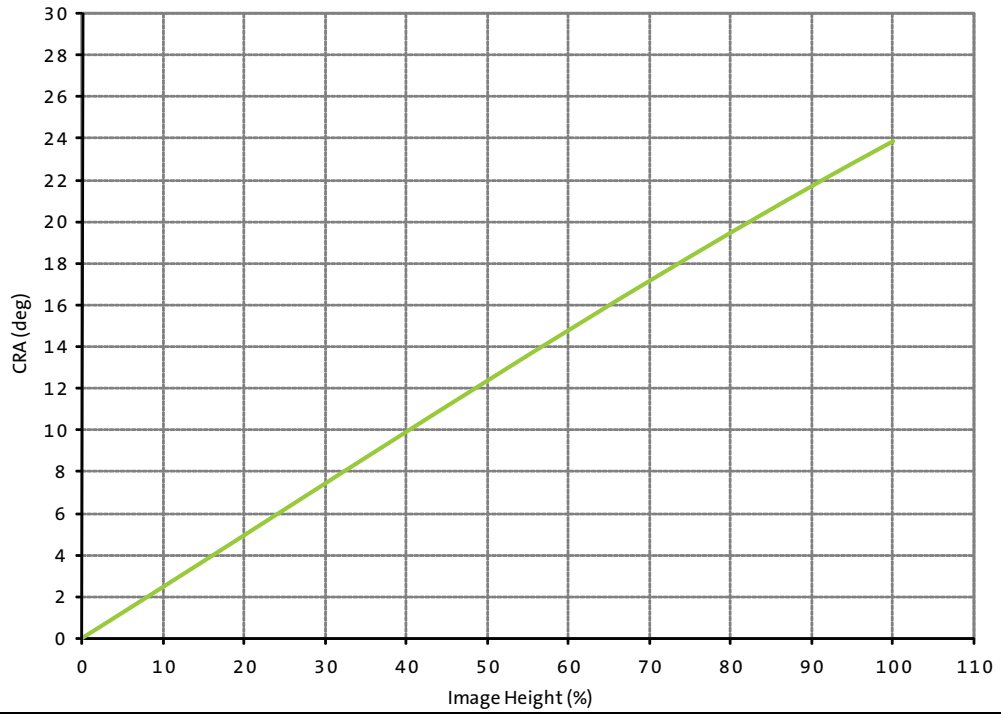
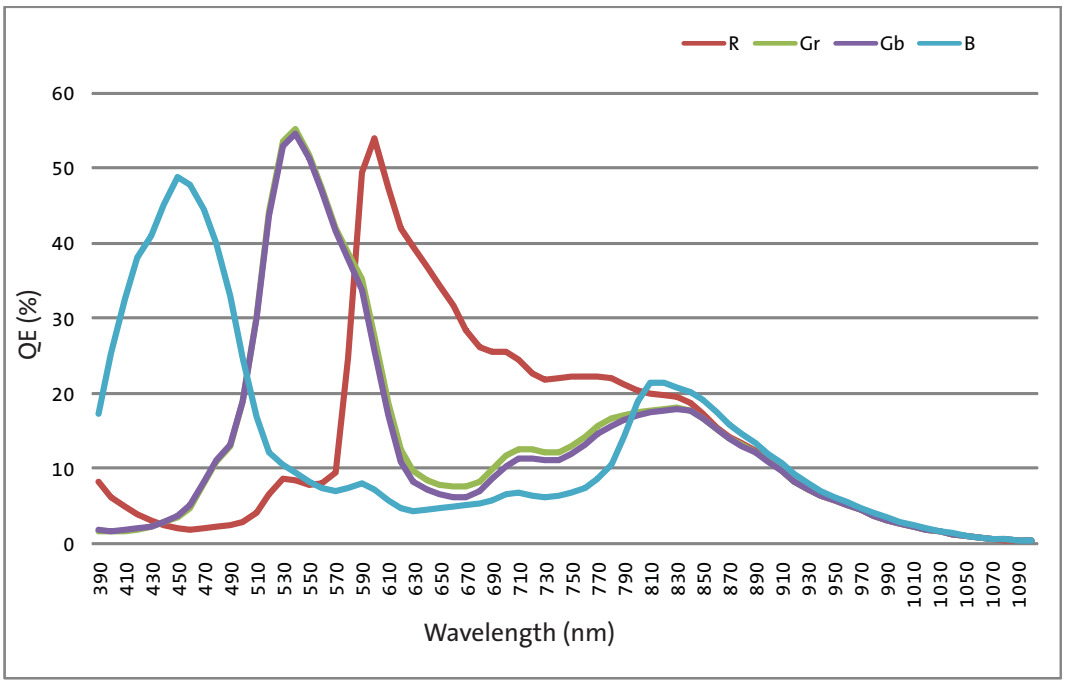


Image Height		CRA
(%)	(mm)	(deg)
0	0	0
5	0.035	1.23
10	0.070	2.46
15	0.105	3.70
20	0.140	4.94
25	0.175	6.18
30	0.210	7.43
35	0.245	8.67
40	0.280	9.90
45	0.315	11.13
50	0.350	12.36
55	0.385	13.57
60	0.420	14.77
65	0.455	15.97
70	0.490	17.14
75	0.525	18.31
80	0.560	19.45
85	0.595	20.58
90	0.630	21.69
95	0.665	22.77
100	0.700	23.83

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Figure 29: Quantum Efficiency



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Electrical Specifications

Caution **Stresses above those listed in Table 13 may cause permanent damage to the device.**

Table 13: Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
		Min	Max	
V_{DD}	Core digital voltage	–0.3	2.4	V
V_{DD_IO}	I/O digital voltage	–0.3	4.0	V
V_{AA}	Analog voltage	–0.3	4.0	V
V_{AA_PIX}	Pixel supply voltage	–0.3	4.0	V
V_{DD_PLL}	PLL supply voltage	–0.3	4.0	V
V_{PP}	OTPM power supply	7.5	9.5	V
V_{IN}	Input voltage	–0.3	V_{DD_IO} + 0.3	V
T_{OP}	Operating temperature (measure at junction)	–30	70	°C
T_{STG} [1]	Storage temperature	–40	85	°C

Note: This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Table 14: Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units
V_{DD}	Core digital voltage	1.7	1.8	1.95	V
V_{DD_IO}	I/O digital voltage	2.5	2.8	3.1	V
		1.7	1.8	1.95	V
V_{AA}	Analog voltage	2.5	2.8	3.1	V
V_{DD_PHY}	MIPI supply voltage	2.5 in MIPI mode V_{DD_IO} in parallel mode	2.8 in MIPI mode V_{DD_IO} in parallel mode	3.1 in MIPI mode V_{DD_IO} in parallel mode	V
V_{AA_PIX}	Pixel supply voltage	2.5	2.8	3.1	V
V_{DD_PLL}	PLL supply voltage	2.5	2.8	3.1	V
V_{PP}	OTPM power supply	8.5	8.5	9	V
T_J	Operating temperature (at junction)	–30	55	70	°C

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Table 15: DC Electrical Characteristics

Symbol	Parameter	Condition	Min	Max	Unit
V_{IH}	Input HIGH voltage		0.7 * V_{DD_IO}	V_{DD_IO} + 0.5	V
V_{IL}	Input LOW voltage		–0.3	0.3 * V_{DD_IO}	V
I_{IN}	Input leakage current	V_{IN} = 0V or V_{IN} = V_{DD_IO}		10	µA
V_{OH}	Output HIGH voltage	V_{DD_IO} = 1.8V, I_{OH} = 2mA	1.7	–	V
		V_{DD_IO} = 1.8V, I_{OH} = 4mA	1.6	–	V
		V_{DD_IO} = 1.8V, I_{OH} = 8mA	1.4	–	V
		V_{DD_IO} = 2.8V, I_{OH} = 2mA	2.7	–	V
		V_{DD_IO} = 2.8V, I_{OH} = 4mA	2.6	–	V
		V_{DD_IO} = 2.8V, I_{OH} = 8mA	2.5	–	V
V_{OL}	Output LOW voltage	V_{DD_IO} = 1.8V, I_{OH} = 2mA	–	0.1	V
		V_{DD_IO} = 1.8V, I_{OH} = 4mA	–	0.2	V
		V_{DD_IO} = 1.8V, I_{OH} = 8mA	–	0.4	V
		V_{DD_IO} = 2.8V, I_{OH} = 2mA	–	0.1	V
		V_{DD_IO} = 2.8V, I_{OH} = 4mA	–	0.2	V
		V_{DD_IO} = 2.8V, I_{OH} = 8mA	–	0.4	V

Table 16: Operating/Standby Current Consumption

^{f}EXTCLK = 44 MHz; ^{f}PIXCLK = 22 MHz; voltages = Typ; T_J = Typ; excludes V_{DD_IO} current

Symbol	Parameter	Condition	Typ	Max	Unit
I_{DD}	Digital operating current		9	9.5	mA
I_{AA}	Analog operating current		8	8.5	mA
I_{DD_PLL}	PLL supply current		5.5	6	mA
	Total supply current		22.5	24	mA
	Total power consumption		54	57.7	mW
I_{DD} (MIPI)	Digital operating current		11	12	mA
I_{AA} (MIPI)	Analog operating current		8	8.5	mA
I_{DD_PLL} (MIPI)	PLL supply current		5.5	6	mA
I_{DD_PHY} (MIPI)	MIPI PHY supply current		6.5	7	mA
	Total supply current (MIPI)		31	33.5	mA
	Total power consumption (MIPI)		75.8	81.8	mW
Hard standby (clock off)	Total standby current when asserting the STANDBY signal		19	22	µA [1]
	Standby power		45	53	µW[1]
Soft standby (clock on)	Total standby current	f_{EXTCLK} = 44 MHz, Soft standby mode	2.3	2.5	mA[1]
	Standby power		4.5	4.9	mW [1]
Soft standby (clock off)	Total standby current	Soft standby mode	19	22	µA [1]
	Standby power		45	53	µW[1]

Note: 1. This does not include V_{DD_IO} current.

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Table 17: AC Electrical Characteristics

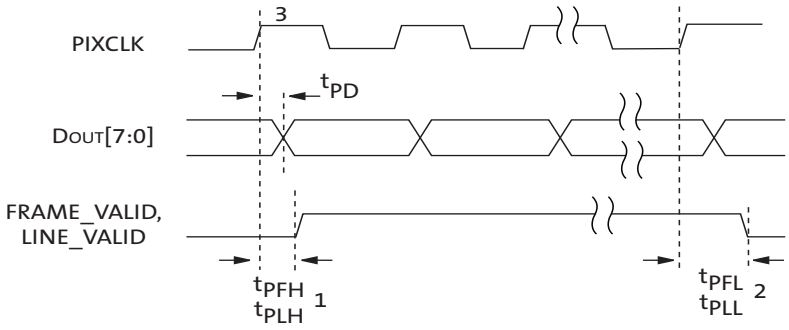
^{f}EXTCLK = 4–44 MHz; V_{DD} = 1.8V; V_{DD}_IO = 1.8V–2.8V; V_{AA} = 2.8V; VAA_PIX = 2.8V; V_{DD}_PLL = 2.8V; C_{LOAD} = 30pF

Symbol	Parameter	Conditions		Min	Typ	Max	Unit	Note
^{f}EXTCLK	External clock frequency	PLL enabled		4		44	MHz	
^{t}R	Input clock rise time			–	–	5	ns	2
^{t}F	Input clock fall time				–	5	ns	2
	Clock duty cycle			45	–	55	%	
^{t}JITTER	Input clock jitter (peak-to-peak jitter)				–	1	ns	
Output signal slew	Rise and fall time of parallel output signals (PIXCLK FV, LV, DOUT) with slew rate programmed to 7. See SYSCTL register 0x001E.	V_{DD}_IO = 2.8V Input clock = 48 MHz	C_{LOAD} = 30pf	–	3	–	ns	
			C_{LOAD} = 50pf	–	4	–	ns	
	Rise and fall time of parallel output signals (PIXCLK, FV, LV, DOUT) with slew rate programmed to 4. See SYSCTL register 0x001E. =		C_{LOAD} = 30pf	–	4	–	ns	
			C_{LOAD} = 50pf	–	5	–	ns	
	Rise and fall time of parallel output signals (PIXCLK, FV, LV, DOUT) with slew rate programmed to 0. See SYSCTL register 0x001E.	V_{DD}_IO = 2.8V Input clock = 48 MHz	C_{LOAD} = 30pf	–	9	–	ns	
			C_{LOAD} = 50pf	–	11	–	ns	
^{f}PIXCLK	PIXCLK frequency			–	–	22	MHz	1
^{t}PIXCLK_JITTER	Pixel clock jitter (output jitter, peak-to-peak)			1.3	2.1	3.7	ns	
^{t}PD	PIXCLK to data valid	Input clock = 44 MHz, C_{LOAD} = 30pF		–	–	5	ns	
^{t}PFH	PIXCLK to FV HIGH			–	–	4	ns	
^{t}PLH	PIXCLK to LV HIGH			–	–	4	ns	
^{t}PFL	PIXCLK to FV LOW			–	–	4	ns	
^{t}PLL	PIXCLK to LV LOW			–	–	4	ns	
C_{IN}	Input pin capacitance				7	–	pF	

Notes:
1. PIXCLK output signal can be inverted internally by programming register.
2. It is only necessary to meet this spec when the PLL is bypassed. If the PLL is being using then VIH/VIL should be met.

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Figure 30: Parallel Pixel Bus Timing Diagram



Notes:
1. PLL disabled.
2. FRAME_VALID leads LINE_VALID by 6 PIXCLKs.
3. FRAME_VALID trails LINE_VALID by 6 PIXCLKs.
4. DOUT[7:0], FRAME_VALID, and LINE_VALID are shown with respect to the rising edge of PIXCLK. This feature is programmable and DOUT[7:0], FRAME_VALID, and LINE_VALID can be synchronized to the falling edge of PIXCLK.
5. Propagation delay is measured from 50% of rising and falling edges

Table 18: MIPI Timing Measurements: Clock

Parameter	MIPI Spec 1.0	Min	Typical (Median)	Max	Units	Register	Set to
TCLK-POST	>(60ns+52UI) 355.45	603	603	605	ns	0x3C52[8-13]	9 (13)
TEOT	<(102+12UI) 10.18	89	90	90	ns	N/A	N/A
TCLK-TRAIL	>60	78	78	78	ns	0x3C54[8-11]	2
THS-EXIT	>100	5187	5189	5189	ns	0x3C50[8-13]	3
TLPX	>50	90	91	92	ns	0x3C56[0-5]	2
TCLK-PREPARE	38 – 95	61	63	65	ns	0x3C5A[2-3]	2
TCLK-ZERO	No Spec	442	445	446	ns	0x3C54[0-5]	7
TCLK-PREPARE & TCLK-ZERO	>300	508	508	509	ns	N/A	N/A
TCLK-PRE	>(8UI) 45.45	81	83	83	ns	0x3C52[0-5]	2

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Figure 31: MIPI Clock Timing

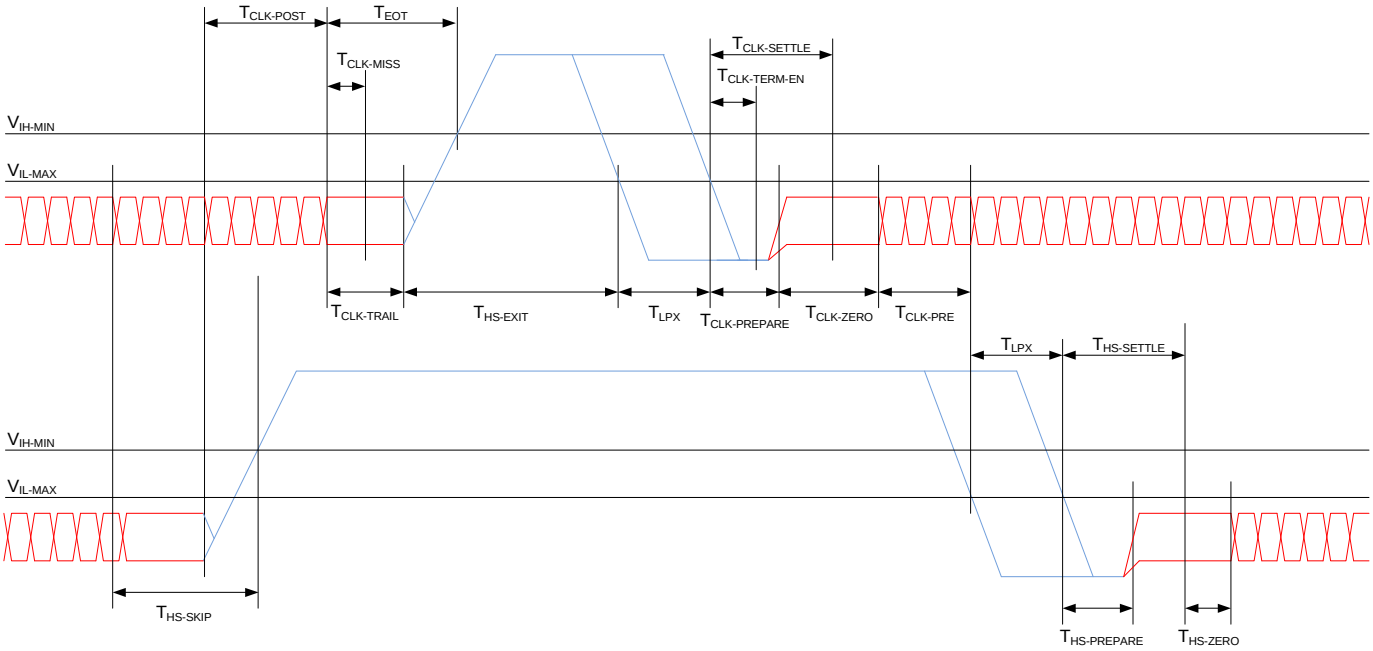


Table 19: MIPI Timing Measurements: Data

Parameter	MIPI Spec 1.0	Min	Typical (Median)	Max	Units	Register	Set To
TLPX	>50	92	93	93	ns	0x3C56[0-5]	2
THS-PREPARE	(40+4UI)to (85+6UI) 62.73 –119.09	64	67	69	ns	0x3C5A[0-1]	2
THS-ZERO	No Spec	630	630	635	ns	0x3C4E[8-11]	5
THS-PREPARE & THS-ZERO	>(145+10UI) >201.82	697	700	703	ns	N/A	N/A
THS-TRAIL	>(60+4UI) & >(8UI) 82.73 -45.45	165	165	167	ns	0x3C50[0-3]	3

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Table 20: MIPI High Speed (HS)

Parameter	MIPI Spec 1.0	Min	Typical (Median)	Max	Units
|VOD| HS transmit differential voltage	140 - 270	203	209	219	mV
VCMTX HS transmit static common mode voltage	150 - 250	196	201	213	mV
|ΔVOD| HS VOD mismatch	•10	2	5	7	mV
|ΔVCMTX(1,0)| VCMTX mismatch	•5	0	1	1	mV
V_{OHHS} HS Output HIGH Voltage	<360	300	308	322	mV
ZOS Single ended output impedance	40 – 62.5	43	45	46	Ω
ΔZOS Single ended output impedance mismatch	•10%	0.66	1.75	3.6	%
tR 20%-80% rise time	150ps to 0.3UI (1.7ns)	322	364	408	ps
tF 20%-80% fall time	150ps to 0.3UI (1.7ns)	351	397	438	ps
Eye width			5.581		ns
UI Error	±0.2		0.0177		UI
Data to Clock Skew	±0.15	0.006	0.004	0.001	UI
|VOD| HS transmit differential voltage	140 - 270	203	209	219	mV

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Table 21: MIPI Low Power (LP)

Parameter	MIPI Spec 1.0	Min	Typical (Median)	Max	Units
VOL output low level	±50	4.12	6.70	13.9	mV
VOH output high level	1.1 –1.3	1.18	1.21	1.24	V
ZOLP Output impedance of LP	≥ 110	140	147	156	Ω
tRLP 15%-85% Rise Time	≤ 25	142.8	15.27	15.86	ns
tFLP 15%-85% Fall Time	≤ 25	13.79	14.35	16.15	ns
tRLP 15%-85% Rise Time (Heavy load)	≤ 25	12.18	13.19	13.62	ns
tFLP 15%-85% Fall Time (Heavy load)	≤ 25	11.95	12.61	13.45	ns
Slew rate, (CLOAD = 0pF)	≤ 500	N/A	N/A	N/A	mV/ns
Slew rate, (CLOAD = 5pF)	≤ 300	N/A	N/A	N/A	mV/ns
Slew rate, (CLOAD = 20pF)	≤ 250	62.1	91.81	151	mV/ns
Slew rate, (CLOAD = 70pF)	≤ 150	69.39	76.06	85.32	mV/ns
Slew rate, (CLOAD = 20pF) (Heavy Load)	≤ 250	94.9	117.2	179	mV/ns
Slew rate, (CLOAD = 70pF) (Heavy Load)	≤ 150	55	91.85	102.65	mV/ns

Figure 32: MIPI Data Timing

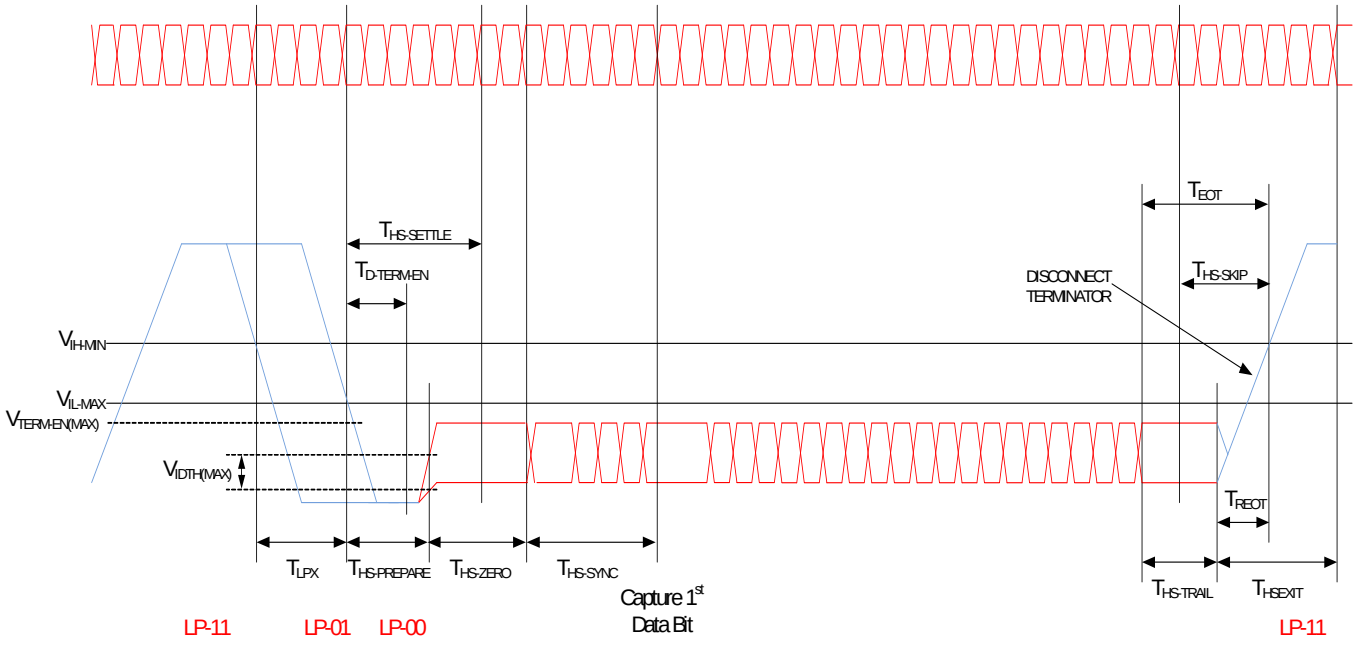


Table 22: Two-Wire Serial Interface Timing Data

^{f}EXTCLK = 14 MHz; V_{DD} = 1.8V; V_{DD_IO} = 1.8V; V_{AA} = 2.8V; V_{AA_PIX} = 2.8V; V_{DD_PLL} = 2.8V; T_J = 70°C; C_{LOAD} = 68.5pF

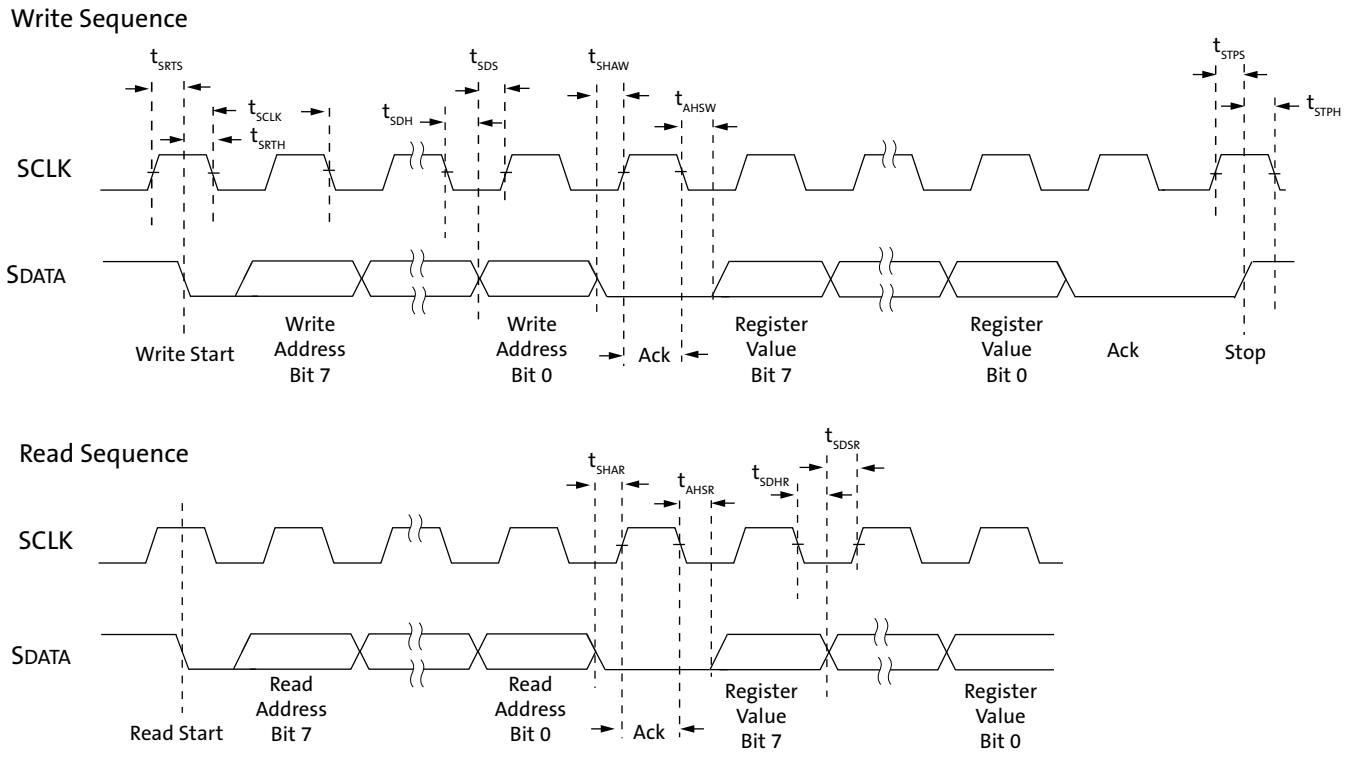
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
^{f}SCLK	Serial interface input clock frequency		100		400	kHz
^{t}SCLK	Serial interface input clock period		2.5		10	µs
	SCLK duty cycle			50	55	%
^{t}LOW	SCLK LOW period		1			µs

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
^{t}HIGH	SCLK HIGH PERIOD		1			µs
^{t}r	SCLK/SDATA rise time				300	ns
^{t}SRTS	Start setup time	Master write to slave	600			ns
^{t}SRTH	Start hold time	Master write to slave	300			ns
^{t}SDH	SDATA hold	Master write to slave	300			ns
^{t}SDS	SDATA setup	Master write to slave	300			ns
^{t}SHAW	SDATA hold to ack	Master read from slave	300			ns
^{t}AHSW	Ack hold to SDATA	Master read from slave	300			ns
^{t}STPS	Stop setup time	Master write to slave	300			ns
^{t}STPH	Stop hold time	Master write to slave	600			ns
^{t}SHAR	SDATA hold to ack	Master write to slave	150			ns
^{t}AHSR	Ack hold to SDATA	Master write to slave	150			ns
^{t}SDHR	SDATA hold	Master read from slave	300		650	ns
^{t}SDSR	SDATA setup	Master read from slave	300			ns

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Figure 33: Two-Wire Serial Bus Timing Parameters



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Power Sequence

Power-Up Sequence

Powering up the sensor requires the supply rails to be applied in a particular order to ensure sensor start up in a normal operation and prevent undesired condition such as latch up from happening. Refer to Figure 34 andTable 23 for detailed timing requirement.

Figure 34: Power-Up Sequence

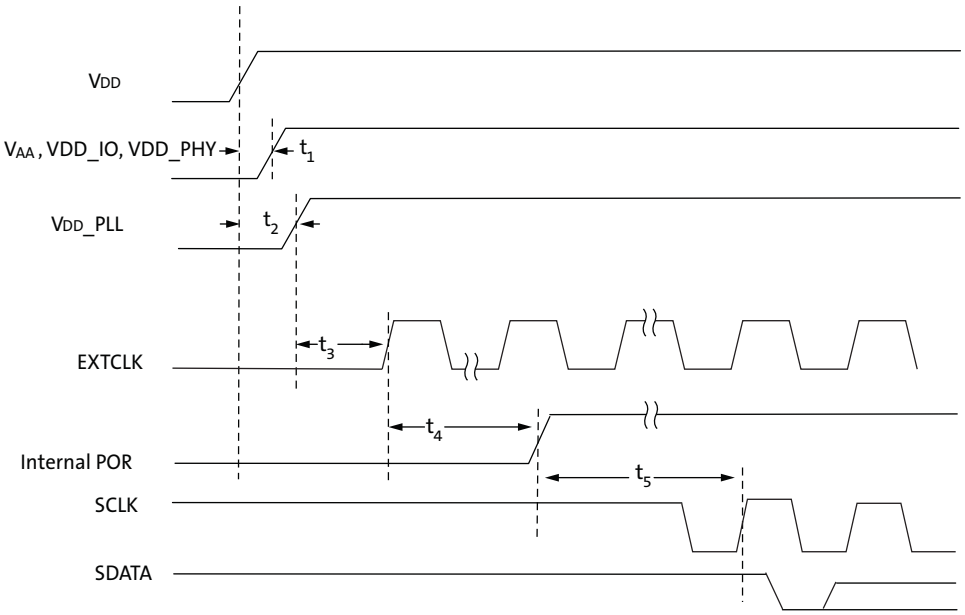


Table 23: Power- Up Signal Timing

Symbol	Parameter	Min	Typ	Max	Unit
t1	Delay from VDD to VAA and VDD_IO and VDD_PHY	0	–	500	ms
t2	Delay from VDD to VDD_PLL	0	–	500	ms
t3	EXTCLK activation	0	500	–	ms
t4	Internal POR Duration	70	-	-	EXTCLKs
t5	First Serial Write	50	-	-	EXTCLKs

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Power-Down Sequence

Figure 35: Power-Down Sequence

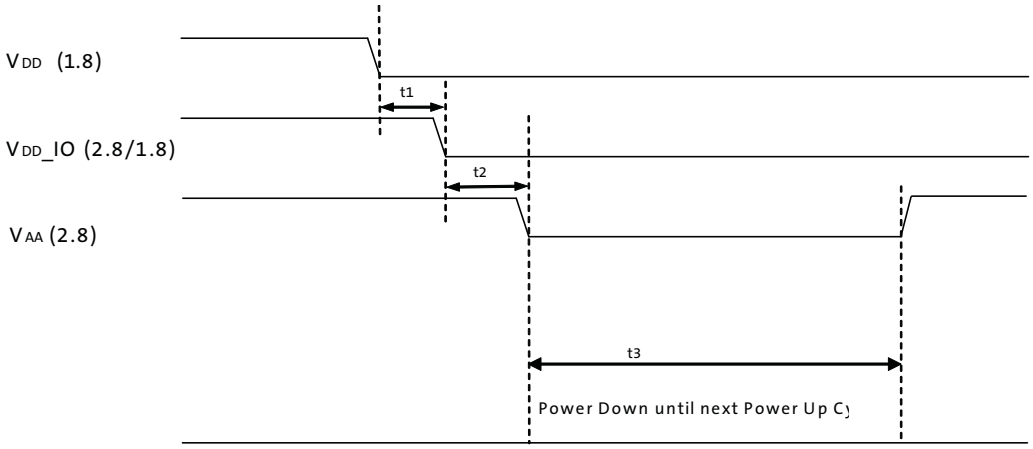


Table 24: Power-Down Supply Rail Timing

Definition	Symbol	Minimum	Typical	Maximum	Unit
VDD to VDD_IO and VDD_PHY	t1	0	-	500	ms
VDD_IO and VDD_PHY to VAA	t2	0	-	500	ms
PwrDn until Next PwrUp Time[1]	t3	100	-	-	ms

Note: 1. t3 is required between power down and next power up time, all decoupling caps from regulators must completely discharged before next power up.

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Revision History

Rev. E 5/5/15

- Updated to ON Semiconductor template
- Removed Confidential marking
- Updated “Ordering Information” on page 2

Rev. D 9/29/11

- Updated Table 16, “Operating/Standby Current Consumption,” on page 41

Rev. C 6/16/11

- Updated Table 1 on page 1
- Updated Figure 1 on page 6
- Updated Figure 2 on page 8
- Updated Table 3 on page 10
- Updated Table 4 on page 10
- Updated “Power-On Reset” on page 11
- Updated “Exiting Standby Mode” on page 12
- Updated “De-assert STANDBY signal (LOW).” on page 12
- Updated “Entering Standby Mode” on page 13
- Updated Figure 4 on page 13
- Updated“Parallel Image Data Output Interface” on page 14
- Updated Figure 5 on page 14
- Updated “Serial Port” on page 15
- Replaced Figure 14 on page 21 with new figure
- Updated Figure 15 on page 23
- Updated “Gamma Correction” on page 25
- Updated Figure 17, Figure 18, and Figure 19
- Updated “Flicker Detection and Avoidance” on page 28
- Updated Table 12 on page 32
- Added Figure 29: “Quantum Efficiency,” on page 39
- Updated Table 16, “Operating/Standby Current Consumption,” on page 41
- Add Table 18, Table 19, Table 20 and Table 21
- Add Figure 31 on page 44 and Figure 32 on page 46
- Updated Table 23 on page 49 and Table 24 on page 50

Rev. B 1/13/10

- Added “Hard Standby Mode” on page 11 and“Soft Standby Mode” on page 12
- Added “Power Sequence” on page 48
- Updated Table 1, “Key Parameters,” on page 1
- Added note to“Features” on page 1
- Updated “Power-On Reset” on page 11
- Added odd before “BT656” on page 31
- Updated Table 17, “AC Electrical Characteristics,” on page 42

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Rev. A, Advance 9/16/10

- Initial release.

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