



LR18943A

Preliminary

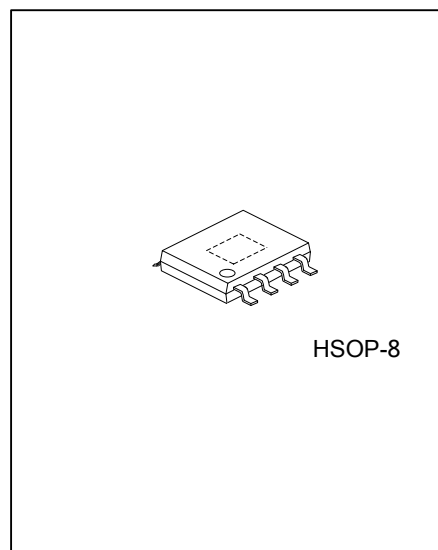
LINEAR INTEGRATED CIRCUIT

1.0A LOW DROPOUT LINEAR REGULATOR WITH OUTPUT VOLTAGE SETTING OPTIONS

■ DESCRIPTION

The UTC **LR18943A** is a typical LDO that features output voltage setting options, very low dropout voltage as low as 0.3V at output current 1.0A, an enable input and the soft-start reduces inrush current of the load capacitors and minimizes stress on the input power source during start-up. An enable pin to further reduce power dissipation while shutdown..

The UTC **LR18943A** is stable with any type of output capacitor of 10 μ F or more. A precision reference and feedback control deliver 2% accuracy.



HSOP-8

■ FEATURES

- * Low V_{IN} and wide V_{IN} range: 1.0V~5.5V
- * Bias voltage (V_{PP}) range: 3.0V~5.5V
- * Low V_{OUT} range: 0.8V~3.3V
- * 300mV dropout @1.0A, V_{PP} =5V
- * 2% output Voltage
- * output voltage setting options
- * Programmable soft-start provides linear voltage startup
- * Stable with any output capacitor $\geq$ 10 μ F

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
LR18943AL-SH2-R	LR18943AG-SH2-R	HSOP-8	Tape Reel

LR18943AG-SH2-R	(1)Packing Type (2)Package Type (3)Green Package	(1) R: Tape Reel (2) SH2: HSOP-8 (3) G: Halogen Free and Lead Free, L: Lead Free
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Pin configuration diagram for the LM317 voltage regulator. The diagram shows a 3-pin package with pins 1, 2, and 3 on the left and pins 8, 7, 6, and 5 on the right. Pin 1 is labeled V_{IN} , Pin 2 is labeled V_{PP} , Pin 3 is labeled SET1, Pin 8 is labeled V_{OUT} , Pin 7 is labeled ADJ, Pin 6 is labeled SSC, and Pin 5 is labeled EN. A dashed rectangle labeled GND connects pins 1, 2, 3, 5, 6, 7, and 8.

PIN NO.	PIN NAME	DESCRIPTION
1	V _{IN}	Input voltage. Large bulk capacitance should be placed closely to this pin, A 10uF ceramic capacitor is recommended at this pin
2	V _{PP}	Input voltage for controlling circuit
3	SET1	Output voltage setting pin. Pull-high: 1, Pull-Low; 0
4	SET2	Output voltage setting pin. Pull-high: 1, Pull-Low; 0
5	EN	Enable input. Pulling this pin below 0.4V turns the regulator off, reducing the quiescent current to a fraction of its operating value. The device will be disabled if this pin is left open
6	SSC	Inrush current limit pin
7	ADJ	Resistor ratio of external feedback for output voltage by $V_O = 0.8 \cdot (R_1 + R_2) / R_2$ Volts
8	V _{OUT}	The power output of the device. A pull low resistance exists when device deactivated by EN pin

The simplified block diagram shows the power MOSFET driver circuit. It includes a MOSFET with its gate connected to a Gate Driver block. The Gate Driver is connected to the MOSFET gate and has feedback inputs from the Current Limit and Thermal Shutdown blocks. The MOSFET source is connected to GND, and its drain is connected to the output node V_{OUT}. The input V_{IN} is connected to the MOSFET drain. The Gate Driver is also connected to V_{PP} and has a feedback input from the SSC block. The Gate Driver output is also connected to the non-inverting input (+) of a comparator. The comparator has a reference voltage of 0.8V and its output is connected to the SET1 pin. The SET2 pin is also connected to the comparator output. The ADJ pin is connected to the inverting input (-) of the comparator. The SET1 pin is also connected to the inverting input (-) of the comparator. The SET2 pin is also connected to the inverting input (-) of the comparator.

■ ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATINGS	UNIT
Input Voltage (V_{PP} , V_{IN} , EN, ADJ, V_{OUT} , SSC, SET1, SET2)	V_{IN}	7	V
Power Dissipation	P_D	Internally limited	W
Junction Temperature	T_J	150	°C
Storage Temperature Range	T_{STG}	$-65 \leq T_J \leq +150$	°C
Operation Conditions			
V_{IN} Voltage	V_{IN}	1.0~5.5	V
V_{PP} Voltage	V_{PP}	3~5.5	V
($V_{PP} \geq V_{IN}$ for normal operation) Temperature Range	T_{OPR}	$-40 \leq T_A \leq +85$	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged.
Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ THERMAL CHARACTERISTICS

PARAMETER	SYMBOL	RATINGS	UNIT
Junction To Ambient	θ_{JA}	143	°C/W

■ ELECTRICAL CHARACTERISTICS

$V_{PP}=5V$, $V_{IN}=3.3V$, $V_{EN}=V_{PP}$, $I_{OUT}=10mA$, $C_{IN}=10\mu F$, $C_{OUT}=10\mu F$, $T_A=T_J=25^\circ C$

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/ of MAX limits are 100% tested at $+25^\circ C$ unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}						
Input Voltage Range	V_{IN}	$V_{IN} > V_O$	1.0		5.5	V
V_{PP}						
V_{PP} Voltage Range	V_{PP}	$V_{PP} > V_O + 1V$ and $V_{PP} > 3V$	3		5.5	V
V_{OUT}						
Output Voltage	V_O	Internally set voltage $V_{IN} = V_O + 0.5V$	0.882	0.9	0.918	V
			1.029	1.05	1.071	
			1.176	1.2	1.224	
			1.47	1.5	1.53	
			1.764	1.8	1.836	
			2.45	2.5	2.55	
			3.234	3.3	3.366	
		Externally set voltage $V_{IN} = V_O + 0.5V$ $V_{O(S)}$: V_O Voltage setting	$V_{O(S)} - 2\%$	$V_{O(S)}$	$V_{O(S)} + 2\%$	V
Line Regulation		$V_{IN} = (V_O + 0.5V) \sim 5V$, $I_{OUT} = 100mA$ $(\Delta V_{OUT} / \Delta V_{IN}) \cdot V_{OUT}$		0.05	0.2	%/V
Ripple ejection		$f = 1kHz$		70		dB
Load Regulation		$10mA \leq I_O \leq 1$		0.2	1	%
Dropout Voltage	V_D	$I_O = 1A$, $V_O = 1.8V$		300		mV
Short Circuit Current				500		mA
Current Limit	I_{LIM}		1.2			A
V_{OUT} Pull Low Resistance		$V_{EN} = 0V$		35		Ω

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{OUT}						
Soft Start Time	T _{SS}	C _{SS} : Capacitor on SSC pin V _{IN} =V _O +1V, I _{OUT} =1A, C _{SS} =3nF Time period when V _{SSC} rises from 0~0.8V		2		mS
		C _{SS} : Capacitor on SSC pin V _{IN} =V _O +1V, I _{OUT} =1A, C _{SS} =0nF Time period when V _{SSC} rises from 0~0.8V		0.2		mS
ADJ						
Reference Voltage	V _{REF}	V _{ADJ} = V _O	0.784	0.8	0.816	V
Adjust Pin Current	I _{ADJ}				100	nA
Adjust Pin Threshold			0.03	0.1	0.25	V
EN						
EN Pin Voltage High	V _{ENH}		1.6			V
EN Pin Voltage Low	V _{ENL}				0.4	V
EN Pin Down Resistor	R _{EN}			2.5		MΩ
SET1, SET2						
SET1, SET2 Pin Voltage High	V _{SET1H} , V _{SET2H}		V _{PP} -0.5			V
SET1, SET2 Pin Voltage Low	V _{SET1L} , V _{SET2L}				0.5	V
Over Temperature Protection						
Over Temperature	T _{OT}			150		°C
Over Temperature Hysteresis	T _{OTHY}			30		°C

■ OUTPUT VOLTAGE SETTING OPTION

Internal V_O setting table:

SET1	SET2	V _{OUT}
0	0	0.9
0	F	1.05
0	1	1.2
F	0	1.5
F	F	ADJ mode
F	1	1.5
1	0	1.8
1	F	2.5
1	1	3.3

* 0: pin voltage low, 1: pin voltage high, F: pin floating

External V_O setting:

$$V_O = \{(R1+R2)/R2\} \cdot V_{ADJ}$$

* If ADJ pin is connected to gnd, V_O follows internal V_O setting

* ADJ pin has the priority than set1 pin and set2 pin

