FM25640C

64Kb Serial 5V F-RAM Memory

Features

64K bit Ferroelectric Nonvolatile RAM

- Organized as 8,192 x 8 bits
- High Endurance 1 Trillion (10^{12}) Read/Writes
- 36 Year Data Retention at +75°C
- NoDelay™ Writes
- Advanced high-reliability ferroelectric process

Very Fast Serial Peripheral Interface - SPI

- Up to 20 MHz maximum bus frequency
- Direct hardware replacement for EEPROM
- SPI Mode 0 & 3 (CPOL, CPHA=0,0 & 1,1)

Sophisticated Write Protection Scheme

- Hardware Protection
- Software Protection

Low Power Consumption

- 250 µA Active Current (1 MHz)
- 4 µA (typ.) Standby Current

Industry Standard Configuration

- Industrial Temperature -40°C to +85°C
- 8-pin "Green"/RoHS SOIC (-G)

Description

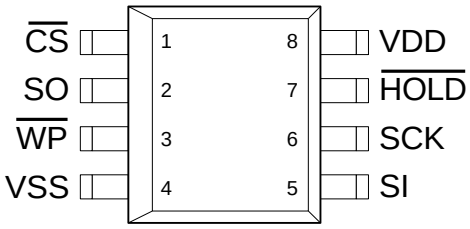
The FM25640C is a 64-kilobit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile but operates in other respects as a RAM. It provides reliable data retention for 36 years while eliminating the complexities, overhead, and system level reliability problems caused by EEPROM and other nonvolatile memories.

The FM25640C performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after it has been successfully transferred to the device. The next bus cycle may commence immediately without the need for data polling. The FM25640C is capable of supporting up to 10^{12} read/write cycles, or a million times more write cycles than EEPROM.

These capabilities make the FM25640C ideal for nonvolatile memory applications requiring frequent or rapid writes. Examples range from data collection, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss.

The FM25640C provides substantial benefits to users of serial EEPROM, in a hardware drop-in replacement. The FM25640C uses the high-speed SPI bus, which enhances the high-speed write capability of F-RAM technology. The specifications are guaranteed over an industrial temperature range of -40°C to +85°C.

Pin Configuration



Pin Names	Function
/CS	Chip Select
/HOLD	Hold
/WP	Write Protect
SCK	Serial Clock
SI	Serial Data Input
SO	Serial Data Output
VDD	5V
VSS	Ground

Ordering Information	
FM25640C-G	"Green"/RoHS 8-pin SOIC
FM25640C-GTR	"Green"/RoHS 8-pin SOIC, Tape & Reel

Ramtron International Corporation
1850 Ramtron Drive, Colorado Springs, CO 80921
(800) 545-F-RAM, (719) 481-7000
www.ramtron.com

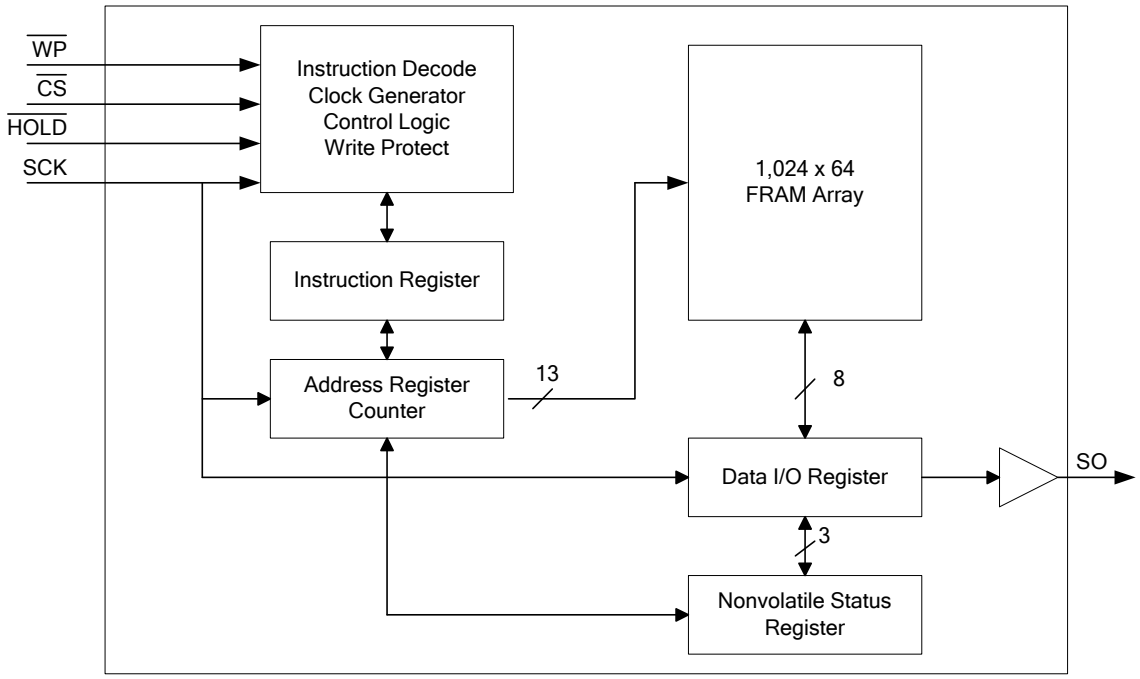


Figure 1. Block Diagram

Pin Description

Pin Name	I/O	Pin Description
/CS	Input	Chip Select: Enables and disables the device. When /CS is high, the output pin SO is hi-Z, all other inputs are ignored, and the device remains in a low-power standby mode. When /CS is low, the part will respond to the SCK signal. A falling edge on /CS must occur for every op-code.
SCK	Input	Serial Clock: All I/O activity is synchronized to the serial clock. Inputs are latched on the rising edge and outputs occur on the falling edge. The device is static so the clock frequency may be any value between 0 and 20 MHz and may be interrupted at any time.
/HOLD	Input	Hold: The /HOLD signal is used when the host CPU must interrupt a memory operation for another task. Asserting the /HOLD signal low pauses the current operation. The device ignores SCK and /CS. All transitions on /HOLD must occur while SCK is low.
/WP	Input	Write Protect: This pin prevents write operations to the status register. This is critical since other write protection features are controlled through the status register. A complete explanation of write protection is provided below. *Note that the function of /WP is different from the FM25040 where it prevents all writes to the part.
SI	Input	Serial Input: SI is the data input pin. It is sampled on the rising edge of SCK and is ignored otherwise. It should always be driven to a valid logic level to meet IDD specifications. * SI may be connected to SO for a single pin data interface.
SO	Output	Serial Output: SO is the data output pin. It is driven during read cycles and remains hi-Z at all other times including when HOLD\ is low. Data transitions are driven on the falling edge of the serial clock. * SO can be connected to SI for a single pin data interface since the part communicates in half-duplex.
VDD	Supply	Supply Voltage: 5V
VSS	Supply	Ground

Overview

The FM25640C is a serial F-RAM memory. The memory array is logically organized as 8,192 x 8 and is accessed using an industry standard Serial Peripheral Interface or SPI bus. Functional operation of the F-RAM is similar to serial EEPROMs. The major difference between the FM25640C and a serial EEPROM with the same pinout relates to its superior write performance.

Memory Architecture

When accessing the FM25640C, the user addresses 8,192 locations of 8 data bits each. These data bits are shifted in and out serially. The addresses are accessed using the SPI protocol, which includes a chip select (to permit multiple devices on the bus), an op-code and a two-byte address. The upper 3 bits of the address range are ignored by the device. The complete address of 13-bits specifies each byte address uniquely.

Most functions of the FM25640C either are controlled by the SPI interface or are handled automatically by on-board circuitry. The access time for memory operation essentially is zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the SPI bus. Unlike an EEPROM, it is not necessary to poll the device for a ready condition since writes occur at bus speed. That is, by the time a new bus transaction can be shifted into the part, a write operation will be complete. This is explained in more detail in the interface section.

Users expect several obvious system benefits from the FM25640C due to its fast write cycle and high endurance as compared with EEPROM. However there are less obvious benefits as well. For example in a high noise environment, the fast-write operation is less susceptible to corruption than an EEPROM since it is completed quickly. By contrast, an EEPROM requiring milliseconds to write is vulnerable to noise during much of the cycle.

Note that the FM25640C contains no power management circuits other than a simple internal power-on reset. It is the user's responsibility to ensure that V_{DD} is within datasheet tolerances to prevent incorrect operation. It is recommended that the part is not powered down with chip enable active.

Serial Peripheral Interface – SPI Bus

The FM25640C employs a Serial Peripheral Interface (SPI) bus. It is specified to operate at speeds up to 20 MHz. This high-speed serial bus provides high performance serial communication to a host microcontroller. Many common microcontrollers have hardware SPI ports allowing a direct interface. It is quite simple to emulate the port using ordinary port pins for microcontrollers that do not. The FM25640C operates in SPI Mode 0 and 3.

The SPI interface uses a total of four pins: clock, data-in, data-out, and chip select. It is possible to connect the two data lines together. Figure 2 illustrates a typical system configuration using the FM25640C with a microcontroller that offers an SPI port. Figure 3 shows a similar configuration for a microcontroller that has no hardware support for the SPI bus.

Protocol Overview

The SPI interface is a synchronous serial interface using clock and data lines. It is intended to support multiple devices on the bus. Each device is activated using a chip select. Once chip select is activated by the bus master, the FM25640C will begin monitoring the clock and data lines. The relationship between the falling edge of /CS, the clock, and data is dictated by the SPI mode. The device will make a determination of the SPI mode on the falling edge of each chip select. While there are four such modes, the FM25640C supports modes 0 and 3. Figure 4 shows the required signal relationships for modes 0 and 3. In both cases, data is clocked into the FM25640C on the rising edge of SCK and data is expected on the first rising edge after /CS goes active. If the clock begins from a high state, it will fall prior to beginning data transfer in order to create the first rising edge.

The FM25640C is controlled by SPI op-codes. These op-codes specify the commands to the part. After /CS is asserted, the first byte transferred from the bus master is the op-code. Following the op-code, addresses and data are then transferred. Note that the WREN and WRDI op-codes are commands with no subsequent data transfer.

Important: The /CS must go inactive after an operation is complete and before a new op-code can be issued. There is one valid op-code only per active chip select.

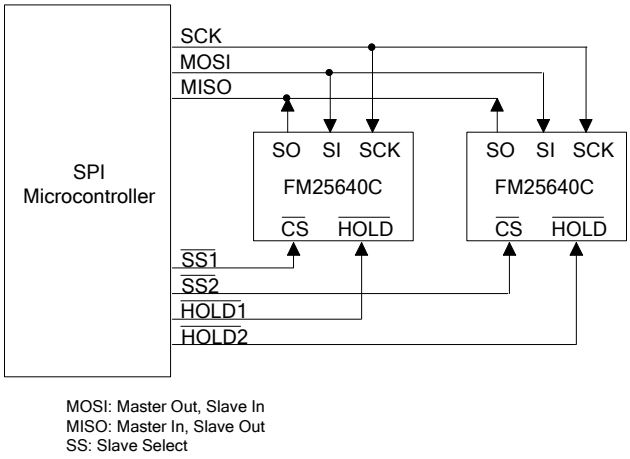


Figure 2. System Configuration with SPI port

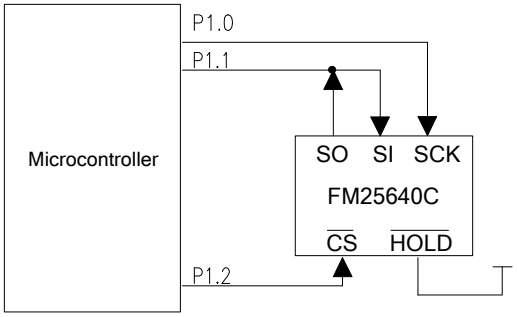
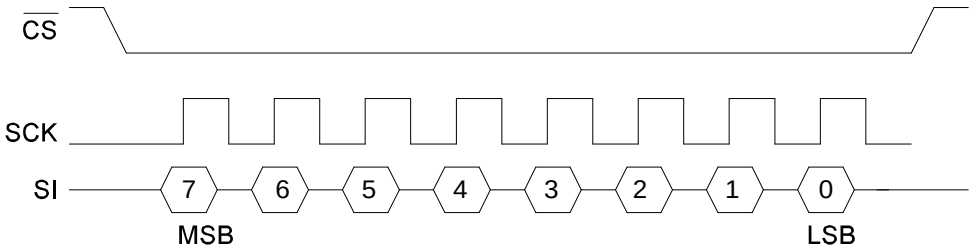


Figure 3. System Configuration without SPI port

SPI Mode 0: CPOL=0, CPHA=0



SPI Mode 3: CPOL=1, CPHA=1

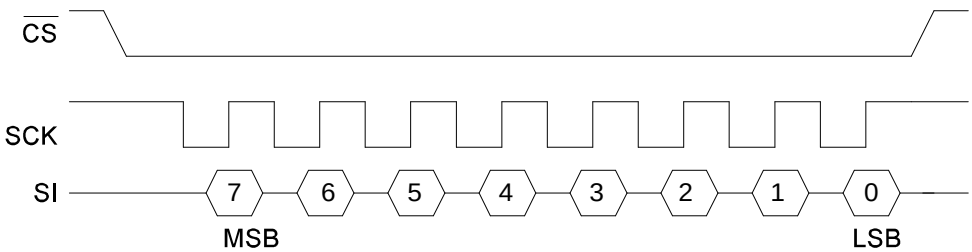


Figure 4. SPI Modes 0 & 3

Data Transfer

All data transfers to and from the FM25640C occur in 8-bit groups. They are synchronized to the clock signal (SCK) and they transfer most significant bit (MSB) first. Serial inputs are registered on the rising edge of SCK. The SO output is driven from the falling edge of SCK.

Command Structure

There are six commands called op-codes that can be issued by the bus master to the FM25640C. They are listed in the table below. These op-codes control the functions performed by the memory. They can be divided into three categories. First, there are commands that have no subsequent operations. They perform a single function such as to enable a write operation. Second are commands followed by one byte, either in or out. They operate on the status register. The third group includes commands for memory transactions followed by an address and one or more bytes of data.

Table 1. Op-code Commands

Name	Description	Op-code value
WREN	Set Write Enable Latch	0000_0110b
WRDI	Write Disable	0000_0100b
RDSR	Read Status Register	0000_0101b
WRSR	Write Status Register	0000_0001b
READ	Read Memory Data	0000_0011b
WRITE	Write Memory Data	0000_0010b

WREN - Set Write Enable Latch

The FM25640C will power up with writes disabled. The WREN command must be issued prior to any write operation. Sending the WREN op-code will allow the user to issue subsequent op-codes for write operations. These include writing the status register and writing the memory.

Sending the WREN op-code causes the internal Write Enable Latch to be set. A flag bit in the status register, called WEL, indicates the state of the latch. WEL=1 indicates that writes are permitted. Attempting to write the WEL bit in the status register has no effect. Completing any write operation will automatically clear the write-enable latch and prevent further writes without another WREN command. Figure 5 illustrates the WREN command bus configuration.

WRDI - Write Disable

The WRDI command disables all write activity by clearing the Write Enable Latch. The user can verify that writes are disabled by reading the WEL bit in the status register and verifying that WEL=0. Figure 6 illustrates the WRDI command bus configuration.

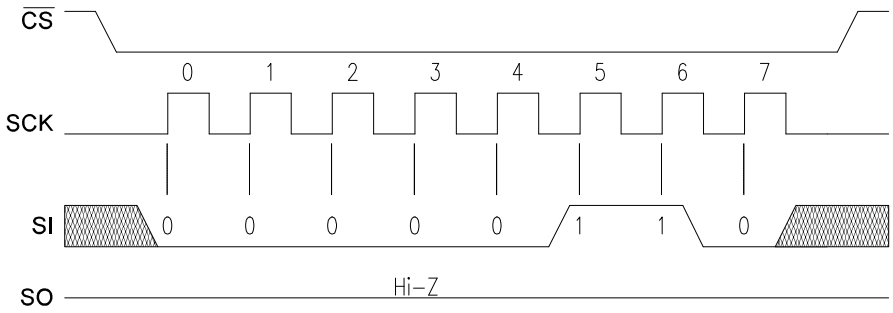


Figure 5. WREN Bus Configuration

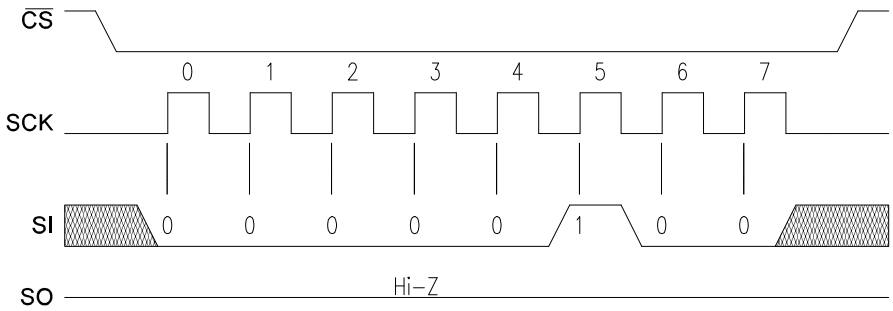


Figure 6. WRDI Bus Configuration

RDSR - Read Status Register

The RDSR command allows the bus master to verify the contents of the Status register. Reading Status provides information about the current state of the write protection features. Following the RDSR op-code, the FM25640C will return one byte with the contents of the Status register. The Status register is described in detail below.

WRSR – Write Status Register

The WRSR command allows the user to select certain write protection features by writing a byte to the Status register. Prior to issuing a WRSR command, the /WP pin must be high or inactive. Note that on the FM25640C, /WP only prevents writing to the Status register, not the memory array. Prior to sending the WRSR command, the user must send a WREN command to enable writes. Note that executing a WRSR command is a write operation and therefore clears the Write Enable Latch. The bus configuration of RDSR and WRSR in the timing diagrams below.

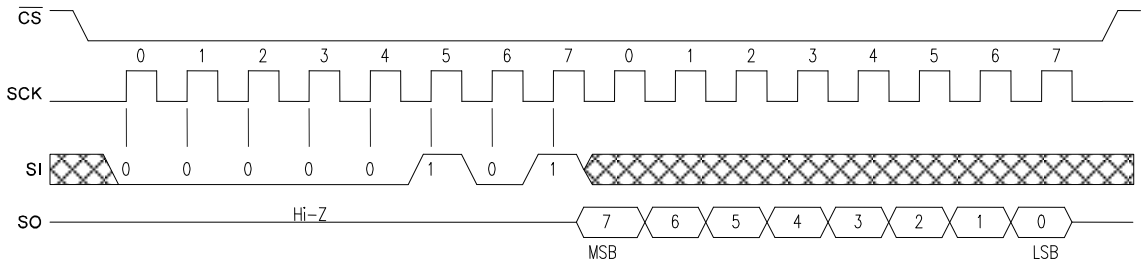


Figure 7. RDSR Bus Configuration

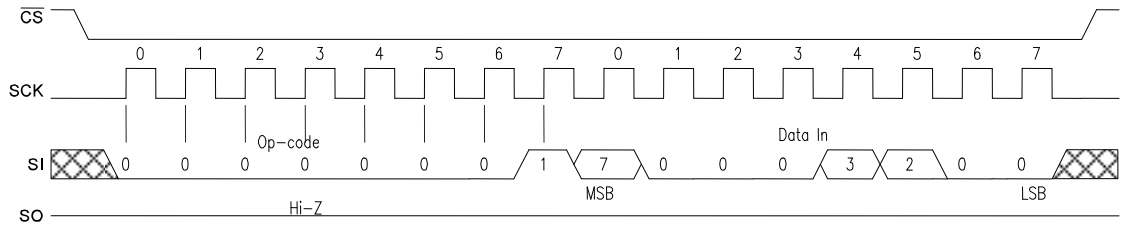


Figure 8. WRSR Bus Configuration

Status Register & Write Protection

The write protection features of the FM25640C are multi-tiered. First, a WREN op-code must be issued prior to any write operation. Assuming that writes are enabled using WREN, writes to memory are controlled by the Status register. As described above, writes to the status register are performed using the WRSR command and subject to the /WP pin. The Status Register is organized as follows.

Table 2. Status Register

Bit	7	6	5	4	3	2	1	0
Name	WPEN	0	0	0	BP1	BP0	WEL	0

Bits 0 and 4-6 are fixed at 0 and cannot be modified. Note that bit 0 (Ready in EEPROMs) is unnecessary as the F-RAM writes in real-time and is never busy. The WPEN, BP1 and BP0 control write protection features. They are nonvolatile (shaded yellow). The WEL flag indicates the state of the Write Enable Latch. This bit is internally set by the WREN command and is cleared by terminating a write cycle (/CS high) or by using the WRDI command.

BP1 and BP0 are memory block write protection bits. They specify portions of memory that are write-protected as shown in the following table.

Table 3. Block Memory Write Protection

BP1	BP0	Protected Address Range
0	0	None
0	1	1800h to 1FFFh (upper ¼)
1	0	1000h to 1FFFh (upper ½)
1	1	0000h to 1FFFh (all)

The BP1 and BP0 bits and the Write Enable Latch are the only mechanisms that protect the memory from writes. The remaining write protection features protect inadvertent changes to the block protect bits.

The WPEN bit controls the effect of the hardware /WP pin. When WPEN is low, the /WP pin is ignored. When WPEN is high, the /WP pin controls write access to the status register. Thus the Status register is write protected if WPEN=1 and /WP=0.

This scheme provides a write protection mechanism, which can prevent software from writing the memory under any circumstances. This occurs if the BP1 and BP0 are set to 1, the WPEN bit is set to 1, and /WP is set to 0. This occurs because the block protect bits prevent writing memory and the /WP signal in hardware prevents altering the block protect bits (if WPEN is high). Therefore in this condition, hardware must be involved in allowing a write operation. The following table summarizes the write protection conditions.

Table 4. Write Protection

WEL	WPEN	/WP	Protected Blocks	Unprotected Blocks	Status Register
0	X	X	Protected	Protected	Protected
1	0	X	Protected	Unprotected	Unprotected
1	1	0	Protected	Unprotected	Protected
1	1	1	Protected	Unprotected	Unprotected

Memory Operation

The SPI interface, with its relatively high maximum clock frequency, highlights the fast write capability of the F-RAM technology. Unlike SPI-bus EEPROMs, the FM25640C can perform sequential writes at bus speed. No page register is needed and any number of sequential writes may be performed.

Write Operation

All writes to the memory array begin with a WREN op-code. The next op-code is the WRITE instruction. This op-code is followed by a two-byte address value. The upper 3-bits of the address are ignored. In total, the 13-bits specify the address of the first byte of the write operation. Subsequent bytes are data and they are written sequentially. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 1FFFh is reached, the counter will roll over to 0000h. Data is written MSB first.

Unlike EEPROMs, any number of bytes can be written sequentially and each byte is written to memory immediately after it is clocked in (after the 8th clock). The rising edge of /CS terminates a WRITE op-code operation.

Read Operation

After the falling edge of /CS, the bus master can issue a READ op-code. Following this instruction is a two-byte address value. The upper 3-bits of the address are ignored. In total, the 13-bits specify the address of the first byte of the read operation. After the op-code and address are complete, the SI line is ignored. The bus master issues 8 clocks, with one bit read out for each. Addresses are incremented internally as long as the bus master continues to issue clocks. If the last address of 1FFFh is reached, the counter will roll over to 0000h. Data is read MSB first. The rising edge of /CS terminates a READ op-code operation. The bus configuration for read and write operations is shown below.

Hold

The /HOLD pin can be used to interrupt a serial operation without aborting it. If the bus master pulls the /HOLD pin low while SCK is low, the current operation will pause. Taking the /HOLD pin high while SCK is low will resume an operation. The transitions of /HOLD must occur while SCK is low, but the SCK pin can toggle during a hold state.

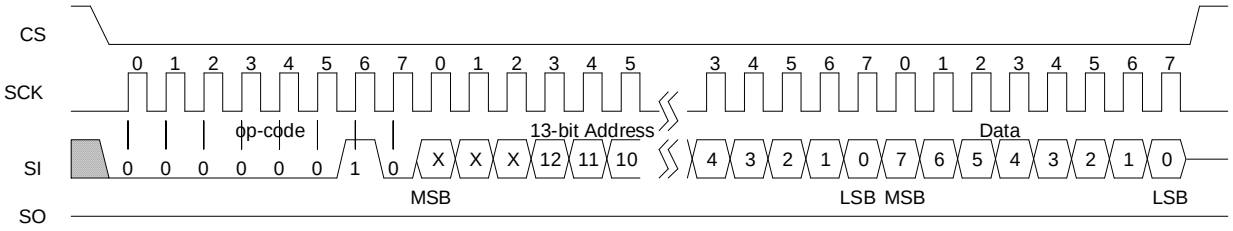


Figure 9. Memory Write

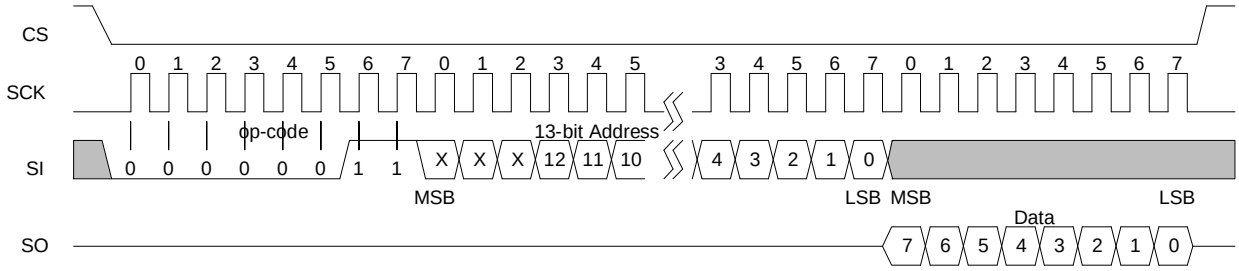


Figure 10. Memory Read

Endurance

Internally, a F-RAM operates with a read and restore mechanism. Therefore, endurance cycles are applied for each access: read or write. The F-RAM architecture is based on an array of rows and columns. Each access causes a cycle for an entire row. In the FM25640C, a row is 64 bits wide. Every 8-byte boundary marks the beginning of a new row.

Endurance can be optimized by ensuring frequently accessed data is located in different rows. Regardless, F-RAM read and write endurance is effectively unlimited at the 20MHz clock speed. Even at 2000 accesses per second to the same row, 15 years time will elapse before 10^{12} endurance cycles occur.

Electrical Specifications

Absolute Maximum Ratings

Symbol	Description	Ratings
V_{DD}	Power Supply Voltage with respect to V_{SS}	-1.0V to +7.0V
V_{IN}	Voltage on any pin with respect to V_{SS}	-1.0V to +7.0V and $V_{IN} < V_{DD}$+1.0V
T_{STG}	Storage Temperature	-55°C to + 125°C
T_{LEAD}	Lead Temperature (Soldering, 10 seconds)	260° C
V_{ESD}	Electrostatic Discharge Voltage - Human Body Model (AEC-Q100-002 Rev. E) - Charged Device Model (AEC-Q100-011 Rev. B) - Machine Model (AEC-Q100-003 Rev. E)	 4.5kV 1.25kV 300V
	Package Moisture Sensitivity Level	MSL-1

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

DC Operating Conditions (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Units	Notes
V_{DD}	Power Supply Voltage	4.5	5.0	5.5	V	
I_{DD}	V_{DD} Supply Current @ SCK = 1.0 MHz @ SCK = 20.0 MHz			 0.25 4.0	 mA mA	1
I_{SB}	Standby Current		4	10	µA	2
I_{LI}	Input Leakage Current			±1	µA	3
I_{LO}	Output Leakage Current			±1	µA	3
V_{IL}	Input Low Voltage	-0.3		0.3 V_{DD}	V	
V_{IH}	Input High Voltage	0.7 V_{DD}		V_{DD} + 0.3	V	
V_{OL}	Output Low Voltage @ I_{OL} = 2 mA			0.4	V	
V_{OH}	Output High Voltage @ I_{OH} = -2 mA	V_{DD} – 0.8			V	
V_{HYS}	Input Hysteresis	0.05 V_{DD}			V	4

Notes

1. SCK toggling between V_{DD}-0.3V and V_{SS}, other inputs V_{SS} or V_{DD}-0.3V
2. SCK = SI = /CS=V_{DD}. All inputs V_{SS} or V_{DD}.
3. V_{IN} or V_{OUT} = V_{SS} to V_{DD}.
4. This parameter is characterized but not 100% tested. Applies only to /CS and SCK pins.

AC Parameters (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

Symbol	Parameter	Min	Max	Units	Notes
f_{CK}	SCK Clock Frequency	0	20	MHz	
t_{CH}	Clock High Time	22		ns	
t_{CL}	Clock Low Time	22		ns	
t_{CSU}	Chip Select Setup	10		ns	
t_{CSH}	Chip Select Hold	10		ns	
t_{OD}	Output Disable		20	ns	2
t_{ODV}	Output Data Valid		20	ns	3
t_{OH}	Output Data Hold	0		ns	
t_D	Deselect Time	60		ns	
t_R	Data In Rise Time		50	ns	1,2
t_F	Data In Fall Time		50	ns	1,2
t_H	Data In Hold Time	5		ns	
t_{SU}	Data In Setup Time	5		ns	
t_{HS}	/HOLD Input Setup Time	10		ns	
t_{HH}	/HOLD Input Hold Time	10		ns	
t_{HZ}	/HOLD Low to Data Out Hi-Z		20	ns	2
t_{LZ}	/HOLD High to Data Out Lo-Z		20	ns	2

Notes
1. Rise and fall times measured between 10% and 90% of waveform.
2. This parameter is characterized but not 100% tested.
3. For Clock High Time $t_{CH} \leq 100$ ns, the parameter t_{ODV} is extended such that $t_{CH} + t_{ODV} \leq 160$ ns.

Capacitance (T_A = 25° C, f=1.0 MHz, V_{DD} = 5V)

Symbol	Parameter	Max	Units	Notes
C_O	Output Capacitance (SO)	8	pF	1
C_I	Input Capacitance	6	pF	1

Notes
1. This parameter is characterized and not 100% tested.

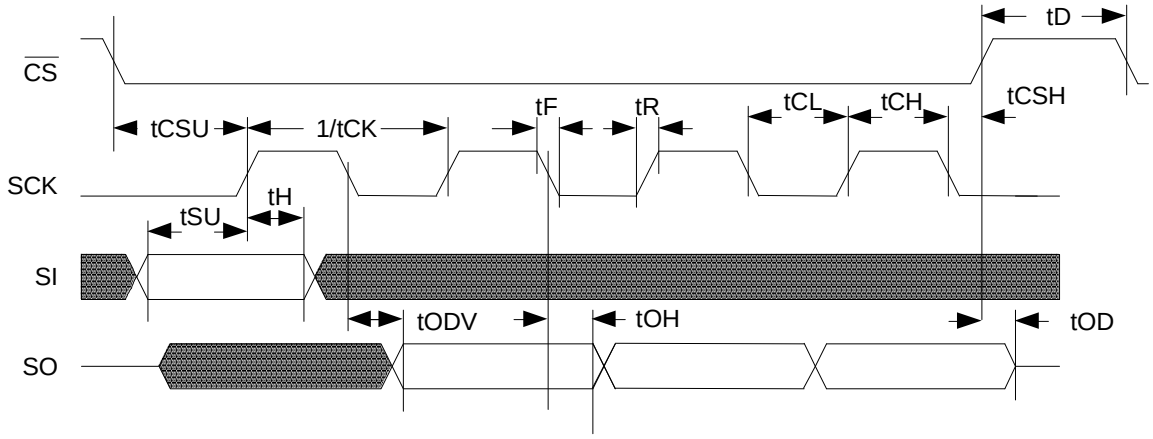
AC Test Conditions

Input Pulse Levels	10% and 90% of V_{DD}
Input rise and fall times	10 ns
Input and output timing levels	0.5 V_{DD}
Output Load Capacitance	100 pF

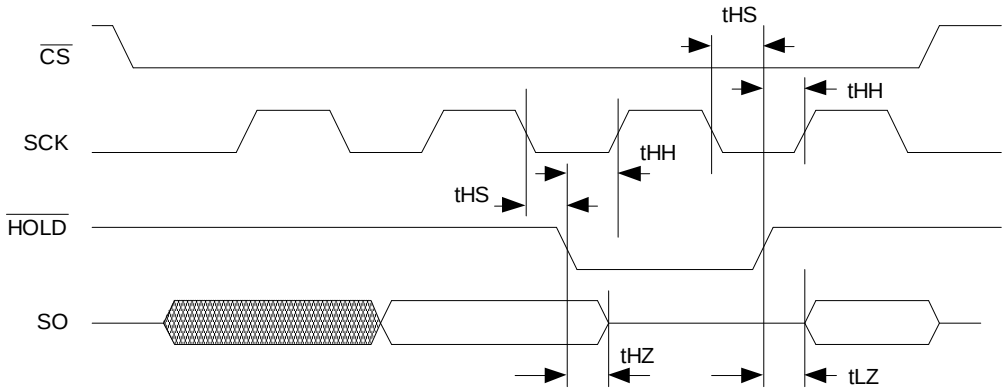
Data Retention

Symbol	Parameter	Min	Max	Units	Notes
T_{DR}	@ +85ºC	10	-	Years	
	@ +80ºC	18	-	Years	
	@ +75ºC	36	-	Years	

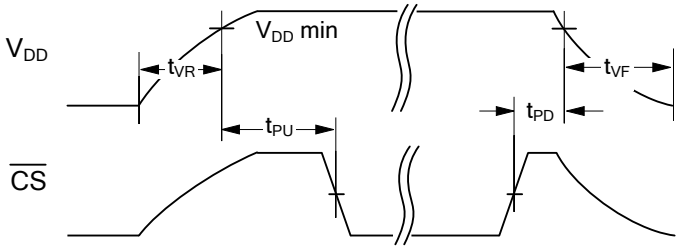
Serial Data Bus Timing



/Hold Timing



Power Cycle Timing



Power Cycle Timing (T_A = -40° C to + 85° C, V_{DD} = 4.5V to 5.5V unless otherwise specified)

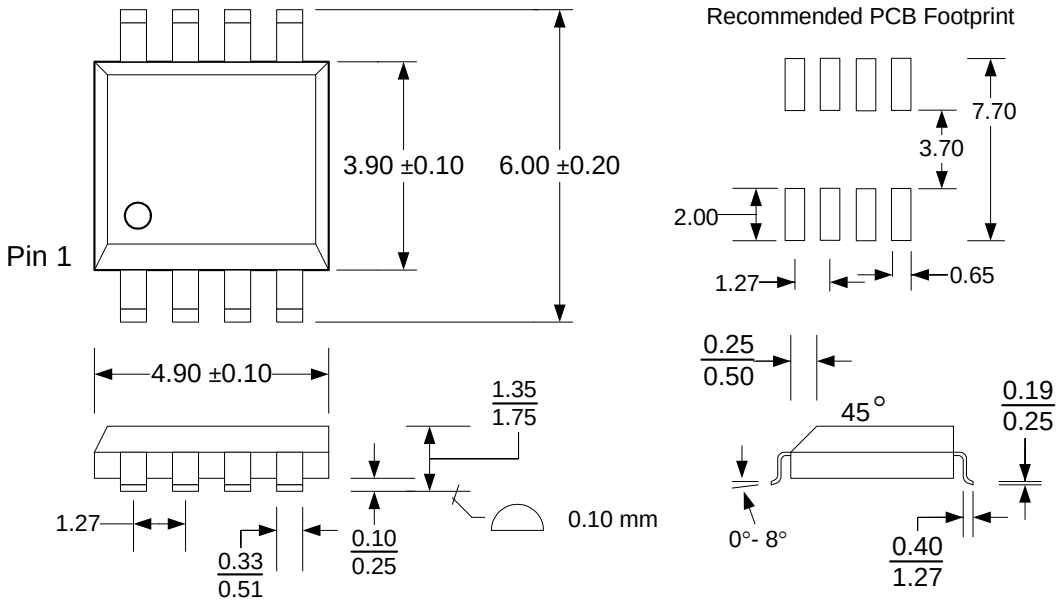
Symbol	Parameter	Min	Max	Units	Notes
t_{PU}	V_{DD}(min) to First Access Start	1	-	ms	
t_{PD}	Last Access Complete to V_{DD}(min)	0	-	µs	
t_{VR}	V_{DD} Rise Time	30	-	µs/V	1
t_{VF}	V_{DD} Fall Time	100	-	µs/V	1

Notes

1. Slope measured at any point on V_{DD} waveform.

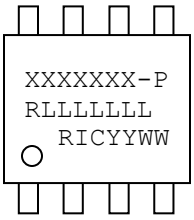
Mechanical Drawing

(8-pin SOIC – JEDEC MS-012, Variation AA)



Refer to JEDEC MS-012 for complete dimensions and notes.
All dimensions in millimeters.

SOIC Package Marking Scheme



Legend:
XXXXXXX= part number, P= package type (G=SOIC)
R=rev code, LLLLLLL= lot code
RIC=Ramtron Int'l Corp, YY=year, WW=work week

Example: FM25640C, "Green" SOIC package, Year 2010, Work Week 51

```
FM25640C-G
A00002G1
RIC1051
```

Revision History

Revision	Date	Summary
1.0	3/22/2011	Initial Release
1.1	6/30/2011	Added ESD ratings.