TOSHIBA

TOSHIBA Original CMOS 16-Bit Microcontroller

TLCS-900/L1 Series

TMP91CY28

TOSHIBA CORPORATION

Semiconductor Company

Preface

Thank you very much for making use of Toshiba microcomputer LSIs.
Before use this LSI, refer the section, “Points of Note and Restrictions”.
Especially, take care below cautions.

CMOS 16-Bit Microcontroller

TMP91CY28FG

1. Outline

The TMP91CY28 is a high-speed and high-performance 16-bit microcontroller suitable for low-voltage and low-power applications.

The TMP91CY28FG comes in a 100-pin mini flat package. Features of the TMP91CY28FG include the following:

(1) High-speed 16-bit CPU (900/L1 CPU)
- Instruction set is upwardly assembly-code compatible.
- 16-Mbyte linear address space
- Architecture based on general-purpose registers and register banks
- 16-bit multiply/divide instructions and bit transfer/arithmetic instructions
- 4-channel micro DMA (1.6 μs/2 bytes at 10 MHz)

(2) Minimum instruction execution time: 400 ns (at 10 MHz)

(3) 8-Kbyte on-chip RAM
256-Kbyte on-chip ROM

(4) External memory expansion
- 16-Mbyte off-chip address space for code and data
- External bus interface with dynamic bus sizing for 8-bit and 16-bit data ports

(5) 4-channel 8-bit timer

(6) 2-channel 16-bit timer

(7) 4-channel general-purpose serial interface
- Both UART and synchronous transfer modes are supported.

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(8) 2-channel serial bus interface

- Either I^2C mode or clocked-synchronous mode can be selected.

(9) 8-channel 10-bit AD converter (with internal sample/hold)

(10) Watchdog timer

(11) Key wakeup interrupt with 8-bit inputs

(12) WAKE output pin

(13) BCD adder/subtractor

(14) Program patch logic

- 6 banks of registers

(15) 4-channel chip select/wait controller

(16) 48 interrupt sources

- 9 CPU interrupts: Triggered by software interrupt instruction or upon the execution of an undefined instruction
- 21 internal interrupts: 7 priority levels
- 18 external interrupts: 7 priority levels (16 interrupts supporting selection of triggering edge)

(17) 80-pin input/output ports

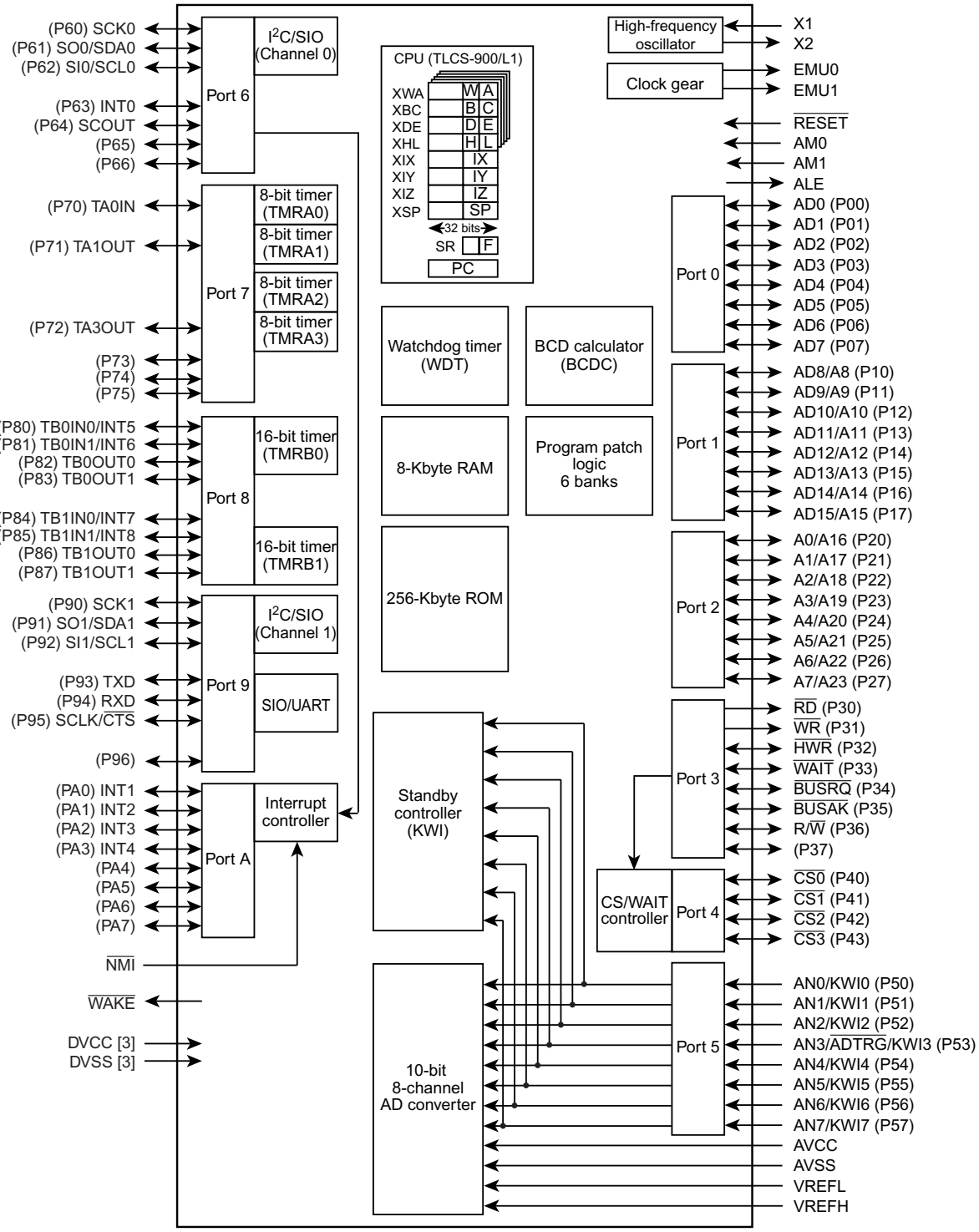
(18) Three HALT modes: Programmable IDLE2, IDLE1 and STOP

(19) Clock control

- Clock gear: Switches the frequency of high-frequency clock within the range from fc to fc/16

(20) Operating voltage range: VCC = 1.8 to 2.6 V (fc max = 10 MHz)

(21) Package: P-LQFP100-1414-0.50F



( ): Beginning state after reset

Figure 1.1 TMP91CY28 Block Diagram

2. Signal Descriptions

This section contains pin assignments for the TMP91CY28 as well as brief descriptions of the TMP91CY28 input and output signals.

2.1 Pin Assignment

The following illustrates the TMP91CY28FG pin assignment.

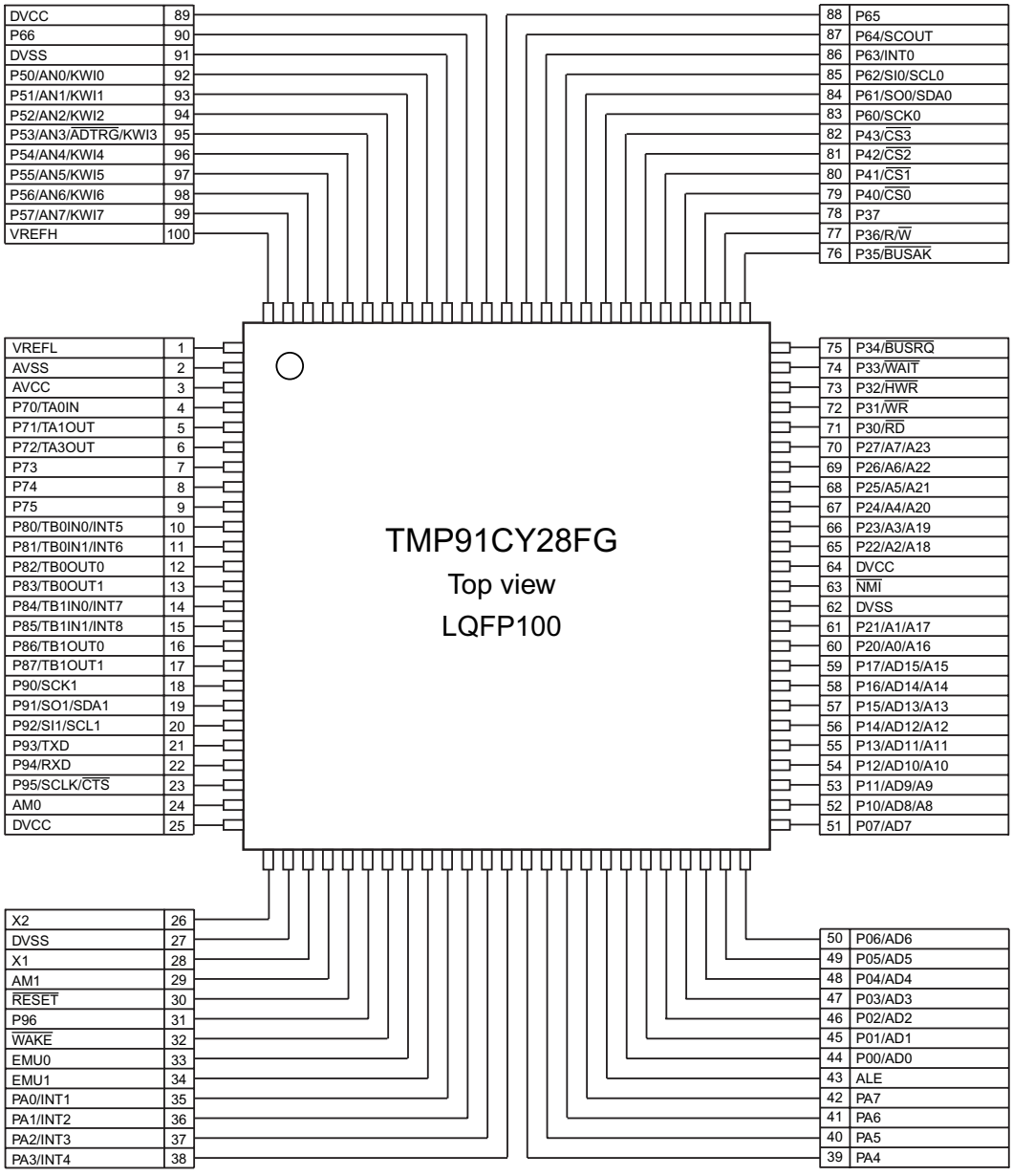


Figure 2.1.1 100-Pin LQFP Pin Assignment

2.2 Pin Usage Information

Table 2.2.1 to Table 2.2.4 list the input and output pins of the TMP91CY28, including alternate pin names and functions for multi-function pins.

Table 2.2.1 Pin Names and Functions (1/4)

Pin Name	Number of Pins	I/O	Function
P00 to P07 AD0 to AD7	8	I/O I/O	Port 0: Individually programmable as input or output Address (Lower): Bits 0 to 7 of the address/data bus
P10 to P17 AD8 to AD15 A8 to A15	8	I/O I/O Output	Port 1: Individually programmable as input or output Address (Upper): Bits 8 to 15 for address and data bus Address: Bits 8 to 15 of the address bus
P20 to P27 A0 to A7 A16 to A23	8	I/O Output Output	Port 2: Individually programmable as input or output Address: Bits 0 to 7 of the address bus Address: Bits 16 to 23 of address bus
P30 $\overline{RD}$	1	Output Output	Port 30: Output only Read strobe: Asserted during a read operation from an external memory device. Also asserted during a read from internal memory if P3<P30> = 0 and P3FC<P30F> = 1.
P31 $\overline{WR}$	1	Output Output	Port 31: Output only Write strobe: Asserted during a write operation on D0 to D7
P32 $\overline{HWR}$	1	I/O Output	Port 32: Programmable as input or output (with internal pull-up resistor) Higher write strobe: Asserted during a write operation on D8 to D15
P33 $\overline{WAIT}$	1	I/O Input	Port 33: Programmable as input or output (with internal pull-up resistor) Wait: Causes the CPU to suspend external bus activity ((1 + N) WAIT mode)
P34 $\overline{BUSRQ}$	1	I/O Input	Port 34: Programmable as input or output (with internal pull-up resistor) Bus request: Asserted by an external bus master to request bus mastership.
P35 $\overline{BUSAK}$	1	I/O Output	Port 35: Programmable as input or output (with internal pull-up resistor) Bus acknowledge: Indicates that the CPU has relinquished the bus in response to $\overline{BUSRQ}$ (for external DMAC).
P36 R/$\overline{W}$	1	I/O Output	Port 36: Programmable as input or output (with internal pull-up resistor) Read/Write: Indicates the direction of data transfer on the bus: 1 = Read or dummy cycle, 0 = Write cycle
P37	1	I/O	Port 37: Programmable as input or output (with internal pull-up resistor)
P40 $\overline{CS0}$	1	I/O Output	Port 40: Programmable as input or output (with internal pull-up resistor) Chip select 0: Asserted low to enable external devices at programmed addresses.

Note: An external DMA controller configured with the $\overline{BUSRQ}$ and $\overline{BUSAK}$ pins cannot access the on-chip memory and peripheral function of the TMP91CY28.

Table 2.2.2 Pin Names and Functions (2/4)

Pin Name	Number of Pins	I/O	Function
P41 $\overline{CS1}$	1	I/O Output	Port 41: Programmable as input or output (with internal pull-up resistor) Chip select 1: Asserted low to enable external devices at programmed addresses.
P42 $\overline{CS2}$	1	I/O Output	Port 42: Programmable as input or output (with internal pull-up resistor) Chip select 2: Asserted low to enable external devices at programmed addresses.
P43 $\overline{CS3}$	1	I/O Output	Port 43: Programmable as input or output (with internal pull-up resistor) Chip select 3: Asserted low to enable external devices at programmed addresses.
P50 to P57 AN0 to AN7 $\overline{ADTRG}$ KWI0 to KWI7	8	Input Input Input Input	Port 5: Input-only Analog input: Input to the on-chip AD converter AD trigger: Start an AD converter (Multiplexed with P53). Key wakeup input (Multiplexed with P50 to P57)
P60 SCK0	1	I/O I/O	Port 60: Programmable as input or output Clock input/output pin when the serial bus interface 0 is in SIO mode.
P61 SO0 SDA0	1	I/O Output I/O	Port 61: Programmable as input or output (with internal pull-up resistor) Data transmit pin when the serial bus interface 0 is in SIO mode. Data transmit/receive pin when the serial bus interface 0 is in I^2C mode; programmable as an open-drain output.
P62 SI0 SCL0	1	I/O Input I/O	Port 62: Programmable as input or output (with internal pull-up resistor) Data receive pin when the serial bus interface 0 is in SIO mode. Clock input/output pin when the serial bus interface 0 is in I^2C mode; programmable as an open-drain output.
P63 INT0	1	I/O Input	Port 63: Programmable as input or output Interrupt request 0: Programmable to be high-level, low-level, rising-edge or falling-edge sensitive.
P64 SCOUT	1	I/O Output	Port 64: Programmable as input or output System clock output: Drives out f_{FPH} clock.
P65	1	I/O	Port 65: Programmable as input or output
P66	1	I/O	Port 66: Programmable as input or output
P70 TA0IN	1	I/O Input	Port 70: Programmable as input or output (with internal pull-up resistor) 8-bit timer 0 input: Input to timer 0.
P71 TA1OUT	1	I/O Output	Port 71: Programmable as input or output (with internal pull-up resistor) 8-bit timer 1 output: Output from either timer 0 or timer 1.
P72 TA3OUT	1	I/O Output	Port 72: Programmable as input or output (with internal pull-up resistor) 8-bit timer 3 output: Output from either timer 2 or timer 3.

Table 2.2.3 Pin Names and Functions (3/4)

Pin Name	Number of Pins	I/O	Function
P73	1	I/O	Port 73: Programmable as input or output (with internal pull-up resistor)
P74	1	I/O	Port 74: Programmable as input or output (with internal pull-up resistor)
P75	1	I/O	Port 75: Programmable as input or output (with internal pull-up resistor)
P80 TB0IN0 INT5	1	I/O Input Input	Port 80: Programmable as input or output (with internal pull-up resistor) 16-bit timer 0 input 0: Count/capture trigger input to 16-bit timer 0. Interrupt request 5: Programmable to be rising-edge or falling-edge sensitive.
P81 TB0IN1 INT6	1	I/O Input Input	Port 81: Programmable as input or output (with internal pull-up resistor) 16-bit timer 0 input 1: Capture trigger input to 16-bit timer 0. Interrupt request 6: Rising-edge sensitive.
P82 TB0OUT0	1	I/O Output	Port 82: Programmable as input or output (with internal pull-up resistor) 16-bit timer 0 output 0: Output from 16-bit timer 0.
P83 TB0OUT1	1	I/O Output	Port 83: Programmable as input or output (with internal pull-up resistor) 16-bit timer 0 output 1: Output from 16-bit timer 0.
P84 TB1IN0 INT7	1	I/O Input Input	Port 84: Programmable as input or output (with internal pull-up resistor) 16-bit timer 1 input 0: Count/capture trigger input to 16-bit timer 1. Interrupt request 7: Programmable to be rising-edge or falling-edge sensitive.
P85 TB1IN1 INT8	1	I/O Input Input	Port 85: Programmable as input or output (with internal pull-up resistor) 16-bit timer 1 input 1: Capture trigger input to 16-bit timer 1. Interrupt request 8: Rising-edge sensitive.
P86 TB1OUT0	1	I/O Output	Port 86: Programmable as input or output (with internal pull-up resistor) 16-bit timer 1 output 0: Output from 16-bit timer 1.
P87 TB1OUT1	1	I/O Output	Port 87: Programmable as input or output (with internal pull-up resistor) 16-bit timer 1 output 1: Output from 16-bit timer 1.
P90 SCK1	1	I/O I/O	Port 90: Programmable as input or output Clock input/output pin when the serial bus interface 1 is in SIO mode.
P91 SO1 SDA1	1	I/O Output I/O	Port 91: Programmable as input or output (with internal pull-up resistor) Data transmit pin when the serial bus interface 1 is in SIO mode. Data transmit/receive pin when the serial bus interface 1 is in I^2C mode; programmable as an open-drain output.
P92 SI1 SCL1	1	I/O Input I/O	Port 92: Programmable as input or output (with internal pull-up resistor) Data receive pin when the serial bus interface 1 is in SIO mode. Clock input/output pin when the serial bus interface 1 is in I^2C mode; programmable as an open-drain output.
P93 TXD	1	I/O Output	Port 93: Programmable as input or output Serial transmit data: Programmable as an open-drain output.

Table 2.2.4 Pin Names and Functions (4/4)

Pin Name	Number of Pins	I/O	Function
P94 RXD	1	I/O Input	Port 94: Programmable as input or output Serial receive data
P95 SCLK $\overline{CTS}$	1	I/O I/O Input	Port 95: Programmable as input or output Serial clock input/output Serial clear to send
P96	1	I/O	Port 96: Programmable as input or output
PA0 to PA3 INT1 to INT4	4	I/O Input	Ports A0 to A3: Individually programmable as input or output (with internal pull-up resistor) Interrupt request 1 to 4: Individually programmable to be rising-edge or falling-edge sensitive.
PA4 to PA7	4	I/O	Ports A4 to A7: Programmable as input or output (with internal pull-up resistor)
$\overline{WAKE}$	1	Output	STOP mode monitor This pin drives low when the CPU is operating; the pin is in high-impedance state during reset or in STOP mode.
ALE	1	Output	Address latch enable (This pin can be disabled in order to reduce noise.)
$\overline{NMI}$	1	Input	Non-maskable interrupt request: Causes an NMI interrupt on the falling edge. Programmable to be rising-edge sensitive.
AM0 to AM1	2	Input	Both AM0 and AM1 should be held at logic 1.
EMU0	1	Output	Test pin. This pin should be left open.
EMU1	1	Output	Test pin. This pin should be left open.
$\overline{RESET}$	1	Input	Reset (with internal pull-up resistor): Initializes the whole TMP91CY28.
VREFH	1	Input	Input pin for high reference voltage for the AD converter.
VREFL	1	Input	Input pin for low reference voltage for the AD converter.
AVCC	1		Power supply pin for the AD converter.
AVSS	1		Ground pin for the AD converter.
X1/X2	2	I/O	Connection pins for an oscillator crystal.
DVCC DVSS	3 3		Power supply pins. The DVCC pins should be connected to power supply. Ground pins. The DVSS pins should be connected to ground.

Note: All pins that have built-in pull-up resistors (Other than the $\overline{RESET}$ pin) can be disconnected from the built-in pull-up resistor by software.

3. Functional Description

This device is a version of expanding its internal mask ROM size to 256 Kbytes. The configuration and the functionality of this device are the same as those of the TMP91CW28. For the functions of this device that are not described here, refer to the TMP91CW28 data sheet.

3.1 Memory Map

Figure 3.1.1 shows a memory map of the device in single-chip mode and its memory areas that can be accessed in each addressing mode of the CPU.

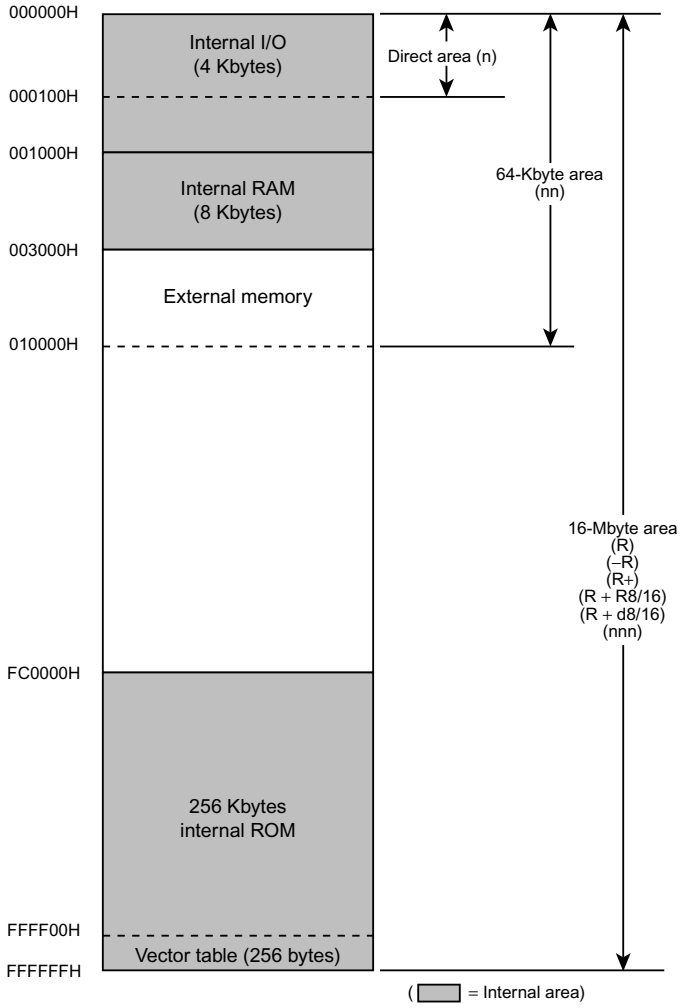


Figure 3.1.1 TMP91CY28 Memory Map (Single chip mode)

4. Electrical Characteristics

4.1 Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.5 to 3.0	V
Input voltage	VIN	−0.5 to V_{CC} + 0.5	
Output current (Per pin)	IOL	2	mA
Output current (Per pin)	IOH	−2	
Output current (Total)	ΣIOL	80	
Output current (Total)	ΣIOH	−80	
Power dissipation (Ta = 85°C)	PD	600	mW
Soldering temperature (10 s)	TSOLDER	260	°C
Storage temperature	TSTG	−55 to 125	
Operating temperature	TOPR	−20 to 70	

Note: The maximum ratings are rated values which must not be exceeded during operation, even for an instant. Any one of the ratings must not be exceeded. If any maximum rating is exceeded, a device may break down or its performance may be degraded, causing it to catch fire or explode resulting in injury to the user. Thus, when designing products which include this device, ensure that no maximum rating value will ever be exceeded.

Point of Note about Solderability of Lead Free Products (Attach “G” to package name)

Test Parameter	Test Condition	Note
Solderability	(1) Use of Sn-63Pb solder bath Solder bath temperature = 230°C, dipping time = 5 [s] Number of times = One, use of R-type flux	Pass: Solderability rate until forming ≥ 95 %
	(2) Use of Sn-3.0Ag-0.5Cu solder bath Solder bath temperature = 245, dipping time = 5 [s] Number of times = One, use of R-type flux (Use of lead free)	

4.2 DC Electrical Characteristics (1/2)

Parameter		Symbol	Conditions		Min	Typ. (Note)	Max	Unit
Supply voltage ($AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V)		V_{CC}	fc = 4 to 10 MHz		1.8		2.6	V
Low-level input voltage	P00 to P17 (AD0 to AD15)	VIL	V_{CC} = 1.8 to 2.6 V		−0.3		0.2 V_{CC}	V
	P20 to P37	VIL1	V_{CC} = 1.8 to 2.6 V				0.2 V_{CC}	
	$\overline{RESET}$, $\overline{NMI}$, P40 to PA7	VIL2	V_{CC} = 1.8 to 2.6 V				0.15 V_{CC}	
	AM0 to AM1	VIL3	V_{CC} = 1.8 to 2.6 V				0.3	
	X1	VIL4	V_{CC} = 1.8 to 2.6 V				0.1 V_{CC}	
High-level input voltage	P00 to P17 (AD0 to AD15)	VIH	V_{CC} = 1.8 to 2.6 V		0.7 V_{CC}		V_{CC} + 0.3	V
	P20 to P37	VIH1	V_{CC} = 1.8 to 2.6 V		0.8 V_{CC}			
	$\overline{RESET}$, $\overline{NMI}$, P40 to PA7	VIH2	V_{CC} = 1.8 to 2.6 V		0.85 V_{CC}			
	AM0 to AM1	VIH3	V_{CC} = 1.8 to 2.6 V		V_{CC} − 0.3			
	X1	VIH4	V_{CC} = 1.8 to 2.6 V		0.9 V_{CC}			
Low-level output voltage		VOL	IOL = 0.4 mA	V_{CC} = 1.8 to 2.6 V			0.15 V_{CC}	V
High-level output voltage		VOH	IOH = −200 μA	V_{CC} = 1.8 to 2.6 V	0.8 V_{CC}			

Note: V_{CC} = 2.0 V, Ta = 25°C, unless otherwise noted.

4.2 DC Electrical Characteristics (2/2)

Parameter	Symbol	Conditions	Min	Typ. (Note 1)	Max	Unit
Input leakage current	ILI	$0.0 \leq V_{IN} \leq V_{CC}$		0.02	±5	μA
Output leakage current	ILO	$0.2 \leq V_{IN} \leq V_{CC} - 0.2$		0.05	±10	
Power-down voltage (while RAM is being backed up in STOP mode)	VSTOP	VIL2 = 0.2 V_{CC}, VIH2 = 0.8 V_{CC}	1.8		2.6	V
$\overline{\text{RESET}}$ pull-up resistor	RRST	V_{CC} = 1.8 to 2.2 V	200		1000	kΩ
		V_{CC} = 2.2 to 2.6 V	100		600	
Pin capacitance	CIO	fc = 1 MHz			10	pF
Schmitt width $\overline{\text{RESET}}$, $\overline{\text{NMI}}$, P40 to P43, KWI0 to KWI7, P60 to PA7	VTH	V_{CC} = 1.8 to 2.6 V	0.3	0.8		V
Programmable pull-up resistor	RKH	V_{CC} = 1.8 to 2.2 V	200		1000	kΩ
		V_{CC} = 2.2 to 2.6 V	100		600	
NORMAL (Note 2)	I_{CC}	V_{CC} = 1.8 to 2.6 V fc = 10 MHz (Typ. value V_{CC} = 2.0 V)		2.2	4.0	mA
IDLE2				0.7	1.6	
IDLE1				0.3	0.9	
STOP		V_{CC} = 1.8 to 2.6 V		0.1	10	μA

Note 1: V_{CC} = 2.0 V, Ta = 25°C, unless otherwise noted.

Note 2: Test conditions for NORMAL I_{CC}: All blocks operating, output pins open, and input pin levels fixed.

4.3 AC Electrical Characteristics

(1) V_{CC} = 1.8 to 2.6 V

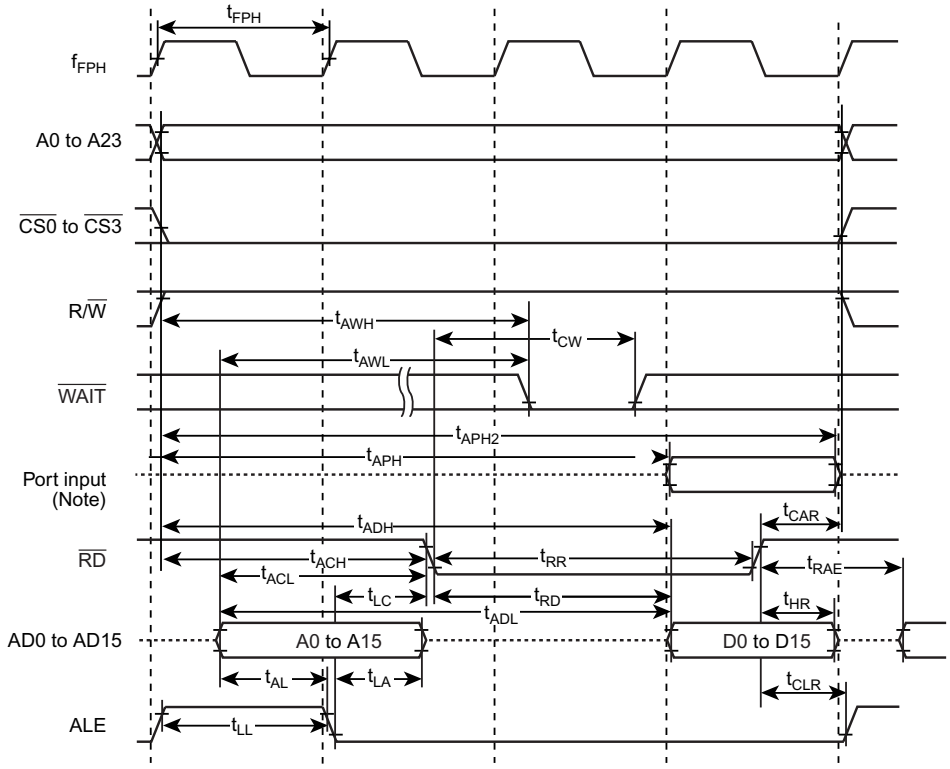
No.	Parameter	Symbol	Equation		f_{FPH} = 10 MHz		Unit
			Min	Max	Min	Max	
1	f_{FPH} cycle period (x)	t_{FPH}	100	250	100		ns
2	A0 to A15 valid to ALE low	t_{AL}	0.5x – 28		22		ns
3	A0 to A15 hold after ALE low	t_{LA}	0.5x – 35		15		ns
4	ALE pulse width high	t_{LL}	x – 40		60		ns
5	ALE low to $\overline{RD}$ to $\overline{WR}$ asserted	t_{LC}	0.5x – 28		22		ns
6	$\overline{RD}$ negated to ALE high	t_{CLR}	0.5x – 20		30		ns
7	$\overline{WR}$ negated to ALE high	t_{CLW}	x – 20		80		ns
8	A0 to A15 valid to $\overline{RD}$ or $\overline{WR}$ asserted	t_{ACL}	x – 75		25		ns
9	A0 to A23 valid to $\overline{RD}$ or $\overline{WR}$ asserted	t_{ACH}	1.5x – 70		80		ns
10	A0 to A23 hold after $\overline{RD}$ negated	t_{CAR}	0.5x – 30		20		ns
11	A0 to A23 hold after $\overline{WR}$ negated	t_{CAW}	x – 30		70		ns
12	A0 to A15 valid to D0 to D15 data in	t_{ADL}		3.0x – 76		224	ns
13	A0 to A23 valid to D0 to D15 data in	t_{ADH}		3.5x – 82		268	ns
14	$\overline{RD}$ asserted to D0 to D15 data in	t_{RD}		2.0x – 60		140	ns
15	$\overline{RD}$ width low	t_{RR}	2.0x – 30		170		ns
16	D0 to D23 hold after $\overline{RD}$ negated	t_{HR}	0		0		ns
17	$\overline{RD}$ negated to next A0 to A23 output	t_{RAE}	x – 30		70		ns
18	$\overline{WR}$ width low	t_{WW}	1.5x – 30		120		ns
19	D0 to D15 valid to $\overline{WR}$ negated	t_{DW}	1.5x – 70		80		ns
20	D0 to D23 hold after $\overline{WR}$ negated	t_{WD}	x – 50		50		ns
21	A0 to A23 valid to $\overline{WAIT}$ input ((1 + N) wait states)	t_{AWH}		3.5x – 120		230	ns
22	A0 to A15 valid to $\overline{WAIT}$ input ((1 + N) wait states)	t_{AWL}		3.0x – 100		200	ns
23	$\overline{WAIT}$ hold after $\overline{RD}$ or $\overline{WR}$ asserted ((1 + N) wait states)	t_{CW}	2.0x + 0		200		ns
24	A0 to A23 valid to port input	t_{APH}		3.5x – 170		180	ns
25	A0 to A23 valid to port hold	t_{APH2}	3.5x		350		ns
26	A0 to A23 valid to port valid	t_{AP}		3.5x + 170		520	ns

AC measurement conditions

- Output levels: High 0.7 × V_{CC}/Low 0.3 × V_{CC}, C_L = 50 pF
- Input levels: High 0.9 × V_{CC}/Low 0.1 × V_{CC}

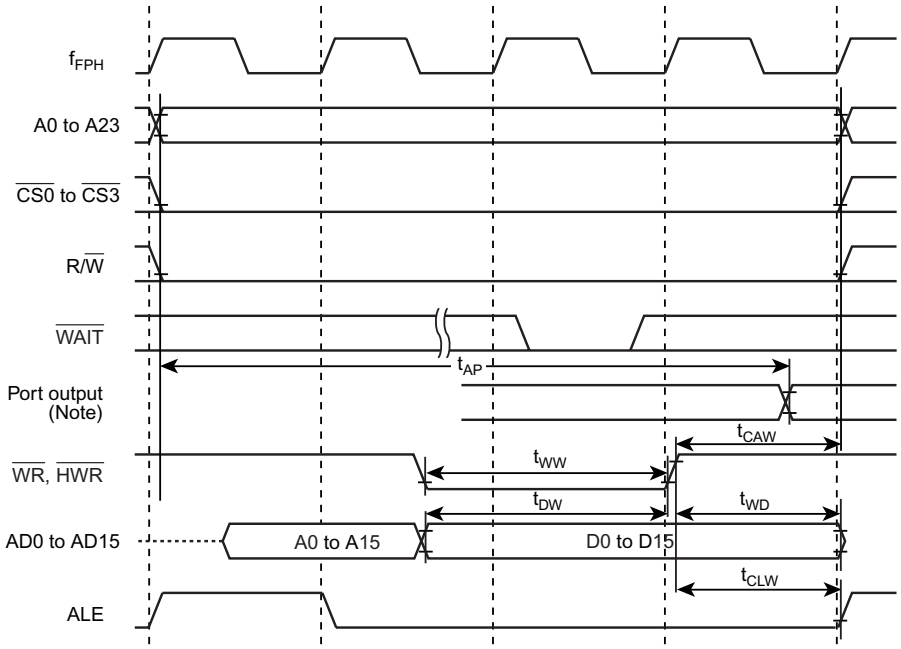
Note: In the table above, the letter x represents the f_{FPH} period, which varies, depending on the programming of the clock gear function. The cycle period of f_{FPH} is half that of the CPU system clock, f_{SYS}.

(2) Read operation timings



Note: Since the CPU accesses the internal area to read data from a port, the control signals of external pins such as $\overline{RD}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

(3) Write operation timings



Note: Since the CPU accesses the internal area to write data to a port, the control signals of external pins such as $\overline{WR}$ and $\overline{CS}$ are not enabled. Therefore, the above waveform diagram should be regarded as depicting internal operation. Please also note that the timing and AC characteristics of port input/output shown above are typical representation. For details, contact your local Toshiba sales representative.

4.4 AD Conversion Characteristics

$AV_{CC} = V_{CC}$, $AV_{SS} = V_{SS}$

Parameter		Symbol	Condition	Min	Typ.	Max	Unit
Analog reference voltage (+)		VREFH	V_{CC} = 1.8 to 2.6 V	V_{CC}	V_{CC}	V_{CC}	V
Analog reference voltage (–)		VREFL	V_{CC} = 1.8 to 2.6 V	V_{SS}	V_{SS}	V_{SS}	
Analog input voltage		VAIN		VREFL		VREFH	
Analog supply current	ADMOD<VREFON> = 1	IREF (VREFL = VSS)	V_{CC} = 1.8 to 2.6 V		0.65	0.90	mA
	ADMOD<VREFON> = 0	IREF (VREFL = VLL)	V_{CC} = 1.8 to 2.6 V		0.02	5.0	μA
Total error (Not including quantization error)		–	V_{CC} = 1.8 to 2.6 V		±1.0	±4.0	LSB

Note 1: 1LSB = (VREFH – VREFL)/1024 [V]

Note 2: Minimum operating frequency

Guaranteed when the frequency of the clock selected whit the clock gear is 4 MHz or higher with fc used.

Note 3: The supply current flowing the AV_{CC} pin is included in the digital supply current parameter (I_{CC}).

4.5 SIO Timing (I/O interface mode)

Note: In the tables below, the letter x represents the f_{FPH} period, which varies, depending on the programming of the clock gear function. The cycle period of f_{FPH} is half that of the CPU system clock, f_{SYS}.

(1) SCLK input mode

Parameter	Symbol	Equation		10 MHz (Note)		Unit
		Min	Max	Min	Max	
SCLK period	t_{SCY}	16X		1.6		μs
TXD data to SCLK rise or fall *	t_{OSS}	$t_{SCY}/2 - 4X - 180$ (V_{CC} = 2 V ± 10%)		220		ns
TXD data hold after SCLK rise or fall *	t_{OHS}	$t_{SCY}/2 + 2X + 0$		1000		ns
RXD data valid to SCLK rise or fall *	t_{HSR}	3X + 10		310		ns
RXD data valid after SCLK rise or fall *	t_{SRD}		$t_{SCY} - 0$		1600	ns
RXD data valid after SCLK rise or fall *	t_{RDS}	0		0		ns

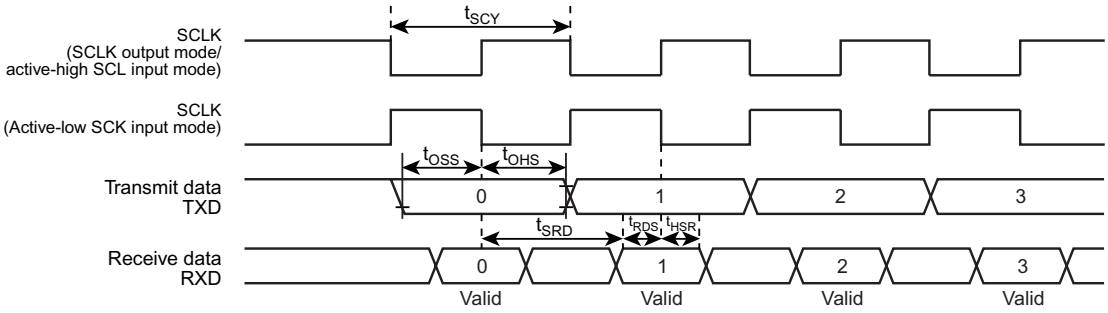
*: SCLK rise or fall: Measured relative to the programmed active edge of SCLK.

Note: t_{SCY} = 16X.

(2) SCLK output mode

Parameter	Symbol	Equation		10 MHz		Unit
		Min	Max	Min	Max	
SCLK period	t_{SCY}	16X	8192X	1.6	819	μs
TXD data to SCLK rise or fall *	t_{OSS}	$t_{SCY}/2 - 40$		760		ns
TXD data hold after SCLK rise or fall *	t_{OHS}	$t_{SCY}/2 - 40$		760		ns
RXD data valid to SCLK rise or fall *	t_{HSR}	0		0		ns
RXD data valid after SCLK rise or fall *	t_{SRD}		$t_{SCY} - 1X - 180$		1320	ns
RXD data valid after SCLK rise or fall *	t_{RDS}	$1X + 180$		280		ns

*: SCLK rise or fall: Measured relative to the programmed active edge of SCLK.



4.6 Event Counter (TA0IN, TB0IN0, TB0IN1, TB1IN0, TB1IN1)

Parameter	Symbol	Equation		10 MHz		Unit
		Min	Max	Min	Max	
Clock cycle period	t_{VCK}	$8X + 100$		900		ns
Clock low pulse width	t_{VCKL}	$4X + 40$		440		ns
Clock high pulse width	t_{VCKH}	$4X + 40$		440		ns

Note: In the tables above, the letter x represents the f_{FPH} period, which varies, depending on the programming of the clock gear function. The cycle period of f_{FPH} is half that of the CPU system clock, f_{SYS}.

4.7 Interrupts and Timer Capture

Note: In the tables below, the letter x represents the f_{FPH} period, which varies, depending on the programming of the clock gear function. The cycle period of f_{FPH} is half that of the CPU system clock, f_{SYS}.

(1) $\overline{NMI}$ and INT0 to INT4 interrupts

Parameter	Symbol	Equation		10 MHz		Unit
		Min	Max	Min	Max	
Low pulse width for $\overline{NMI}$ and INT0 to INT4	t_{INTAL}	4X + 40		440		ns
High pulse width for INT0 to INT4	t_{INTAL}	4X + 40		440		ns

(2) INT5 to INT8 interrupts and capture

The input pulse widths for INT5 to INT8 vary with the selected system clock and prescaler clock. The following table shows the pulse widths for different operation clocks:

Selected Prescaler Clock <PRCK1:0>	t_{INTBL} (INT5 to INT8 low-level pulse width)		t_{INTBH} (INT5 to INT8 high-level pulse width)		Unit
	Equation	f_{FPH} = 10 MHz	Equation	f_{FPH} = 10 MHz	
	Min	Min	Min	Min	
00 (f_{FPH})	8X + 100	900	8X + 100	900	ns
10 (fc/16)	128Xc + 0.1	12.9	128Xc + 0.1	12.9	μs

Note: Xc indicates the period of the high-speed oscillator clock (fc).

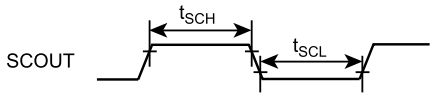
4.8 SCOUT Pin

Parameter	Symbol	Equation		10 MHz		Condition	Unit
		Min	Max	Min	Max		
High-level pulse width	t_{SCH}	0.5T − 25		25		V_{CC} = 1.8 to 2.6 V	ns
Low-level pulse width	t_{SCL}	0.5T − 25		25		V_{CC} = 1.8 to 2.6 V	ns

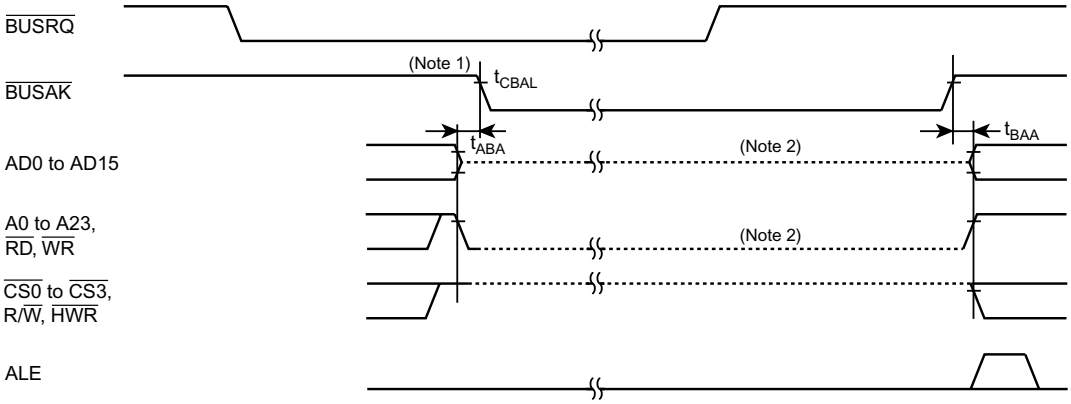
Note: In the table above, the letter T represents the cycle period of the SCOUT output clock.

Measurement condition

- Output levels: High 0.7 V_{CC}/Low 0.3 V_{CC}, C_L = 10 pF



4.9 Bus Request/Bus Acknowledge



Parameter	Symbol	Equation		f_{FPH} = 10 MHz		Condition	Unit
		Min	Max	Min	Max		
Bus float to $\overline{BUSAK}$ asserted	t_{ABA}	0	300	0	300	V_{CC} = 1.8 to 2.6 V	ns
Bus float after $\overline{BUSAK}$ negated	t_{BAA}	0	300	0	300	V_{CC} = 1.8 to 2.6 V	ns

Note 1: If the current bus cycle has not terminated due to wait-state insertion, the TMP91CY28 does not respond to $\overline{BUSRQ}$ until the wait state ends.

Note 2: This broken line indicate that output buffers are disabled, not that the signals are at indeterminate states. The pin holds the last logic value present at that pin before the bus is relinquished. This is dynamically accomplished through external load capacitances. The equipment manufacturer may maintain the bus at a predefined state by means of off-chip resistors, but he or she should design, considering the time (Determined by the CR constant) it takes for a signal to reach a desired state. The on-chip, integrated programmable pull-up/ pull-down resistors remain active, depending on internal signal states.

4.10 Recommended Oscillator Circuit

The TMP91CY28 is evaluated by the following resonator manufacturer. The results of evaluation are shown below.

Note: The additional capacitance of the resonator connecting pins are the sum of load capacitance C1, C2 and the stray capacitance on the target board. Even when recommended constants for C1 and C2 are used, actual load capacitance may vary with the board, possibly resulting in the malfunction of the oscillator. The board should be designed so that the patterns around the oscillator are as short as possible. Toshiba recommends that the resonator be finally evaluated after it is mounted on the target board.

(1) Sample crystal circuit

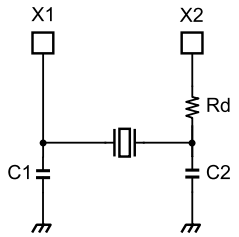


Figure 4.10.1 High-frequency Oscillator Connection Diagram

(2) Recommended ceramic resonators for the TMP91CY28, manufactured by Murata Manufacturing Co., Ltd.

Ta = –20 to 70°C

Component	Oscillating Frequency [MHz]	Recommended Resonator	Recommended Constants			VCC [V]	Note
			C1 [pF]	C2 [pF]	Rd [kΩ]		
High-speed oscillator	4.0	CSTCR4M00G55-R0	(39)	(39)	0	1.8 to 2.6	–
		CSTLS4M00G56-B0	(47)	(47)			
	8.0	CSTCE8M00G55-R0	(33)	(33)			
		CSTLS8M00G56-B0	(47)	(47)			
	10.0	CSTCE10M0G52-R0	(10)	(10)			
		CSTLS10M0G53-B0	(15)	(15)			

- The C1 and C2 constants are enclosed in parentheses for resonator models having built-in capacitors.
- The product numbers and specifications of the resonators by Murata Manufacturing Co., Ltd. are subject to change. For up-to-date information, please refer to the following URL: http://www.murata.co.jp/search/index.html

5. Package Dimension

P-LQFP100-1414-0.50F

Unit: mm

