LM3475 Hysteretic PFET Buck Controller

1 Features

- Easy-to-Use Control Methodology
- 0.8 V to V_{IN} Adjustable Output Range
- High Efficiency (90% Typical)
- ±0.9% (±1.5% Over Temperature) Feedback Voltage
- 100% Duty Cycle Capable
- Maximum Operating Frequency up to 2 MHz
- Internal Soft-Start
- Enable Pin

2 Applications

- TFT Monitor
- Auto PC
- Vehicle Security
- Navigation Systems
- Notebook Standby Supply
- Battery Powered Portable Applications
- Distributed Power Systems

3 Description

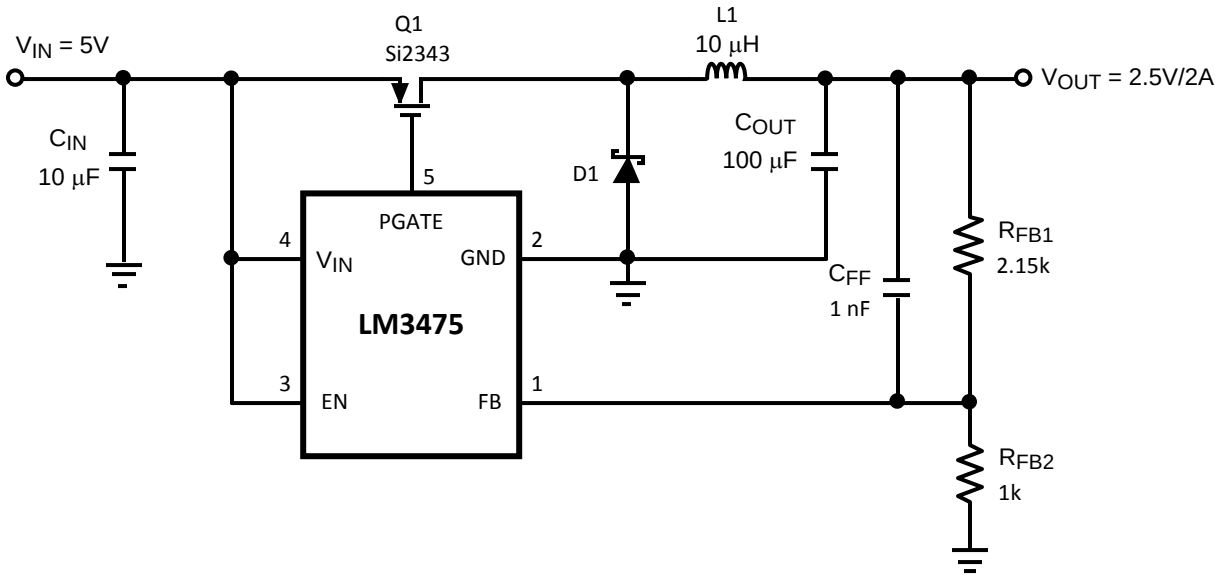
The LM3475 is a hysteretic P-FET buck controller designed to support a wide range of high efficiency applications in a very small SOT-23-5 package. The hysteretic control scheme has several advantages, including simple system design with no external compensation, stable operation with a wide range of components, and extremely fast transient response. Hysteretic control also provides high efficiency operation, even at light loads. The PFET architecture allows for low component count as well as 100% duty cycle and ultra-low dropout operation.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM3475	SOT-23 (5)	1.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (March 2013) to Revision C — **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

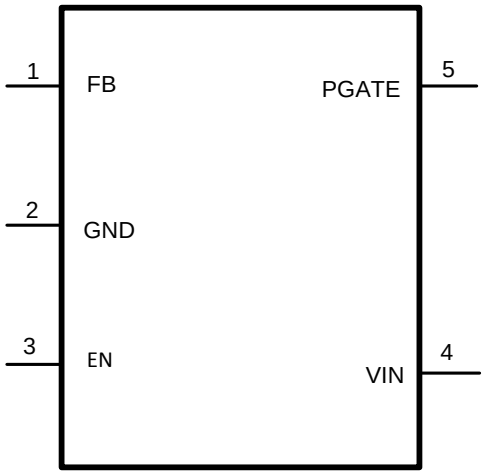
Changes from Revision A (March 2013) to Revision B — **Page**

- Changed layout of National Data Sheet to TI format. ... 1

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5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	1	I	Feedback input. Connect to a resistor divider between the output and GND.
GND	2	G	Ground.
EN	3	O	Enable. Pull this pin above 1.5 V (typical) for normal operation. When EN is low, the device enters shutdown mode.
VIN	4	P	Power supply input.
PGATE	5	O	Gate drive output for the external PFET.

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6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)

			MIN	MAX	UNIT
	V_{IN}		−0.3	16	V
	PGATE		−0.3	16	V
	FB		−0.3	5	V
	EN		−0.3	16	V
	Power dissipation (3)			440	mW
	Lead temperature	Vapor phase (60 s)		215	°C
		Infrared (15 s)		220	
T_{stg}	Storage temperature		−65	1150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) The maximum allowable power dissipation is a function of the maximum junction temperature, T_{J_MAX}, the junction-to-ambient thermal resistance, θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_{D_MAX} = (T_{J_MAX} - T_A)/\theta_{JA}$. The maximum power dissipation of 0.44 W is determined using T_A = 25°C, θ_{JA} = 225°C/W, and T_{J_MAX} = 125°C.

6.2 ESD Ratings

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	2500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Ratings

		MIN	NOM	MAX	UNIT
	Supply voltage	2.7		10	V
T_J	Operating junction temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC (1)		LM3475 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	164.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Typical limits are for T_J = 25°C, unless otherwise specified, V_{IN} = EN = 5.0 V. Maximum and minimum specification limits are specified by design, test, or statistical analysis.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_Q	Quiescent current	EN = V_{IN} (PGATE Open)	T_J = 25°C		260		µA
			T_J = −40°C to +125°C	170		320	
		EN = 0V	T_J = 25°C		7		
			T_J = −40°C to +125°C	4		10	
V_{FB}	Feedback voltage	T_J = 25°C			0.8		V
		T_J = −40°C to +125°C		0.788		0.812	
$\%\Delta V_{FB}/\Delta V_{IN}$	Feedback voltage line regulation	2.7 V < V_{IN} < 10 V			0.01		%/V
V_{HYST}	Comparator hysteresis	2.7 V < V_{IN} < 10 V	T_J = 25°C		21	28	mV
			−40°C to +125°C		21	32	
I_{FB}	FB bias current	T_J = 25°C			50		nA
		−40°C to +125°C				600	
Vth_{EN}	Enable threshold voltage	Increasing	T_J = 25°C		1.5		V
			−40°C to +125°C	1.2		1.8	
	Hysteresis				365		mV
I_{EN}	Enable leakage current	EN = 10 V	T_J = 25°C		0.025		µA
			−40°C to +125°C			1	
R_{PGATE}	Driver resistance	Source I_{SOURCE} = 100 mA			2.8		Ω
		Sink I_{Sink} = 100 mA			1.8		
I_{PGATE}	Driver output current	Source V_{PGATE} = 3.5 V C_{PGATE} = 1 nF			0.475		A
		Sink V_{PGATE} = 3.5 V C_{PGATE} = 1 nF			1.0		
T_{SS}	Soft-start time	2.7 V < V_{IN} < 10 V (EN Rising)			4		ms
T_{ONMIN}	Minimum on-time	PGATE Open			180		ns
V_{UVD}	Undervoltage detection	Measured at the FB Pin	T_J = 25°C		0.56		V
			−40°C to +125°C	0.487		0.613	

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6.6 Typical Characteristics

Unless specified otherwise, all curves taken at V_{IN} = 5 V, V_{OUT} = 2.5 V, L = 10 µH, C_{OUT} = 100 µF, ESR = 100 mΩ, and T_A = 25°C.

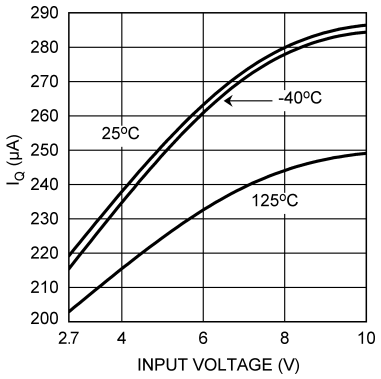


Figure 1. Quiescent Current vs Input Voltage

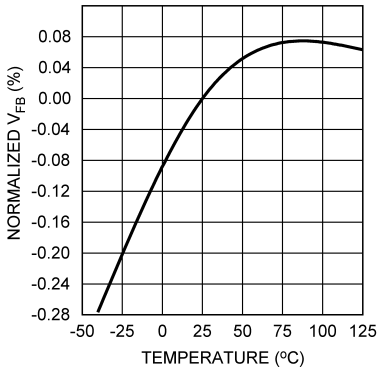


Figure 2. Feedback Voltage vs Temperature

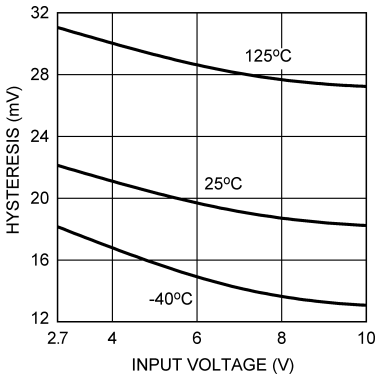


Figure 3. Hysteresis Voltage vs Input Voltage

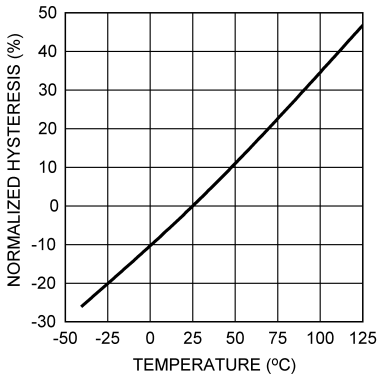


Figure 4. Hysteresis Voltage vs Temperature

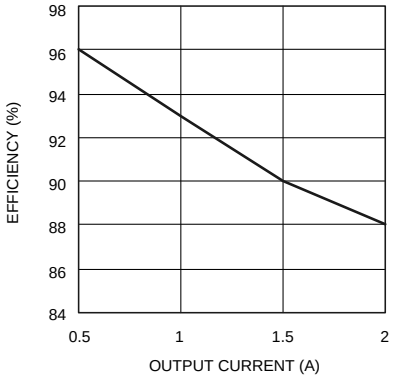


Figure 5. Efficiency vs Load Current

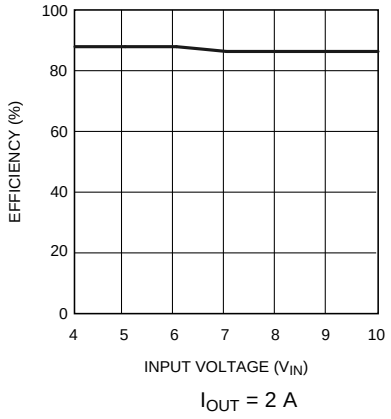


Figure 6. Efficiency vs Input Voltage

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Typical Characteristics (continued)

Unless specified otherwise, all curves taken at V_{IN} = 5 V, V_{OUT} = 2.5 V, L = 10 µH, C_{OUT} = 100 µF, ESR = 100 mΩ, and T_A = 25°C.

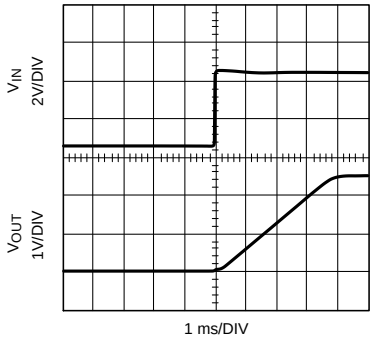


Figure 7. Start Up

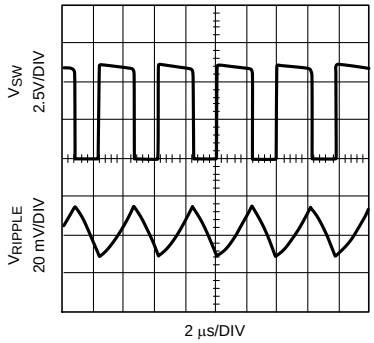


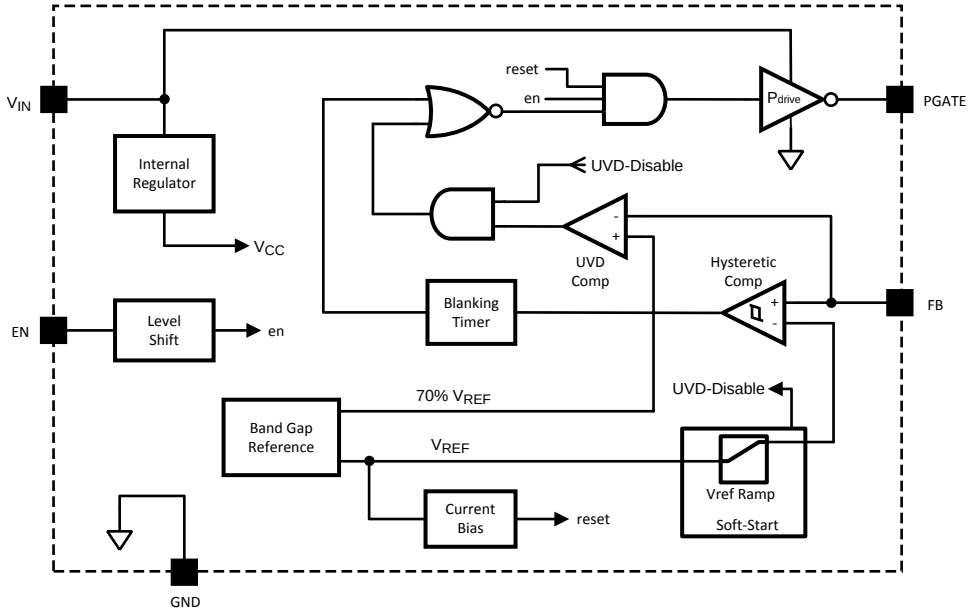
Figure 8. Output Ripple Voltage

7 Detailed Description

7.1 Overview

The LM3475 is a buck (step-down) DC-DC controller that uses a hysteretic control architecture, which results in Pulse Frequency Modulated (PFM) regulation. The hysteretic control scheme does not utilize an internal oscillator. Switching frequency depends on external components and operating conditions. Operating frequency decreases at light loads, resulting in excellent efficiency compared to PWM architectures. Because switching is directly controlled by the output conditions, hysteretic control provides exceptional load transient response.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Hysteretic Control Circuit

The LM3475 uses a comparator-based voltage control loop. The voltage on the feedback pin is compared to a 0.8V reference with 21mV of hysteresis. When the FB input to the comparator falls below the reference voltage, the output of the comparator goes low. This results in the driver output, PGATE, pulling the gate of the PFET low and turning on the PFET.

With the PFET on, the input supply charges C_{OUT} and supplies current to the load through the PFET and the inductor. Current through the inductor ramps up linearly, and the output voltage increases. As the FB voltage reaches the upper threshold (reference voltage plus hysteresis) the output of the comparator goes high, and the PGATE turns the PFET off. When the PFET turns off, the catch diode turns on, and the current through the inductor ramps down. As the output voltage falls below the reference voltage, the cycle repeats. The resulting output, inductor current, and switch node waveforms are shown in Figure 9.

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Feature Description (continued)

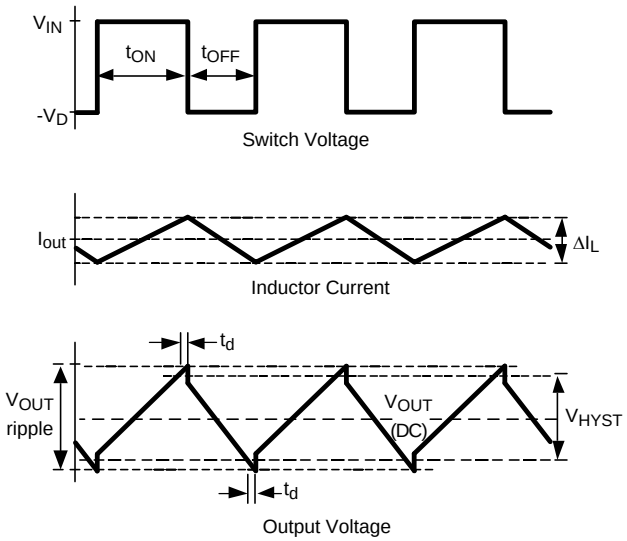


Figure 9. Hysteretic Waveforms

7.3.2 Soft-Start

The LM3475 includes an internal soft-start function to protect components from excessive inrush current and output voltage overshoot. As V_{IN} rises above 2.7 V (typical), the internal bias circuitry becomes active. When EN goes high, the device enters soft-start. During soft-start, the reference voltage is ramped up to the nominal value of 0.8 V in approximately 4ms. Duty cycle and output voltage will increase as the reference voltage is ramped up.

7.3.3 Under Voltage Detection

When the output voltage falls below 70% (typical) of the normal voltage, as measured at the FB pin, the device turns off PFET and restarts a new soft-start cycle. In short circuit, the PFET is always on, and the converter is effectively a resistor divider from input to output to ground. Whether the part restarts depends on the power path resistance and the short circuit resistance. This feature should not be considered as overcurrent protection or output short circuit protection.

7.3.4 PGATE

During switching, the PGATE pin swings from V_{IN} (off) to ground (on). As input voltage increases, the time it takes to slew the gate of the PFET on and off also increases. Also, as the PFET gate voltage approaches V_{IN}, the PGATE current driving capability decreases. This can cause a significant additional delay in turning the switch off when using a PFET with a low threshold voltage. These two effects will increase power dissipation and reduce efficiency. Therefore, a PFET with relatively high threshold voltage and low gate capacitance is recommended.

7.3.5 Minimum On or Off Time

To ensure accurate comparator switching, the LM3475 imposes a blanking time after each comparator state change. This blanking time is 180 ns typically. Immediately after the comparator goes high or low, it will be held in that state for the duration of the blanking time. This helps keep the hysteretic comparator from improperly responding to switching noise spikes (See *Reducing Switching Noise*) and ESL spikes (See *Output Capacitor Selection*) at the output.

At very low or very high duty cycle operation, maximum frequency will be limited by the blanking time. The maximum operating frequency can be determined by the following equations:

$$F_{MAX} = D / ton_{min} \quad (1)$$

$$F_{MAX} = (1-D) / toff_{min}$$

where

Feature Description (continued)

- D is the duty cycle, defined as V_{OUT}/V_{IN}, and ton_{min}
- $toff_{min}$ is the sum of the blanking time, the propagation delay time, and the PFET delay time (see Figure 9) (2)

7.3.6 Enable Pin (EN)

The LM3475 provides a shutdown function via the EN pin to disable the device. The device is active when the EN pin is pulled above 1.5 V (typ) and in shutdown mode when EN is below 1.135 V (typ). In shutdown mode, total quiescent current is less than 10 µA. The EN pin can be directly connected to V_{IN} for always-on operation.

7.4 Device Functional Modes

The LM3475 operates in discontinuous conduction mode at light load current and continuous conduction mode at heavy load current. In discontinuous conduction mode, current through the inductor starts at zero and ramps up to the peak, then ramps down to zero. The next cycle starts when the FB voltage reaches the reference voltage. Until then, the inductor current remains zero. Operating frequency is low, as are switching losses. In continuous conduction mode, current always flows through the inductor and never ramps down to zero.

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM3475 employs a hysteretic control architecture; which provides excellent load transient response and efficiency even at light loads, as compared to its PWM architectures. No external compensation is required which results in a simple design and low component count. A typical schematic is described in the next section.

8.2 Typical Application

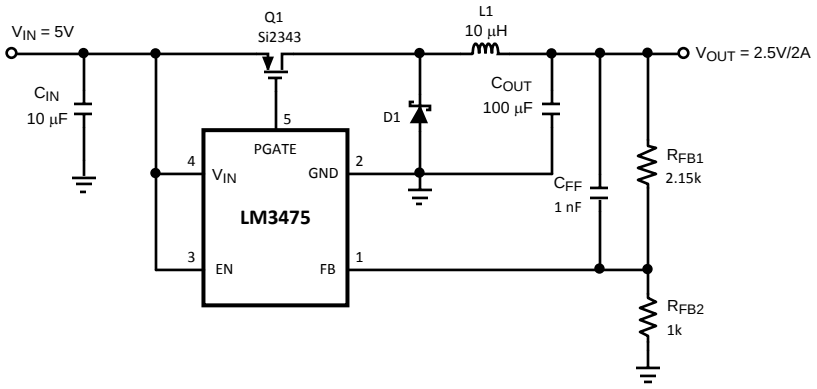


Figure 10. Full Demo Board Schematic

8.2.1 Design Requirements

To properly size the components for the application, the designer needs the following parameters: input voltage range, output voltage, output current range, and required switching frequency. These four main parameters affect the choices of component available to achieve a proper system behavior. Although hysteretic control is a simple control scheme, the operating frequency and other performance characteristics depend on external conditions and components. If the inductance, output capacitance, ESR, VIN, or Cff is changed, there will be a change in the operating frequency and possibly output ripple. Therefore, care must be taken to select components which will provide the desired operating range.

8.2.2 Detailed Design Procedure

Table 1. Bill of Materials

DESIGNATOR	DESCRIPTION	PART NUMBER	VENDOR
C_{IN}	10 µF, 16 V, X5R	EMK325BJ106MN	TAIYO YUDEN
C_{OUT}	100 µF, 6 V, Ta	TPSY107M006R0100	AVX
C_{FF}	1 nF, 25 V, X7R	VJ1206Y102KXXA	Vishay
D1	Schottky, 20 V, 2 A	CMSH2-20L	Central Semiconductor
L1	10 µH, 3.1 A	CDRH103R100	Sumida
Q1	30 V, 2.5 A	Si2343	Vishay
R_{FB2}	1 kΩ, 0805, 1%	CRW08051001F	Vishay
R_{FB1}	2.15 kΩ, 0805, 1%	CRCW08052151F	Vishay

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8.2.2.1 Setting Output Voltage

The output voltage is programmed using a resistor divider between V_{OUT} and GND as shown in Figure 11. The feedback resistors can be calculated as follows:

$$V_{OUT} = \frac{R_1 + R_2}{R_2} \times V_{FB} \quad (3)$$

where

- Vfb is 0.8 V typically

The feedback resistor ratio, α = (R1+R2) / R2, will also be used below to calculate output ripple and operating frequency.

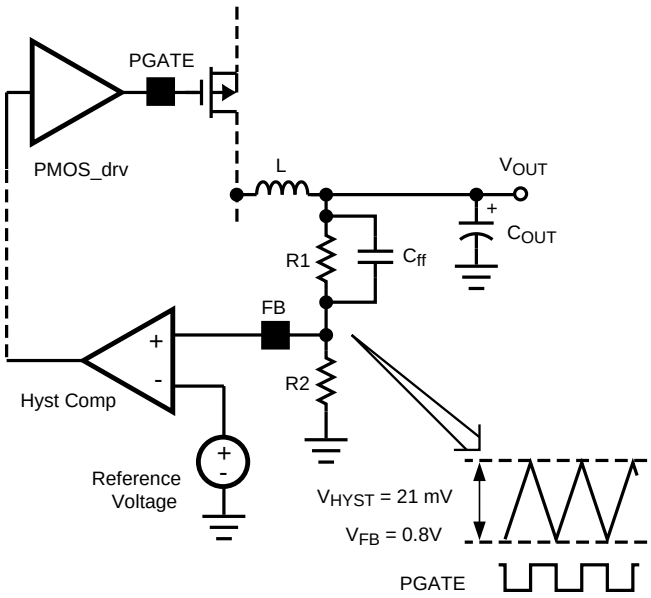


Figure 11. Hysteretic Window

8.2.2.2 Setting Operating Frequency and Output Ripple

Although hysteretic control is a simple control scheme, the operating frequency and other performance characteristics depend on external conditions and components. If the inductance, output capacitance, ESR, V_{IN}, or C_{ff} is changed, there will be a change in the operating frequency and possibly output ripple. Therefore, care must be taken to select components which will provide the desired operating range. The best approach is to determine what operating frequency is desirable in the application and then begin with the selection of the inductor and output capacitor ESR. The design process usually involves a few iterations to select appropriate standard values that will result in the desired frequency and ripple.

Without the feedforward capacitor (C_{ff}), the operating frequency (F) can be approximately calculated using the formula:

$$F = \frac{V_{OUT}}{V_{IN}} \times \frac{(V_{IN} - V_{OUT}) \times ESR}{(V_{HYST} \times \alpha \times L) + (V_{IN} \times delay \times ESR)} \quad (4)$$

where

- Delay is the sum of the LM3475 propagation delay time and the PFET delay time
- The propagation delay is 90ns typically

Minimum output ripple voltage can be determined using the following equation:

$$V_{OUT_PP} = V_{HYST} (R1 + R2) / R2 \quad (5)$$

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8.2.2.3 Using a Feed-forward Capacitor

The operating frequency and output ripple voltage can also be significantly influenced using a speed up capacitor, C_{ff}, as shown in Figure 11. C_{ff} is connected in parallel with the high side feedback resistor, R1. The output ripple causes a current to be sourced or sunk through this capacitor. This current is essentially a square wave. Since the input to the feedback pin (FB) is a high impedance node, the bulk of the current flows through R2. This superimposes a square wave ripple voltage on the FB node. The end result is a reduction in output ripple and an increase in operating frequency. When adding C_{ff}, calculate the formula above with α= 1. The value of C_{ff} depends on the desired operating frequency and the value of R2. A good starting point is 1nF ceramic at 100kHz decreasing linearly with increased operating frequency. Also note that as the output voltage is programmed below 1.6V, the effect of C_{ff} will decrease significantly.

8.2.2.4 Inductor Selection

The most important parameters for the inductor are the inductance and the current rating. The LM3475 operates over a wide frequency range and can use a wide range of inductance values. Minimum inductance can be calculated using the following equation:

$$L = \frac{V_{IN} - V_{SD} - V_{OUT}}{\Delta I} \times \frac{D}{F}$$

where

- D is the duty cycle, defined as V_{OUT}/V_{IN}
- ΔI is the allowable inductor ripple current (6)

Maximum allowable inductor ripple current should be calculated as a function of output current (I_{OUT}) as shown below:

$$\Delta I_{max} = I_{OUT} \times 0.3$$

The inductor must also be rated to handle the peak current (I_{PK}) and RMS current given by:

$$I_{PK} = (I_{OUT} + \Delta I/2) \times 1.1 \quad (7)$$

$$I_{RMS} = \sqrt{I_{OUT}^2 + \frac{\Delta I^2}{3}} \quad (8)$$

The inductance value and the resulting ripple is one of the key parameters controlling operating frequency.

8.2.2.5 Output Capacitor Selection

Once the desired operating frequency and inductance value are selected, ESR must be selected based on Equation 4. This process may involve a few iterations to select standard ESR and inductance values.

In general, the ESR of the output capacitor and the inductor ripple current create the output ripple of the regulator. However, the comparator hysteresis sets the first order value of this ripple. Therefore, as ESR and ripple current vary, operating frequency must also vary to keep the output ripple voltage regulated. The hysteretic control topology is well suited to using ceramic output capacitors. However, ceramic capacitors have a very low ESR, resulting in a 90° phase shift of the output voltage ripple. This results in low operating frequency and increased output ripple. To fix this problem a low value resistor could be added in series with the ceramic output capacitor. Although counter intuitive, this combination of a ceramic capacitor and external series resistance provide highly accurate control over the output voltage ripple. Another method is to add an external ramp at the FB pin as shown in Figure 12. By proper selection of R1 and C2, the FB pin sees faster voltage change than the output ripple can cause. As a result, the switching frequency is higher while the output ripple becomes lower. The switching frequency is approximately:

$$F = \frac{V_{IN}}{2\pi \times R_1 \times C_2 \times V_{HYS}} \quad (9)$$

Other types of capacitor, such as Sanyo POSCAP, OS-CON, and Nichicon 'NA' series are also recommended and may be used without additional series resistance. For all practical purposes, any type of output capacitor may be used with proper circuit verification.

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Capacitors with high ESL (equivalent series inductance) values should not be used. As shown in Figure 9, the output ripple voltage contains a small step at both the high and low peaks. This step is caused by and is directly proportional to the output capacitor's ESL. A large ESL, such as in an electrolytic capacitor, can create a step large enough to cause abnormal switching behavior.

8.2.2.6 Input Capacitor Selection

A bypass capacitor is required between V_{IN} and ground. It must be placed near the source of the external PFET. The input capacitor prevents large voltage transients at the input and provides the instantaneous current when the PFET turns on. The important parameters for the input capacitor are the voltage rating and the RMS current rating. Follow the manufacturer's recommended voltage de-rating. RMS current and power dissipation (PD) can be calculated with the equations below:

$$I_{RMS_CIN} = \frac{I_{OUT}}{V_{IN}} \sqrt{V_{OUT} \times (V_{IN} - V_{OUT})} \tag{10}$$

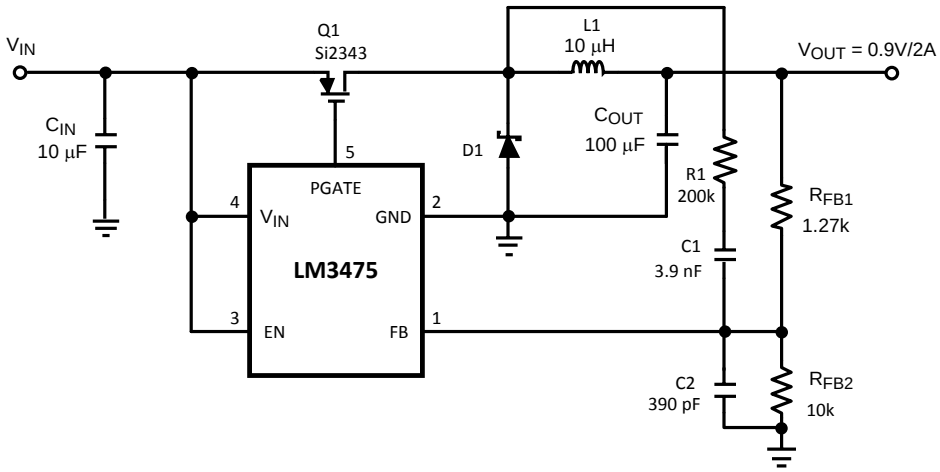


Figure 12. External Ramp

8.2.2.7 Diode Selection

The catch diode provides the current path to the load during the PFET off time. Therefore, the current rating of the diode must be higher than the average current through the diode, which be calculated as shown:

$$I_{D_AVE} = I_{OUT} \times (1 - D) \tag{11}$$

The peak voltage across the catch diode is approximately equal to the input voltage. Therefore, the diode's peak reverse voltage rating should be greater than 1.3 times the input voltage.

A Schottky diode is recommended, since a low forward voltage drop will improve efficiency.

For high temperature applications, diode leakage current may become significant and require a higher reverse voltage rating to achieve acceptable performance.

8.2.2.8 P-Channel MOSFET Selection

The PFET switch should be selected based on the maximum Drain-Source voltage (VDS), Drain current rating (I_D), maximum Gate-Source voltage (VGS), on resistance (R_{DSON}), and Gate capacitance. The voltage across the PFET when it is turned off is equal to the sum of the input voltage and the diode forward voltage. The VDS must be selected to provide some margin beyond the sum of the input voltage and Vd.

Since the current flowing through the PFET is equal to the current through the inductor, I_D must be rated higher than the maximum I_{PK}. During switching, PGATE swings the PFET's gate from V_{IN} to ground. Therefore, A PFET must be selected with a maximum VGS larger than V_{IN}. To insure that the PFET turns on completely and quickly, refer to the *PGATE* section.

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The power loss in the PFET consists of switching losses and conducting losses. Although switching losses are difficult to precisely calculate, the equation below can be used to estimate total power dissipation. Increasing R_{DSON} will increase power losses and degrade efficiency. Note that switching losses will also increase with lower gate threshold voltages.

$$PD_{switch} = R_{DSON} x (I_{OUT})^2 x D + F x I_{OUT} x V_{IN} x (t_{on} + t_{off})/2$$

where

- t_{on} = FET turn on time
- t_{off} = FET turn off time
- A value of 10ns to 50ns is typical for ton and toff

(12)

Note that the R_{DSON} has a positive temperature coefficient. At 100°C, the R_{DSON} may be as much as 150% higher than the value at 25°C.

The Gate capacitance of the PFET has a direct impact on both PFET transition time and the power dissipation in the LM3475. Most of the power dissipated in the LM3475 is used to drive the PFET switch. This power can be calculated as follows:

The amount of average gate driver current required during switching (I_G) is:

$$I_G = Q_g x F \quad (13)$$

And the total power dissipated in the device is:

$$I_q V_{IN} + I_G V_{IN}$$

where

- I_q is typically 260µA as shown in *Electrical Characteristics*

(14)

As gate capacitance increases, operating frequency may need to be reduced, or additional heat sinking may be required to lower the power dissipation in the device.

In general, keeping the gate capacitance below 2000 pF is recommended to keep transition times (switching losses), and power losses low.

8.2.2.9 Reducing Switching Noise

Although the LM3475 employs internal noise suppression circuitry, external noise may continue to be excessive. There are several methods available to reduce noise and EMI.

MOSFETs are very fast switching devices. The fast increase in PFET current coupled with parasitic trace inductance can create unwanted noise spikes at both the switch node and at V_{IN}. Switching noise will increase with load current and input voltage. This noise can also propagate through the ground plane, sometimes causing unpredictable device performance. Slowing the rise and fall times of the PFET can be very effective in reducing this noise. Referring to Figure 13, the PFET can be slowed down by placing a small (1-Ω to 10-Ω) resistor in series with PGATE. However, this resistor will increase the switching losses in the PFET and will lower efficiency. Therefore it should be kept as small as possible and only used when necessary. Another method to reduce switching noise (other than good PCB layout, see Layout) is to use a small RC filter or snubber. The snubber should be placed in parallel with the catch diode, connected close to the drain of the PFET, as shown in Figure 13. Again, the snubber should be kept as small as possible to limit its impact on system efficiency. A typical range is a 10-Ω to 100-Ω resistor and a 470-pF to 2.2-nF ceramic capacitor.

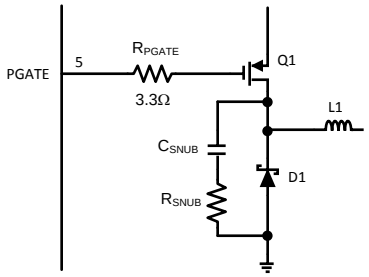


Figure 13. PGATE Resistor and Snubber

8.2.3 Application Curves

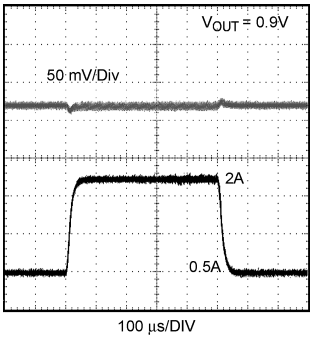


Figure 14. Load Transient Response with External Ramp (Circuit from Figure 12)

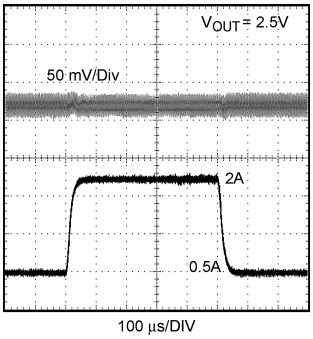


Figure 15. Load Transient Response (Typical Application Circuit from Figure 16)

9 Power Supply Recommendations

The LM3475 controller is designed to operate from various DC power supplies. VIN input should be protected from reversal voltage and voltage dump over 16 volts. The impedance of the input supply rail should be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected by using long wires, additional bulk capacitance may be required in addition to normal input capacitor.

10 Layout

10.1 Layout Guidelines

PC board layout is very important in all switching regulator designs. Poor layout can cause EMI problems, excess switching noise and poor operation.

As shown in Figure 16, place the ground of the input capacitor as close as possible to the anode of the diode. This path also carries a large AC current. The switch node, the node connecting the diode cathode, inductor, and PFET drain, should be kept as small as possible. This node is one of the main sources for radiated EMI.

The feedback pin is a high impedance node and is therefore sensitive to noise. Be sure to keep all feedback traces away from the inductor and the switch node, which are sources of noise. Also, the resistor divider should be placed close to the FB pin. The gate pin of the external PFET should be located close to the PGATE pin.

TI also recommends using a large, continuous ground plane, particularly in higher current applications.

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10.2 Layout Example

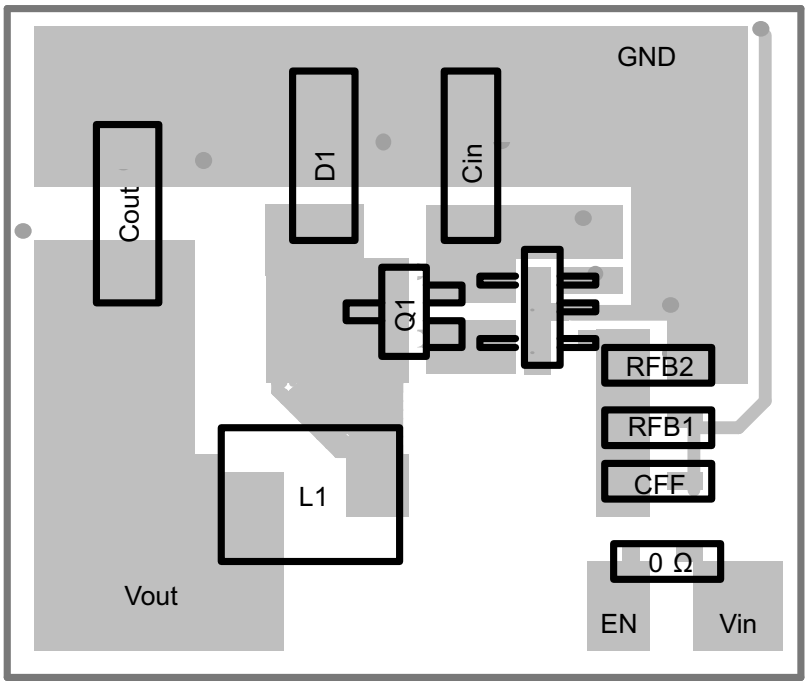


Figure 16. Layout Example (2:1 Scale)

11 Device and Documentation Support

11.1 Device Support

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3475MF	NRND	SOT-23	DBV	5		TBD	Call TI	Call TI	-40 to 125	S65B	
LM3475MF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S65B	Samples
LM3475MFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S65B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

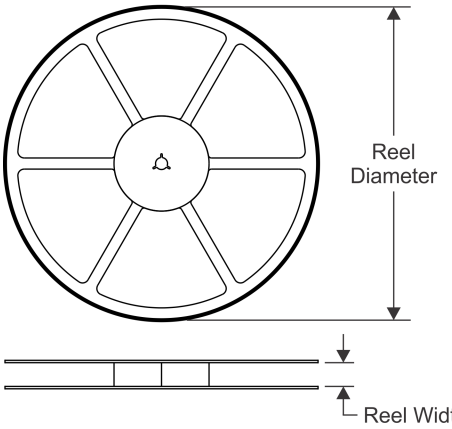
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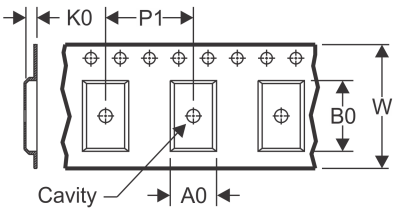
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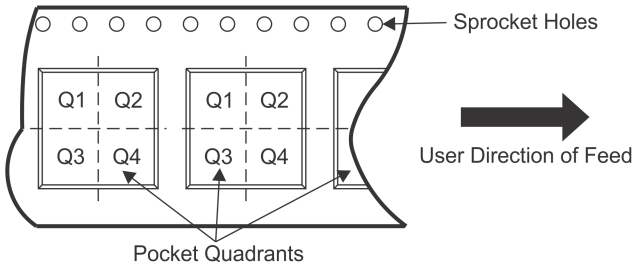


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

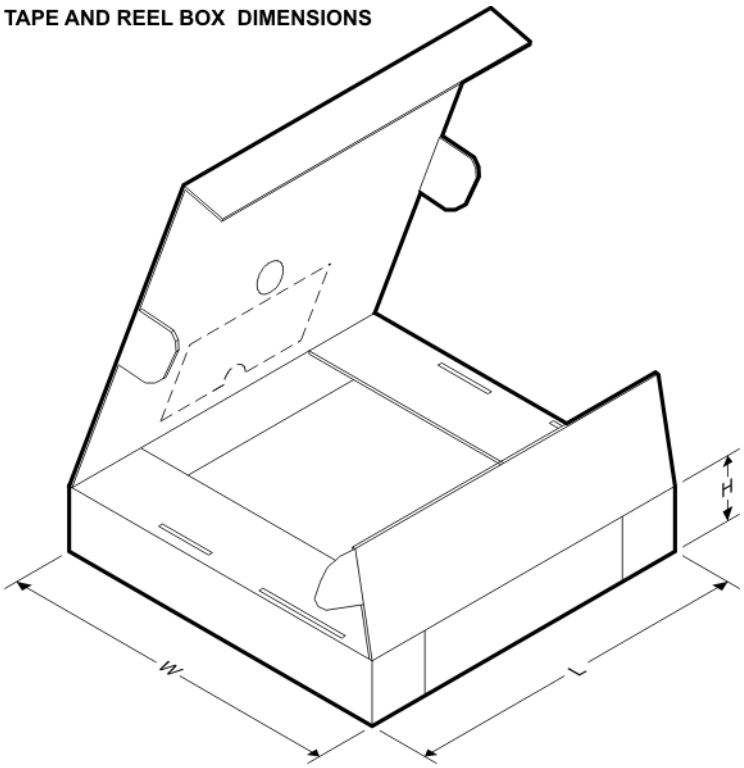
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3475MF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM3475MFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

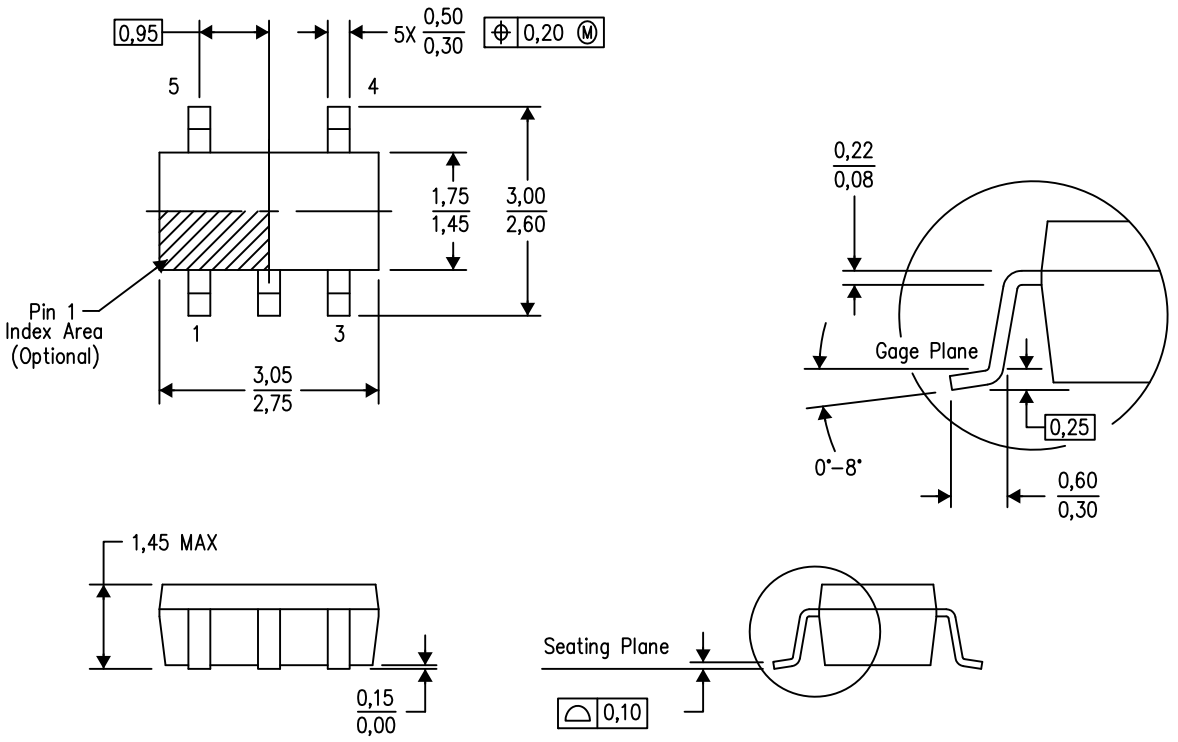
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3475MF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM3475MFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

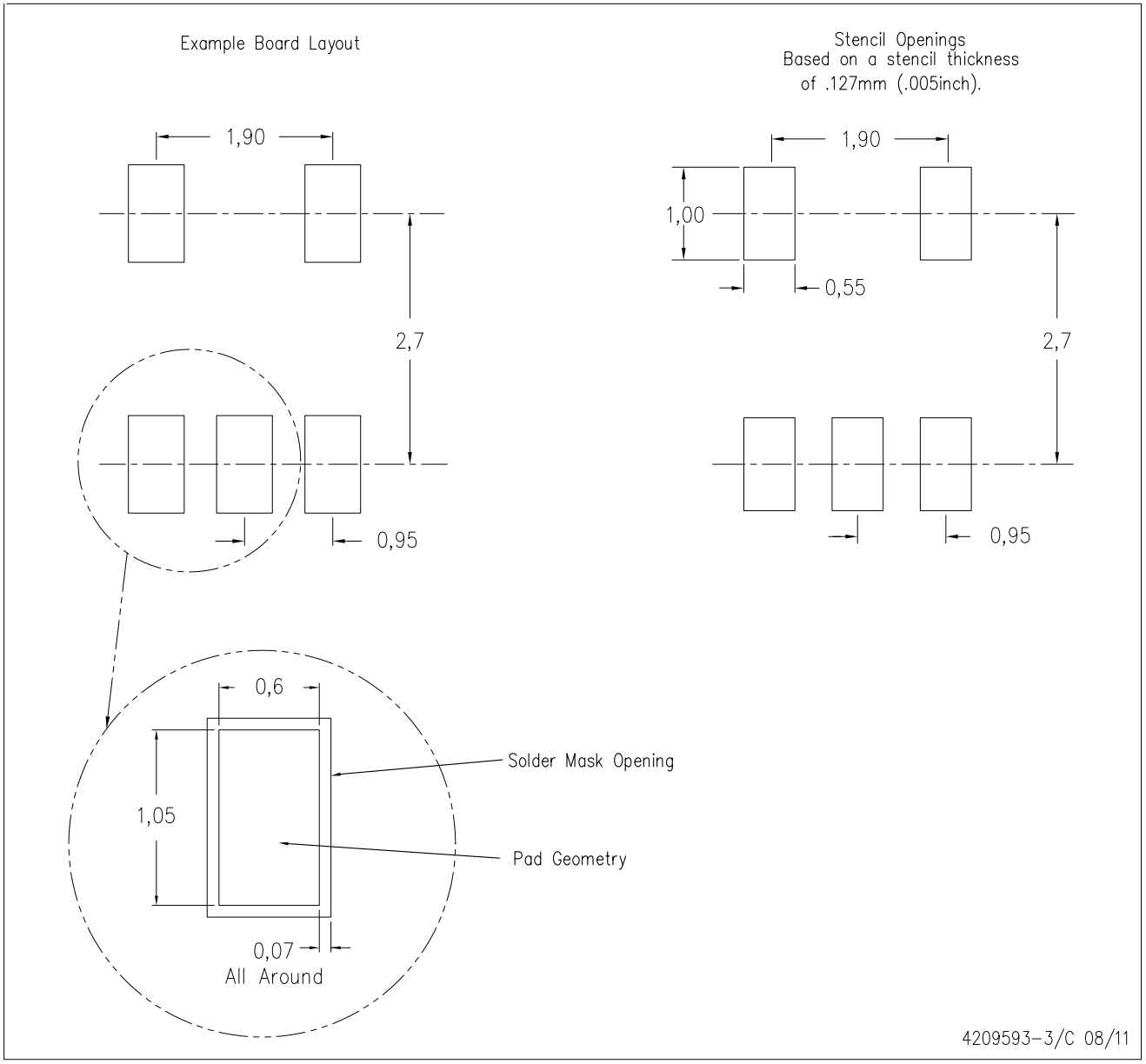
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/N 12/14

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

DBV (R–PDSO–G5) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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